Errata to MPC8323E PowerQUICC II Pro Integrated Host Processor Family Reference Manual, Rev. 2

This errata describes corrections to the *MPC8323E PowerQUICC II Pro Integrated Host Processor Family Reference Manual*, Revision 2. For convenience, the section number and page number of the errata item in the reference manual are provided.

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Section, Page No.	Changes
2.4, 2-21	In Table 2-4, "Detailed QUICC Engine Memory Map," add CEURNR register at Offset 0x001B8, as follows:

Table 2-4. Detailed QUICC Engine Memory Map

Internal Address	Abbreviation	Name	Size	Section/Page	Comments
Communications Processor					
0x0_01B8	CEURNR	QUICC Engine microcode revision number register	4 bytes	19.4.7/19-13	—

Chapter 3	Replace MEMC_MA[0:13] with MEMC_MA[13:0] throughout chapter.
4.3.2.1, 4-12	In Figure 4-3, "Reset Configuration Word Low Register (RCWLR)," add field SVCOD (bits 2–3), with the following field description: "System PLL VCO division. See Section 4.3.2.1.1, "System PLL VCO Division.""

4.3.2.1.1, 4-13 Add Section 4.3.2.1.1 “System PLL VCO Division,” as follows:

4.3.2.1.1 System PLL VCO Division

The RCWLR field SVCOD (system PLL VCO division), shown in Table 4-9, establishes the internal ratio between the system PLL VCO frequency and the PLL output clock frequency. The PLL output clock frequency equals *csb_clk* frequency if RCWLR[LBCM] and RCWLR[DDRCM] are both cleared or twice the csb_clk frequency if RCWLR[LBCM] or RCWLR[DDRCM] or both of them are set.

Table 4-9 describes the setting of SVCOD bits.

Table 4-9. System PLL VCO Division

Reset Configuration Word Low Register (RCWLR) Bits	Field Name	Value (Binary)	VCO Division Factor
2–3	SVCOD	00	4
		01	8
		10	2
		11	Reserved

4.3.3.1, 4-19 Add the following to the end of the first paragraph: “+ LCS0 is the default for GPCM, so GPCM controlled is used to read the reset configuration word from EEPROM. /LGTA should be high to avoid unintended early termination of the read cycle.”

4.5.1.6, 4-33 Change the first sentence to say the following: “RCR, shown in Figure 4-19, can be used by software to initiate a hard reset sequence.”

4.5.2.3, 4-37 In Table 4-34, “SCCR Bit Descriptions,” add the following note to ENCCM (bits 6–7) field description:

“**Note:** The encryption core must have the same clock ratio as the USB unit, unless one of them has its clock disabled.”

5.3.1, 5-16 In Table 5-20, “System Configuration Register Memory Map,” add the following row between the last two reserved rows:

Table 5-20. System Configuration Register Memory Map

Local Memory Offset (Hex)	Register	Access	Reset	Section/Page
0x00128	DDR control driver register (DDRCDR)	R/W	0x0004_0000	5.3.2.6/5-22

5.3.2.6, 5-22 Add Section 5.3.2.6, “DDR Control Driver Register (DDRCDR),” as follows:

5.3.2.6 DDR Control Driver Register (DDRCDR)

The DDR control driver register (DDRCDR) contains bits that allow control over the driver of the DDR SDRAM controller.

DDRCDR is shown in Figure 5-15.

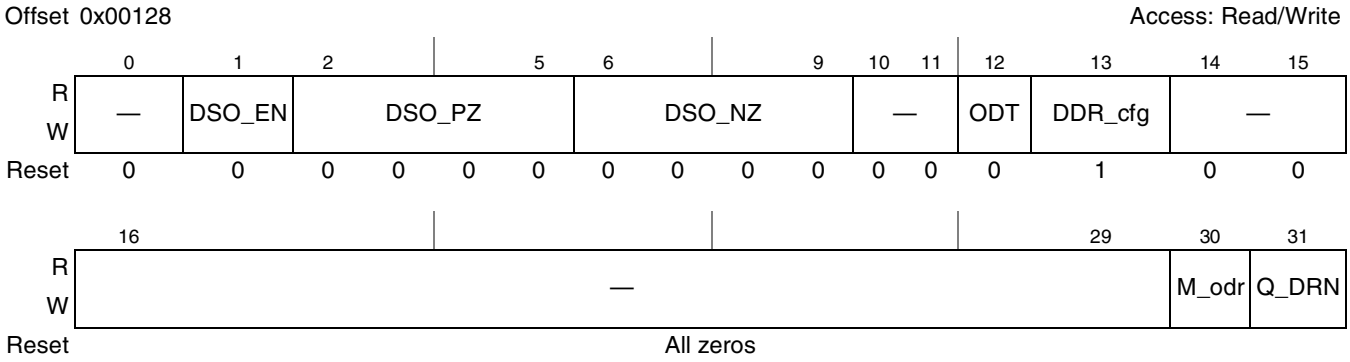

Figure 5-15. DDR Control Driver Register (DDRCDR)

Table 5-28 shows the bit definition of the DDRCDR.

Table 5-28. DDRCDR Field Descriptions

Bits	Name	Description
0	—	Reserved
1	DSO_EN	0 DDR driver software override disable 1 DDR driver software override enable
2–5	DSO_PZ	DDR driver software p-impedance override 0000 Half strength—Highest Z 1000 Much higher Z than nominal 1100 Higher Z than nominal 1110 Nominal impedance setting 1111 Lower Z than nominal
6–9	DSO_NZ	DDR driver software n-impedance override 0000 Half strength—Highest Z 1000 Much higher Z than nominal 1100 Higher Z than nominal 1110 Nominal impedance setting 1111 Lower Z than nominal
10–11	—	Reserved. Should be cleared.
12	ODT	ODT termination value for I/Os 0 75 Ω 1 150 Ω
13	DDR_cfg	Selects voltage level for DDR pads 0 DDR2 (1.8V mode) nominal impedance—18 Ω 1 DDR1 (2.5V mode) nominal impedance—18 Ω **Note:** DDR_cfg must be set according to the logical type of the DDR memory devices, as it effects logic behavior of the DDR controller as well as the physical parameters of the DDR I/O pads.

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Table 5-28. DDRCDR Field Descriptions (continued)

Bits	Name	Description
14–29	—	Reserved
30	M_odr	Disable memory transaction reordering 0 Memory transaction reordering enabled 1 Memory transaction reordering disabled
31	Q_DRN	0 Drain queue before sleep disable 1 Drain queue before sleep enable

5.5.5, 5-35	In Table 5-39, “RTEVR Bit Settings,” update AIF (bit 30) field description to read as follows: “The bit is set if the RTC issues an interrupt when the RTC counter value equals RTALR[ALRM].”
5.6.5.5, 5-41	In Table 5-48, “PTEVR Bit Settings,” change PIF (bit 31) field description to say the following: “Periodic interrupt flag bit. It is asserted after the SPMPIT counter counts to zero. This status bit should be cleared by software.”
5.7.4, 5-47	In Table 5-50, “GTM External Signals—Detailed Signal Descriptions,” in the State Meaning of signal $\overline{\text{TGATE}}n$ description, change “In a reset gate mode...” to “In a restart gate mode...”. In the State Meaning of signal $\overline{\text{TOUT}}n$, clarify #2 by changing “$\overline{\text{TOUT}}n$ changes occur on the rising edge of the system clock” to “$\overline{\text{TOUT}}n$ begins or stops counting, depending on the signal state and the configured mode.”; also clarify Timing by changing “system clock” to “timer input clock”.
5.7.5.6/5-54	Change title of Table 5-60, “GTEVR*n* Bit Settings,” to “GTEVR Field Descriptions,” and change the ‘1’ setting to read as follows in REF (bit 14) field description: “The counter has “exceeded” the GTRFR*n*[TRV] value.”
5.7.6.1, 5-55	In the second paragraph, change “65,537” to “65,536”.
5.7.6.3, 5-57	In the Note, change “the counter begins counting after...” to “the counter begins or stops after...”
6.2.1, 6-3	In Table 6-2, “ACR Field Descriptions,” reserved fields change from “Write reserved, read = 0” to “Reserved, write should preserve reset value.”
6.3.1.3, 6-13	Change “After the completion of snoop copyback, the arbiter grants the bus back to the master that had its transaction ARTRYed” to: “After the completion of snoop copyback, the arbiter grants the bus to the most ahead master among those masters which have an active bus request signal at that time, which may or may not be the same master that had its transaction ARTRYed. Only when a transaction address phase is completed with no ARTRY (and no repeat conditions), the master moves to the end of the line.”
7.3.1.3.3, 7-18	In Table 7-2, “e300 HID0 Bit Descriptions,” add the following note to EBA and EBD field descriptions: “Do not set this bit; the CSB does not have parity signals.”

Section, Page No.	Changes
9.3.2.1, 9-6	In Table 9-3, “Memory Interface Signals—Detailed Signal Descriptions,” change signal description of MA[13:0] to the following: “Assertion/Negation—The address lines are only driven when the controller has a command scheduled to issue on the address/CMD bus; otherwise they will be at high-Z. It is valid when a transaction is driven to DRAM (when $\overline{\text{MCS}}$ is active).”
9.5, 9-29	In third paragraph, replace sentence “Bank sizes up to 512 Mbytes are supported, providing up to a maximum of 512 Mbytes of DDR main memory,” with the following: “Bank sizes up to 512 Mbytes are supported, providing up to a maximum of 512 Mbits of DDR main memory per chip select.”
9.5.9, 9-48	In first paragraph, replace sentence “For example, if a write transaction is desired with a size of one double word (8 bytes), then the second, third, and fourth beats of data are not written to DRAM,” with the following: “For example, if a write transaction is desired with a size of one word (4 bytes), then the second, third, and fourth beats of data are not written to DRAM, as the width of the data bus is 32 bits.”
10.4.2.3, 10-41	Update Figure 10-29, “External Termination of GPCM Access,” as follows:

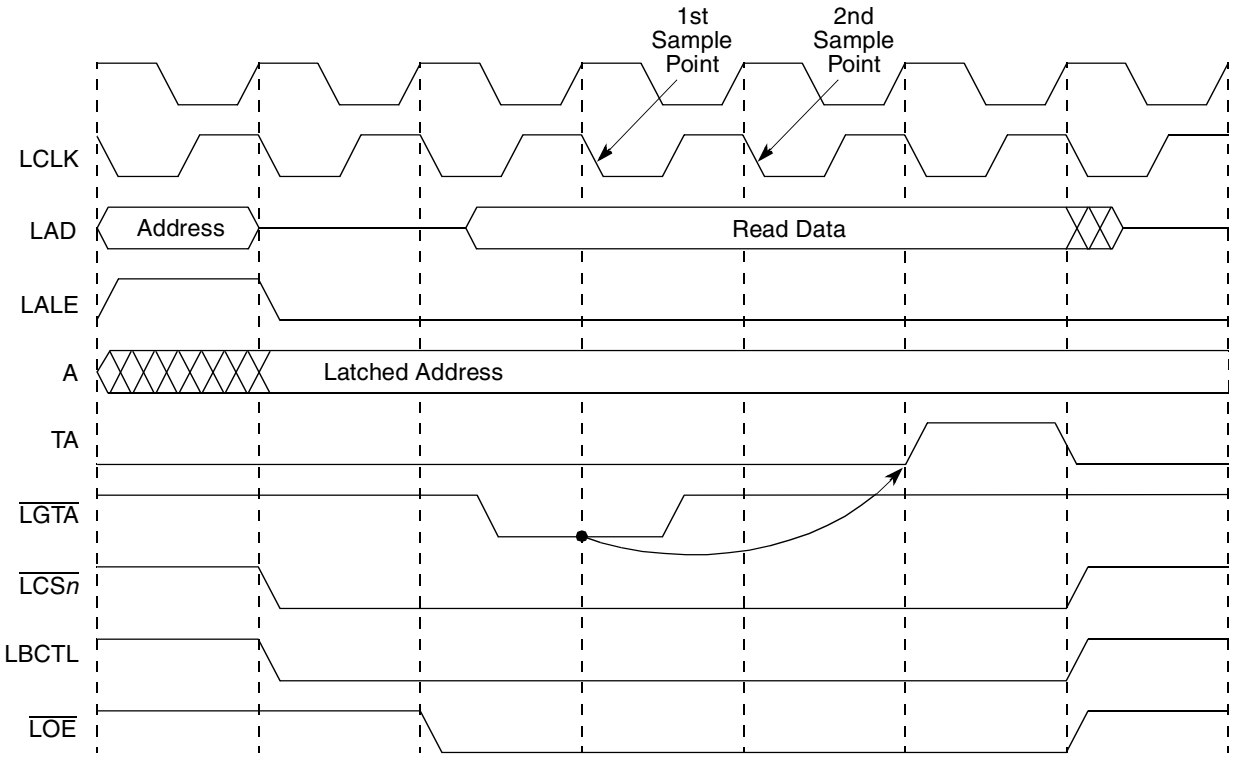

Figure 10-29. External Termination of GPCM Access

10.4.3.5, 10-57	Remove Section 10.4.3.5, “Synchronous Sampling of LUPWAIT for Early Transfer Acknowledge.”

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14.4.3.9.1, 14-52	Change: • IV1 holds the least significant bytes of the initialization vector (bytes 1–8). • IV2 holds the most significant bytes of the initialization vector (bytes 9–16). to: • IV1 holds the most significant bytes of the initialization vector (bytes 1–8). • IV2 holds the least significant bytes of the initialization vector (bytes 9–16).
14.6.4.6, 14-76	In Figure 14-46, “IP Block Revision Register,” and its introductory sentence, change reset value from 0x0000_0000_0002_00A0 to 0x0000_0000_0001_00A0.
16.2.2, 16-4	In Table 16-2, “DUART Signals—Detailed Signal Descriptions,” for $\overline{\text{UART\_RTS}}$[1:2], change sentence in description from “Can be programmed to be automatically negated and asserted by either the receiver or transmitter” to “Can be programmed to be negated and asserted by either the receiver or transmitter.
16.3.1.3, 16-8	Update calculating percent error value step 1 calculation from “AFI = baud rate × 16” to “AFI = baud rate × 16 × divisor.”

Section, Page No.	Changes
19.3.7, 19-13	Add Section 19.3.7, “QUICC Engine Serial Interrupt Mask Register (CESIMR),” as follows:

19.3.7 QUICC Engine Serial Interrupt Mask Register (CESIMR)

These registers enable the QUICC Engine RISC to respond to an interrupt generated by the QUICC Engine peripherals, off-loading this task from the core processor. An interrupt request from a QUICC Engine peripheral (if unmasked in CESIMR register) triggers the execution of a microcode interrupt routine handler on the QUICC Engine RISC. Each bit in the register corresponds to a specific QUICC Engine peripheral. The request generated by this register has the SNUM=0xE1.

Offset QUICC Engine base address + 0x00128 Access: Read/Write

	0	1	2	3	4	5	6	7	8	12	13	14	15
R W	UCC1	UCC2	UCC3	UCC4	UCC5	UCC6	UCC7	UCC8	—		PTP2	PTP1	RTC
Reset	All zeros												

	16	17	18	19	20	21	22	23	24	31
R W	—	USB	SPI1	SPI2	MCC1	MCC2	—		—	
Reset	All zeros									

Figure 19-9. QUICC Engine Serial Interrupt Request Mask Register (CESIMR)

Table 19-12. CESIMR Field Descriptions

Bits	Name	Description
0–23	All bits	Enable request to QUICC Engine block if relevant interrupt signal is asserted (as marked in Figure 19-9). The reason for the interrupt is determined after reading the relevant event register through the serial bus.
24-31	—	Reserved

19.3.8, 19-14 Add Section 19.3.8, “QUICC Engine Interrupt from Serial Event/Mask Register (CEISER/CEISMR),” as follows:

19.3.8 QUICC Engine Interrupt from Serial Event/Mask Register (CEISER/CEISMR)

This set of registers is used to issue and mask interrupts which are related to SNUM=0xE1 (See Section 19.3.7, “QUICC Engine Serial Interrupt Mask Register (CESIMR)”). Event bits are cleared by the core processor by writing 1 to the appropriate bit in the event register.

Figure 19-10 shows the CEISER.

Offset QUICC Engine base address + 0x001BC Access: w1c

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	ISE0	ISE1	ISE2	ISE3	ISE4	ISE5	ISE6	ISE7	ISE8	ISE9	ISE10	ISE11	ISE12	ISE13	ISE14	ISE15
W	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c
Reset	All zeros															

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	ISE16	ISE17	ISE18	ISE19	ISE20	ISE21	ISE22	ISE23	ISE24	ISE25	ISE26	ISE27	ISE28	ISE29	ISE30	ISE31
W	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c
Reset	All zeros															

Figure 19-10. QUICC Engine Interrupt from Serial Event Register (CEISER)

Table 19-13 shows the CEISER field descriptions.

Table 19-13. CEISER Field Descriptions

Bits	Name	Description
0–31	ISE0–ISE31	Interrupt from Serial Event bit 0-31. 0 No event 1 An event has occurred. This bit is set by writing a 1 from the spr bus, and is cleared by writing a 1 from the slave bus

Figure 19-11 shows the CEISMR.

Offset QUICC Engine base address + 0x001C0 Access: Read/Write

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R W	ISM0	ISM1	ISM2	ISM3	ISM4	ISM5	ISM6	ISM7	ISM8	ISM9	ISM10	ISM11	ISM12	ISM13	ISM14	ISM15
Reset	All zeros															

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R W	ISM16	ISM17	ISM18	ISM19	ISM20	ISM21	ISM22	ISM23	ISM24	ISM25	ISM26	ISM27	ISM28	ISM29	ISM30	ISM31
Reset	All zeros															

Figure 19-11. QUICC Engine Interrupt from Serial Mask Register (CEISMR)

Table 19-14 shows the CEISMR field descriptions.

Table 19-14. CEISMR Field Descriptions

Bits	Name	Description
0–31	ISM0–ISM31	QUICC Engine Interrupt from Serial Mask bit 0-31. 0 No Mask 1 Mask event bit. No interrupt occurs if this bit is set, regardless of the state of the appropriate interrupt from serial event bit in the CEISER register.

19.4.5, 19-11	Remove the note above Figure 19-6, “IRAM Address Register (IADD).”
19.4.9, 19-15	In Table 19-14, “CETSCR Field Descriptions,” add the following to CETPS1 and CETPS2 field descriptions: “This field can also be used to pre-scale an external clock, if it is configured as the clock source. The first increment of the timer is after (CETPS1 + 1) clocks. It is only starting from the second increment that the timer increments after (CETPS1 +2) clocks for each single increment.”
19.5.1, 19-18	In Table 19-15, “RISC Timer Table Parameter RAM,” modify footnote to say “Offset from timer base address (0x8A00).”
19.7, 19-21	In Table 19-17, “SNUM Table,” add “CESIMR Interrupt” at SNUM = 0xE1.
20.7, 20-24	Change title of Table 20-12, “BRGCx Field Descriptions,” to “BRGC*n* Field Descriptions,” and remove cross-reference from EXTC (bits 16–17) field description.
20.8, 20-26	Modify the last paragraph to say the following: “Note that the UCC associated with this BRG must be programmed to UART mode and select the 16· option for TDCR and RDCR in the general UCC mode register low. Input frequencies such as 1.8432, 3.68, 7.36, and 14.72 MHz should be used.”
20.9, 20-27	Change “GSMRx” to “GUMRx” in AsyncBaudRate equation and the introductory text to the “Typical Baud Rates for Asynchronous Communication,” which now reads as follows: “Table 20-14 lists typical bit rates of asynchronous communication. Note that here the internal clock rate is assumed to be 16 × the baud rate; that is, GUMRx_L[TDCR] = GUMRx_L[RDCR] = 0b10.”
21.1.3.3, 21-4	Remove the following sentence from the last paragraph, “The maximum sustained data rate that the SPI supports is QUICC Engine clk/50.”

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21.4.1, 21-18	In Table 21-8, “Rx/Tx Bus Mode Register Field Descriptions,” modify CETM bit description to read as follows: “This is useful to mark on the bus the transactions initiated by the QUICC Engine block for debug purposes. See the “Debug Configuration” subsection in your device reference manual. The level of this bit is reflected on the main system bus on signal M1SRCID4 or M2SRCID4 or LSRCID4 depending on the actual external bus where the transaction occurs.”
22.8, 22-15	Add Section 22.8, “Reconfiguring the UCC,” and Section 22.9, “Saving Power,” as follows:

22.8 Reconfiguring the UCC

The proper reconfiguration sequence must be followed for UCC parameters that cannot be changed dynamically. The steps in the following sections show how to disable, reconfigure and re-enable a UCC to ensure that buffers currently in use are properly closed before reconfiguring the UCC and that subsequent data goes to or from new buffers according to the new configuration.

Modifying parameter RAM does not require the UCC to be fully disabled. See the parameter RAM description for when values can be changed. To disable all peripheral controllers, set CECR[RST] to reset the entire QUICC Engine module.

22.8.1 General Reconfiguration Sequence for a UCC Transmitter

A UCC transmitter can be reconfigured by following these general steps:

1. If the UCC is sending data, issue a STOP TRANSMIT command. Transmission should stop smoothly. If the UCC is not transmitting (no TxBDs are ready or the GRACEFUL STOP TRANSMIT command has been issued and completed) or the INIT TX PARAMETERS command is issued, the STOP TRANSMIT command is not required.
2. Clear GUMR_L[ENT] to disable the UCC transmitter and put it in reset state.
3. Modify UCC Tx parameters or parameter RAM. To switch protocols or restore the initial Tx parameters, issue an INIT TX PARAMETERS command.
4. If an INIT TX PARAMETERS command was not issued in step 3, issue a RESTART TRANSMIT command.
5. Set GUMR_L[ENT]. Transmission begins using the TxBD pointed to by TBPTR, assuming the R bit is set.

22.8.2 Reset Sequence for a UCC Transmitter

The following steps reinitialize a UCC transmit parameters to the reset state:

1. Clear GUMR_L[ENT].
2. Make any modifications then issue the INIT TX PARAMETERS command.
3. Set GUMR_L[ENT].

22.8.3 General Reconfiguration Sequence for a UCC Receiver

A UCC receiver can be reconfigured by following these steps:

1. Clear GUMR_L[ENR]. The UCC receiver is now disabled and put in a reset state. If a protocol switch is performed from fast protocol, follow step 2 in Section 2.8.5, “Switching Protocols.”
2. Modify UCC Rx parameters or parameter RAM. To switch protocols or restore Rx parameters to their initial state, issue an INIT RX PARAMETERS command.
3. If the INIT RX PARAMETERS command was not issued in step 2, issue an ENTER HUNT MODE command.
4. Set GUMR_L[ENR]. Reception begins using the RxBD pointed to by RBPTR, assuming the E bit is set.

22.8.4 Reset Sequence for a UCC Receiver

To reinitialize the UCC receiver to the state it was in after reset, follow these steps:

1. Clear GUMR_L[ENR].
2. Make any modifications then issue the INIT RX PARAMETERS command.
3. Set GUMR_L[ENR].

22.8.5 Switching Protocols

To switch a UCC’s protocol without resetting the board or affecting other UCCs, follow these steps:

1. Clear GUMR_L[ENT, ENR].
2. If a protocol switch is preformed from fast protocol: Issue the Pushsched host command for UCC Transmitter (CECDR value 0x80). Issue the Pushsched host command for UCC Receiver (CECDR value 0x82).
3. Make protocol changes in the GUMR and additional parameters then issue the INIT TX and RX PARAMETERS command to initialize both Tx and Rx parameters.
4. Set GUMR_L[ENT, ENR] to enable the UCC with the new protocol.

22.9 Saving Power

To save power when not in use, a UCC can be disabled by clearing GUMR_L[ENT, ENR].

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23.1, 23-1	In the features list, remove bullet “Supports automatic control of the $\overline{\text{RTS}}$, $\overline{\text{CTS}}$, and $\overline{\text{CD}}$ modem signals”
23.4.1, 23-12	In Table 23-5, “RBMRx /TBMRx Field Descriptions,” modify CETM bit description to read as follows: “This is useful to mark on the bus the transactions initiated by the QUICC Engine block for debug purposes. See the “Debug Configuration” subsection in your device reference manual. The level of this bit is reflected on the main system bus on signal M1SRCID4 or M2SRCID4 or LSRCID4 depending on the actual external bus where the transaction occurs.”
24.3.2, 24-6	In Table 24-3, “UART-Specific UCC Parameter RAM Memory Map,” change “datalength (5–9)” to “datalength (5–8)” in **MAX_IDL**.
24.5.4, 24-22	Last sentence now reads as follows: “To reduce this latency, set GUMRx_H[TFL] to decrease the FIFO size to one character before enabling the transmitter.”
24.5.4, 24-22	In Table 24-13, “TOSEQ Field Descriptions,” change CT (bit 4) field description to the following: “Clear-to-send lost. Operates only if the UCC monitors $\overline{\text{CTS}}$ (GUMR*x*_L[DIAG]). The RISC sets this bit if $\overline{\text{CTS}}$ negates when the TOSEQ character is sent. If $\overline{\text{CTS}}$ negates and the TOSEQ character is sent during a buffer transmission, the TxBD[CT] status bit is also set.”
24.18.3, 24-32	In Table 24-24, “UPSMR Field Descriptions,” add the following note to NBO (bit 15) field description: “In HDLC nibble mode, GUMR[RTSM] must be set for internal loopback mode.”
26.4.2.1, 26-8	In Table 26-2, “GUMR (in Fast Mode) Register Field Descriptions,” add the following note to CDP (bit 5) field description: “This bit must be cleared if this UCC is used with the TSA in HDLC mode.”
26.4.2.1, 26-10	Add Table 26-3, “GUMR $\overline{\text{CTS}}$ and $\overline{\text{CD}}$—Pulse and Sampling Settings,” as follows:

Table 26-3. GUMR $\overline{\text{CTS}}$ and $\overline{\text{CD}}$—Pulse and Sampling Settings

	TSA and Transparent	TSA and HDLC	NMSI and Transparent	NMSI and HDLC	UCC[1] Internal Loopback	ISDN-D IDL
GUMR[CDP]	1	0	0	0	—	0
GUMR[CTSP]	1	x	0	0	0	0
GUMR[CDS]	1	x	x	x	1	1
GUMR[CTSS]	1	x	x	x	x	1

[1] Note that in HDLC Nibble mode, GUMR[RTSM] must be set for internal loopback mode.

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26.4.6, 26-12	In Table 26-3, “RBMRx/TBMRx Field Descriptions,” modify CETM bit description to read as follows: “This is useful to mark on the bus the transactions initiated by the QUICC Engine block for debug purposes. See the “Debug Configuration” subsection in your device reference manual.
29.4.17.2, 29-27	Change the value for GUMR[DIAG] from 10 to 11 in the following sentence: “For echo and loopback at the same time set GUMR[DIAG]=11 and UPSMR[RLPB]=0.”
29.5.1.3, 29-32	In Figure 29-15, “Ethernet Status Register (UCCS),” update offset address from “UCCx_base + 0x17 UCCS” to “UCCx_base+0x18 UCCS.”
29.5.3.10, 29-71	Update the first paragraph to say the following: “For every Rx queue, there are 16 bytes in the RxBD parameter table and there are also 4 prefetched RxBDs (4 × 8 bytes = 32 bytes) used by the QUICC Engine block. Therefore it is necessary to allocate space in memory of the size ((16 + 32) × number of Rx Queues) bytes using the RBDQPTR field in the Rx global parameter RAM. The RxBD parameter table is described in Table 29-37 with 16 bytes for each Rx queue. The remaining space in internal memory is 32 bytes of prefetched RxBD for each queue. As described in Table 29-37, the user is only required to initialize the External BD ringn base pointer. The other parameters are initialized by the QUICC Engine block.”
29.7, 29-88	Modify sentence, “The firmware counters are updated if UPSMR[MON] is set by the user” to say, “The firmware counters are updated if UPSMR[HSE] is set by the user.”
30.2.14.1.1, 30-24	Replace incomplete sentence, “If the scale factor is not zero the offset calculation for each VCLT is different and has...” with cross-reference to Table 30-26, “Address Look-Up Table.”
30.3.4.1, 30-66	In Table 30-31, “RCT Field Descriptions,” modify CETM bit description to read as follows: “This is useful to mark on the bus the transactions initiated by the QUICC Engine block for debug purposes. See the “Debug Configuration” subsection in your device reference manual. The level of this bit is reflected on the main system bus on signal M1SRCID4 or M2SRCID4 or LSRCID4 depending on the actual external bus where the transaction occurs.”
30.3.4.2, 30-70	In Table 30-34, “TCT Field Descriptions,” modify CETM bit description to read as follows: “This is useful to mark on the bus the transactions initiated by the QUICC Engine block for debug purposes. See the “Debug Configuration” subsection in your device reference manual.

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	The level of this bit is reflected on the main system bus on signal M1SRCID4 or M2SRCID4 or LSRCID4 depending on the actual external bus where the transaction occurs.”
30.3.8, 30-95	In Table 30-50, “V-TCT Field Descriptions,” modify CETM bit description to read as follows: “This is useful to mark on the bus the transactions initiated by the QUICC Engine block for debug purposes. See the “Debug Configuration” subsection in your device reference manual. The level of this bit is reflected on the main system bus on signal M1SRCID4 or M2SRCID4 or LSRCID4 depending on the actual external bus where the transaction occurs.”
31.3.4, 31-9	In Table 31-1, “SPHY Related Modes,” change the row field setting names to UPUC[TMP], UPUC[TSP], and UPUC[TB2B].
Chapter 34, 34-1	Modify the first paragraph to read as follows: “The QUICC multi-channel controller (QMC) functionality can emulate up to 64 time-division serial channels using a single unified communication controller (UCC) and a time-division multiplexed (TDM) physical interface. Up to 2 UCCs can be configured to QMC functionality. Each UCC has its own parameter table and the channel’s specific parameters. Each UCC also has its own event register, so the functionality of each UCC is orthogonal to that of adjacent UCCs.”
34.3.4.1.2, 34-18	In Table 34-6, “TSTATE Field Descriptions (HDLC),” modify CETM bit description to read as follows: “This is useful to mark on the bus the transactions initiated by the QUICC Engine block for debug purposes. See the “Debug Configuration” subsection in your device reference manual. The level of this bit is reflected on the main system bus on signal M1SRCID4 or M2SRCID4 or LSRCID4 depending on the actual external bus where the transaction occurs.”
34.3.4.1.4, 34-19	In Table 34-7, “RSTATE Field Descriptions (HDLC),” modify CETM bit description to read as follows: “This is useful to mark on the bus the transactions initiated by the QUICC Engine block for debug purposes. See the “Debug Configuration” subsection in your device reference manual. The level of this bit is reflected on the main system bus on signal M1SRCID4 or M2SRCID4 or LSRCID4 depending on the actual external bus where the transaction occurs.”
34.3.4.2.2, 34-22	In Table 34-10, “TSTATE Field Descriptions (Transparent Mode),” modify CETM bit description to read as follows: “This is useful to mark on the bus the transactions initiated by the QUICC Engine block for debug purposes. See the “Debug Configuration” subsection in your device reference manual.

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	The level of this bit is reflected on the main system bus on signal M1SRCID4 or M2SRCID4 or LSRCID4 depending on the actual external bus where the transaction occurs.”
34.3.4.2.5, 34-26	In Table 34-11, “RSTATE Field Descriptions (Transparent),” modify CETM bit description to read as follows: “This is useful to mark on the bus the transactions initiated by the QUICC Engine block for debug purposes. See the “Debug Configuration” subsection in your device reference manual. The level of this bit is reflected on the main system bus on signal M1SRCID4 or M2SRCID4 or LSRCID4 depending on the actual external bus where the transaction occurs.”
Chapter 36	Change “DPRAM” or “dual-port RAM” to “multi-user RAM” throughout.
36.4.6, 36-16	In Table 36-8, “RBMR and TBMR Fields,” modify CETM bit description to read as follows: “This is useful to mark on the bus the transactions initiated by the QUICC Engine block for debug purposes. See the “Debug Configuration” subsection in your device reference manual. The level of this bit is reflected on the main system bus on signal M1SRCID4 or M2SRCID4 or LSRCID4 depending on the actual external bus where the transaction occurs.”
36.7, 36-34	In Table 36-21, “USB Controller Transmission Errors,” remove the row for “Tx data not ready”.

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