This errata describes corrections to the *Programming Environments Manual for 32-Bit Implementations of the PowerPC Architecture, Rev 2*. For convenience, the section number and page number of the errata item in the programming manual are provided.

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In Table 4-37, add the following two sentences to the end of the **dcbi** operation:

Note that some implementations may execute this instruction as a **dcbf**. This instruction is optional.

Replace the fourth paragraph with the following:

The segment information, used to generate the interim virtual addresses, is stored as segment descriptors. These descriptors may reside in on-chip segment registers (32-bit implementations).

Remove this section.

Replace the target address CTR || 0b00 of **bcctr** with CTR[0–29] || 0b00. The code sequence should read as follows:

```plaintext
cond_ok ← BO[0] | (CR[BI] ≡ BO[1])
if cond_ok then
  NIA ← iea CTR[0–29] || 0b00
if LK then LR ← iea CIA + 4
```

In the first sentence after Table 8-9, replace the target address CTR || 0b00 of **bcctr** with CTR[0–29] || 0b00. The sentence should read as follows:

The branch target address is CTR[0–29] || 0b00.

Replace the target address LR || 0b00 of **bclr** with CTR[0–29] || 0b00, the code sequence should read as follows:

```plaintext
if ¬ BO[2] then CTR ← CTR – 1
ctr_ok ← BO[2] | ((CTR ≠ 0) ⊕ BO[3])
cond_ok ← BO[0] | (CR[BI] ≡ BO[1])
if ctr_ok & cond_ok then
  NIA ← iea LR[0–29] || 0b00
if LK then LR ← iea CIA + 4
```

In the first sentence after Table 8-11, replace the target address LR || 0b00 of **bclr** with LR[0–29] || 0b00. The sentence should read as follows:

The branch target address is LR[0–29] || 0b00.

Add the following two sentences to the end of the **dcbi** description:

Note that some implementations may execute this instruction as a **dcbf**. This instruction is optional.
<table>
<thead>
<tr>
<th>Section, Page No.</th>
<th>Changes</th>
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<tbody>
<tr>
<td>8.2, 8-44</td>
<td>After the third paragraph, add the following paragraph: The coherency state of a cache block after a write access (caused by a <code>dcbst</code>) is implementation-dependent. For example, some implementations may mark the cache block exclusive, where others may mark it invalid.</td>
</tr>
<tr>
<td>8.2, 8-163</td>
<td>Replace the first sentence of the only paragraph, the sentence should read as follows: The contents of <code>rS</code> are shifted right the number of bits specified by <code>rB[27–31]</code>.</td>
</tr>
</tbody>
</table>
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