

# CM RTCESL 4.7.1 Release Notes

## 1 Overview

These release notes are for the Arm<sup>®</sup> Cortex<sup>®</sup>-M0+, Cortex-M4(F), Cortex-M7(F), and Cortex-M33(F) Real-Time Control Embedded Software Libraries release 4.7.1

The purpose of this release is to publish all Keil libraries recompiled in Keil IDE compiler version.

## Contents

1	Overview .....	1
2	What is new .....	2
3	Description .....	2



## 2 What is new

All Keil libraries are recompiled by new compiler version.

## 3 Description

This release of RTCESL supports the following platforms:

- Arm Cortex-M0+ (optionally the MMDVSQ peripheral).
- Arm Cortex-M33NODSP. The DSP is not required (optionally the PQ module).
- Arm Cortex-M33 requires the DSP extension (optionally the PQ module).
- Arm Cortex-M33F requires the DSP extension and the FPU (optionally the PQ module).
- Arm Cortex-M4 requires the DSP extension.
- Arm Cortex-M4F requires the DSP extension and the FPU.
- Arm Cortex-M7 requires the DSP extension (optionally the RAM relocation support).
- Arm Cortex-M7F requires the DSP extension and the FPU (optionally the RAM relocation support).

It contains the following libraries:

- MLIB
- GFLIB
- GDFLIB
- GMCLIB
- AMCLIB
- PCLIB

It is compiled using the following IDEs:

- MCUX 11.4.0 [Build 6224] IDE.
- IAR 9.10.2. 39460IDE.
- Keil 5.37.0.2 IDE.

The following optimization is used:

- The accuracy is not guaranteed for some of the float functions in this version.
- The maximum speed optimization is used for all libraries on all compilers.

**The following algorithms are in the release for CM33F, CM4F, and CM7F cores (16-/32-bit fixed-point and 32-bit single-precision floating-point, non-float variants CM33, CM33NODSP, CM4 and CM7 do not include the functions that require the FPU):**

AMCLIB_ACIMCtrlMTPAInit_FLT	GDFLIB_FilterMA_F16
AMCLIB_ACIMCtrlMTPA_FLT	GDFLIB_FilterMA_FLT
AMCLIB_ACIMRotFluxObsrvInit_FLT	
AMCLIB_ACIMRotFluxObsrv_FLT	GFLIB_Acos_F16
AMCLIB_ACIMSpeedMRASInit_FLT	GFLIB_Acos_FLT
AMCLIB_ACIMSpeedMRAS_FLT	GFLIB_Asin_F16
AMCLIB_AngleTrackObsrvInit_A32	GFLIB_Asin_FLT
AMCLIB_AngleTrackObsrvInit_F16	GFLIB_AtanYX_A32f
AMCLIB_AngleTrackObsrv_A32ff	GFLIB_AtanYX_F16
AMCLIB_AngleTrackObsrv_F16	GFLIB_AtanYX_FLT
AMCLIB_CtrlFluxWkngInit_F16	GFLIB_Atan_A32f
AMCLIB_CtrlFluxWkngInit_FLT	GFLIB_Atan_F16
AMCLIB_CtrlFluxWkng_F16	GFLIB_Atan_FLT
AMCLIB_CtrlFluxWkng_FLT	GFLIB_Cos_F16
AMCLIB_PMSMBemfObsrvABInit_F16	GFLIB_Cos_FLT
AMCLIB_PMSMBemfObsrvABInit_FLT	GFLIB_Cos_FLTa
AMCLIB_PMSMBemfObsrvAB_F16	GFLIB_CtrlBetaIPDpAWInit_F16
AMCLIB_PMSMBemfObsrvAB_FLT	GFLIB_CtrlBetaIPDpAWInit_FLT
AMCLIB_PMSMBemfObsrvDQInit_A32fff	GFLIB_CtrlBetaIPDpAW_F16
AMCLIB_PMSMBemfObsrvDQInit_F16	GFLIB_CtrlBetaIPDpAW_FLT
AMCLIB_PMSMBemfObsrvDQ_A32fff	GFLIB_CtrlBetaIPpAWInit_F16
AMCLIB_PMSMBemfObsrvDQ_F16	GFLIB_CtrlBetaIPpAWInit_FLT
AMCLIB_TrackObsrvInit_A32af	GFLIB_CtrlBetaIPpAW_F16
AMCLIB_TrackObsrvInit_F16	GFLIB_CtrlBetaIPpAW_FLT
AMCLIB_TrackObsrv_A32af	GFLIB_CtrlPIDpAWInit_F16
AMCLIB_TrackObsrv_F16	GFLIB_CtrlPIDpAWInit_FLT
	GFLIB_CtrlPIDpAW_F16
	GFLIB_CtrlPIDpAW_FLT
GDFLIB_FilterExpInit_F16	GFLIB_CtrlPIpAWInit_F16
GDFLIB_FilterExpInit_FLT	GFLIB_CtrlPIpAWInit_FLT
GDFLIB_FilterExp_F16	GFLIB_CtrlPIpAW_F16
GDFLIB_FilterExp_FLT	GFLIB_CtrlPIpAW_FLT
GDFLIB_FilterIIR1Init_F16	GFLIB_CtrlPIpAW_FLT
GDFLIB_FilterIIR1Init_FLT	GFLIB_DFlexRampCalcIncr_F16
GDFLIB_FilterIIR1_F16	GFLIB_DFlexRampCalcIncr_FLT
GDFLIB_FilterIIR1_FLT	GFLIB_DFlexRampInit_F16
GDFLIB_FilterIIR2Init_F16	GFLIB_DFlexRampInit_FLT
GDFLIB_FilterIIR2Init_FLT	GFLIB_DFlexRamp_F16
GDFLIB_FilterIIR2_F16	GFLIB_DFlexRamp_FLT
GDFLIB_FilterIIR2_FLT	GFLIB_DRampInit_F16
GDFLIB_FilterIIR3Init_F16	GFLIB_DRampInit_F32
GDFLIB_FilterIIR3Init_FLT	GFLIB_DRampInit_FLT
GDFLIB_FilterIIR3_F16	GFLIB_DRamp_F16
GDFLIB_FilterIIR3_FLT	GFLIB_DRamp_F32
GDFLIB_FilterIIR4Init_F16	GFLIB_DRamp_FLT
GDFLIB_FilterIIR4Init_FLT	GFLIB_FlexRampCalcIncr_F16
GDFLIB_FilterIIR4_F16	GFLIB_FlexRampCalcIncr_FLT
GDFLIB_FilterIIR4_FLT	GFLIB_FlexRampInit_F16
GDFLIB_FilterMAInit_F16	GFLIB_FlexRampInit_FLT
GDFLIB_FilterMAInit_FLT	GFLIB_FlexRamp_F16

GFLIB_FlexRamp_FLT	GMCLIB_DTCompLut1D_F16
GFLIB_FlexSRampCalcIncr_F16	GMCLIB_ElimDcBusRipFOC_F16
GFLIB_FlexSRampCalcIncr_FLT	GMCLIB_ElimDcBusRipFOC_F16fff
GFLIB_FlexSRampInit_F16	GMCLIB_ElimDcBusRip_F16fff
GFLIB_FlexSRampInit_FLT	GMCLIB_ElimDcBusRip_F16sas
GFLIB_FlexSRamp_F16	GMCLIB_ParkInv_F16
GFLIB_FlexSRamp_FLT	GMCLIB_ParkInv_FLT
GFLIB_Hyst_F16	GMCLIB_Park_F16
GFLIB_Hyst_FLT	GMCLIB_Park_FLT
GFLIB_IntegratorInit_F16	GMCLIB_SvmDpwm_F16
GFLIB_IntegratorInit_FLT	GMCLIB_SvmExDpwm_F16
GFLIB_Integrator_F16	GMCLIB_SvmIct_F16
GFLIB_Integrator_FLT	GMCLIB_SvmStd_F16
GFLIB_Limit_F16	GMCLIB_SvmStdShifted_F16
GFLIB_Limit_F32	GMCLIB_SvmU0n_F16
GFLIB_Limit_FLT	GMCLIB_SvmU7n_F16
GFLIB_LowerLimit_F16	
GFLIB_LowerLimit_F32	MLIB_AbsSat_F16
GFLIB_LowerLimit_FLT	MLIB_AbsSat_F32
GFLIB_Lut1DInit_FLT	MLIB_Abs_F16
GFLIB_Lut1D_F16	MLIB_Abs_F32
GFLIB_Lut1D_F32	MLIB_Abs_FLT
GFLIB_Lut1D_FLT	MLIB_Add4Sat_F16
GFLIB_LutPer1DInit_FLT	MLIB_Add4Sat_F32
GFLIB_LutPer1D_F16	MLIB_Add4_F16
GFLIB_LutPer1D_F32	MLIB_Add4_F32
GFLIB_LutPer1D_FLT	MLIB_Add4_FLT
GFLIB_RampInit_F16	MLIB_AddSat_F16
GFLIB_RampInit_F32	MLIB_AddSat_F32
GFLIB_RampInit_FLT	MLIB_Add_A32as
GFLIB_Ramp_F16	MLIB_Add_A32ss
GFLIB_Ramp_F32	MLIB_Add_F16
GFLIB_Ramp_FLT	MLIB_Add_F32
GFLIB_Sin_F16	MLIB_Add_FLT
GFLIB_Sin_FLT	MLIB_Clb_U16l
GFLIB_Sin_FLTa	MLIB_Clb_U16s
GFLIB_Sqrt_F16	MLIB_ConvSc_A32ff
GFLIB_Sqrt_F16l	MLIB_ConvSc_F16ff
GFLIB_Sqrt_FLT	MLIB_ConvSc_F32ff
GFLIB_Tan_F16	MLIB_ConvSc_FLTaf
GFLIB_Tan_FLT	MLIB_ConvSc_FLTlf
GFLIB_Tan_FLTa	MLIB_ConvSc_FLTsf
GFLIB_UpperLimit_F16	MLIB_Conv_A32f
GFLIB_UpperLimit_F32	MLIB_Conv_F16f
GFLIB_UpperLimit_FLT	MLIB_Conv_F16l
GFLIB_VectorLimit1_F16	MLIB_Conv_F32f
GFLIB_VectorLimit1_FLT	MLIB_Conv_F32s
GFLIB_VectorLimit_F16	MLIB_Conv_FLTa
GFLIB_VectorLimit_FLT	MLIB_Conv_FLTl
	MLIB_Conv_FLTs
GMCLIB_ClarkInv_F16	MLIB_Div1QSat_A32as
GMCLIB_ClarkInv_FLT	MLIB_Div1QSat_F16
GMCLIB_Clark_F16	MLIB_Div1QSat_F16l1
GMCLIB_Clark_FLT	MLIB_Div1QSat_F16ls
GMCLIB_DecouplingPMSM_F16	MLIB_Div1QSat_F32
GMCLIB_DecouplingPMSM_FLT	MLIB_Div1QSat_F32ls

MLIB_Div1Q_A32as	MLIB_MnacSat_F32
MLIB_Div1Q_A3211	MLIB_MnacSat_F321ss
MLIB_Div1Q_A321s	MLIB_Mnac_A32ass
MLIB_Div1Q_A32ss	MLIB_Mnac_F16
MLIB_Div1Q_F16	MLIB_Mnac_F32
MLIB_Div1Q_F1611	MLIB_Mnac_F321ss
MLIB_Div1Q_F161s	MLIB_Mnac_FLT
MLIB_Div1Q_F32	MLIB_Msu4RndSat_F16
MLIB_Div1Q_F321s	MLIB_Msu4RndSat_F32
MLIB_DivSat_A32as	MLIB_Msu4Rnd_F16
MLIB_DivSat_F16	MLIB_Msu4Rnd_F32
MLIB_DivSat_F1611	MLIB_Msu4Sat_F32ssss
MLIB_DivSat_F161s	MLIB_Msu4_F32ssss
MLIB_DivSat_F32	MLIB_Msu4_FLT
MLIB_DivSat_F321s	MLIB_MsuRndSat_F16
MLIB_Div_A32as	MLIB_MsuRndSat_F32
MLIB_Div_A3211	MLIB_MsuRndSat_F3211s
MLIB_Div_A321s	MLIB_MsuRnd_A32ass
MLIB_Div_A32ss	MLIB_MsuRnd_F16
MLIB_Div_F16	MLIB_MsuRnd_F32
MLIB_Div_F1611	MLIB_MsuRnd_F3211s
MLIB_Div_F161s	MLIB_MsuSat_F16
MLIB_Div_F32	MLIB_MsuSat_F32
MLIB_Div_F321s	MLIB_MsuSat_F321ss
MLIB_Div_FLT	MLIB_Msu_A32ass
MLIB_Log2_U16	MLIB_Msu_F16
MLIB_Mac4RndSat_F16	MLIB_Msu_F32
MLIB_Mac4RndSat_F32	MLIB_Msu_F321ss
MLIB_Mac4Rnd_F16	MLIB_Msu_FLT
MLIB_Mac4Rnd_F32	MLIB_MulNegRndSat_A32
MLIB_Mac4Sat_F32ssss	MLIB_MulNegRndSat_F16as
MLIB_Mac4_F32ssss	MLIB_MulNegRnd_A32
MLIB_Mac4_FLT	MLIB_MulNegRnd_F16
MLIB_MacRndSat_F16	MLIB_MulNegRnd_F16as
MLIB_MacRndSat_F32	MLIB_MulNegRnd_F32
MLIB_MacRndSat_F3211s	MLIB_MulNegRnd_F321s
MLIB_MacRnd_A32ass	MLIB_MulNegSat_A32
MLIB_MacRnd_F16	MLIB_MulNegSat_F16as
MLIB_MacRnd_F32	MLIB_MulNeg_A32
MLIB_MacRnd_F3211s	MLIB_MulNeg_F16
MLIB_MacSat_F16	MLIB_MulNeg_F16as
MLIB_MacSat_F32	MLIB_MulNeg_F32
MLIB_MacSat_F321ss	MLIB_MulNeg_F32ss
MLIB_Mac_A32ass	MLIB_MulNeg_FLT
MLIB_Mac_F16	MLIB_MulRndSat_A32
MLIB_Mac_F32	MLIB_MulRndSat_F16
MLIB_Mac_F321ss	MLIB_MulRndSat_F16as
MLIB_Mac_FLT	MLIB_MulRndSat_F32
MLIB_MnacRndSat_F16	MLIB_MulRndSat_F321s
MLIB_MnacRndSat_F32	MLIB_MulRnd_A32
MLIB_MnacRndSat_F3211s	MLIB_MulRnd_F16
MLIB_MnacRnd_A32ass	MLIB_MulRnd_F16as
MLIB_MnacRnd_F16	MLIB_MulRnd_F32
MLIB_MnacRnd_F32	MLIB_MulRnd_F321s
MLIB_MnacRnd_F3211s	MLIB_MulSat_A32
MLIB_MnacSat_F16	MLIB_MulSat_F16

MLIB\_MulSat\_F16as  
 MLIB\_MulSat\_F32  
 MLIB\_MulSat\_F32ss  
 MLIB\_Mul\_A32  
 MLIB\_Mul\_F16  
 MLIB\_Mul\_F16as  
 MLIB\_Mul\_F32  
 MLIB\_Mul\_F32ss  
 MLIB\_Mul\_FLT  
 MLIB\_NegSat\_F16  
 MLIB\_NegSat\_F32  
 MLIB\_Neg\_F16  
 MLIB\_Neg\_F32  
 MLIB\_Neg\_FLT  
 MLIB\_Rcp1Q1\_A32s  
 MLIB\_Rcp1Q\_A32s  
 MLIB\_Rcp1\_A32s  
 MLIB\_Rcp\_A32s  
 MLIB\_RndSat\_F16l  
 MLIB\_Rnd\_F16l  
 MLIB\_Sat\_F16a  
 MLIB\_Sh1LSat\_F16  
 MLIB\_Sh1LSat\_F32  
 MLIB\_Sh1L\_F16  
 MLIB\_Sh1L\_F32  
 MLIB\_Sh1R\_F16  
 MLIB\_Sh1R\_F32  
 MLIB\_ShLBiSat\_F16  
 MLIB\_ShLBiSat\_F32  
 MLIB\_ShLBi\_F16  
 MLIB\_ShLBi\_F32  
 MLIB\_ShLSat\_F16  
 MLIB\_ShLSat\_F32  
 MLIB\_ShL\_F16  
 MLIB\_ShL\_F32  
 MLIB\_ShRBiSat\_F16  
 MLIB\_ShRBiSat\_F32  
 MLIB\_ShRbi\_F16  
 MLIB\_ShRbi\_F32  
 MLIB\_ShR\_F16

MLIB\_ShR\_F32  
 MLIB\_Sign\_F16  
 MLIB\_Sign\_F32  
 MLIB\_Sign\_FLT  
 MLIB\_Sub4Sat\_F16  
 MLIB\_Sub4Sat\_F32  
 MLIB\_Sub4\_F16  
 MLIB\_Sub4\_F32  
 MLIB\_Sub4\_FLT  
 MLIB\_SubSat\_F16  
 MLIB\_SubSat\_F32  
 MLIB\_Sub\_A32as  
 MLIB\_Sub\_A32ss  
 MLIB\_Sub\_F16  
 MLIB\_Sub\_F32  
 MLIB\_Sub\_FLT  
  
 PCLIB\_Ctrl2P2ZInit\_F16  
 PCLIB\_Ctrl2P2Z\_F16  
 PCLIB\_Ctrl3P3ZInit\_F16  
 PCLIB\_Ctrl3P3Z\_F16  
 PCLIB\_CtrlPIDInit\_F16  
 PCLIB\_CtrlPID\_F16  
 PCLIB\_CtrlPIInit\_F16  
 PCLIB\_CtrlPI\_F16  
 PCLIB\_CtrlPIandLPInit\_F16  
 PCLIB\_CtrlPIandLP\_F16

For the CM33 core with the Power Quad peripheral module :

GFLIB\_AtanYXPQ\_F16  
 GFLIB\_CosPQ\_F16  
 GFLIB\_SinPQ\_F16  
 GFLIB\_CosPQ\_FLT  
 GFLIB\_SinPQ\_FLT  
 GFLIB\_SqrtPQ\_F16l  
 GFLIB\_SqrtPQ\_F16  
 GDFLIB\_FilterIIR2InitPQ\_F16  
 GDFLIB\_FilterIIR2PQ\_F16

**The following algorithms are in the release for the CM0+ core (16-bit and 32-bit fixed-point versions):**

AMCLIB\_AngleTrackObsrvInit\_F16  
 AMCLIB\_AngleTrackObsrv\_F16  
 AMCLIB\_CtrlFluxWkngInit\_F16  
 AMCLIB\_CtrlFluxWkng\_F16  
 AMCLIB\_PMSMBemfObsrvABInit\_F16  
 AMCLIB\_PMSMBemfObsrvAB\_F16  
 AMCLIB\_PMSMBemfObsrvDQInit\_F16  
 AMCLIB\_PMSMBemfObsrvDQ\_F16  
 AMCLIB\_TrackObsrvInit\_F16

AMCLIB\_TrackObsrv\_F16  
  
 GDFLIB\_FilterExpInit\_F16  
 GDFLIB\_FilterExp\_F16  
 GDFLIB\_FilterIIR1Init\_F16  
 GDFLIB\_FilterIIR1\_F16  
 GDFLIB\_FilterIIR2Init\_F16  
 GDFLIB\_FilterIIR2\_F16  
 GDFLIB\_FilterMAInit\_F16

GDFLIB_FilterMA_F16	GMCLIB_SvmU7n_F16
GFLIB_AtanYX_F16	MLIB_AbsSat_F16
GFLIB_Atan_F16	MLIB_AbsSat_F32
GFLIB_Cos_F16	MLIB_Abs_F16
GFLIB_CtrlBetaIppAWInit_F16	MLIB_Abs_F32
GFLIB_CtrlBetaIppAW_F16	MLIB_Add4Sat_F16
GFLIB_CtrlPIpAWInit_F16	MLIB_Add4Sat_F32
GFLIB_CtrlPIpAW_F16	MLIB_Add4_F16
GFLIB_DFlexRampCalcIncr_F16	MLIB_Add4_F32
GFLIB_DFlexRampInit_F16	MLIB_AddSat_F16
GFLIB_DFlexRamp_F16	MLIB_AddSat_F32
GFLIB_DRampInit_F16	MLIB_Add_A32as
GFLIB_DRampInit_F32	MLIB_Add_A32ss
GFLIB_DRamp_F16	MLIB_Add_F16
GFLIB_DRamp_F32	MLIB_Add_F32
GFLIB_FlexRampCalcIncr_F16	MLIB_Clb_U16l
GFLIB_FlexRampInit_F16	MLIB_Clb_U16s
GFLIB_FlexRamp_F16	MLIB_Conv_F16l
GFLIB_Hyst_F16	MLIB_Conv_F32s
GFLIB_IntegratorInit_F16	MLIB_Div1QSat_A32as
GFLIB_Integrator_F16	MLIB_Div1QSat_F16
GFLIB_Limit_F16	MLIB_Div1QSat_F16l1
GFLIB_Limit_F32	MLIB_Div1QSat_F16ls
GFLIB_LowerLimit_F16	MLIB_Div1QSat_F32
GFLIB_LowerLimit_F32	MLIB_Div1QSat_F32ls
GFLIB_Lut1D_F16	MLIB_Div1Q_A32as
GFLIB_Lut1D_F32	MLIB_Div1Q_A32l1
GFLIB_LutPer1D_F16	MLIB_Div1Q_A32ls
GFLIB_LutPer1D_F32	MLIB_Div1Q_A32ss
GFLIB_RampInit_F16	MLIB_Div1Q_F16
GFLIB_RampInit_F32	MLIB_Div1Q_F16l1
GFLIB_Ramp_F16	MLIB_Div1Q_F16ls
GFLIB_Ramp_F32	MLIB_Div1Q_F32
GFLIB_Sin_F16	MLIB_Div1Q_F32ls
GFLIB_F16l	
GFLIB_Sqrt_F16	MLIB_DivSat_A32as
GFLIB_Sqrt_F16l	MLIB_DivSat_F16
GFLIB_UpperLimit_F16	MLIB_DivSat_F16l1
GFLIB_UpperLimit_F32	MLIB_DivSat_F16ls
GFLIB_VectorLimit1_F16	MLIB_DivSat_F32
	MLIB_DivSat_F32ls
GMCLIB_ClarkInv_F16	MLIB_Div_A32as
GMCLIB_Clark_F16	MLIB_Div_A32l1
GMCLIB_DecouplingPMSM_F16	MLIB_Div_A32ls
GMCLIB_DTCompLut1D_F16	MLIB_Div_A32ss
GMCLIB_ElimDcBusRipFOC_F16	MLIB_Div_F16
GMCLIB_ElimDcBusRip_F16sas	MLIB_Div_F16l1
GMCLIB_ParkInv_F16	MLIB_Div_F16ls
GMCLIB_Park_F16	MLIB_Div_F32
GMCLIB_SvmDpwm_F16	MLIB_Div_F32ls
GMCLIB_SvmExDpwm_F16	MLIB_Log2_U16
GMCLIB_SvmIct_F16	MLIB_Mac4RndSat_F16
GMCLIB_SvmStd_F16	MLIB_Mac4RndSat_F32
GMCLIB_SvmStdShifted_F16	MLIB_Mac4Rnd_F16
GMCLIB_SvmU0n_F16	MLIB_Mac4Rnd_F32

MLIB_Mac4Sat_F32ssss	MLIB_MulNegRnd_F321s
MLIB_Mac4_F32ssss	MLIB_MulNegSat_A32
MLIB_MacRndSat_F16	MLIB_MulNegSat_F16as
MLIB_MacRndSat_F32	MLIB_MulNeg_A32
MLIB_MacRndSat_F3211s	MLIB_MulNeg_F16
MLIB_MacRnd_A32ass	MLIB_MulNeg_F16as
MLIB_MacRnd_F16	MLIB_MulNeg_F32
MLIB_MacRnd_F32	MLIB_MulNeg_F32ss
MLIB_MacRnd_F3211s	MLIB_MulRndSat_A32
MLIB_MacSat_F16	MLIB_MulRndSat_F16
MLIB_MacSat_F32	MLIB_MulRndSat_F16as
MLIB_MacSat_F3211s	MLIB_MulRndSat_F32
MLIB_Mac_A32ass	MLIB_MulRndSat_F321s
MLIB_Mac_F16	MLIB_MulRnd_A32
MLIB_Mac_F32	MLIB_MulRnd_F16
MLIB_Mac_F3211s	MLIB_MulRnd_F16as
MLIB_MnacRndSat_F16	MLIB_MulRnd_F32
MLIB_MnacRndSat_F32	MLIB_MulRnd_F321s
MLIB_MnacRndSat_F3211s	MLIB_MulSat_A32
MLIB_MnacRnd_A32ass	MLIB_MulSat_F16
MLIB_MnacRnd_F16	MLIB_MulSat_F16as
MLIB_MnacRnd_F32	MLIB_MulSat_F32
MLIB_MnacRnd_F3211s	MLIB_MulSat_F32ss
MLIB_MnacSat_F16	MLIB_Mul_A32
MLIB_MnacSat_F32	MLIB_Mul_F16
MLIB_MnacSat_F3211s	MLIB_Mul_F16as
MLIB_Mnac_A32ass	MLIB_Mul_F32
MLIB_Mnac_F16	MLIB_Mul_F32ss
MLIB_Mnac_F32	MLIB_NegSat_F16
MLIB_Mnac_F3211s	MLIB_NegSat_F32
MLIB_Msu4RndSat_F16	MLIB_Neg_F16
MLIB_Msu4RndSat_F32	MLIB_Neg_F32
MLIB_Msu4Rnd_F16	MLIB_Rcp1Q1_A32s
MLIB_Msu4Rnd_F32	MLIB_Rcp1Q_A32s
MLIB_Msu4Sat_F32ssss	MLIB_Rcp1_A32s
MLIB_Msu4_F32ssss	MLIB_RcpHw1Q1_A32s
MLIB_MsuRndSat_F16	MLIB_RcpHw1Q_A32s
MLIB_MsuRndSat_F32	MLIB_RcpHw1_A32s
MLIB_MsuRndSat_F3211s	MLIB_RcpHw_A32s
MLIB_MsuRnd_A32ass	MLIB_Rcp_A32s
MLIB_MsuRnd_F16	MLIB_RndSat_F161
MLIB_MsuRnd_F32	MLIB_Rnd_F161
MLIB_MsuRnd_F3211s	MLIB_Sat_F16a
MLIB_MsuSat_F16	MLIB_Sh1LSat_F16
MLIB_MsuSat_F32	MLIB_Sh1LSat_F32
MLIB_MsuSat_F3211s	MLIB_Sh1L_F16
MLIB_Msu_A32ass	MLIB_Sh1L_F32
MLIB_Msu_F16	MLIB_Sh1R_F16
MLIB_Msu_F32	MLIB_Sh1R_F32
MLIB_Msu_F3211s	MLIB_ShLBiSat_F16
MLIB_MulNegRndSat_A32	MLIB_ShLBiSat_F32
MLIB_MulNegRndSat_F16as	MLIB_ShLBi_F16
MLIB_MulNegRnd_A32	MLIB_ShLBi_F32
MLIB_MulNegRnd_F16	MLIB_ShLSat_F16
MLIB_MulNegRnd_F16as	MLIB_ShLSat_F32
MLIB_MulNegRnd_F32	MLIB_ShL_F16



MLIB\_ShL\_F32  
 MLIB\_ShRBiSat\_F16  
 MLIB\_ShRBiSat\_F32  
 MLIB\_ShRBi\_F16  
 MLIB\_ShRBi\_F32  
 MLIB\_ShR\_F16  
 MLIB\_ShR\_F32  
 MLIB\_Sign\_F16  
 MLIB\_Sign\_F32  
 MLIB\_Sub4Sat\_F16  
 MLIB\_Sub4Sat\_F32  
 MLIB\_Sub4\_F16  
 MLIB\_Sub4\_F32  
 MLIB\_SubSat\_F16  
 MLIB\_SubSat\_F32  
 MLIB\_Sub\_A32as  
 MLIB\_Sub\_A32ss  
 MLIB\_Sub\_F16  
 MLIB\_Sub\_F32  
  
 PCLIB\_Ctrl2P2ZInit\_F16  
 PCLIB\_Ctrl2P2Z\_F16  
 PCLIB\_Ctrl3P3ZInit\_F16  
 PCLIB\_Ctrl3P3Z\_F16  
 PCLIB\_CtrlPIDInit\_F16  
 PCLIB\_CtrlPID\_F16  
 PCLIB\_CtrlPIInit\_F16  
 PCLIB\_CtrlPI\_F16  
 PCLIB\_CtrlPIandLPInit\_F16  
 PCLIB\_CtrlPIandLP\_F16  
  
 MLIB\_DivHwSat\_F16ls  
 MLIB\_DivHwSat\_F32  
 MLIB\_DivHwSat\_F32ls  
 MLIB\_DivHwSat\_F32ls  
 MLIB\_DivHw\_A32ll  
 MLIB\_DivHw\_A32ls  
 MLIB\_DivHw\_A32ss  
 MLIB\_DivHw\_F16  
 MLIB\_DivHw\_F16ll  
 MLIB\_DivHw\_F16ls  
 MLIB\_DivHw\_F32  
 MLIB\_DivHw\_F32ls  
 MLIB\_DivHw\_F32ls

For the CM0+ core with the MMDVSQ peripheral module :

AMCLIB\_PMSMBemfObsrvABHw\_F16  
 AMCLIB\_PMSMBemfObsrvDQHw\_F16  
 GFLIB\_AtanYXHw\_F16  
 GFLIB\_DFlexRampCalcIncrHw\_F16  
 GFLIB\_FlexRampCalcIncrHw\_F16  
 GFLIB\_SqrtHw\_F16  
 GFLIB\_VectorLimit1Hw\_F16  
 GMCLIB\_ElimDcBusRipFOCHw\_F16  
 GMCLIB\_ElimDcBusRipHw\_F16sas  
 MLIB\_DivHwIQSat\_F16  
 MLIB\_DivHwIQSat\_F16ll  
 MLIB\_DivHwIQSat\_F16ls  
 MLIB\_DivHwIQSat\_F32  
 MLIB\_DivHwIQSat\_F32ls  
 MLIB\_DivHwIQSat\_F32ls  
 MLIB\_DivHwIQ\_A32ll  
 MLIB\_DivHwIQ\_A32ls  
 MLIB\_DivHwIQ\_A32ss  
 MLIB\_DivHwIQ\_F16  
 MLIB\_DivHwIQ\_F16ll  
 MLIB\_DivHwIQ\_F16ls  
 MLIB\_DivHwIQ\_F32  
 MLIB\_DivHwIQ\_F32ls  
 MLIB\_DivHwIQ\_F32ls  
 MLIB\_DivHwSat\_F16  
 MLIB\_DivHwSat\_F16ll

**How to Reach Us:**

**Home Page:**

[www.nxp.com](http://www.nxp.com)

**Web Support:**

[www.nxp.com/support](http://www.nxp.com/support)

Information in this document is provided solely to enable system and software implementers to use NXP products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. NXP reserves the right to make changes without further notice to any products herein. NXP makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in NXP data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. NXP does not convey any license under its patent rights nor the rights of others. NXP sells products pursuant to standard terms and conditions of sale, which can be found at the following address: [nxp.com/SalesTermsandConditions](http://nxp.com/SalesTermsandConditions).

NXP, the NXP logo, NXP SECURE CONNECTIONS FOR A SMARTER WORLD, Freescale, and the Freescale logo are the trademarks of NXP B.V. All other product or service names are the property of their respective owners. ARM, the ARM Powered logo, and Cortex are registered trademarks of ARM Limited (or its subsidiaries) in the EU and/or elsewhere. All rights reserved.

© 2022— NXP B.V.

