

IEC60730B CM33 4.0

by: NXP Semiconductors

1 Introduction

IEC60730B_CM33_4_0 is the actual version of the core self-test library for NXP devices with the CM33 core. The library is certified by VDE. It is dedicated for use in applications compliant with the Safety class B standard (specified by IEC 60730, IEC60335 and/or UL 60730, and UL 1998).

The library is released in a precompiled format, together with functional example projects and documentation describing the respective tests.

The library is created in close cooperation with the application team, who have vast experience in customer projects. We also take the feedback from our customers into consideration.

2 What is new

This version is based on the CM4_CM7 library.

When compared to the previous version its predecessor, the main changes are:

- Functional examples are now available only in the MCUXpresso SDK as middleware packages.
- Changed/simplified the API of the test routines

2.1 Description

The supported devices are:

- LPC55Sxx

The supported/recommended IDEs:

- IAR v8.40 and higher
- Keil µVision V5.28 (C compiler V6) and higher
- MCUXpresso IDE V11.1 and higher

The tested components are:

- CPU registers
- Program counter
- Variable memory (RAM)
- Invariable memory (flash)
- Clock
- Digital I/O
- Analog I/O
- Stack

Contents

1 Introduction.....	1
2 What is new.....	1
3 Optimizations, improvements and changes:	2



- Watchdog

3 Optimizations, improvements and changes:

3.1 Library

Changed the names of functions, input parameters, macros, and variables.

The tests that are not related to core and memory were unified across the devices with Arm cores.

The CPU tests are adapted to the trusted-zone support.

The new functions are:

- CPU:
 - FS_CM33_CPU_SPmain_S()
 - FS_CM33_CPU_SPmain_NS()
 - FS_CM33_CPU_SPmain_Limit_S()
 - FS_CM33_CPU_SPmain_Limit_NS()
 - FS_CM33_CPU_SPprocess_S()
 - FS_CM33_CPU_SPprocess_NS()
 - FS_CM33_CPU_SPprocess_Limit_S()
 - FS_CM33_CPU_SPprocess_Limit_NS()
 - FS_CM33_CPU_Control_S()
 - FS_CM33_CPU_Control_NS()
 - FS_CM33_CPU_Special8PriorityLevels_S()
 - FS_CM33_CPU_Special8PriorityLevels_NS()

The new functions due to the LPCs peripherals:

- Clock test:
 - FS_CLK_CTIMER_LPC()
- Flash test:
 - FS_CM33_FLASH_HW16()
 - FS_CM33_FLASH_HW32()
- Digital I/O test:
 - FS_DIO_Output_LPC()
 - FS_DIO_InputExt_LPC()
 - FS_DIO_ShortToSupplySet_LPC()
 - FS_DIO_ShortToAdjSet_LPC()
- Analog I/O test:
 - FS_AIO_InputInit_LPC_ADC16()
 - FS_AIO_InputTrigger()
 - FS_AIO_InputSet_LPC55SXX()
 - FS_AIO_InputCheck_LPC55SXX()

- Watchdog test:
 - FS_WDOG_Setup_WWDT_LPC()
 - FS_WDOG_Check_WWDT_LPC55SXX()

3.2 Documentation

The documents for all test routines are merged into one document.

3.3 Examples

The example projects are available only in the MCUXpresso SDK as middleware.

To open an example:

- Go to <http://mcuxpresso.nxp.com>.
- Click Select Development Board.
- Select the supported board and click to add the Safety middleware.
- Perform the SDK package build and download.

How To Reach Us

Home Page:

nxp.com

Web Support:

nxp.com/support

Information in this document is provided solely to enable system and software implementers to use NXP products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. NXP reserves the right to make changes without further notice to any products herein.

NXP makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in NXP data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. NXP does not convey any license under its patent rights nor the rights of others. NXP sells products pursuant to standard terms and conditions of sale, which can be found at the following address: nxp.com/SalesTermsandConditions.

While NXP has implemented advanced security features, all products may be subject to unidentified vulnerabilities. Customers are responsible for the design and operation of their applications and products to reduce the effect of these vulnerabilities on customer's applications and products, and NXP accepts no liability for any vulnerability that is discovered. Customers should implement appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP, the NXP logo, NXP SECURE CONNECTIONS FOR A SMARTER WORLD, COOLFLUX, EMBRACE, GREENCHIP, HITAG, I2C BUS, ICODE, JCOP, LIFE VIBES, MIFARE, MIFARE CLASSIC, MIFARE DESFire, MIFARE PLUS, MIFARE FLEX, MANTIS, MIFARE ULTRALIGHT, MIFARE4MOBILE, MIGLO, NTAG, ROADLINK, SMARTLX, SMARTMX, STARPLUG, TOPFET, TRENCHMOS, UCODE, Freescale, the Freescale logo, Altivec, C-5, CodeTEST, CodeWarrior, ColdFire, ColdFire+, C-Ware, the Energy Efficient Solutions logo, Kinetis, Layerscape, MagniV, mobileGT, PEG, PowerQUICC, Processor Expert, QorIQ, QorIQ Qonverge, Ready Play, SafeAssure, the SafeAssure logo, StarCore, Symphony, VortiQa, Vybrid, Airfast, BeeKit, BeeStack, CoreNet, Flexis, MXC, Platform in a Package, QUICC Engine, SMARTMOS, Tower, TurboLink, UMEMS, EdgeScale, EdgeLock, eIQ, and Immersive3D are trademarks of NXP B.V. All other product or service names are the property of their respective owners. AMBA, Arm, Arm7, Arm7TDMI, Arm9, Arm11, Artisan, big.LITTLE, Cordio, CoreLink, CoreSight, Cortex, DesignStart, DynamIQ, Jazelle, Keil, Mali, Mbed, Mbed Enabled, NEON, POP, RealView, SecurCore, Socrates, Thumb, TrustZone, ULINK, ULINK2, ULINK-ME, ULINK-PLUS, ULINKpro, µVision, Versatile are trademarks or registered trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere. The related technology may be protected by any or all of patents, copyrights, designs and trade secrets. All rights reserved. Oracle and Java are registered trademarks of Oracle and/or its affiliates. The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks and service marks licensed by Power.org.

© NXP B.V. 2020.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 03/2020

Document identifier: IEC60730BCM3340RN

