RN00003

PN5190 B1 firmware release v02.0E

Rev. 1.9 — 16 September 2026 **Release notes**

Document information

Information	Content
Keywords	PN5190, PN5190 B1, NFC frontend controller
Abstract	Contains information about a specific release product and component information.

1 Document purpose

This document describes the tested functionality and limitations of the firmware PN5190 B1 FW v02.0E.

It also describes the release summary, release history, known issues, work-arounds, limitations, and recommendations.

The functionality and limitations of the hardware and product support material (for example, customer development board and support software) are described in separate documents.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

2 PN5190 B1 firmware version information

PN5190 B1 software package version (including host utilities): v02.0E

PN5190 B1 secure firmware version: v02.0E

Note: *This firmware version is meant only for the PN5190 B1 IC. This firmware cannot be used for the PN5190 B2 IC version.*

For new designs, it is recommended to always use the latest firmware version available.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

3 Features supported in this release

This section provides the features supported in this firmware/software version release.

3.1 RF protocols

Table 1. RF protocols

Feature/functionality
Reader mode A (106/212/424/848 kbit/s)
Reader mode B (106/212/424/848 kbit/s)
Reader mode FeliCa (212/424 kbit/s)
Reader mode ISO/IEC15693 (26/53/106/212 kbit/s) - all data rates as specified in the data sheet
Reader mode ISO/IEC18000 3M3 - all data rates as specified in the data sheet
Host card emulation / Card mode ISO/IEC 14443 A-106, A-212, A-424, A-848
Peer-Peer passive communication (ISO18092, PI106, PI212, PI424, PT106, PT212, PT424)
Peer-Peer passive communication with proprietary baud rates (PI212, PI424, PI848, PT212, PT424, PT848)

3.2 Other system features/functionality protocols

Table 2. Other system features

Feature/functionality
Low-power card detection (LPCD) and ultra low-power card detection (ULPCD)
Dynamic power control
Automatic waveshape control
Automatic receiver control
Internal DC-DC for TX driver
Over temperature protection (automatic shutdown of TX drivers and entering low-power mode (Standby), over temperature event on GPIO)
Current limiter (automatic shutdown of TX drivers and event notification to host)
Supported to route analog and digital signals on AUX1(analog) and GPIO0 (digital).
Trimming of RF parameters (TX_NOV, current sensor, NFCLD, RFLD).

3.3 Compliancy with this firmware and PNEV5190B hardware (customer development board)

Table 3. Compliancy with this firmware and PNEV5190B hardware (customer development board)

Feature/Functionality
EMVCo L1 digital compliance
ISO 10373-PCD digital compliance
ISO 10373-PICC digital compliance
NFC Forum CR11 analog and digital compliance. NFC Forum CR13 internally qualified.
ISO 23917 Peer-Peer Passive compliance

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

4 Version history

This section contains the firmware release version history only for PN5190 B1 based device firmware.

Table 4. Firmware updates from v02.0D to v02.0E

Sl No.	Function/feature update
1	Fixed an issue where DPR DYNAMIC_POWERLEVEL_REG (0x0064) was holding a random value during corner scenarios like short VEN (where VEN pulse differs from the specification in the PN5190 data sheet) and ULPCD/ULP standby cases.
2	Added Integrity Checks for User Area and Protocol Area. During boot PN5190 will indicate boot notification if the integrity check failed (BOOT_PROTOCOL_AREA_INTEGRITY_ LOST and BOOT_USER_AREA_INTEGRITY_ LOST). During updates of the user area and protocol area using WRITE_E2PROM and UPDATE_RF_ CONFIGURATION commands, PN5190 first checks the integrity before updating the settings and returns with PN5190_STATUS_INTEGRITY_RECOVERED, host /user needs to recover the entire area.
3	Automatic NFCLD/RFLD calibration during first boot after FW update has been removed, calibrations to be triggered by user using register 0x006A (NFCLD_RFLD_REG) after Secure FW update. Write operations to NFCLD_RFLD_REG [bit0]: 1: Perform NFCLD/RFLD Calibrations only if valid bits (EEPROM: 0x06D3) are zero, update & set valid bits. 0: Writing zero has no impact. Read NFCLD_RFLD_REG [bit0]: 1: Indicates calibration is done and valid bits are set. 0: Indicates calibration not done and valid bits are cleared.
4	Added noise robustness feature to improve RF communication in noisy environment, the algorithm dynamically adjusts receiver threshold settings and filter settings to improve communication.
5	Added card protection feature, this feature helps to identify NFC targets as passive cards or battery powered devices.
6	Added new register 0x65 (ULPCD_TESTBUS_CONFIG) for routing ULPCD test signals to GPIO pads. ULPCD_TESTBUS_MUX_SEL [Bit 4:1]: MUX_SEL will select a particular set of test signals to be available on GPIO pads. ULPCD_TESTBUS_ENABLE [Bit 0]: 1 → ULPCD Testbus enabled 0 → ULPCD Testbus disabled.
7	HCE Eeprom settings wDpllPhaseRfON (0x02D2) and wDpllPhaseCeA (0x02D4) are now made public. wDpllPhaseRfON (0x02D2): Initial phase on RF ON, is a Signed phase compensation with 1/4 degree resolution: 16 bits signed value (using complement of 2) Degree ranges from 0 to 90: 2 Byte computation, 4 times of selected degree, meaning: a. 0 ° → 0, b. 5 ° → 5*4 = 20, c. 90 ° → 90*4 = 360 wDpllPhaseCeA (0x02D4) For card emulation Type A, is a signed phase compensation with 1/4 degree resolution: 16 bits signed value (using complement of 2). Degree ranges from 0 to 90: 2 Byte computation, 4 times of selected degree, meaning: a. 0 ° → 0, b. 5 ° → 5*4 = 20, c. 90 ° → 90*4 = 360

Table 5. Firmware updates from v02.0B to v02.0D

Sl No.	Function/feature update
1	Added Delay feature to support scenarios where Standby entry is prevented when the Host is slow to deassert NSS. Delay feature: Added a new EEPROM field to configure NSS time delay, how long to wait for NSS to go low while entering standby.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 5. Firmware updates from v02.0B to v02.0D

Sl No.	Function/feature update
	Name: bDelayNTSAssert. Address Offset: 0xD0D Size: 1 Byte. Description: Time to wait in microseconds for NSS to go low while entering standby The default is 0x64 = 100 µs.

Table 6. Firmware updates from v02.0A to v02.0B

Sl No.	Function/feature update
1	Fix for issue in the second MIFARE Classic authentication, seen only with a particular card and only when the coupling between card and reader is strong enough.
2	Update in firmware to improve robustness during LPCD and Standby power modes.

Table 7. Firmware updates from v02.09 to v02.0A

Sl No.	Function/feature update
1	Added new LPCD command option which makes the IC enter LPCD mode and returns with an Autocoll Event if an external RF is detected. In SWITCH_MODE_LPCD (0x23) command, bControl field option LPCD_WITH_AUTOCOLL_EVENT (0x13) is added to support LPCD with Autocoll event when wake-up occurs due to load change/Ext RF from LPCD standby scenarios. Added a new EEPROM field to configure the time-out for Autocoll expiry: Name: LpcdWithAutocollExpiryInterval. Address Offset: 0xCEE Size: 1 Byte. Description: This field is the time before Autocoll expires when LPCD is used with Autocoll option. 1unit - 100 ms. The default is 10 ms.
2	Added a new command CTS_FAST_CONFIGURE (0x2B) which both configures and enables CTS. For Enabling CTS, the Length should be 0x27 (including both Configs and Enabling bytes). This command cannot be used for disabling CTS. First fast Init+Configure takes about 50 ms, second time onwards about 50 µs.
3	Added configuration to initialize the pullup/down state of SPI Pads (ATX Pins) in the secure flash init. This feature is disabled by default. Added the following EEPROM fields for reconfiguration of SPI pad configurations: Name: EnableHIFPadsReConfig. Address Offset: 0xCEF Size: 1 Byte. Description: Enable/Disable reconfiguration of the SPI Pads configuration. Name: SPIPadReConfig. Address Offset: 0xCF0 Size: 4 Bytes. Description: SPI Pads PullUp/Down Configuration.
4	Fixed an issue which prevented exit from Autocoll in some scenarios, when external RF is removed.
5	Fixed an issue that caused changes in amplitude of response during Host Card emulation, when higher VDDPA values are used in APC TX entries.

Table 8. Firmware updates from v02.08 to v02.09

Sl No.	Function/feature update
1	Feature implemented DPR (Dynamic Power Regulation). Added new register DYNAMIC_POWERLEVEL_REG (Reg Addr: 0x64).

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 8. Firmware updates from v02.08 to v02.09*...continued*

Sl No.	Function/feature update
2	Feature implemented LFO timing calibration using frequency meter for higher LPCD pulse interval accuracy. Added new EEPROM setting LFO_TRIM_CALIBRATION (EEPROM Addr.0xCED).
3	Updated the DPC algorithm for higher control accuracy.
4	Updated command GET_CRC_USER_AREA (Command code: 0x29)

Table 9. Firmware updates from v02.07 to v02.08

Sl No.	Function/feature update
1	Resolved the issue of DPC not recovering to expected VDDPA regulation during load change conditions, when in some corner case scenarios the DPC has to manage other priority tasks.

Table 10. Firmware updates from v02.06 to v02.07

Sl No.	Function/feature update
1	Fixed an issue in the UPDATE_RF_CONFIGRUATION and GET_RF_CONFIGURATION commands that occurred when used for TX index 0x0F (ISO180003m3_TARI_18.88us) and 0x10 (ISO180003m3_TARI_ 9.44us).
2	Fixed an issue of not-restoring the analog TX settings when switching from reader mode to card mode. Removing of type-b detection during Autocoll. Supporting only Type-A and Type-F detection as part of Autocoll procedure.
3	Introduced a new EEPROM configuration: ENABLE_ULFO_TRIM_CALIBRATION (0xCEC). This configuration enables/disables the calibration of wake-up counter value based on the ULFO accuracy measured with a frequency meter with XTAL as reference. ***Note:*** *This feature must be used only when XTAL is available and configured for use*
4	Deprecated the P2P active communication target mode functionality.

Table 11. Firmware updates from v02.05 to v02.06

Sl No.	Function/feature update
1	Added new command:GET_CRC_USER_AREA[0x29]: This command is used to calculate the CRC for the complete User area including the Protocol area. This command helps customers to ensure the integrity of their RF and analog settings by detecting manipulation of this area.
2	Modified SOF timing: In this FW version, we have modified the protocol settings of TypeB106 such that it supports SOF timing adjustment, and provide better results during EMVCo L1 analog test.

Table 12. Firmware updates from v02.03 to v02.05

Sl No.	Function/feature update
1	If there is an XTAL error during Boot, the error notification is sent as XTAL START ERROR bit as part of General Error event in BootStatus.
2	Added support to route analog and digital signals on AUX1(Analog) and GPIO0(Digital). This is done as part of AnalogTestbus Instruction in Combined mode. Therefore, we configured the Combined_Mode Signal payload field with value 2 (Analog and Digital combined) then analog and digital test bus is routed on AUX1(Analog Signal) and GPIO0(Digital Signal). The signals to be routed are configured in the EEPROM offset address as mentioned below:

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 12. Firmware updates from v02.03 to v02.05*...continued*

Sl No.	Function/feature update
	"DigitalTBSignalIndex" Offset="0xCE9" Value="0x9B" "DigitalTBSignalBit" Offset="0xCEA" Value="0x04" "AnalogTBSignal" Offset="0xCEB" Value="0x78" Refer to Instruction: CONFIGURE_TESTBUS_ANALOG (CMD ID: 0x13) Introduced new instruction to configure Signals from two test bus at once. Refer to: Command CONFIGURE_MULTIPLE_TESTBUS_DIGITAL (CMD ID: 0x2A)
3	Added FastFieldON as a configuration at Bit 4 position in SYSTEM_CONFIG(Addr: 0x00) Register. If this bit is set, TXLDO/DCDC is not disabled during the RF OFF instruction. Only TX_DRIVER is disabled as part of RF OFF and in RF ON TX_DRIVER is enabled.
4	New CLIF Registers CLIF_TIMER0_OUTPUT, CLIF_TIMER1_OUTPUT, CLIF_TIMER2_CONFIG, CLIF_TIMER2_RELOAD and CLIF_TIMER2_OUTPUT are provided for user configuration.
5	Modified value of bGuardTimeBeforeTx to 0xFF: During PN5190 dynamic stability analysis with Type A-106 tags, there were errors such as parity/integrity/protocol error observed. Therefore, it is decided to change the value of bGuardTimeBeforeTx to 0xFF, which corresponds to 255 µs guard time before TX.

Table 13. Firmware updates from v02.01 to v02.03

Sl No.	Function/feature update
1	The GPIO1 (general-purpose input/output) pin can be enabled to wake up an external DC-DC from power down for the VDDPA supply during LPCD.
2	Updated Type-A 106 Antenna-specific Protocol register settings for EMVCo to solve few EMVCo Card activation failures during fast card movement within the Field.
3	Update to handle SWITCH_MODE_NORMAL (Abort) scenarios even when Functional CMD and SWITCH_MODE_NORMAL CMD are sent to back within 10 µs
4	Introduced a new DPC_CONFIG register to handle Dynamic Enable/Disable of DPC without depending on the DPC setting from EEPROM User Area.
5	Card Mode (SWITCH_MODE_AUTOCOLL Command) support with Ultra Low-Power standby feature (in Autonomous mode with Standby mode) along with the existing Low-Power standby configuration using EEPROM settings.
6	Update to indicate Length Error when received FeliCa response is greater than 28 Bytes when RX_MULTIPLE is Enabled
7	Update to indicate the correct numbers of received bytes when RETRIEVE_RF_DATA is used to retrieve FeliCa response packets received when RX_MULTIPLE is Enabled.
8	Update to fix the issue of EXCHANGE_RF_DATA returning with success even before Receiving RF Response on few ICs upon POR.
9	Update to clear all pending Interrupt Status bits before performing RF Exchange to fix TX Failure observed when FeliCa response is received around FDT timeout.
10	Added a new feature to extend RX Guard Timer in Integer multiple of ‘dwRXIRQ_GuardTime’ EEPROM timeout configuration in order to extend RX Guard Timeout beyond 1.048 s.

Table 14. Firmware updates from v02.00 to v02.01

Sl No.	Function/feature update
1	NFCLD_ON threshold setting update to PASS NFC Forum Power ON/OFF test. With the new setting, the NFCLD wake-up H-Field strength was changed from 100mA/m to 150mA/m.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 14. Firmware updates from v02.00 to v02.01*...continued*

Sl No.	Function/feature update
2	Clearing the general error status register on read, ensuring the General Error status register is cleared when READ is performed.
3	RF-Setting Update to pass NFC Forum analog, updated the default rise and fall times for Type B.
4	Communication failure due to DCO. In the CLIF_DGRM_CONFIG_REG, the bit field DGRM_DCO_TRACK_ TH_SEL was updated to value '3'. This was the stable setting found to solve far-distance communication problems.
5	TXLDO_ERROR in GENERAL_ERROR_STATUS set to 1 when communication fail. Ensuring the delay for DC-DC shutdown is sufficient to ensure proper shutdown of DC-DC. The TXLDO error was getting set as part of the next RF ON since the LDO would not start
6	Update: Dynamic Boost Setting to avoid the sporadic boost noise. Updated the duty cycle for specific boost setting to resolve the sporadic boost noise.

Table 15. Firmware updates from v01.07 to v02.00

Sl No.	Function/feature update
1	Update of RF settings • TypeB waveshape settings improvements to pass EMVCo analog with external compliance tool resolved the Undershoot failures with EMVCo PICC2 • IIR filter settings update in ARC table for 45x45 antenna. Enable IIR filter for A106, which takes effect at close distance only. Enabling IIR filter reduces the swing of the received ADC data, therefore avoid clipping and give benefit of using the static BBA gain • PLL settings update for P2P Active communication to pass interoperability with mobile phones. Updated PLL setting ANA_PLL_CTRL_XTAL value to 0xA6EA8A00. • Updated settings for DPC with RDON feature to pass NFC Forum analog compliance. The DPC settings with RDON were not changed, instead DPC target current was reduced from 306 mA to 286 mA due to limit power within maximum limit for Listener-3 and 6. This was in specific changed for 45x45 antenna and only for NFC Forum. • Updated register setting of RM_PREAMBLE_SC_TRIGGER set to 0x08 for F212 and F424.
2	Fix for 3 failing test cases in NFC Forum CR11 digital compliance for card mode. This fix is related to an incorrect mapping of a handler for a Register bit in the SystemConfig register.
3	Fixed an issue of graceful entry into standby due to temperature error. In this fix, we are Turning RF OFF before entering standby due to temperature error.
4	Updated ARC implementation to refer to the correct ARC_106_FDT table during FDT for TypeA106. Fix in the ARC algorithm to apply the ARC_106_FDT values during FDT.

Note: *Note that default settings had been worked out based on the customer development board with default 45 x 45mm antenna and default matching. A custom antenna or modified matching require a verification and potentially a modification of these default settings.*

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

5 Recommendations, known limitations, and precautions

This section provides the known limitations in the FW/HW recommendations.

5.1 Known limitations

1. LPCD_CONFIG bit 4 and bit 5 to be considered as single group where both should be enabled/disabled , otherwise unexpected general status event will be observed.
2. In noisy environment, after thousands of RF exchanges TypeA communication starts failing continuously with protocol error, even after the noise is removed. PN5190 needs IC Reset i.e. VEN reset to perform RF communication again.
3. FW02.09 or higher requires a DPR register initialization to ZERO/intended value before performing RF-ON command. This is mandatory when :
   a. The startup VEN timing is different than recommended, or
   b. After every wake-up from ULP_Standby/ULPCD.
4. TX amplitude fading is observed when pairing PN5190 with another PN5190, and DC/DC is enabled. Issue not observed when using TXLDO power supply.
   Note: *Specific only to PN5190 as initiator as well as target (PN5190 vs PN5190).*
5. Randomly, PN5190 FW does not respond to the first REQA from an iPhone 12 Mini phone with HCE Mode + LPCD enabled.
   Note: *Specific only to iPhone 12 Mini phone.*
6. During Stress test scenarios where LPCD and Card mode are enabled, Firmware sends multiple responses, containing random data.
   Note: *Internal buffer overflow issue. Host can read and discard the additional responses, and then restart the operation.*
7. Performing SWITCH_MODE_STANDBY command while RF is ON, may damage the IC.
   Note: *Perform RF OFF before entering Standby (SWITCH_MODE_STANDBY command).*
8. During LPCD and StandBy, when LFO and ULFO trimming feature is enabled, and Timeout is set to Max, IC wakes up immediately due to overflow.
   Note: *Disable the LFO and ULFO trimming feature.*
9. Inconsistent behaviour of ARC, when DPC is disabled.
   Note: *Disable the ARC when disabling the DPC.*
10. With the default FDT settings for ISO18000 (dwFDT_18000_DefVal parameter, which is 1.26 ms), performance @ -40 °C is reduced when TARI = 18.88 µs.
    This shall be appropriately adjusted for better performance.

5.2 Recommendations

The following clock parameters for XTAL are recommended for active communication on the customer development board PNEV5190B and 45 mm x 45 mm antenna.

Table 16. Recommendations for v02.00 to v02.01 and above

Address	Parameter name	Default value	Value for active communication
1	ANA_PLL_CTRL_XTAL	0x00	0xC1
2	ANA_PLL_CTRL_XTAL	0x8A	0x13
3	ANA_PLL_CTRL_XTAL	0xEA	0xE8
4	ANA_PLL_CTRL_XTAL	0xA6	0xA6

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

5.3 Precautionary notes

1. Do not disable the DPC and activate the RF field for ICs connected to antennas matched "Symmetric" (for example, customer development board antenna). Possible damage of the transmitter drivers due to overcurrent over a long period might occur.
2. PN5190 B1 samples cannot be upgraded with the PN5190 B2 FW.
   However, PN5190 B1 samples can be updated with this FW version.
3. FW v2.00 or FW V01.xx samples can be upgraded to the latest version of PN5190 FW via Secure firmware download. However, samples after upgrading to FW v02.xx, cannot be reverted to FW v01.xx.
4. The ULPCD requires a specific power configuration with no DC-DC active and requires modifications to both the customer development board PNEV5190B EEPROM settings as described in the application notes.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

6 Revision history

Table 17. Revision history

Document ID	Release date	Description
RN00003 v.1.9	16 September 2026	PN5190 B1 firmware v02.0E release: Section 4 "Version history": updated.
RN00003 v.1.8	15 October 2025	PN5190 B1 firmware v02.0D release: Section 4 "Version history": updated.
RN00003 v.1.7	24 June 2025	PN5190 B1 firmware v02.0B release: Section 4 "Version history": updated.
RN00003 v.1.6	9 December 2024	PN5190 B1 firmware v02.0A release: Section 4 "Version history": updated.
RN00003 v.1.5	17 June 2024	PN5190 B1 firmware v02.09 release: Section 4 "Version history": updated.
RN00003 v.1.4	29 May 2024	PN5190 B1 firmware v02.08 release: Section 4 "Version history": updated.
RN00003 v.1.3	12 September 2023	PN5190 B1 firmware v02.07 release: Section 4 "Version history": updated.
RN00003 v.1.2	17 January 2023	PN5190 B1 firmware v02.06 release: Section 4 "Version history": updated.
RN00003 v.1.1	27 June 2022	PN5190 B1 firmware v02.05 release: Section 4 "Version history": updated.
RN00003 v.1.0	7 September 2021	PN5190 B1 firmware v02.03 release: Section 4 "Version history": updated.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Legal information

Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at https://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this document expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

HTML publications — An HTML version, if available, of this document is provided as a courtesy. Definitive information is contained in the applicable document in PDF format. If there is a discrepancy between the HTML document and the PDF document, the PDF document has priority.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP B.V. — NXP B.V. is not an operating company and it does not distribute or sell products.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Licenses

Purchase of NXP ICs with NFC technology — Purchase of an NXP Semiconductors IC that complies with one of the Near Field Communication (NFC) standards ISO/IEC 18092 and ISO/IEC 21481 does not convey an implied license under any patent right infringed by implementation of any of those standards. Purchase of NXP Semiconductors IC does not include a license to any NXP patent (or other IP right) covering combinations of those products with other products, whether hardware or software.

Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

EdgeVerse — is a trademark of NXP B.V.

FeliCa — is a trademark of Sony Corporation.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Tables

Tab. 1. RF protocols 4
Tab. 2. Other system features 4
Tab. 3. Compliancy with this firmware and PNEV5190B hardware (customer development board) 4
Tab. 4. Firmware updates from v02.0D to v02.0E 5
Tab. 5. Firmware updates from v02.0B to v02.0D 5
Tab. 6. Firmware updates from v02.0A to v02.0B 6
Tab. 7. Firmware updates from v02.09 to v02.0A 6
Tab. 8. Firmware updates from v02.08 to v02.09 6
Tab. 9. Firmware updates from v02.07 to v02.08 7
Tab. 10. Firmware updates from v02.06 to v02.07 7
Tab. 11. Firmware updates from v02.05 to v02.06 7
Tab. 12. Firmware updates from v02.03 to v02.05 7
Tab. 13. Firmware updates from v02.01 to v02.03 8
Tab. 14. Firmware updates from v02.00 to v02.01 8
Tab. 15. Firmware updates from v01.07 to v02.00 9
Tab. 16. Recommendations for v02.00 to v02.01 and above 10
Tab. 17. Revision history 12

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Contents

1 Document purpose 2
2 PN5190 B1 firmware version information 3
3 Features supported in this release 4
3.1 RF protocols 4
3.2 Other system features/functionality protocols 4
3.3 Compliancy with this firmware and PNEV5190B hardware (customer development board) 4
4 Version history 5
5 Recommendations, known limitations, and precautions 10
5.1 Known limitations 10
5.2 Recommendations 10
5.3 Precautionary notes 11
6 Revision history 12
Legal information 13

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© 2026 NXP B.V. **All rights reserved.**