MPC106/D
(Motorola Order Number)

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PowerPC™

Application Note

Adapting the MPC106 PCI Bridge/ Memory Controller to Existing MPC105 Systems

This document describes how to use the MPC106 in systems designed for the MPC105. The principal differences between the MPC105 and the MPC106 are as follows:

- The MPC106 provides a PowerPC common hardware reference platform (HRP) compliant bridge between the PowerPC microprocessor family and the Peripheral Component Interconnect (PCI) bus.
- The MPC106 alternately supports an external L2 cache controller or integrated L2 cache module.
- The MPC106 supports EDO DRAM. This is a change from the MPC105's support of SDRAM.

The following sections describe, in detail, the changes needed in MPC105 systems to support the MPC106.

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1.1 Signal Differences

The following sections discuss the changes that must be made to signals in order to run an MPC106 on an MPC105 system.

1.1.1 Configuration Signals

The configuration pins of the MPC106 have changed slightly from their implementation on the MPC105. The MPC106 uses a different signal to select addressing map options. On the MPC105, this was the $\overline{\text{XATS}}$ signal, on the MPC106 it is the $\overline{\text{DBG0}}$. In both cases, Map A is selected through a pull-up resistor. Since MacOS™, AIX™, and Windows NT™ systems all use Map A, the only change needed for many systems is adding a pull-up resistor to $\overline{\text{DBG0}}$. If Map B is needed, the circuitry used to drive $\overline{\text{XATS}}$ low during reset should be disconnected and reattached to $\overline{\text{DBG0}}$.

The MPC106 supports accessing the ROM memory space through the PCI bus. To prohibit this from occurring on systems where the MPC105 accesses the ROM on the processor data bus, insure that a pull-up resistor is connected to $\overline{\text{RCS0}}$.

The MPC105 uses the FNR signal to determine the type (ROM or Flash) and width (8 bit or 64 bit) of the decoded ROM space. The MPC106 uses $\overline{\text{FOE}}$ to determine the width, with no hardware distinction made between ROM or Flash. For MPC105-based systems which have one bank of Flash or ROM, a pull-up resistor should be added to $\overline{\text{FOE}}$ if Flash (8 bit) memory is used; otherwise a pull-down should be added to indicate ROM (64 bit). If there are two banks of Flash or ROM, add a pull-up to $\overline{\text{FOE}}$ and connect the MPC106 signal, $\overline{\text{RCS1}}$, to the chip-select signals of the second bank of ROM.

The MPC106 does not support 32-bit bus mode, selected by a pull-down resistor on the DL0 signal. It is unlikely that a 64-bit MPC106 can be successfully used on an existing 32-bit system, so no work-around will be possible. If the system includes a pull-up on DL0 to guarantee 64-bit mode, it may be removed from new designs, but will cause no harm if left in place.

1.1.2 Cache Controller Signals

The MPC106 has had numerous changes to the cache controller. In some instances this is simply a renaming of previous signals, but several have been reused for quite different purposes. In particular, some versions of the MPC105 provide eight byte-write enables ($\overline{\text{DWE0}}$–$\overline{\text{DWE7}}$) for the secondary cache controller, while earlier versions expected these signals to be created by an external PAL. The MPC106 has only three write enables ($\overline{\text{DWE0}}$– $\overline{\text{DWE2}}$). These are actually identical signals, buffered to reduce loading, and cannot be used as byte enables.

If the system in question uses the on-chip byte decode mode of the MPC105 (that is, uses all eight of the $\overline{\text{DWE0}}$–$\overline{\text{DWE7}}$ signals), then installing an MPC106 requires disconnecting the redefined $\overline{\text{DWE}}$ signals (found at pin locations J13, N4, L11, J10, H10, N15), connecting pins P3 and H11 to the eight $\overline{\text{WE}}$ signals of the cache data RAMs, and using the write mode CF_WMODE = 0. Pin N4 should have a pullup attached. Refer to Figure 1.

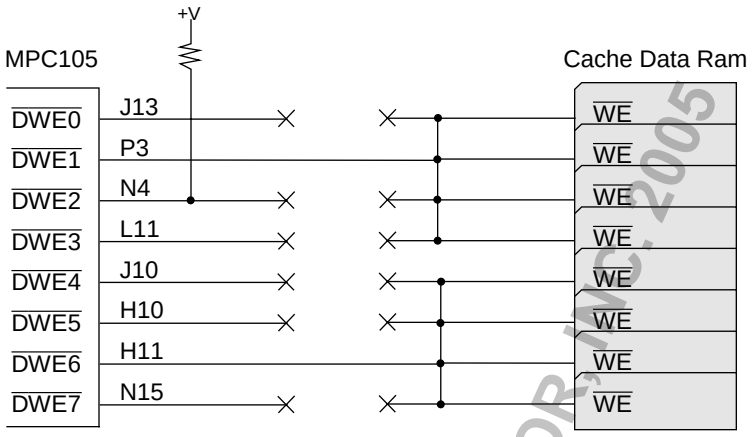

Figure 1. Cache Conversion for Internal Byte Decodes

If an external registered PAL provides the decode logic for the cache data RAM, and the MPC105 uses only the signal $\overline{\text{DWE}}/\overline{\text{DWE1}}$ to control the PAL, then no modifications will be necessary to the target system. Note that $\overline{\text{DWE}}/\overline{\text{DWE1}}$ on the MPC105 is identical to $\overline{\text{DWE}}/\overline{\text{DWE0}}$ on the MPC106.

If the cache system uses asynchronous SRAM, then one of the burst address signals (BA0) will need modification. The TALE/BA0 signal (pin T1) has been redefined as a cache RAM chip select ($\overline{\text{DCS}}$), while the BA0 has changed to pin location T5 ($\overline{\text{TALOE}}$ on the MPC105). The BA1 signal remains in pin location P4. The asynchronous SRAM $\overline{\text{CS}}$ inputs may be connected to $\overline{\text{DCS}}$, or they can be tied to be permanently active.

Additionally, the signals TV and BA0, now may be input signals if the secondary cache controller (L2) is disabled. These signals should all have a pull-up resistor attached.

1.1.3 Dual-Wide ROM Banks

The MPC106 has redefined one of the signals used to address the second bank of a 64-bit wide ROM bank. In such a system, it will be necessary to move the chip enables of the second bank of ROMs from the $\overline{\text{FOE}}/\overline{\text{RCS1}}$ signal of the MPC105 (pin D13) to the $\overline{\text{RCS1}}$ signal of the MPC106 (pin J13).

Note that this change does not apply to systems using byte-wide Flash ROMs (whether one bank or two), nor does it apply to systems using only one bank of 64-bit wide ROM.

1.1.4 Unused Signals

Systems using the MPC105 may have certain signals left unconnected (see Table 1). These signals either have new or changed definitions and should, if not used, have a pull-up resistor attached.

Table 1. Pull-ups Required

MPC105 Signal	MPC106 Signal	Signal Location
$\overline{\text{FOE}}$/$\overline{\text{RCS2}}$	$\overline{\text{FOE}}$	D13
$\overline{\text{DBG0}}$		L5
$\overline{\text{TALOE}}$	BA0	T5
$\overline{\text{ADS}}$/DALE		R3
$\overline{\text{LB\_CLAIM}}$		N4

1.2 Software Changes

In general, the registers in the MPC106 are backward-compatible with the MPC105 and will power-up with values that should allow software to operate transparently. The primary changes in the register set are those for the control of SDRAM and for 32-bit bus mode. The following table summarizes the changes (all SDRAM control bits excluded).

Table 2. Changed Register Definitions

Register	MPC105 Bit Name	Bit(s)	MPC106 Changes/Definitions
Device ID	all		MPC105 = 0x0001
			MPC106 = 0x0002
ERREN1		4	PCI master error enable moved to bit 3, now used for memory refresh overflow error enable.
	—	3	Was reserved; now PCI master error enable.
MCCR1	FNR	22	Always zero; examine next bit instead.
	32N64	21	Changed to 8N64, use to determine Flash or ROM settings.
MCCR2	SRF	18–31	Always zero.
	WMODE	0	Always zero; with no 32-bit bus, ROMs are read in 8-beat bursts.
MCCR4	WCBUF	21	Always zero; there is no latching on writes to memory.
PICR1	XATS	16	Renamed ADDRESS_MAP since it is no longer externally controlled via the $\overline{\text{XATS}}$ pin. **NOTE:** This bit is now writeable; if a zero is written, the MPC106 will switch to Map B.

Table 2. Changed Register Definitions (Continued)

Register	MPC105 Bit Name	Bit(s)	MPC106 Changes/Definitions
PICR2	L2_UPDATE_EN L2_EN	31 30	These bits defaulted to 0 upon reset in the MPC105, while in the MPC106 they default to 1.
	CF_BYTE_DECODE	25	Cache-byte writes no longer allowed; now used to lock the Flash ROM (renamed FLASH_WR_LOCKOUT_EN)
	CF_BURST_RATE	8	This bit now indicates the number of cache banks present and was renamed CF_TWO_BANKS. The old function has been removed; synchronous SRAM is now always one clock cycle, while asynchronous is always two.

In addition, many registers have additional bits defined to provide support for ECC memory systems, EDO DRAMs, and to generally improve performance. In such cases, the bits are set to MPC105-compatible values upon reset.

1.3 Summary of Differences Between the MPC105 and MPC106

The following sub-sections provide a summary of differences between the MPC105 and MPC106 processors.

1.3.1 Changed Functions

Table 3 describes the signals whose functions were completely changed between the MPC105 and the MPC106. Any system which uses these signals should examine their new uses carefully.

Table 3. Changed Signal Functions

MPC105 Signal	MPC106 Signal	Signal Location	Signal Type	Description
$\overline{\text{SDRAS}}$	$\overline{\text{PPEN}}$	J14	Output	SDRAM support deleted, parity buffer control added.
TALE/BA0	$\overline{\text{DCS0}}$	T1	Output	Cache RAM chip select.
$\overline{\text{TALOE}}$	BA0	T5	I/O	Burst address moved from TALE/BA0.

1.3.2 Deleted Functions

Table 4 describes the changes made to the functionality of some signals on the MPC106. The two principal changes made were due to the deletion of SDRAM support, and the deletion of cache-byte write capability.

Table 4. Deleted Signal Functions

MPC105 Signal	MPC106 Signal	Signal Location	Signal Type	Description
$\overline{\text{FOE}}$/$\overline{\text{RCS1}}$	$\overline{\text{FOE}}$	D13	Output	ROM chip select function moved to $\overline{\text{RCS1}}$.
$\overline{\text{SDCAS}}$/$\overline{\text{MDLE}}$	$\overline{\text{MDLE}}$	E13	Output	SDRAM support deleted.

Table 4. Deleted Signal Functions (Continued)

MPC105 Signal	MPC106 Signal	Signal Location	Signal Type	Description
DQM7/CAS7	CAS7	E14	Output	SDRAM support deleted.
DQM6/CAS6	CAS6	F14	Output	SDRAM support deleted.
DQM5/CAS5	CAS5	G13	Output	SDRAM support deleted.
DQM4/CAS4	CAS4	G14	Output	SDRAM support deleted.
DQM3/CAS3	CAS3	E16	Output	SDRAM support deleted.
DQM2/CAS2	CAS2	G16	Output	SDRAM support deleted.
DQM1/CAS1	CAS1	H15	Output	SDRAM support deleted.
DQM0/CAS0	CAS0	J15	Output	SDRAM support deleted.
CS7/RAS7	RAS7	K11	Output	SDRAM support deleted.
CS6/RAS6	RAS6	J12	Output	SDRAM support deleted.
CS5/RAS5	RAS5	L10	Output	SDRAM support deleted.
CS4/RAS4	RAS4	K12	Output	SDRAM support deleted.
CS3/RAS3	RAS3	K14	Output	SDRAM support deleted.
CS2/RAS2	RAS2	K13	Output	SDRAM support deleted.
CS1/RAS1	RAS1	L13	Output	SDRAM support deleted.
CS0/RAS0	RAS0	M14	Output	SDRAM support deleted.
CKE/DWE7	MA0	N16	Output	Cache-byte write replaced with new MSB address.
DWE6	DWE1	H11	Output	Cache-byte strobe set.
DWE5	INT	H10	Output	Cache-byte write removed.
DWE4	DBGLB	J10	Output	Cache-byte write removed.
CKO/DWE3	CKO/DWE2	L11	Output	Cache-byte write removed.
DWE2	LBCLAIM	N4	Output	Cache-byte write removed.
DWE/DWE1	DWE(0)	P3	Output	Cache-byte write removed.
FNR/DWE0	RCS1	J13	Output	Cache-byte write replaced with ROM chip select.
DL0	DL0	U6	I/O	No power-up configuration option.
DBG0	DBG0	L5	Output	Includes power-up configuration option now.
XATS	XATS	P1	Input	No power-up configuration option.

1.3.3 New Functions

Table 5 describes the functionality of MPC106 signals that have been created by adding to existing MPC105 signals. In all cases, this occurred to add support for the glance lookaside cache controller. Existing systems should have no difficulty with these signals.

Table 5. New Signal Functions

MPC105 Signal	MPC106 Signal	Signal Location	Signal Type	Description
$\overline{\text{BAA}}$/BA1	$\overline{\text{BAA}}$/BA1/$\overline{\text{BGL2}}$	P4	Output	Added glance support
$\overline{\text{ADS}}$/DALE	$\overline{\text{ADS}}$/DALE/$\overline{\text{BRL2}}$	R3	I/O	Added glance support
$\overline{\text{DOE}}$	$\overline{\text{DOE}}$/$\overline{\text{DBGL2}}$	U5	Output	Added glance support

1.3.4 Renamed Signals

Table 6 describes the changes made by simply renaming the MPC105 signals on the MPC106 implementation. In all cases this is due to the addition of a new MSB (MA0) for the DRAM memory address, so the remaining addresses were renumbered. The function of the signals remain the same, and should not cause any changes to the target system.

Table 6. Renamed Signals

MPC105 Signal	MPC106 Signal	Signal Location	Signal Type	Description
MA_AR11	MA_AR12	J16	Output	Renumbered for consistency.
MA_AR10	MA_AR11	K16	Output	Renumbered for consistency.
MA_AR9	MA_AR10	K15	Output	Renumbered for consistency.
MA_AR8	MA_AR9	L15	Output	Renumbered for consistency.
MA_AR7	MA_AR8	M16	Output	Renumbered for consistency.
MA_AR6	MA_AR7	M15	Output	Renumbered for consistency.
MA_AR5	MA_AR6	N16	Output	Renumbered for consistency.
MA_AR4	MA_AR5	P16	Output	Renumbered for consistency.
MA_AR3	MA_AR4	P15	Output	Renumbered for consistency.
MA_AR2	MA_AR3	R16	Output	Renumbered for consistency.
MA_AR1	MA_AR2	T16	Output	Renumbered for consistency.
MA_AR0	MA_AR1	U16	Output	Renumbered for consistency.

1.4 Conversion Limitations

There are some limitations encountered in converting from the MPC105 to the MPC106. In general, existing systems must not:

- Use the 32-bit bus mode.
- Use the on-chip byte-write mode for L2 cache.
- Use SDRAM for system memory.

All other revisions can be accommodated by making appropriate cuts and jumpers or by adding pull-up resistors to properly account for signal changes on the MPC106.

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