1. General description

This specification describes the electrical, physical and dimensional properties of Au-bumped sawn wafers on FFC of I-CODE SLI-S Label ICs on an NXP C075EE process and is the base for delivery of tested I-CODE SLI-S Label ICs.

2. Ordering information

Table 1. Ordering information

<table>
<thead>
<tr>
<th>Type number</th>
<th>Package Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SL2ICS5311EW/V7</td>
<td>Wafer</td>
<td>Bumped sawn wafer on UV-tape</td>
</tr>
</tbody>
</table>

3. Mechanical specification

3.1 Wafer

- Diameter: 8"
- Thickness: 150 \( \mu m \pm 15 \mu m \)

3.2 Wafer backside

- Material: Si
- Treatment: ground + stress release
- Roughness: \( R_a \max. 0.5 \mu m \)
  \( R_t \max. 5 \mu m \)

3.3 Chip dimensions

- Chip size: 940 x 900 \( \mu m^2 \)
- Scribe lines: 50 / 50 \( \mu m \)

3.4 Passivation

- Type: sandwich structure
- Material: PSG / Nitride (on top)
- Thickness: 500 nm / 600 nm
3.5 Au bump

- Bump material: > 99.9 % pure Au
- Bump hardness: 35 – 80 HV 0.005
- Bump shear strength: > 70 MPa
- Bump height: 18 μm
- Bump height uniformity:
  - within a die: ± 2 μm
  - within a wafer: ± 3 μm
  - wafer to wafer: ± 4 μm
- Bump flatness: ± 1.5 μm
- Bump size:
  - LA, LB 60 x 60 μm²
  - VSS¹, TEST¹ 60 x 60 μm²
- Bump size variation: ± 5 μm
- Under bump metallization: sputtered TiW

¹.Pads VSS and TEST are disconnected when wafer is sawn.
3.6 Reference die definition (SECS II Wafer map format)

- Physical appearance: no chip structure, full die size
- Local coordinates: x=-67, y=-20

Fig 1. Wafer layout with reference die
4. Fail die identification

4.1 Fail die identification

No inkdots are applied to the wafer.

Electronic wafer mapping (SECS II format) covers the electrical test results and additionally the results of mechanical/visual inspection.

4.2 Wafer mapping

Wafer mapping for failed die information is available on floppy-disk.

Format: SECS II format
5. Limiting values

Table 2. Limiting values\(^{[1][2][3][4]}\)

**Absolute Maximum Ratings**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>T(_{\text{STOR}})</td>
<td>storage temperature range</td>
<td>-55</td>
<td>+140</td>
<td>°C</td>
</tr>
<tr>
<td>T(_{j})</td>
<td>junction temperature</td>
<td>-55</td>
<td>+140</td>
<td>°C</td>
</tr>
<tr>
<td>V(_{\text{ESD}})</td>
<td>electrostatic discharge voltage</td>
<td>-</td>
<td>±2</td>
<td>kV(_{\text{peak}})</td>
</tr>
<tr>
<td>I(_{\text{max LA-LB}})</td>
<td>maximum input peak current</td>
<td>-</td>
<td>±60</td>
<td>mA(_{\text{peak}})</td>
</tr>
<tr>
<td>T(_{\text{JOP}})</td>
<td>operating junction temperature</td>
<td>-25</td>
<td>+85</td>
<td>°C</td>
</tr>
<tr>
<td>I(_{\text{LA-LB}})</td>
<td>input current</td>
<td>-</td>
<td>30</td>
<td>mA(_{\text{rms}})</td>
</tr>
</tbody>
</table>

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the Operating Conditions and Electrical Characteristics section of this specification is not implied.

[2] This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.


[4] The voltage between LA and LB is limited by the on-chip voltage limitation circuitry (corresponding to parameter I\(_{\text{LA-LB}}\)\)
6. Characteristics

6.1 Electrical characteristics

$T_{op}= -25 \text{ to } 85^\circ C$

Table 3. Characteristics [1]

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{LA-LB}$</td>
<td>Minimum Supply Voltage for READ/WRITE</td>
<td>-</td>
<td>2.5</td>
<td>2.7</td>
<td>$V_{rms}$</td>
<td></td>
</tr>
<tr>
<td>$C_{res}$</td>
<td>Input Capacitance between LA – LB ( V_{LA-LB} = 2 V_{rms} )</td>
<td>[3]</td>
<td>22.3</td>
<td>23.5</td>
<td>24.7</td>
<td>pF</td>
</tr>
<tr>
<td>$P_{min}$</td>
<td>Minimum Operating Supply Power</td>
<td>[4]</td>
<td>-</td>
<td>280</td>
<td>-</td>
<td>$\mu W$</td>
</tr>
<tr>
<td>$m$</td>
<td>Modulation of RF Voltage for Demodulator Response ( m = \frac{V_{max} - V_{min}}{V_{max} + V_{min}} )</td>
<td>[5]</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>%</td>
</tr>
<tr>
<td>$t_{psm}$</td>
<td>Modulation Pulse Length of RF Voltage</td>
<td>[5]</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>$\mu s$</td>
</tr>
<tr>
<td>$t_D$</td>
<td>Demodulator Response Time ( m \geq 10 %, 100 % )</td>
<td>[5]</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>$\mu s$</td>
</tr>
<tr>
<td>$R_{load}$</td>
<td>Load Modulation</td>
<td>[5]</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>$\Omega$</td>
</tr>
<tr>
<td>$t_{ret}$</td>
<td>EEPROM Data Retention</td>
<td>( T_{amb} \leq 55 , ^\circ C )</td>
<td>40</td>
<td>-</td>
<td>-</td>
<td>years</td>
</tr>
<tr>
<td>$n_{write}$</td>
<td>EEPROM Write Endurance</td>
<td></td>
<td>100000</td>
<td>-</td>
<td>-</td>
<td>cycles</td>
</tr>
</tbody>
</table>

[1] Typical ratings are not guaranteed. These values listed are at room temperature.
[2] Bandwidth limitation ($\pm 7 \, kHz$) according to ISM band regulations.
[4] Including losses in resonant capacitor and rectifier
[5] Refer to ISO/IEC 15693-2 and 15693-3 including pulse shapes and tolerances; proper coil design assumed
7. Chip orientation and bond pad locations

- Minimum yield per wafer: 30% of 29941 potential good dies
- Minimum yield per lot: 30%

8. Final wafer test specification
9. References

[1] Data sheet - General specification for 8” wafers on UV-tape
[3] Application note - SECS II wafer map format
10. Revision history

Table 4. Revision history

<table>
<thead>
<tr>
<th>Document ID</th>
<th>Release date</th>
<th>Data sheet status</th>
<th>Change notice</th>
<th>Supersedes</th>
</tr>
</thead>
<tbody>
<tr>
<td>131030</td>
<td>20080508</td>
<td>Product data sheet</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

- Initial version
11. Legal information

11.1 Data sheet status

<table>
<thead>
<tr>
<th>Document status</th>
<th>Product status</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Objective [short] data sheet</td>
<td>Development</td>
<td>This document contains data from the objective specification for product development.</td>
</tr>
<tr>
<td>Preliminary [short] data sheet</td>
<td>Qualification</td>
<td>This document contains data from the preliminary specification.</td>
</tr>
<tr>
<td>Product [short] data sheet</td>
<td>Production</td>
<td>This document contains the product specification.</td>
</tr>
</tbody>
</table>

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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