AH1308

Application Hints - Standalone high speed CAN transceivers Mantis TJA1044 / TJA1057, Mantis-GT TJA1044GT / TJA1057GT and Dual-Mantis-GT TJA1046

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Document information

Info	Content
Title	**Application Hints - Standalone high speed CAN transceivers Mantis TJA1044 / TJA1057, Mantis-GT TJA1044GT / TJA1057GT and Dual-Mantis-GT TJA1046**
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Summary

The Mantis family consists of two basic device subcategories: The Mantis covering the TJA1044 and TJA1057 and the Mantis-GT, covering the TJA1044GT and TJA1057GT. The TJA1057(GT) is also available in a version with VIO pin (TJA1057(GT)/3). Both are variants form the 3rd generation of standalone high speed CAN transceivers as TJA1042 and TJA1051 from NXP Semiconductors. Mantis is intended to be used in 12V automotive and any industrial environments whereas the GT variant is the first choice for chokeless and CAN-FD applications.

The Dual-Mantis-GT transceiver TJA1046 includes two fully independent TJA1044GT transceivers.

This document provides the necessary information for hardware and software designers for creation of automotive applications using the new high speed CAN transceiver generation products. It describes the advantages in terms of characteristics and functions offered to a system and how the system design can be simplified by replacing other HS-CAN transceivers.

Revision history

Rev	Date	Description
0.1	26th April 2013	Initial version
1.0	3rd May 2013	Final Version
1.1	6th June 2014	Changed naming “Mantis One” to “Mantis”
1.2	20th November 2014	Updated chapter 1.2 “Differences between TJA1051/TJA1042 and Mantis Family”, chapter 3.3.1 “TXD dominant clamping detection in Normal Mode” and chapter 4.5. “Remote Wake-up (via CAN bus)”: Updating and renaming of parameters
2.0	30th April 2015	New derivates TJA1057(GT)/3 with VIO pin and Dual-Mantis-GT TJA1046 included

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1. Introduction

NXP introduces its next generation high speed CAN (HS-CAN) transceivers: The Mantis Family which consists of the Mantis parts TJA1044T and TJA1057T and the Mantis-GT variants TJA1044GT and TJA1057GT.

Please note, that in the following the naming TJA1044 and TJA1057 respectively TJA1057/3 are used for both variants: Mantis as well as Mantis-GT. If needed a distinction is mentioned explicitly.

The TJA1057 is available in two versions, with and without VIO supply pin.

Another variant is the dual HS-CAN transceiver TJA1046 containing two fully independent TJA1044GT transceivers.

Mantis devices are Standby and Basic HS-CAN transceivers for 12V automotive applications. They fully meet – and exceed – G5 EMC specifications, allowing removal of common-mode choke and can be used with 5V and 3.3V microcontrollers.

The Mantis-GT transceivers have all features contained in Mantis products. They are optimized for CAN FD active communication, with an additional specification for the loop delay symmetry and a faster propagation delay giving robust communication at higher data rates and to support longer cable length.

All transceivers provide the physical link between the protocol controller and the physical transmission medium according to the ISO11898 ([4], [7]) and SAE J2284 [8]. This ensures full interoperability with other ISO11898 compliant transceiver products.

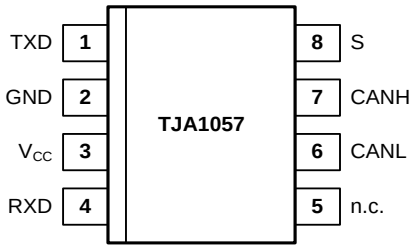
All Mantis transceivers are allowing drop-in replacements for the TJA1040, TJA1042, TJA1050 and TJA1051 as long as a Split or VIO pin is not used. They can be directly connected to any 5V or 3.3V microcontroller as long as the 3V3 type microcontroller provides 5V tolerant interfacing pins towards the transceivers. The TJA1057/3 with VIO supply pin allows drop-in replacement for the TJA1051/3.

With this extended portfolio of high speed CAN transceivers NXP Semiconductors enables ECU designers to find the best application fitting standalone transceiver product in order to cover all main application specific requirements.

1.1 Mantis Standalone high speed CAN transceiver products

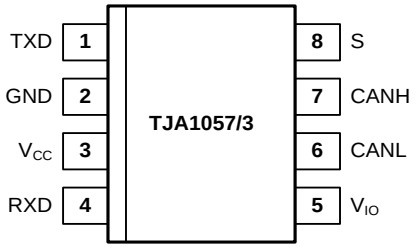
1.1.1 TJA1057 – Basic high speed CAN transceiver

TJA1057 – Basic high speed CAN transceiver



- Compatible to the TJA1050 and TJA1051 basic high speed CAN transceivers
- Normal Mode (transmit / receive CAN data)
- Silent Mode (receiving CAN data only)
- Undervoltage detection on pin V_{CC}

TJA1057/3 – Basic high speed CAN transceiver with VIO pin

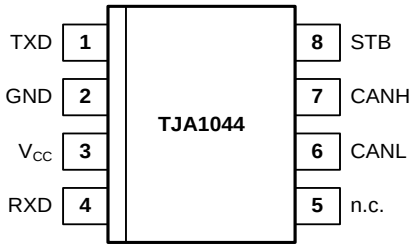


- Compatible to the TJA1051/3 basic high speed CAN transceiver
- Normal Mode (transmit / receive CAN data)
- Silent Mode (receiving CAN data only)
- Undervoltage detection on pins V_{CC} and V_{IO}

Fig 1. Pin configuration and short functional description of the TJA1057 and TJA1057/3

1.1.2 TJA1044 – High speed CAN transceiver with Standby Mode

TJA1044 – High speed CAN transceiver with Standby Mode

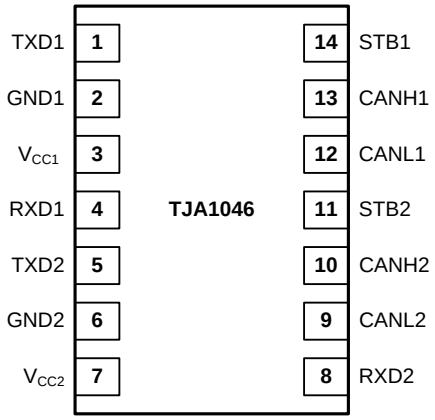


- Compatible to the TJA1040 and TJA1042 high speed CAN transceivers
- Normal Mode (transmit / receive CAN data)
- Standby Mode (low power mode with CAN wake-up capability)
- Bus dominant time-out function in Standby Mode
- Undervoltage detection on pin V_{CC}

Fig 2. Pin configuration and short functional description of the TJA1044

1.1.3 TJA1046 – Dual high speed CAN transceiver with Standby Modes

TJA1046 – Dual high speed CAN transceiver with Standby Modes



- Two fully independent high speed CAN transceivers
- Normal Modes (transmit / receive CAN data)
- Standby Modes (low power mode with CAN wake-up capability)
- Bus dominant time-out function in Standby Mode
- Undervoltage detection on pins V_{CCx}

Fig 3. Pin configuration and short functional description of the TJA1046

1.2 Differences between TJA1051/TJA1042 and Mantis Family

Feature / Requirement	TJA1042/51	TJA1044/57/46
VCC voltage range	+/-10%	+/-5%
Absolute max voltage	+7V	+7V
DC voltage at CAN pins	+/-58V	+/-42V
Common mode voltage	+/-30V	+/-12V
Supported bus load range	45 … 65Ohm	50 … 65Ohm
SPLIT pin	yes	no
Low power mode	yes	yes
Simple time filter for bus wake-up	yes	no
ISO11898-5 conformant enhanced wake up pattern filter	no	yes
TXD dominant time-out filter	yes	yes
Enable pin	yes	no
VIO pin	yes (TJA1042/3, TJA1051/3)	yes (TJA1057/3)
3V3 µC support	yes, via VIO	yes, via VIO or if µC provides 5V tolerance on interface
ESD IEC 61000-4-2 at pins CANH and CANL	8kV	8kV
ESD-HBM (at CANH/CANL)	8kV	8kV
ESD-HBM (at other pins)	4kV	4kV
ESD-MM	300V	200V
ESD-CDM	750 / 500V	750 / 500V
G5 compliance	yes	yes

2. Basics of high speed CAN applications

2.1 Example of a high speed CAN application

Fig 4 illustrates an example of a high speed CAN application. Several ECUs (Electronic Control Units) are connected via stubs to a linear bus topology. Each bus end is terminated with 120Ω (R_T), resulting in the nominal 60Ω bus load according to ISO11898. The figure shows the split termination concept, which in general is improving the EMC performance of high speed CAN bus systems. The former single 120Ω termination resistor is split into two resistors of half value ($R_T/2$) with the center tap connected to ground via the capacitor C_{spl}.

Detailed rules and recommendations for in-vehicle CAN networks can be found in a separate technical note [5].

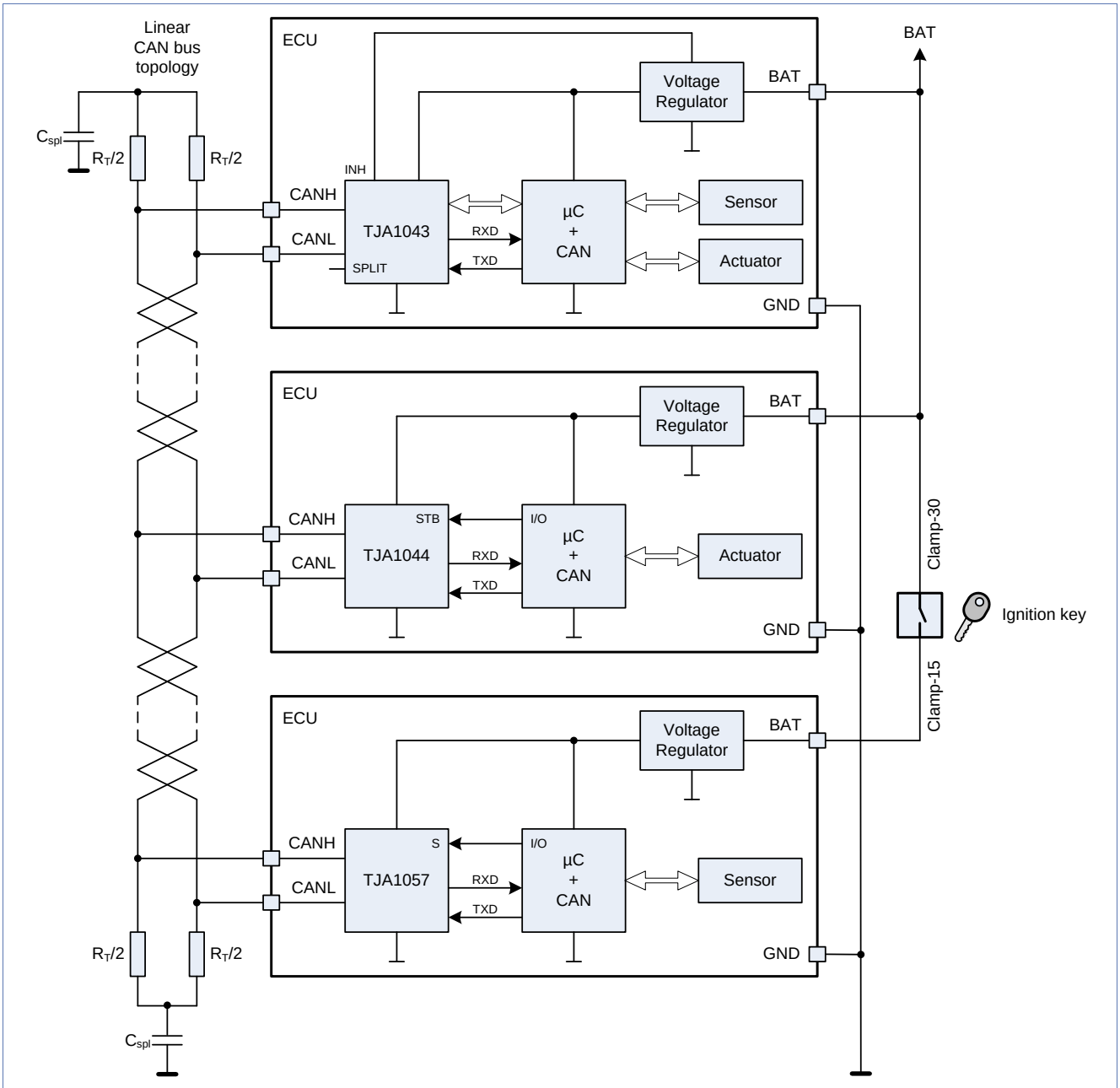


Fig 4. High speed CAN application example

The block diagram in Fig 4 describes the internal structure of an ECU. Typically, an ECU consists of a standalone transceiver (here the TJA1044, TJA1057 and TJA1043) and a host microcontroller with integrated CAN-controller, which are supplied by one or more voltage regulators. While the high speed CAN transceiver needs a +5 V supply to support the ISO11898 bus levels, new microcontroller products are increasingly using lower supply voltages like 3.3V. To support such microcontrollers the TJA1057 and TJA1044 have a fully compatible interface towards 3.3V-microcontroller as long as the microcontroller interfacing pins are 5V tolerant. The TJA1057/3 offers an additional VIO supply pin to adapt the transceiver interfacing pins to the supply voltage of the microcontroller.

The protocol controller is connected to the transceiver via a serial data output line (TXD) and a serial data input line (RXD). The transceiver is attached to the bus lines via its two bus terminals CANH and CANL, which provide differential receive and transmit capability.

Depending on the selected transceiver different mode control pins (STB or S) are connected to I/O pins of the host microcontroller for operation mode control.

Note: Details of the mentioned TJA1043 can be found in a separate application hints document [4] and the product data sheet.

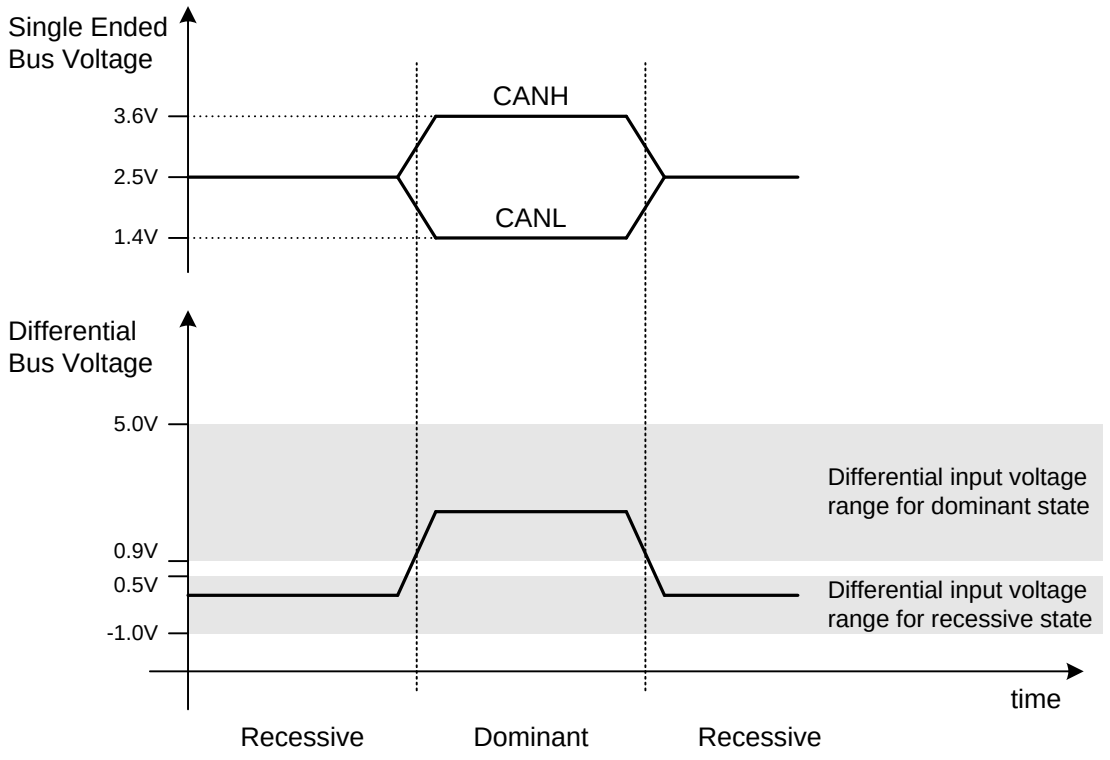


Fig 5. Nominal bus levels according to ISO11898

The protocol controller outputs a serial transmit data stream to the TXD input of the transceiver. An internal pull-up function within each NXP high speed CAN transceiver sets the TXD input to logic HIGH, which means that the bus output driver stays recessive in the case of a TXD open circuit condition e.g. during start-up, reset or in case of a failure. In the recessive state (Fig 5) the CANH and CANL pins are biased to a voltage level of $V_{CC}/2$. If a logic LOW level is applied to TXD, the output stage is activated, generating a dominant state on the bus line (Fig 5). The output driver CANH provides a source output from V_{CC} and the output driver CANL a sink output towards GND as illustrated in Fig 6.

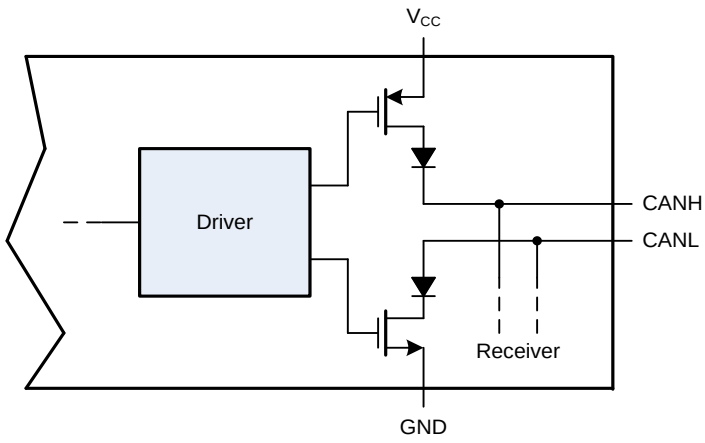


Fig 6. High speed CAN output driver

If no bus node transmits a dominant bit, the bus stays in recessive state. If one or multiple bus nodes transmit a dominant bit, then the bus lines enter the dominant state overriding the recessive state (wired-AND characteristic).

The receiver converts the differential bus signal to a logic level signal, which is output at RXD. The serial receive data stream is provided to the bus protocol controller for decoding. The internal receiver comparator is always active. It monitors the bus while the bus node is transmitting a message. This is required to support the non-destructive bit-by-bit arbitration scheme of CAN.

3. TJA1057 – Basic high speed CAN transceiver

3.1 Main features

The TJA1057 is the basic high speed CAN transceiver and is backwards compatible with the TJA1050 and TJA1051.

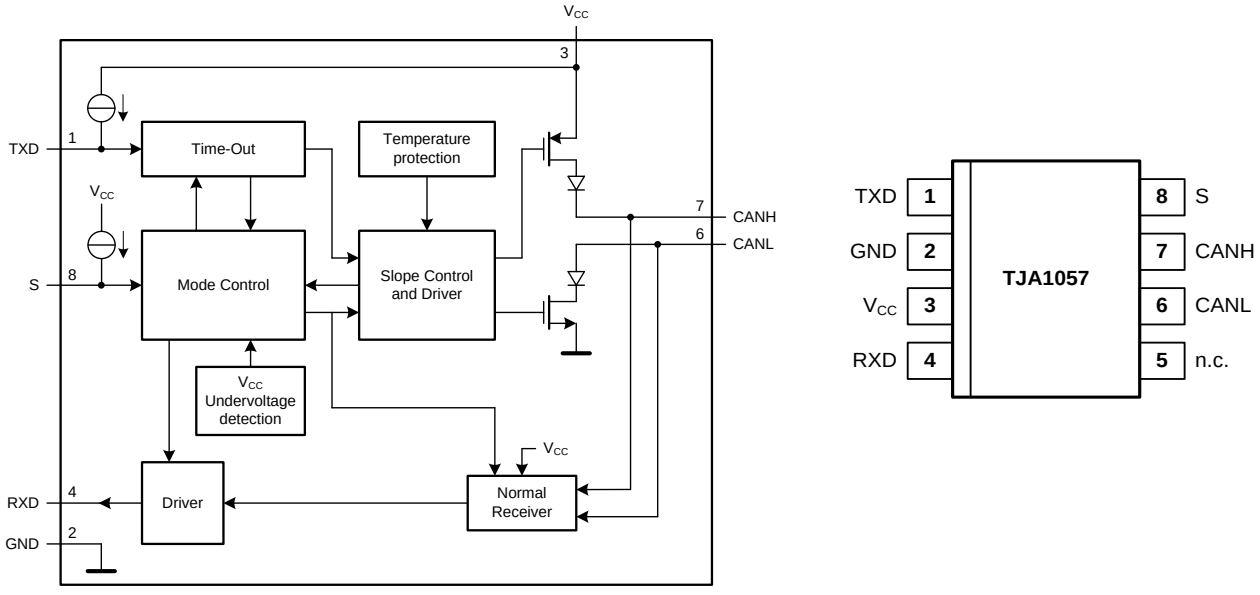


Fig 7. Block diagram and pinning of the TJA1057

The TJA1057/3 offers the same functionality as the TJA1057 but with additional VIO supply pin. It is backwards compatible with the TJA1051/3.

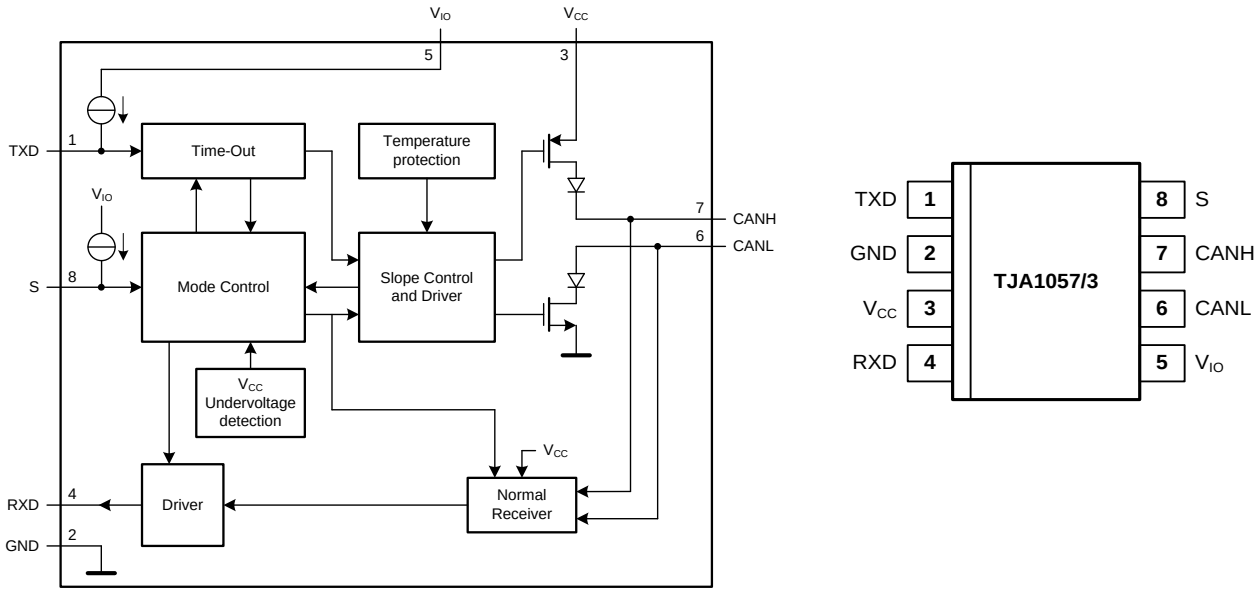


Fig 8. Block diagram and pinning of the TJA1057/3

3.2 Operation modes

The TJA1057 offers 2 different power modes, Normal Mode and Silent Mode which are directly selectable through the S-pin. Taking into account the undervoltage detection a third power mode is available, the so-called OFF Mode. Fig 9 shows how the different operation modes can be entered. Every mode provides a certain behavior and terminates the CAN channel to a certain value. The following sub-chapters give a short overview of those features.

The TJA1057/3 behaves in the same way as the TJA1057 but with an additional mode condition for the undervoltage detection at pin VIO.

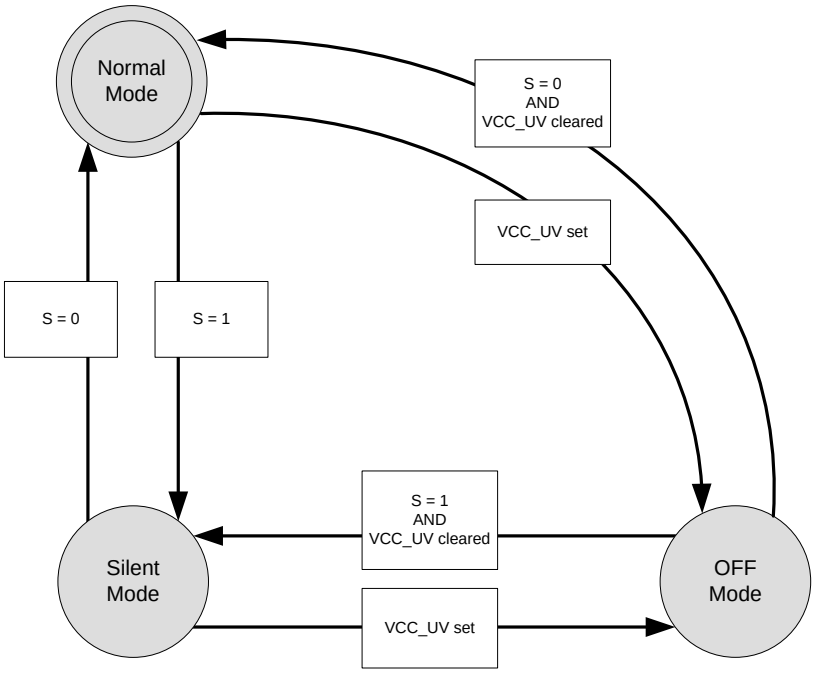


Fig 9. State diagram TJA1057

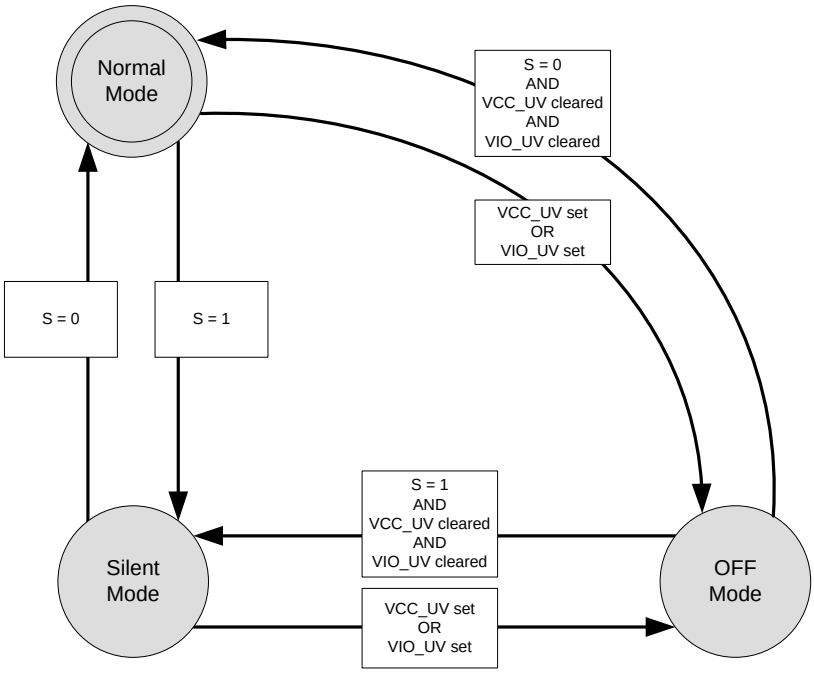


Fig 10. State diagram TJA1057/3

3.2.1 Normal Mode

In Normal Mode the CAN communication is enabled. The digital bit stream input at TXD is transferred into corresponding analog bus signals. Simultaneously, the transceiver monitors the bus, converting the analog bus signals into the corresponding digital bit stream output at RXD. The bus lines are biased to $V_{CC}/2$ in recessive state and the transmitter is enabled. The Normal Mode is entered setting pin S to LOW.

In Normal Mode the transceiver provides following functions:

- The CAN transmitter is active.
- The CAN receiver is active.
- CANH and CANL are biased to $V_{CC}/2$.
- V_{CC} undervoltage detector is active for undervoltage detection.
- TJA1057/3 only: V_{IO} undervoltage detector is active for undervoltage detection.

3.2.2 Silent Mode

The Silent Mode is used to disable the transmitter of the TJA1057(/3) regardless of the TXD input signal. In Silent Mode the TJA1057(/3) is not capable of transmitting CAN messages, but all other functions, including the receiver, continue to operate. The Silent Mode is entered setting pin S to HIGH. Due to an internal pull-up function it is the default mode if pin S is unconnected e.g. during power-on or reset.

Babbling idiot protection

The Silent Mode allows a node to be set to a state, in which it is silent to the bus. It becomes necessary when a CAN-controller gets out of control and might unintentionally send messages (“Babbling idiot”) that block the bus. Activating the Silent Mode by the microcontroller allows the bus to be released even when there is no direct access from the microcontroller to the CAN-controller. The Silent Mode is very useful for achieving high system reliability required by today’s electronic applications.

Listen-only function

In Silent Mode RXD monitors the bus lines as usual. Thus, the Silent Mode provides a listen-only behaviour for diagnostic features. It ensures that a node does not influence the bus with dominant bits.

In Silent Mode the transceiver provides following functions:

- The CAN transmitter is off.
- The CAN receiver is active.
- CANH and CANL are biased to $V_{CC}/2$.
- V_{CC} undervoltage detector is active for undervoltage detection.
- TJA1057/3 only: V_{IO} undervoltage detector is active for undervoltage detection.

3.2.3 OFF Mode

The non-operation OFF Mode offers total passive behaviour to the CAN bus system. The OFF Mode is entered by undervoltage detection on V_{CC}. This feature is very usefull in applications, which by intention get completely unpowered in some use cases. The total passive behavior makes sure, that the remaining CAN network does not get influenced by such an unpowered node.

In OFF Mode the transceiver provides following functions:

- The CAN transmitter is off.
- The CAN receiver is off.
- CANH and CANL are floating (lowest leakage current on bus pins).
- V_{CC} undervoltage detector is active for undervoltage recovery.
- TJA1057/3 only: V_{IO} undervoltage detector is active for undervoltage recovery.

Table 1. TJA1057: Characteristics of the different modes

Operating mode	S pin	V_{CC} undervolt.	RXD pin		Bus bias	TXD pin	CAN driver
			Bus dominant	Bus recessive			
Normal	0	no	LOW	HIGH	$V_{CC}/2$	0	dominant [1]
						1	recessive
Silent	1	no	LOW	HIGH	$V_{CC}/2$	X	off
OFF	X	yes	V_{CC} [2]	V_{CC} [2]	float	X	off

[1] $t < t_{to(dom)TXD}$, afterwards the TXD dominant clamping detection disables the transmitter. A recessive HIGH level at TXD will release the CAN driver.

[2] RXD follows the V_{CC} voltage

Table 2. TJA1057/3: Characteristics of the different modes

Operating mode	S pin	V_{CC} undervolt.	V_{IO} undervolt.	RXD pin		TXD pin	CAN driver	Bus bias
				Low	High			
Normal	0	no	no	Bus dominant	Bus recessive	0	dominant [1]	$V_{CC}/2$
						1	recessive	
Silent	1	no	no	Bus dominant	Bus recessive	X	off	$V_{CC}/2$
OFF	X	yes	no	high-Z		X	off	float
		no	yes	high-Z		X	off	float
		yes	yes	high-Z		X	off	float

[1] $t < t_{to(dom)TXD}$, afterwards the TXD dominant clamping detection disables the transmitter. A recessive HIGH level at TXD will release the CAN driver.

3.3 System fail-safe features

3.3.1 TXD dominant clamping detection in Normal Mode

The TXD dominant clamping detection prevents an erroneous CAN-controller from clamping the bus to dominant level by a continuously dominant TXD signal.

After a maximum allowable TXD dominant time $t_{to(dom)TXD}$ the transmitter is disabled. According to the CAN protocol only a maximum of eleven successive dominant bits are allowed on TXD (worst case of five successive dominant bits followed immediately by an error frame). Along with the minimum allowable TXD dominant time, this limits the minimum bit rate to 25 kbit/s.

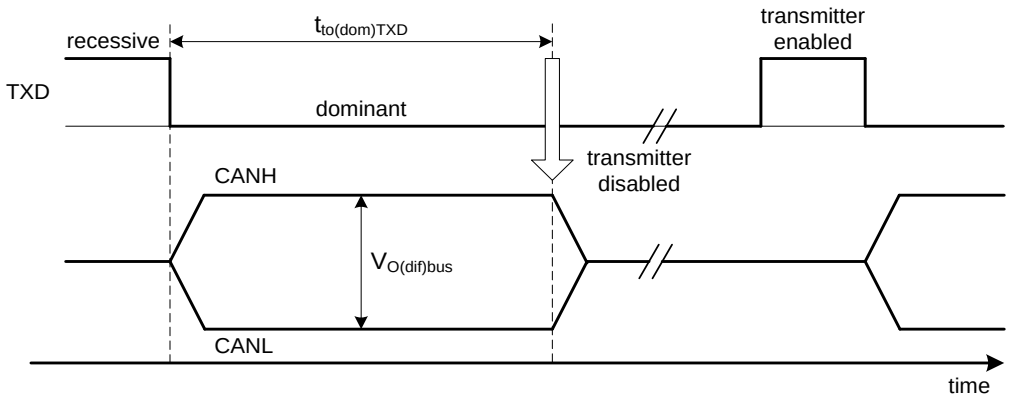


Fig 11. TXD dominant clamping in Normal Mode

3.3.2 Bus dominant clamping prevention at entering Normal Mode

Before transmitting the first dominant bit to the bus the TXD pin once needs to be set HIGH while the transceiver is in Normal Mode in order to prevent a transceiver initially clamping the entire bus when starting up with not well defined TXD port setting of the microcontroller.

3.3.3 Default Silent Mode

As long as the S pin is not correctly driven by the µC during power-on, reset or in case of a system failure, the TJA1057(/3) stays in Silent mode to prevent the bus to be driven dominant.

The S pin needs to actively driven to low level to enter Normal mode before any dominant transitions on TXD are forwarded to the bus lines.

Note that this is a different implementation compared to the TJA1051 that starts up in Normal mode. But in most applications no hard- or software changes are needed to replace the TJA1051(/3) with the TJA1057(/3).

3.3.4 Undervoltage detection & recovery

Compared to the TJA1050, the TJA1057(/3) (as well as the TJA1051(/3)) take advantage of high precision integrated undervoltage detection on its supply pins (see Table 3). Without this function undervoltage conditions might result in unwanted system behaviour, if the supply leaves the specified range. (e.g. the bus pins might bias to GND).

Table 3. TJA1057: Mode control at undervoltage conditions

Supply condition	TJA1057
VCC above $V_{uvd(VCC)}$ [1]	Normal or Silent
VCC below $V_{uvd(VCC)}$ [1]	OFF

[1] $V_{uvd(VCC)}$ undervoltage detection voltage on pin V_{CC}

Table 4. TJA1057/3: Mode control at undervoltage conditions

Supply condition		TJA1057/3
VCC	VIO	
VCC above $V_{uvd(VCC)}$ [1]	VIO above $V_{uvd(VIO)}$ [2]	Normal or Silent
VCC above $V_{uvd(VCC)}$ [1]	VIO below $V_{uvd(VIO)}$ [2]	OFF
VCC below $V_{uvd(VCC)}$ [1]	VIO above $V_{uvd(VIO)}$ [2]	OFF
VCC below $V_{uvd(VCC)}$ [1]	VIO below $V_{uvd(VIO)}$ [2]	OFF

[1] $V_{uvd(VCC)}$ undervoltage detection voltage on pin V_{CC}
[2] $V_{uvd(VIO)}$ undervoltage detection voltage on pin V_{IO}

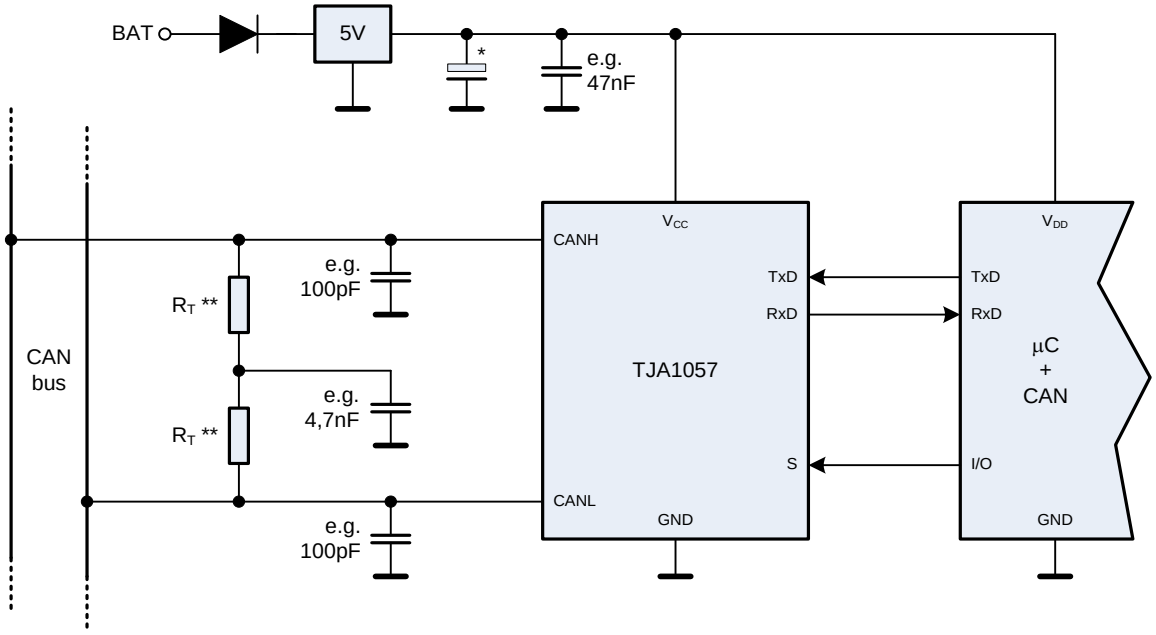
3.3.5 Overtemperature protection

An overtemperature condition may occur either if the transceiver is operated in an environment with high ambient temperature or if there is a short circuit condition on the bus. To protect the transceiver from self-destruction the transmitter is disabled automatically whenever the junction temperature exceeds the allowed limit.

After an overtemperature condition the transmitter is released if the junction temperature is below the limit. The transmitter will remain in the recessive state to prevent continuous re-triggering of the overtemperature condition. Normal operation is restored on the first TXD recessive state.

3.4 Hardware application

Fig 12 and Fig 13 show how to integrate the TJA1057 within a typical application. The application examples assume either a 5V or a 3.3V supplied host microcontroller. In each example there is a dedicated 5V regulator supplying the TJA1057 transceiver on its VCC supply pin (necessary for proper CAN transmit capability according to ISO11898).



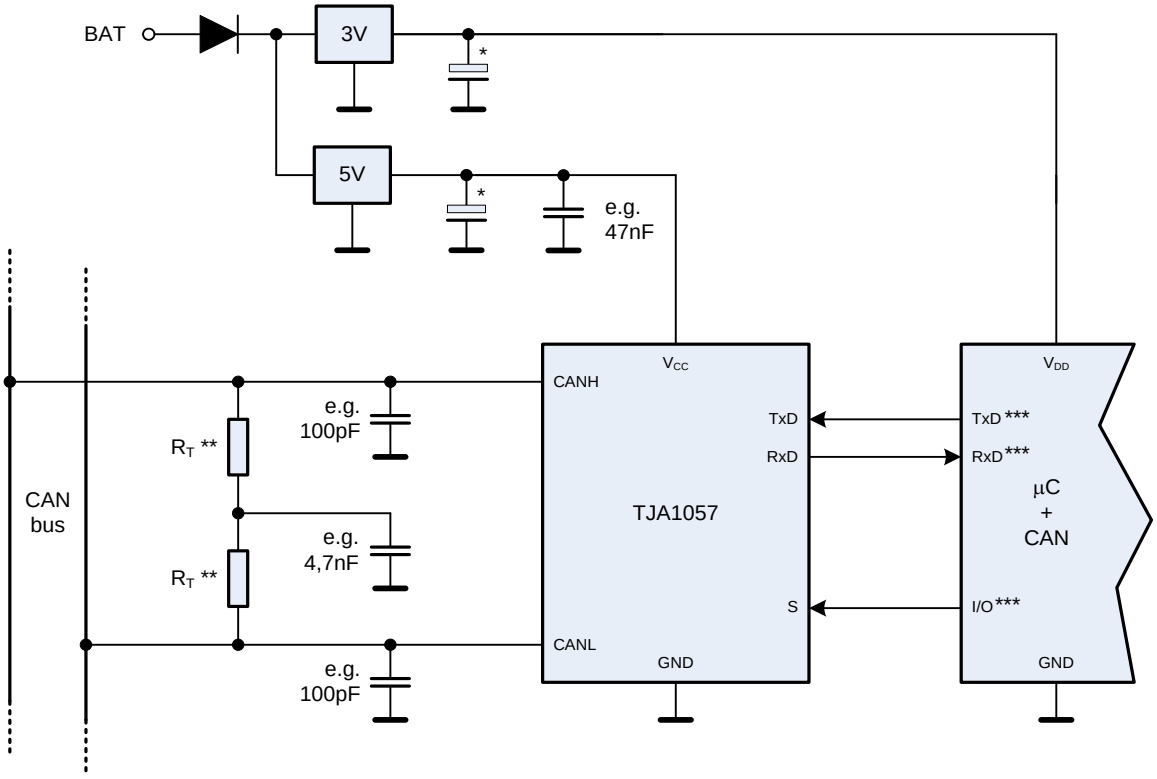
* Size of capacitor depends on regulator.

** For bus line end nodes RT = 60Ohm in order to support the „Split termination concept“
For stub nodes an optional "weak" termination of e.g. RT = 1,3kOhm can be foreseen, if required by the OEM.

General remark: A dedicated application may depend on specific OEM requirements.

Fig 12. Typical application with TJA1057 and a 5V microcontroller

To support 3.3V supplied microcontrollers the TJA1057 has a fully compatible interface towards 3.3V-microcontroller as long as the microcontroller pins connected to RXD, TXD and S are 5V tolerant.



* Size of capacitor depends on regulator.

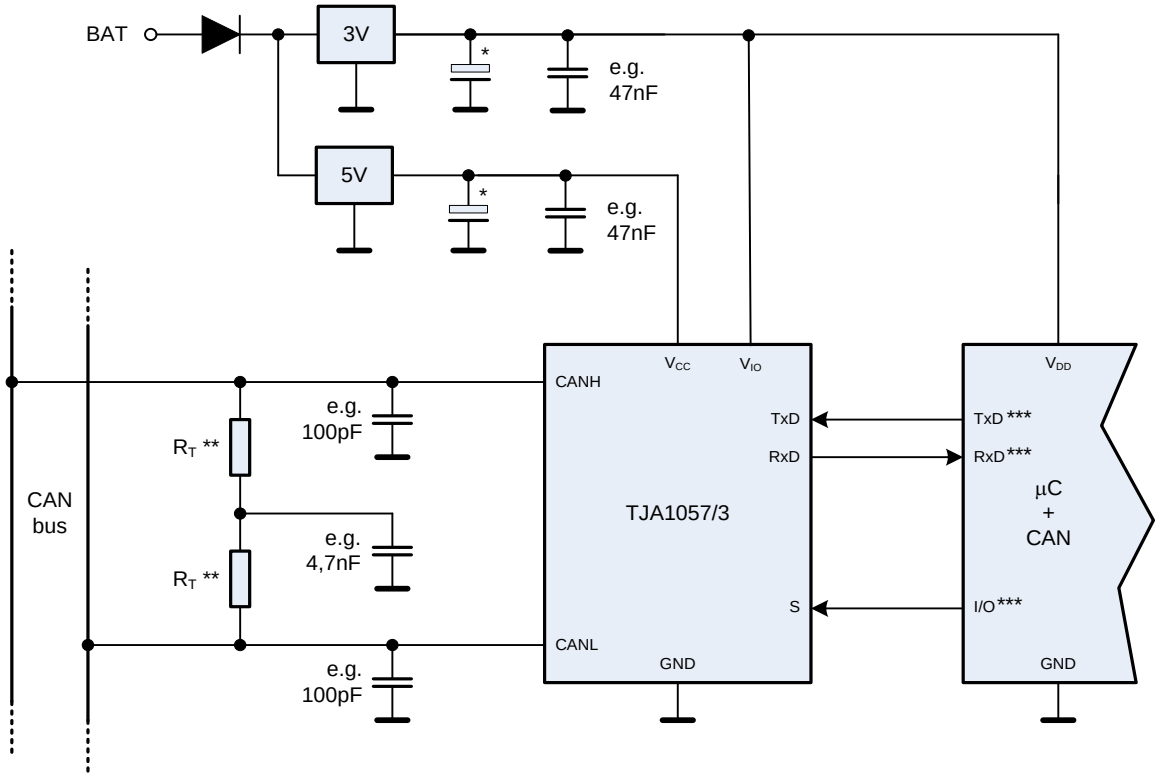
** For bus line end nodes R_T = 60Ohm in order to support the „Split termination concept“.
For stub nodes an optional "weak" termination of e.g. R_T = 1,3kOhm can be foreseen, if required by the OEM.

*** The RXD, TXD and I/O pins of the µC need to be 5V tolerant.

General remark: A dedicated application may depend on specific OEM requirements.

Fig 13. Typical application with TJA1057 and a 3.3V microcontroller

The application of the TJA1057/3 is given in Fig 14.



* Size of capacitor depends on regulator.

** For bus line end nodes R_T = 60Ohm in order to support the „Split termination concept“.
For stub nodes an optional "weak" termination of e.g. R_T = 1,3kOhm can be foreseen, if required by the OEM.

*** The RXD, TXD and I/O pins of the µC need to be 5V tolerant.

General remark: A dedicated application may depend on specific OEM requirements.

Fig 14. Typical application with TJA1057/3 and a 3.3V microcontroller

Note: For detailed hardware application guidance please refer to chapter 5 explaining how the pins of the TJA1057 are properly connected in an application environment.

4. TJA1044 – High speed CAN transceiver with Standby Mode

4.1 Main features

The TJA1044 is the high speed CAN transceiver providing a low power mode (called Standby Mode) beside a Normal Mode.

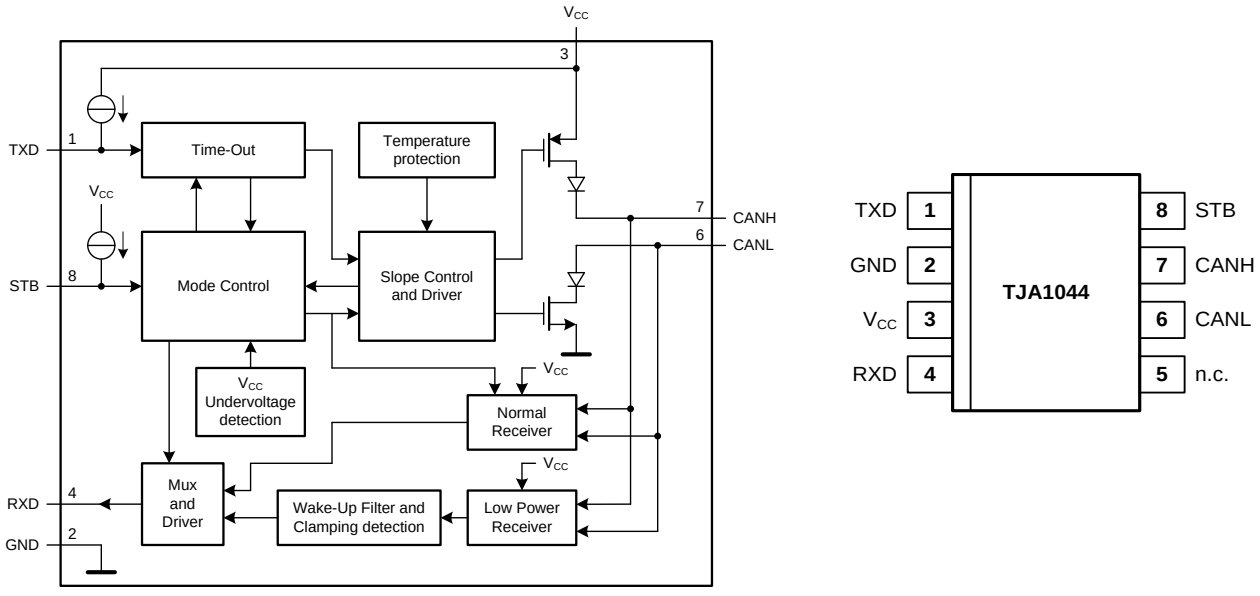


Fig 15. Block diagram and pinning of the TJA1044

4.2 Operation modes

The TJA1044 offers 2 different power modes, Normal Mode and Standby Mode which are directly selectable through the pin STB. Taking into account the undervoltage detection a third power mode is available, the so-called OFF Mode. Fig 16 shows how the different operation modes can be entered. Every mode provides a certain behavior and terminates the CAN channel to a certain value. The following sub-chapters give a short overview of those features.

VCC_UVup flag is set if V_{CC} is lower than the upper threshold $V_{uvd(stb)(VCC)}$, while VCC_UVlow refers to the lower under voltage detection threshold $V_{uvd(swoff)(VCC)}$. The flags are cleared as soon as V_{CC} exceeds the related threshold. See Chapter 4.3.4 for more details regarding the undervoltage detection feature.

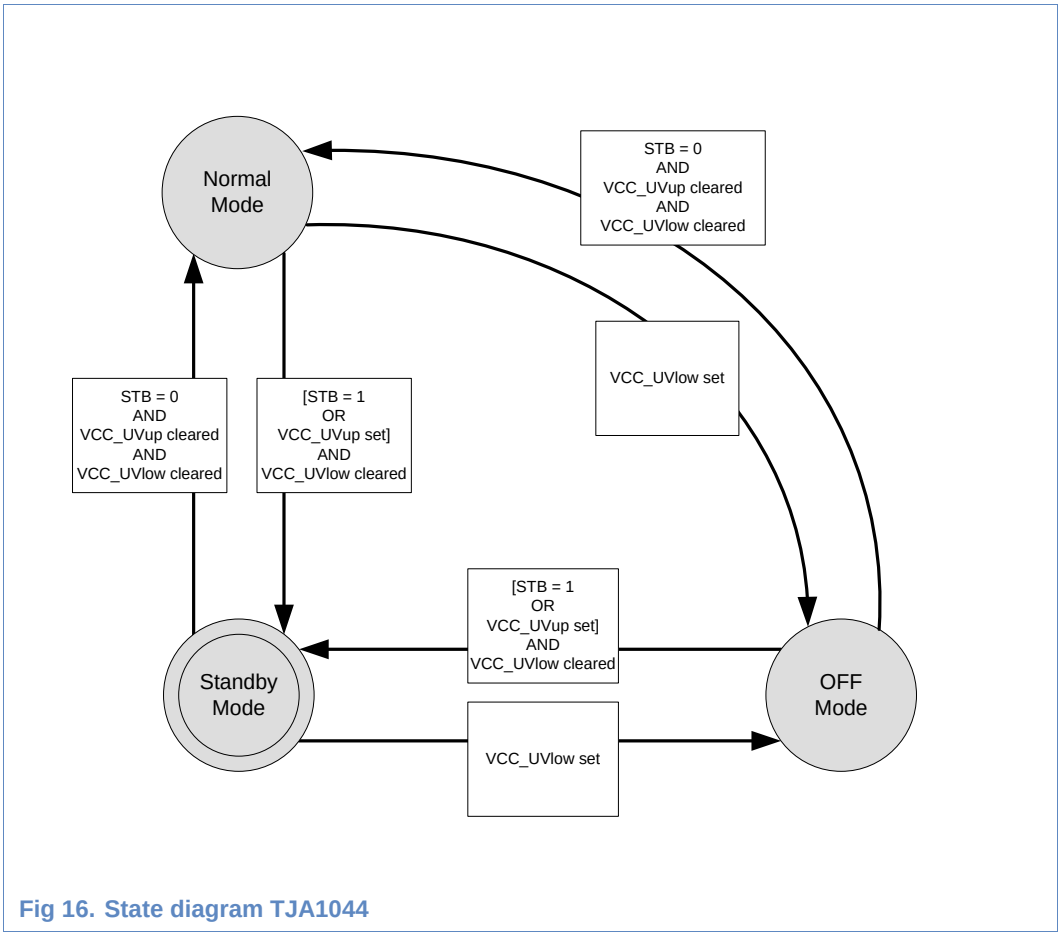


Fig 16. State diagram TJA1044

4.2.1 Normal Mode

In Normal Mode the CAN communication is enabled. The digital bit stream input at TXD is transferred into corresponding analog bus signals. Simultaneously, the transceiver monitors the bus, converting the analog bus signals into the corresponding digital bit stream output at RXD. The bus lines are biased to $V_{CC}/2$ in recessive state and the transmitter is enabled. The Normal Mode is entered setting pin STB to LOW.

In Normal Mode the transceiver provides following functions:

- The CAN transmitter is active.
- The normal CAN receiver is active.
- The low power CAN receiver is active.
- CANH and CANL are biased to $V_{CC}/2$.
- Pin RXD reflects the normal CAN Receiver.
- V_{CC} undervoltage detectors are active for undervoltage detection (see Chapter 4.3.4 for details).

4.2.2 Standby Mode

The Standby Mode is used to reduce the power consumption of the TJA1044 significantly. In Standby Mode the TJA1044 is not capable of transmitting and receiving regular CAN messages, but it monitors the bus for CAN messages.

Only the low power CAN receiver is active, monitoring the bus lines for activity. The bus wake-up filter ensures that only bus dominant and bus recessive states that persist longer than $t_{fltr(wake)bus}$ are reflected on the RXD pin. The low-power receiver is supplied as long as VCC stays above the lower undervoltage detection threshold $V_{uvd(swoff)(VCC)}$ (see Chapter 4.3.4 for details).

To reduce the current consumption as much as possible the bus is terminated to GND rather than biased to $V_{CC}/2$ as in Normal Mode in accordance with ISO11898-5. The Standby Mode is selected setting pin STB to HIGH or if V_{CC} drops below the upper undervoltage detection threshold $V_{uvd(stb)(VCC)}$. Due to an internal pull-up function on the STB pin Standby Mode is the default mode of the transceiver if pin STB is unconnected or during power-on or reset.

In Standby Mode the transceiver provides following functions:

- The CAN transmitter is off.
- The normal CAN receiver is off.
- The low power CAN receiver is active.
- CANH and CANL are biased to GND.
- Pin RXD reflects the bus levels through the low-power CAN Receiver, after successful pattern wake up detection.
- V_{CC} undervoltage detectors are active for undervoltage detection and recovery (see Chapter 4.3.4 for details).

4.2.3 OFF Mode

The non-operation OFF Mode is introduced offering total passive behaviour to the CAN bus system. The OFF Mode is entered if VCC drops below the lower undervoltage detection threshold $V_{uvd(swoff)(VCC)}$. This feature is very usefull in applications, which by intention get completely unpowered in some use cases. The total passive behavior makes sure, that the remaining CAN network does not get influenced by such an unpowered node.

In OFF Mode the transceiver provides following functions:

- The CAN transmitter is off.
- The normal CAN receiver is off.
- The low power CAN receiver is off.
- CANH and CANL are floating (lowest leakage current on bus pins).
- V_{CC} undervoltage detectors are active for undervoltage recovery (see Chapter 4.3.4 for details).

Table 5. Characteristics of the different modes

Operating mode	STB pin	V_{CC} undervoltage		RXD pin		Bus bias	TXD pin	CAN driver
		< $V_{uvd(swoff)(VCC)}$	< $V_{uvd(stb)(VCC)}$	Bus dominant	Bus recessive			
Normal	0	no	no	LOW	HIGH	$V_{CC}/2$	0	dominant [1]
							1	recessive
Standby	1	no	no	LOW (after wake-up pattern detection) [2]	HIGH [2]	GND	X	off
	X	no	yes					
OFF	X	yes	(yes)	V_{CC} [3]	V_{CC} [3]	float	X	off

[1] $t < t_{to(dom)TXD}$, afterwards the TXD dominant clamping detection disables the transmitter.

[2] RXD follows the bus via its low power receiver

[3] RXD follows the V_{CC} voltage

4.3 System fail-safe features

4.3.1 TXD dominant clamping detection in Normal Mode

The TJA1044 provides TXD dominant clamping detection in Normal Mode (as for the TJA1057). Please refer to chapter 3.3.1 for more details.

4.3.2 Bus dominant clamping prevention at entering Normal Mode

The TJA1044 provides bus dominant clamping prevention at entering Normal Mode (as for the TJA1057). Please refer to chapter 3.3.2 for more details.

4.3.3 Bus dominant clamping detection in Standby Mode

For system safety reasons a new bus dominant timeout function in Standby Mode is introduced in the TJA1044. At any bus dominant condition in Standby Mode the RXD pin

gets switched LOW once the wake-up pattern is detected correctly. If the dominant condition holds for longer than the timeout $t_{to(dom)bus}$, the RXD pin gets set HIGH again in order to prevent generating a permanent wake-up request at a bus failure condition. Consequently a system can now enter the Standby Mode even with a permanently dominant clamped bus.

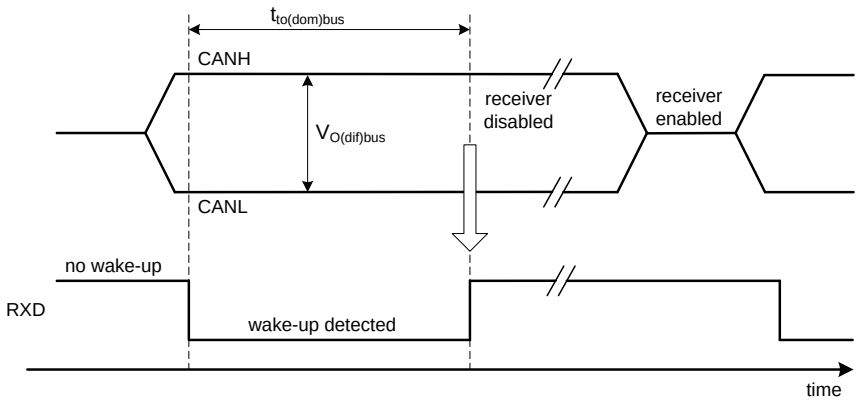


Fig 17. Bus dominant clamping in Standby Mode [1]

[1] A valid wake-up pattern needs to be detected before

4.3.4 Undervoltage detection & recovery

The TJA1044 takes advantage of high precision integrated undervoltage detection on its supply pin V_{CC} (see Table 6). Without this function undervoltage conditions might result in unwanted system behavior, if the supply leaves the specified range (e.g. the bus pins might bias to GND).

The TJA1044 offers two different undervoltage detection thresholds:

- Upper threshold $V_{uvd(stb)(VCC)}$:
  - As long as V_{CC} stays above this threshold the transceiver can stay in Normal mode and is able to proper receive and transmit data via the normal receiver and transmitter stages. The bus is biased to $V_{CC}/2$.
  - If V_{CC} drops below this threshold the transceiver will forced into stand-by mode but is still able to observe the bus on CAN traffic via the low power receiver. The bus is biased to GND.
- Lower threshold $V_{uvd(swoff)(VCC)}$:
  - If V_{CC} drops below this threshold the transceiver will forced into OFF mode and also the low power receiver is switched off. The bus will be disengaged and becomes floating.

The transceiver will recover automatically as soon as V_{CC} ramps above one of the thresholds.

Table 6. TJA1044 mode control at undervoltage conditions

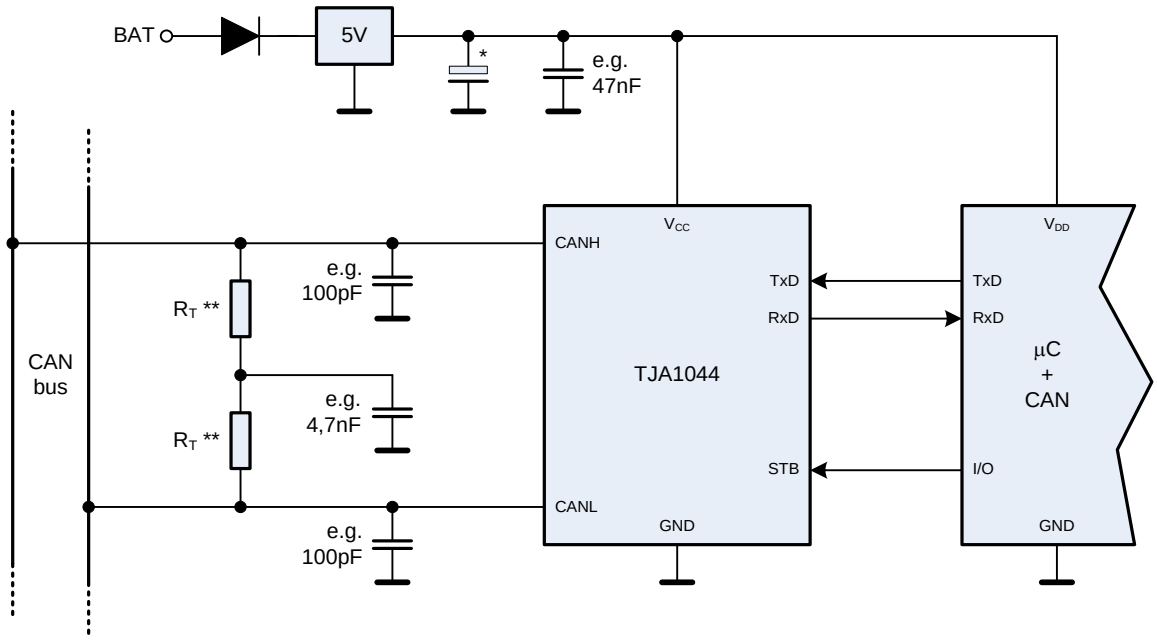
Supply condition		TJA1044
VCC > $V_{uvd(stb)(VCC)}$	VCC > $V_{uvd(swoff)(VCC)}$	Normal or Standby
VCC < $V_{uvd(stb)(VCC)}$	VCC > $V_{uvd(swoff)(VCC)}$	Standby
VCC > $V_{uvd(stb)(VCC)}$	VCC < $V_{uvd(swoff)(VCC)}$	*not applicable*
VCC < $V_{uvd(stb)(VCC)}$	VCC < $V_{uvd(swoff)(VCC)}$	OFF

4.3.5 Overtemperature protection

As the TJA1057 the TJA1044 provides an overtemperature protection. Please refer to chapter 3.3.5 for more details.

4.4 Hardware application

Fig 18 and Fig 19 show how to integrate the TJA1044 within typical applications. The application examples assume either a 5V or a 3.3V supplied host microcontroller. In each example there is a dedicated 5V regulator supplying the TJA1044 transceiver on its V_{CC} supply pin (necessary for proper CAN transmit capability compliant to ISO 11898).



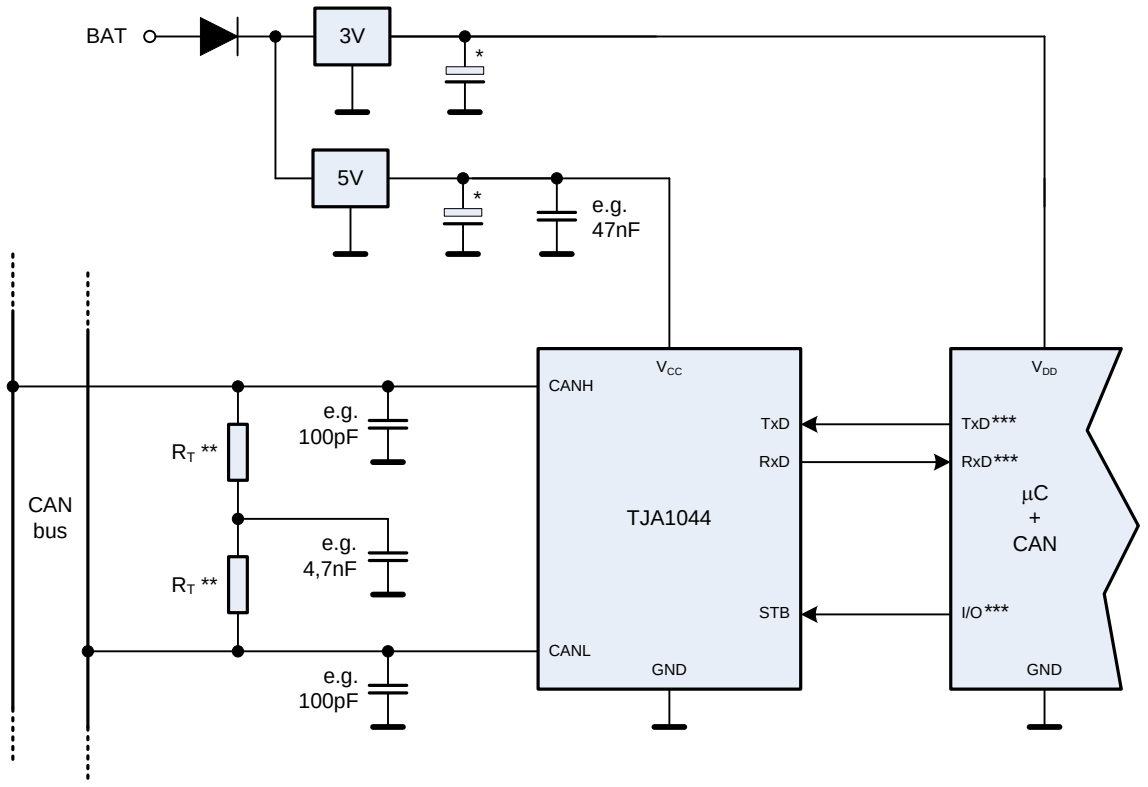
* Size of capacitor depends on regulator.

** For bus line end nodes RT = 60Ohm in order to support the „Split termination concept“
For stub nodes an optional "weak" termination of e.g. RT = 1,3kOhm can be foreseen, if required by the OEM.

General remark: A dedicated application may depend on specific OEM requirements.

Fig 18. Typical application with TJA1044 and a 5V microcontroller

To support 3.3V supplied microcontrollers the TJA1044 has a fully compatible interface towards 3.3V-microcontroller as long as the microcontroller pins connected to RXD, TXD and STB are 5V tolerant.



* Size of capacitor depends on regulator.

** For bus line end nodes R_T = 60Ohm in order to support the „Split termination concept“.
For stub nodes an optional "weak" termination of e.g. R_T = 1,3kOhm can be foreseen, if required by the OEM.

*** The RXD, TXD and I/O pins of the µC need to be 5V tolerant.

General remark: A dedicated application may depend on specific OEM requirements.

Fig 19. Typical application with TJA1044 and a 3.3V microcontroller

Note: For detailed hardware application guidance please refer to chapter 5 explaining how the pins of the TJA1044 are properly connected in an application environment.

4.5 Remote Wake-up (via CAN bus)

The TJA1044 wakes up from Standby mode when a dedicated wake-up pattern as specified in ISO11898-5 is detected on the bus. This filtering helps to avoid spurious wake-up events. A spurious wake-up sequence could be triggered by, for example, a dominant clamped bus or by dominant phases due to noise or spikes on the bus.

The wake-up pattern consists of:

- A dominant phase of at least $t_{wake(busdom)}$ followed by
- A recessive phase of at least $t_{wake(busrec)}$ followed by
- A dominant phase of at least $t_{wake(busdom)}$

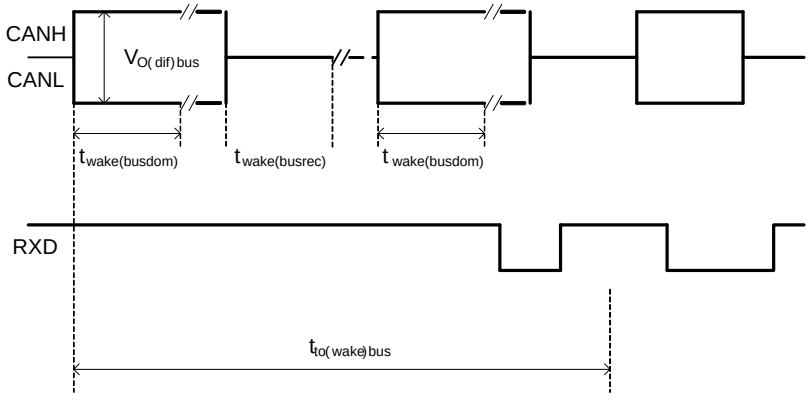
Dominant or recessive bits in-between the above mentioned phases which are shorter than the minimum $t_{wake(busdom)}$ time respectively $t_{wake(busrec)}$ are ignored.

The complete dominant-recessive-dominant pattern must be received within $t_{to(wake)bus}$ to be recognized as a valid wake-up pattern. Otherwise, the internal wake-up logic is reset. The complete wake-up pattern will then need to be retransmitted to trigger a wake-up event.

Pin RXD remains HIGH in Standby Mode until the wake-up event has been triggered. A wake-up event is not flagged on RXD if any of the following events occurs while a valid wake-up pattern is being received:

- The TJA1044 switches to Normal mode
- The complete wake-up pattern was not received within $t_{to(wake)bus}$
- A V_{CC} undervoltage is detected

If any of these events occurs while a wake-up sequence is being received, the internal wake-up logic will be reset and the complete wake-up sequence will have to be re-transmitted to trigger a wake-up event.



$t_{to(wake)bus}$ = 0.8ms to 6.5ms

$t_{wake(busdom)} = t_{wake(busrec)}$ = 0.5µs to 3µs

Fig 20. Wake-up timings and behaviour

5. TJA1046 – Dual high speed CAN transceiver with Standby Modes

5.1 Main features

The TJA1046 is a dual high speed CAN transceiver comprising two fully independent TJA1044GT transceiver dies on a single piece of silicon.

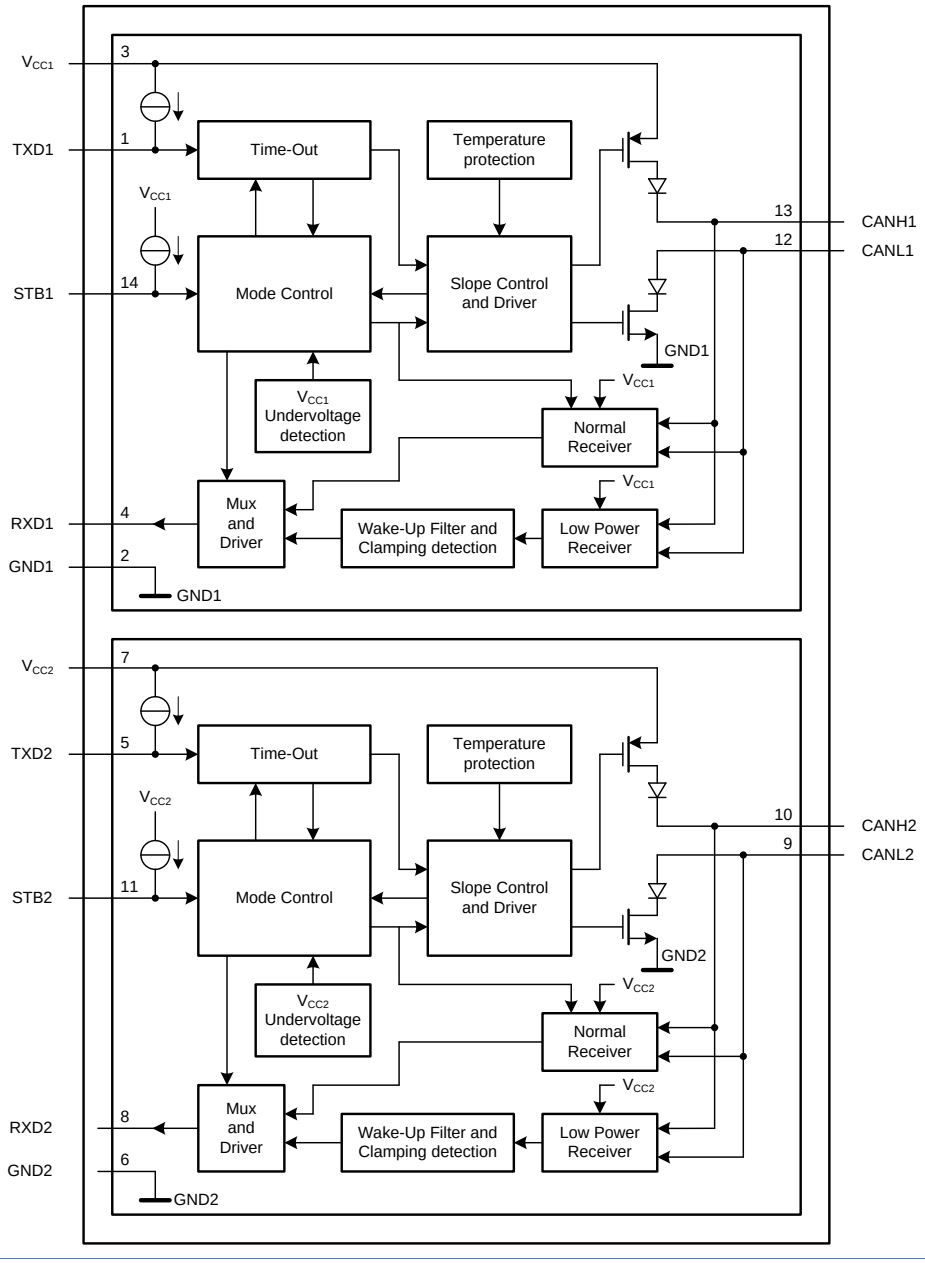


Fig 21. Block diagram of the TJA1046

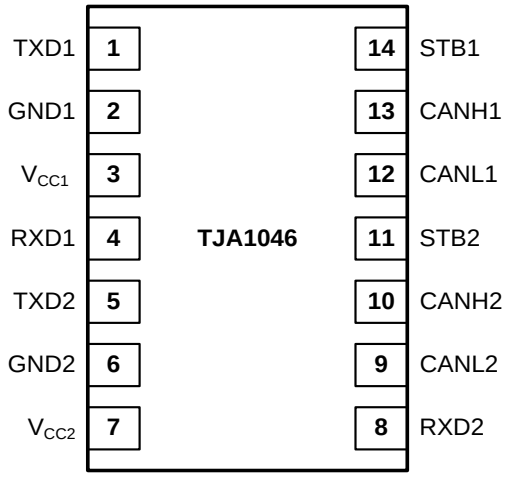


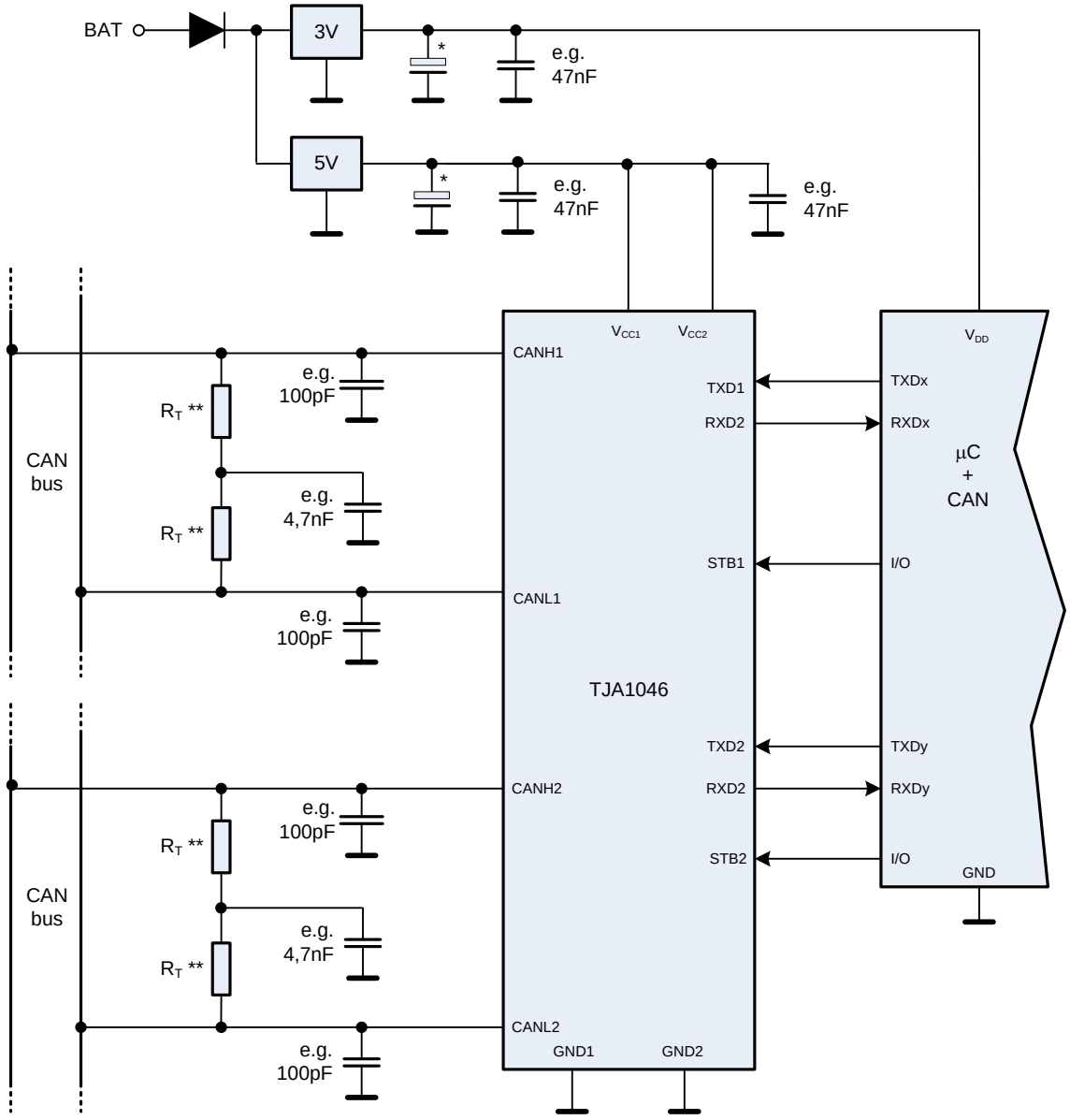
Fig 22. Pinning of the TJA1046

No resources are shared. With this each transceiver channel has its own supply and ground pins without internal interconnections. The mode control, wake up capability, clamping of each channel doesn't influence the other channel.

Because of this all descriptions as given in Chapter 4 "TJA1044 – High speed CAN transceiver with Standby Mode" are also valid for each channel of the TJA1046.

5.2 Hardware application

Fig 23 shows an example how to integrate the TJA1046 within a typical application together with a 3.3V supplied host microcontroller. To support 3.3V supplied microcontrollers the TJA1046 has a fully compatible interface towards 3.3V-microcontroller as long as the microcontroller pins connected to RXDx, TXDx and STBx are 5V tolerant.



* Size of capacitor depends on regulator.

** For bus line end nodes R_T = 60Ohm in order to support the „Split termination concept“.
For stub nodes an optional "weak" termination of e.g. R_T = 1,3kOhm can be foreseen, if required by the OEM.

General remark: A dedicated application may depend on specific OEM requirements.

Fig 23. Typical application with TJA1046 and a 3.3V microcontroller

5.3 Footprint

The footprint of the TJA1046 can be shared with the one of the single channel transceiver TJA1044 in HVSON package, as depicted in Fig 24. This offers the freedom to adapt a single ECU design towards the needs to support either one or two CAN channels.

This is possible because pin 5 of the TJA1044 is internally not bonded and therefore it doesn't matter if this pin is routed to a µC IO or not. This pin equals pin 11 of the TJA1046 device and with this the mode control pin of channel 2.

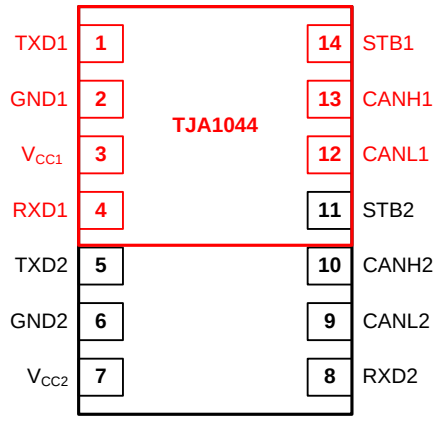


Fig 24. Shared footprint for TJA1044 and TJA1046

5.4 Overtemperature protection

Although each transceiver die has its own overtemperature protection circuitry there will be a temperature crosscoupling. Reason is that both dies are on a single piece of silicon and inside the same package. Heating one transceiver, e.g. due to a bus short cut, will result in heating also the other one.

6. Hardware application of common pins

6.1 Power Supply Pins

6.1.1 V_{CC} pin

The V_{CC} supply provides the current needed for the transmitter and receiver of the high speed CAN transceiver. The V_{CC} supply shall be designed to deliver current of 55 mA in average for the transceiver (see chapter 6.1.2).

Typically a capacitor between 47nF and 100nF is recommended being connected between V_{CC} and GND close to the transceiver. This capacitor buffers the supply voltage during the transition from recessive to dominant, when there is a sharp rise in current demand.

Using a linear voltage regulator, it is recommended to stabilize the output voltage with an additional bypass capacitor (see chapter 6.1.3) that is usually placed at the output of the voltage regulator. Its purpose is to buffer disturbances on the battery line and to buffer extra supply current demand in the case of bus failures. The calculation of the bypass capacitor value is shown in chapter 6.1.3, while in chapter 6.1.2 the average V_{CC} supply current is calculated for thermal load considerations of the V_{CC} voltage regulator. This can be done in absence and in presence of bus short-circuit conditions.

6.1.2 Thermal load consideration for the V_{CC} voltage regulator

The averages V_{CC} supply current can be calculated in absence and in presence of bus short-circuit conditions. Assuming a transmit duty cycle of 50% on pin TXD the maximum average supply current in absence of bus failures calculates to:

$$I_{CC\_norm\_avg} = 0.5 \bullet (I_{CC\_REC\_MAX} + I_{CC\_DOM\_MAX})$$

Table 7. Maximum V_{CC} supply current in recessive and dominant state

Device	$I_{CC\_REC\_MAX}$ [mA]	$I_{CC\_DOM\_MAX}$ [mA]
TJA1057	10	70
TJA1044	10	70

In presence of bus failures the V_{CC} supply current for the transceiver can increase significantly. The maximum dominant V_{CC} supply current $I_{CC\_DOM\_SC\_MAX}$ flows in the case of a short circuit from CANH to GND. Along with the CANH short circuit output current $I_{O(SC)}$ the maximum dominant V_{CC} supply current $I_{CC\_DOM\_SC\_MAX}$ calculates to about 100mA. This results in an average supply current of (100mA + 10mA) / 2 = 55mA in worst case of a short circuit from CANH to GND. The V_{CC} voltage regulator shall be able to handle this average supply current.

6.1.3 Dimensioning the bypass capacitor of the voltage regulator

Depending on the power supply concept, the required worst-case bypass capacitor and the extra current demand in the case of bus failures can be calculated.

$$C_{BUFF} = \frac{\Delta I_{CC\_max\_sc} \cdot t_{dom\_max}}{\Delta V_{max}}$$

Dimensioning the capacitor gets very important with a shared voltage supply between transceiver and microcontroller. Here, extra current demand with bus failures may not lead to an unstable supply for the microcontroller. This input is used to determine the bypass capacitor needed to keep the voltage supply stable under the assumption that all the extra current demand has to be delivered from the bypass capacitor.

The quiescent current delivered from the voltage regulator to the transceiver is determined by the recessive V_{CC} supply current I_{CC_REC}.

In absence of bus failures the maximum extra supply current is calculated by:

$$\Delta I_{CC\_max} = (I_{CC\_DOM\_MAX} - I_{CC\_REC\_MIN})$$

In presence of bus failures the maximum extra supply current may be significantly higher.

Considering the worst case of a short circuit from CANH to GND the maximum extra supply current is calculated by:

$$\Delta I_{CC\_max\_sc} = (I_{CC\_DOM\_SC\_MAX} - I_{CC\_REC\_MIN})$$

Example:

With $I_{CC\_dom\_sc\_max}$ = 100 mA and $I_{CC\_rec\_min}$ = 2 mA the maximum extra supply current calculates to

$$\Delta I_{CC\_max\_sc} = 98 \text{ mA}$$

In the case of a short circuit from CANH to GND, the bus is clamped to the recessive state, and according to the CAN protocol the uC transmits 17 subsequent dominant bits on TXD. That would mean the above calculated maximum extra supply current has to be delivered for at least 17 bit times. The reason for the 17 bit times is that at the moment the CAN controller starts a transmission, the dominant Start Of Frame bit is not fed back to RXD and forces an error frame due to the bit failure condition. The first bit of the error frame again is not reflected at RXD and forces the next error frame (TX Error Counter +8). Latest after 17 bit times, depending on the TX Error Counter Level before starting this transmission, the CAN controller reaches the Error Passive limit (128) and stops sending dominant bits. Now a sequence of 25 recessive bits follows (8 Bit Error Delimiter + 3 Bit Intermission + 8 Bit Suspend Transmission) and the V_{CC} supply current becomes reduced to the recessive one.

Assuming that the complete extra supply current during the 17 bit times has to be buffered by the bypass capacitor, the worst-case bypass capacitor calculates to:

$$C_{BUFF} = \frac{\Delta I_{CC\_max\_sc} \cdot t_{dom\_max}}{\Delta V_{max}}$$

Whereas ΔV_{max} is the maximum allowed voltage drop at pin V_{CC} and t_{dom_max} is the dominant time of 17 bit times at 500kbit/s.

Table 8. Average V_{CC} supply current (assuming 500kbit/s)

Device	$\Delta I_{CC\_max\_sc}$	t_{dom_max}	ΔV_{max}	C_{BuFF}
TJA1057	98mA	34µs	0,5V	≈ 10µF
TJA1044	98mA	34µs	0,5V	≈ 10µF

Of course, depending on the regulation capabilities of the used voltage regulator the bypass capacitor may be much smaller.

6.1.4 V_{IO} pin

Pin V_{IO} is connected to the microcontroller supply voltage to provide the proper voltage reference for the input threshold of digital input pins and for the HIGH voltage of digital outputs. It defines the ratiometric digital input threshold for interface pins TXD and S and the HIGH-level output voltage for RXD. The TJA1057/3 transceiver provide a continuous level adaptation from as low as 2.95V to 5.25V.

6.2 Interface Pins

6.2.1 TXD pin

The transceiver receives the digital bit stream to be transmitted onto the bus via the pin TXD. When applied signals at TXD show very fast slopes, it may cause a degradation of the EMC performance. Depending on the OEM an optimal series resistor of up to 1kΩ within the TXD line between transceiver and microcontroller might be useful. Along with pin capacitance this would help to smooth the edges for some degree. For high bus speeds (close to 1 Mbit/s) the additional delay within TXD has to be taken into account. Please consult the dedicated OEM specification regarding TXD connection to the host microcontroller.

6.2.2 RXD pin

The analog bit stream received from the bus is output at pin RXD for further processing within the CAN-controller. As with pin TXD a series resistor of up to 1 kΩ can be used to smooth the edges at bit transitions. Again the additional delay within RXD has to be taken into account, if high bus speeds close to 1 Mbit/s are used. Please consult the dedicated OEM specification regarding TXD connection to the host microcontroller.

6.3 Mode control pins STB / S

These input pins are mode pins and used for mode control. They are typically directly connected to an output port pin of a microcontroller.

The mode control pins have internal pull-ups to V_{CC} to ensure a safe, defined state in case these pins are left floating. As long as S / STB is not correctly driven by the µC during power-on, reset or in case of a system failure, the transceiver stays in Silent respectively Standby mode to prevent the bus to be driven dominant.

If the S / STB pins are not used they shall be connected to GND to enable a default Normal mode.

6.4 Bus Pins CANH / CANL

The transceiver is connected to the bus via pin CANH/L. Nodes connected to the bus end must show a differential termination, which is approximately equal to the characteristic impedance of the bus line in order to suppress signal reflection. Instead of a one-resistor termination it is highly recommended using the so-called Split Termination, illustrated in Fig 19 EMC measurements have shown that the Split Termination is able to improve significantly the signal symmetry between CANH and CANL, thus reducing emission. Basically each of the two termination resistors is split into two resistors of equal value, i.e. two resistors of 60Ω (or 62Ω) instead of one resistor of 120Ω. The special characteristic of this approach is that the common mode signal, available at the centre tap of the termination, is terminated to ground via a capacitor. The recommended value for this capacitor is in the range of 4,7nF to 47nF and is normally defined by the OEM.

As the symmetry of the two signal lines is crucial for the emission performance of the system, the matching tolerance of the two termination resistors should be as low as possible (desired: <1%).

Additionally it is recommended to load the CANH and CANL pin each with a capacitor of about 100pF close to the connector of the ECU (see Fig 19). The main reason is to increase the robustness to automotive transients and ESD. The matching tolerance of the two capacitors should be as good as possible.

OEMs might have dedicated circuits prescribed in their specifications. Please refer to the corresponding OEM specifications for individual details.

6.5 PCB layout rules (check list)

Following guidelines should be considered for the PCB layout.

- When a common mode choke is used, it should be placed close to the transceiver bus pins CANH and CANL.
- The PCB tracks for the bus signals CANH and CANL should be routed close together in a symmetrical way. Its length should not exceed 10cm.
- Avoid routing other “off-board” signal lines parallel to the CANH/CANL lines on the PCB due to potential “single ended” noise injection into CAN wires.
- The ESD protection should be connected close to the ECU connector bus terminals.
- Place V_{CC} capacitor close to transceiver pin.
- The track length between communication controller / µC and transceiver should be as short as possible
- The ground impedance between communication controller (µC) and transceiver should be as low as possible.
- Avoid applying filter elements into the GND signal of the µC or the transceiver. GND has to be the same for Transceiver, the µC and the external bus system.

7. Appendix

7.1 Pin FMEA

This chapter provides an FMEA (Failure Mode and Effect Analysis) for typical failure situations, when dedicated pins of the 3rd generation HS-CAN transceivers are short-circuited to supply voltages like V_{BAT}, V_{CC}/V_{IO}, GND or to neighbored pins or simply left open. The individual failures are classified, due to their corresponding effects on the transceiver and bus communication in Table 9.

Table 9. Classification of failure effects

Class	Effects
A	- Damage to transceiver - Bus may be affected
B	- No damage to transceiver - No bus communication possible
C	- No damage to transceiver - Bus communication possible - Corrupted node excluded from communication
D	- No damage to transceiver - Bus communication possible - Reduced functionality of transceiver

7.1.1 TJA1057

Table 10. TJA1057 FMEA matrix for pin short-circuits to V_{BAT} and V_{CC}

Pin	Short to V_{BAT} (12V … 40 V)		Short to V_{CC} (5V)	
	Class	Remark	Class	Remark
(1) TXD	A	Limiting value exceeded	C	TXD clamped recessive
(2) GND	C	Node is left unpowered	C	V_{CC} undervoltage detected; TRX enters Off Mode and behaves passive to the bus
(3) V_{CC}	A	Limiting value exceeded	-	-
(4) RXD	A	Limiting value exceeded	C	RXD clamped recessive; Bus communication may be disturbed
(5) n.c.	-	-	-	-
(6) CANL	B	No bus communication	B	No bus communication
(7) CANH	D	Degration of EMC; Bit timing violation possible	D	Degration of EMC; Bit timing violation possible
(8) S	A	Limiting value exceeded	C	Normal Mode not selectable

Table 11. TJA1057 FMEA matrix for pin short-circuits to GND and open

Pin	Short to GND		Open	
	Class	Remark	Class	Remark
(1) TXD	C	TXD dominant clamping; Transmitter is disabled	C	TXD clamped recessive
(2) GND	-	-	C	Undervoltage detected; TRX enters Off Mode and behaves passive to the bus
(3) V_{CC}	C	V_{CC} undervoltage detected; TRX enters Off Mode and behaves passive to the bus	C	V_{CC} undervoltage detected; TRX enters Off Mode and behaves passive to the bus
(4) RXD	C	RXD clamped dominant	C	Node may produce error frames until bus-off is entered
(5) n.c.	-	-	-	-
(6) CANL	C	Degration of EMC; Bit timing violation possible	C	Transmission not possible
(7) CANH	B	No bus communication	C	Transmission not possible
(8) S	D	Silent Mode not selectable	D	Silent Mode not selectable

Table 12. TJA1057 FMEA matrix for pin short-circuits to neighbored pins

Pin	Short to neighbored pin	
	Class	Remark
TXD - GND	C	Transmitter disabled after TXD dominant timeout
GND - V_{CC}	C	V_{CC} undervoltage detected; TRX enters Off Mode and behaves passive to the bus
V_{CC} - RXD	C	RXD clamped recessive
n.c. - CANL	-	-
CANL - CANH	B	No bus communication
CANH - S	C	TRX is not able to enter Normal Mode if the bus is driven dominant

7.1.3 TJA1057/3

Table 13. TJA1057/3 FMEA matrix for pin short-circuits to V_{BAT} and V_{CC}/V_{IO}

Pin	Short to V_{BAT} (12V … 40 V)		Short to V_{CC}/V_{IO} (5V)	
	Class	Remark	Class	Remark
(1) TXD	A	Limiting value exceeded	C	TXD clamped recessive
(2) GND	C	Node is left unpowered	C	V_{CC} undervoltage detected; TRX enters Off Mode and behaves passive to the bus
(3) V_{CC}	A	Limiting value exceeded	-	-
(4) RXD	A	Limiting value exceeded	C	RXD clamped recessive; Bus communication may be disturbed
(5) V_{IO}	A	Limiting value exceeded	-	-
(6) CANL	B	No bus communication	B	No bus communication
(7) CANH	D	Degration of EMC; Bit timing violation possible	D	Degration of EMC; Bit timing violation possible
(8) S	A	Limiting value exceeded	C	Normal Mode not selectable

Table 14. TJA1057/3 FMEA matrix for pin short-circuits to GND and open

Pin	Short to GND		Open	
	Class	Remark	Class	Remark
(1) TXD	C	TXD dominant clamping; Transmitter is disabled	C	TXD clamped recessive
(2) GND	-	-	C	Undervoltage detected; TRX enters Off Mode and behaves passive to the bus
(3) V_{CC}	C	V_{CC} undervoltage detected; TRX enters Off Mode and behaves passive to the bus	C	V_{CC} undervoltage detected; TRX enters Off Mode and behaves passive to the bus
(4) RXD	C	RXD clamped dominant	C	Node may produce error frames until bus-off is entered
(5) V_{IO}	C	V_{IO} undervoltage detected; TRX enters Off Mode and behaves passive to the bus	C	V_{IO} undervoltage detected; TRX enters Off Mode and behaves passive to the bus
(6) CANL	C	Degration of EMC; Bit timing violation possible	C	Transmission not possible
(7) CANH	B	No bus communication	C	Transmission not possible
(8) S	D	Silent Mode not selectable	D	Silent Mode not selectable

Table 15. TJA1057/3 FMEA matrix for pin short-circuits to neighbored pins

Pin	Short to neighbored pin	
	Class	Remark
TXD - GND	C	Transmitter disabled after TXD dominant timeout
GND - V_{CC}	C	V_{CC} undervoltage detected; TRX enters Off Mode and behaves passive to the bus
V_{CC} - RXD	C	RXD clamped recessive
V_{IO} - CANL	B	No bus communication
CANL - CANH	B	No bus communication
CANH - S	C	TRX is not able to enter Normal Mode if the bus is driven dominant

7.1.4 TJA1044

Table 16. TJA1044 FMEA matrix for pin short-circuits to V_{BAT} and V_{CC}

Pin	Short to V_{BAT} (12V … 40 V)		Short to V_{CC} (5V)	
	Class	Remark	Class	Remark
(1) TXD	A	Limiting value exceeded	C	TXD clamped recessive
(2) GND	C	Node is left unpowered	C	V_{CC} undervoltage detected; TRX enters - Standby Mode (TJA1042/3) - Off Mode (TJA1042)
(3) V_{CC}	A	Limiting value exceeded	-	-
(4) RXD	A	Limiting value exceeded	C	RXD clamped recessive; Bus communication may be disturbed
(5) n.c.	-	-	-	-
(6) CANL	B	No bus communication	B	No bus communication
(7) CANH	D	Degration of EMC; Bit timing violation possible	D	Degration of EMC; Bit timing violation possible
(8) STB	A	Limiting value exceeded	C	Normal Mode not selectable

Table 17. TJA1044 FMEA matrix for pin short-circuits to GND and open

Pin	Short to GND		Open	
	Class	Remark	Class	Remark
(1) TXD	C	TXD dominant clamping; Transmitter is disabled	C	TXD clamped recessive
(2) GND	-	-	C	Undervoltage detected; TRX enters Off Mode and behaves passive to the bus
(3) V_{CC}	C	V_{CC} undervoltage detected; TRX enters Standby Mode	C	V_{CC} undervoltage detected; TRX enters Standby Mode
(4) RXD	C	RXD clamped dominant	C	Node may produce error frames until bus-off is entered
(5) n.c.	-	-	-	-
(6) CANL	C	Degration of EMC; Bit timing violation possible	C	Transmission not possible
(7) CANH	B	No bus communication	C	Transmission not possible
(8) STB	D	Standby Mode not selectable	C	Normal Mode not selectable

Table 18. TJA1044 FMEA matrix for pin short-circuits to neighbored pins

Pin	Short to neighbored pin	
	Class	Remark
TXD - GND	C	Transmitter disabled after TXD dominant timeout
GND - V_{CC}	C	V_{CC} undervoltage detected; TRX enters Standby Mode
V_{CC} - RXD	C	RXD clamped recessive
n.c. - CANL	-	-
CANL - CANH	B	No bus communication
CANH - STB	C	TRX is not able to enter Normal Mode if the bus is driven dominant

7.1.6 TJA1046

Table 19. TJA1046 FMEA matrix for pin short-circuits to VBAT and VCC

Pin	Short to V_{BAT} (12V … 42 V)		Short to V_{CC} (5V)	
	Class	Remark	Class	Remark
(1) TXD1	A	Limiting value exceeded	C	TXD1 clamped recessive
(2) GND1	C	Node is left unpowered	C	V_{CC} undervoltage detected; TRX1 CAN bus off
(3) V_{CC1}	A	Limiting value exceeded	-	-
(4) RXD1	A	Limiting value exceeded	C	RXD1 clamped recessive; Channel 1 bus communication may be disturbed
(5) TXD2	A	Limiting value exceeded	C	TXD2 clamped recessive
(6) GND2	C	Node is left unpowered	C	V_{CC} undervoltage detected; TRX2 CAN bus off
(7) V_{CC2}	A	Limiting value exceeded	-	-
(8) RXD2	A	Limiting value exceeded	C	RXD2 clamped recessive; Channel 2 bus communication may be disturbed
(9) CANL2	B	Channel 2 no bus communication	B	Channel 2 no bus communication
(10) CANH2	D	Channel 2 degradation of EMC; Bit timing violation possible	D	Channel 2 degradation of EMC; Bit timing violation possible
(11) STB2	A	Limiting value exceeded	D	Channel 2 Normal Mode not selectable
(12) CANL1	B	Channel 1 no bus communication	B	Channel 1 no bus communication
(13) CANH1	D	Channel 1 degradation of EMC; Bit timing violation possible	D	Channel 1 degradation of EMC; Bit timing violation possible
(14) STB1	A	Limiting value exceeded	D	Channel 1 Normal Mode not selectable

Table 20. TJA1046 FMEA matrix for pin short-circuits to GND and open

Pin	Short to GND		Open	
	Class	Remark	Class	Remark
(1) TXD1	C	TXD1 dominant clamping; Transmitter is disabled	C	TXD1 internally kept recessive
(2) GND1	-	-	C	Undervoltage detected; TRX1 enter Off Mode and behaves passive to the bus
(3) V_{CC1}	C	V_{CC} undervoltage detected; TRX1 CAN bus off	C	V_{CC} undervoltage detected; TRX1 CAN bus off
(4) RXD1	C	RXD1 clamped dominant	C	Node may produce error frames on channel 1 until bus-off is entered
(5) TXD2	C	TXD2 dominant clamping; Transmitter is disabled	C	TXD2 internally kept recessive
(6) GND2	-	-	C	Undervoltage detected; TRX2 enter Off Mode and behaves passive to the bus
(7) V_{CC2}	C	V_{CC} undervoltage detected; TRX2 CAN bus off	C	V_{CC} undervoltage detected; TRX2 CAN bus off
(8) RXD2	C	RXD2 clamped dominant	C	Node may produce error frames on channel 2 until bus-off is entered
(9) CANL2	D	Channel 2 degradation of EMC; Bit timing violation possible	C	Channel 2 transmission not possible
(10) CANH2	B	Channel 2 no bus communication	C	Channel 2 transmission not possible
(11) STB2	C	Channel 2 Standby Mode not selectable	C	Channel 2 Normal Mode not selectable
(12) CANL1	D	Channel 1 degradation of EMC; Bit timing violation possible	C	Channel 1 transmission not possible
(13) CANH1	B	Channel 1 no bus communication	C	Channel 1 transmission not possible
(14) STB1	C	Channel 1 Standby Mode not selectable	C	Channel 1 Normal Mode not selectable

Table 21. TJA1046 FMEA matrix for pin short-circuits to neighbored pins

Pin	Short to neighbored pin	
	Class	Remark
TXD1 – GND1	C	Transmitter 1 disabled after TXD1 dominant timeout
GND1 - V_{CC1}	C	V_{CC} undervoltage detected; TRX1 CAN bus off
V_{CC} - RXD1	C	RXD 1 clamped recessive
RXD1 – TXD2	C	Temporary channel 2 bus blocking possible; CAN bus 2 is released after TXD2 dominant timeout; error frames for channel 1 possible; incorrectly received data from CAN bus 1 at CAN controller 1 possible
TXD2 – GND2	C	Transmitter 2 disabled after TXD2 dominant timeout
GND2 – V_{CC2}	C	V_{CC} undervoltage detected; TRX2 CAN bus off
RXD2 – CANL2	C	RXD dominant threshold may not be reached; bit timing violation possible
CANL2 - CANH2	B	No bus communication on channel 2
CANH2 – STB2	D	TRX2 is not able to enter Normal Mode if the bus is driven dominant
STB2 – CANL1	D	TRX2 is not able to enter Standby Mode if the bus is driven dominant
CANL1 - CANH1	B	No bus communication on channel 1
CANH1 - STB1	D	TRX1 is not able to enter Normal Mode if the bus is driven dominant

7.2 Simulation models

For all NXP HS-CAN transceivers simulation models are available latest at product release. The target simulator are System Vision and SABER/HDL. Please contact NXP Semiconductors for further details.

8. Abbreviations

Table 22. Abbreviations

Acronym	Description
CAN	Controller Area Network
Clamp-15	ECU architecture, Battery supply line after the ignition key, module is temporarily supplied by the battery only (when ignition key is on)
Clamp-30	ECU architecture, direct battery supply line before the ignition key, module is permanently supplied by the battery
DLC	Data Link Control
ECU	Electronic Control Unit
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
FMEA	Failure Mode and Effects Analysis
OEM	Original Equipment Manufacturer
PCB	Printed Circuit Board

9. References

[1] Product data sheet TJA1044, High-speed CAN transceiver with Standby Mode – NXP Semiconductors

[2] Product data sheet TJA1051, High-speed CAN transceiver – NXP Semiconductors

[3] Product data sheet TJA1046, Dual High-speed CAN transceiver with Standby Mode – NXP Semiconductors

[4] TR1014 Application Hints - Standalone high speed CAN transceiver TJA1042 / TJA1043 / TJA1048 / TJA1051, NXP Semiconductors, Document Number: AH1014

[5] TR1135 Rules and recommendations for in-vehicle CAN networks, NXP Semiconductors

[6] Road Vehicles – Controller Area Network (CAN) – Part 2: High-speed medium access unit, ISO 11898-2, International Standardization Organization, 2003

[7] Road Vehicles – Controller Area Network (CAN) – Part 5: High-speed medium access unit with low power mode, ISO 11898-5, International Standardization Organization, 2007

[8] High Speed CAN (HSC) for Vehicle Applications at 500kbps - SAE J2284, 2009

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