Introduction to Vybrid

Rich Apps in Real Time

AMF-ENT-T0805

Freescale Microcontroller Group

Designing with Freescale Market Solutions Seminar – Toronto, Canada

- **Introduction to Vybrid** (2 Hours)
  - Asymmetrical multicore architecture (Cortex A5+M4) enables industrial designs with high end graphical user interfaces and also lowest power embedded control and processing.

- **Speaker:**

Clark Jarvis
Technical Marketer / Enablement Engineer
Freescale Microcontroller Group
Austin, Texas

Introduction to Vybrid - Agenda

- Product Overview, Use Cases, & Key Differentiators
- Software and Tools
- Architectural Details
  - General : Multi-core Communication, Semaphores, Shared Memory, Interrupts, System Power, Memory Details
  - Booting
  - Clocking and Low Power
  - Security
  - Audio and Video
- Demonstrations
- Q&A

Freescale Solutions Built on ARM® Processors

	Kinetis Microcontrollers *Design Potential. Realized*	Vybrid Controller Solutions *Rich Apps in Real Time.*	i.MX Applications Processors *Your Interface to the World.*
Use Case	• Applications requiring embedded flash (microcontrollers) • Low-power applications • Metering, medical, instrumentation, factory automation, building control, consumer, PC accessories, power conversion, appliances	• Real-time applications requiring best-in-class 2D graphics and scalable vector graphics (SVG) • Optimized audio solutions for automotive and consumer • Fine motor control • Industrial Ethernet field bus	• Applications requiring advanced user interface and high-definition multimedia • Industry's premier eReader solutions • Best-in-class infotainment solutions • Display-centric smart devices
Performance within an Application	**Scalable solutions from 50 to 200 MHz built on ARM® Cortex™-M** • Up to 4 MB flash / 512 KB SRAM • Ethernet & USB HS • Support for DDR and NAND • Segment or graphics LCD	**Safe and secure real-time solutions** • ECC support • Ethernet with QoS • Timers for motor control • ADC for fine motor control • DDR-less solutions for SVG	**Industry-leading scalable, versatile and secure solutions** • Single, dual and quad core • Triple play graphics • Up to four displays • Mobile, PC, auto and industrial interfaces
Operating System	• Real-time, deterministic operating systems like MQX, Micrium uC/OS-III, FreeRTOS, ThreadX, embOS	• Real-time, deterministic operating systems like MQX, uCLinux, VelOSity • Linux	• Linux • Android • Windows • QNX

High Performance - Low-Power Embedded MPU

Industrial, Consumer & Medical embedded computing

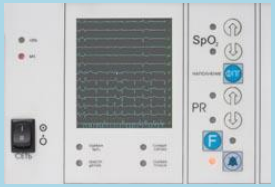
Medical instrumentation

HMI

Point of Service

Digital Video Recorders

Digital Signage



Test & measurement

Applications Needing

- High level operating system + Real-time Control
- Graphics Display, segment LCD, Video/camera Input
- Rich Connectivity: CAN, USB, SDIO, I2C, UART
- Multiple Memory Options: DDR w/ECC, NAND, Quad-SPI
- Wired & wireless networking (Ethernet, WiFi®)
- Secure processing for sensitive solutions like ePOS
- Industrial Ethernet Protocols
- Low power for extended battery life

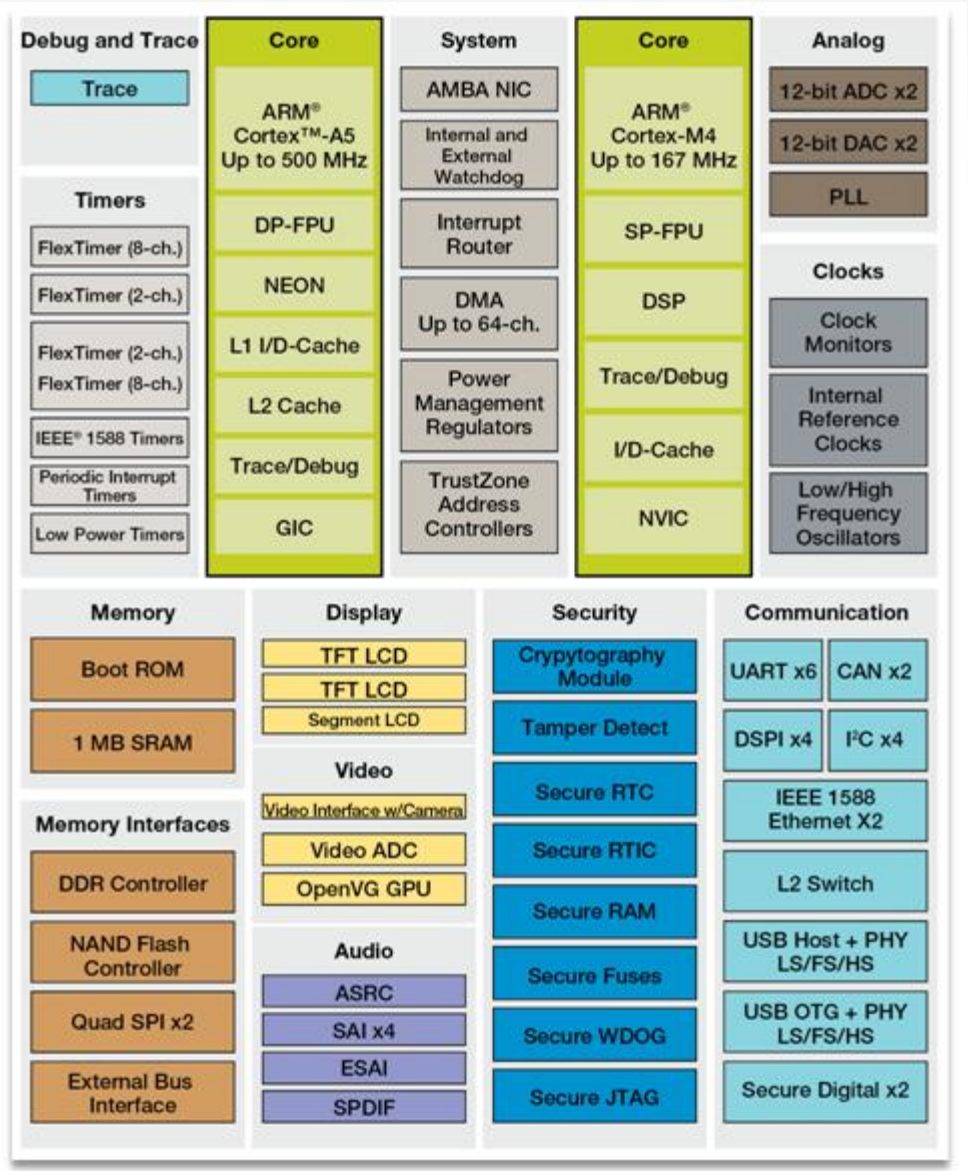
Robotic Arm Control

Single board computing

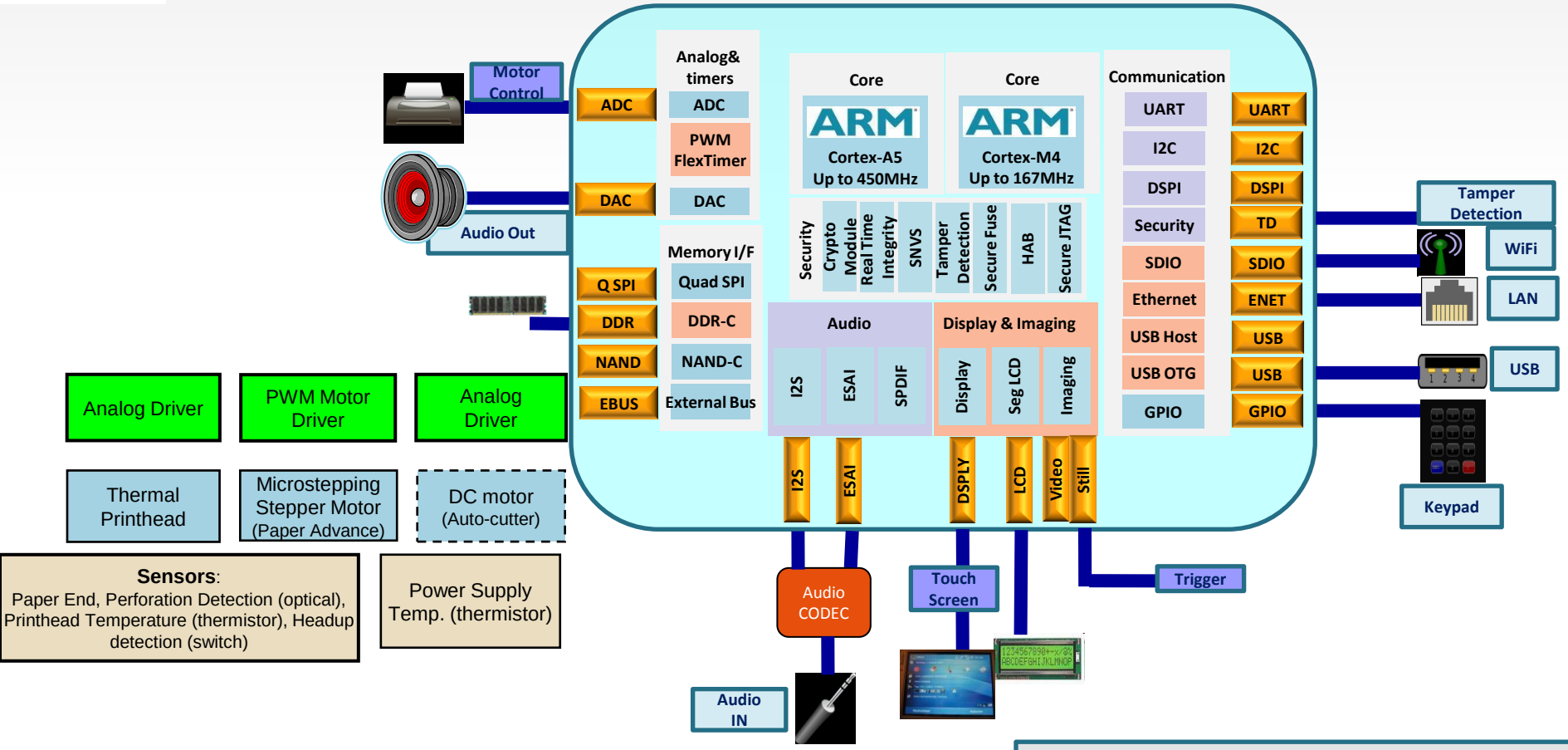
Consumer Media

Vybrid Block Diagram

- Unique heterogeneous architecture with apps processor to run high-level OS (e.g. Linux) and control processor to run RTOS (e.g. MQX)
- Ability to segment tasks that need predictable latencies to execute on the M4 and execute graphical and connectivity tasks on A5
- Secure boot and cryptographic algorithm acceleration for sensitive applications like payment systems
- Multimedia hardware IP that offloads pixels processing from the cores
- Real time sub-system including PWM and ADC for motor control
- Error Correction Code (ECC) on-chip SRAM, DDR controller and NAND flash controller



Multimedia ePOS



A5	M4
• High Level OS i.e. Linux or Android • Graphics, video and camera functions • Connectivity – Ethernet, • Human machine interfaces – Display, camera, LCD, keypad, HMI	• Real-time control – RTOS i.e. MQX – Security: Temp, Tamper – Power Mgmt – Control of I/O peripherals – Audio functions

Common Feature List

- 1.5MB SRAM
- 10/100 Ethernet w/IEEE 1588 Support
- USB HOST and Device have PHY
- USB support for HS/FS/LS
- VIU can take both digital and analog inputs
- GPU for 2.5D acceleration

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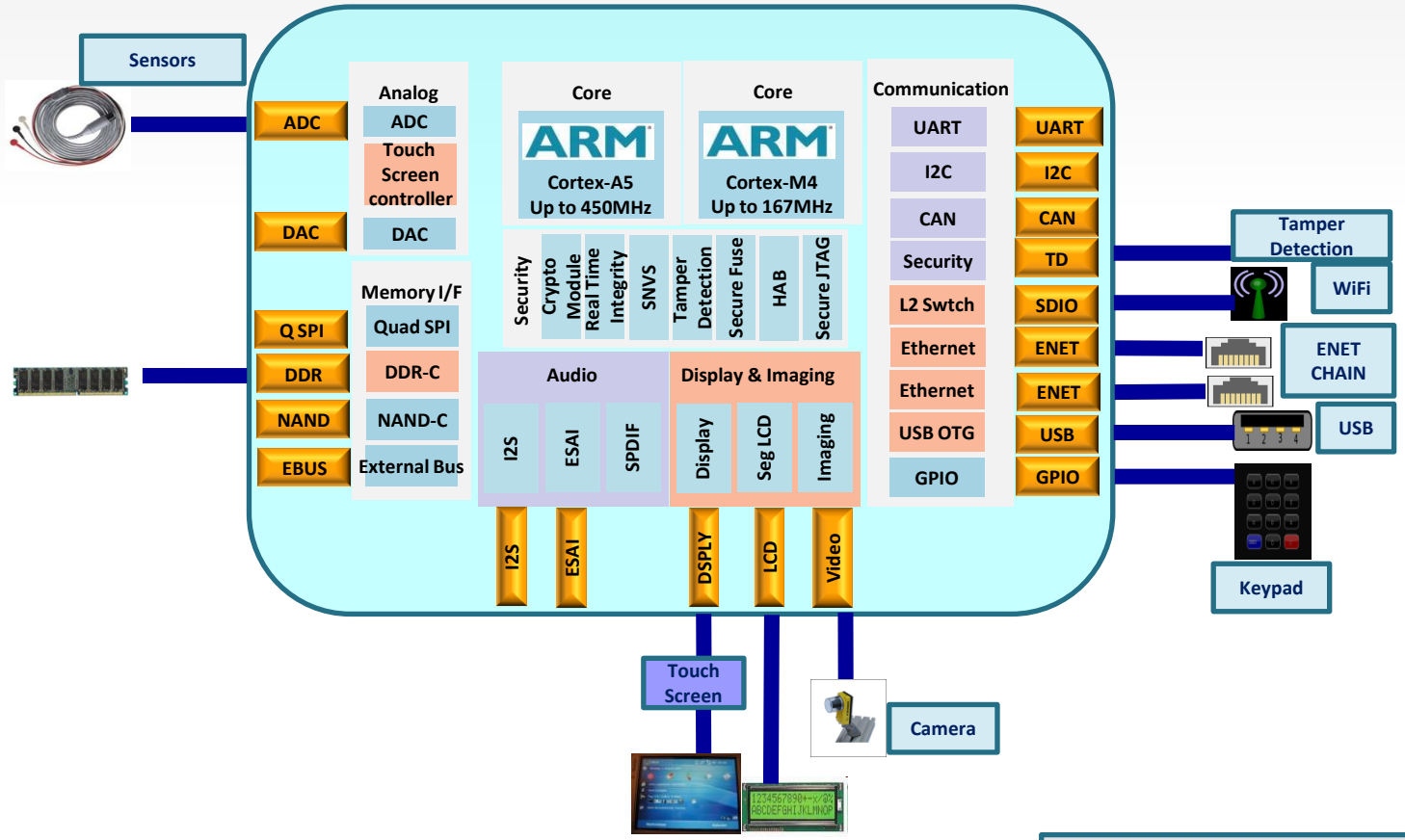
Machine Control with Camera Vision



A5	M4
• Control algorithm – Decide what happens next e.g. Position elevators , Coordinate motion in conveyors • Connectivity – Ethernet daisy chain, CAN • Human machine interfaces – Display, camera, LCD, keypad, HMI	• Real-time actuator or sensor control – Sensor inputs: Temp, current, position – Control outputs – Detect problems

Common Feature List

- 1.5MB SRAM
- 10/100 Ethernet w/IEEE 1588 Support
- USB HOST and Device have PHY
- USB support for HS/FS/LS
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- GPU for 2.5D acceleration

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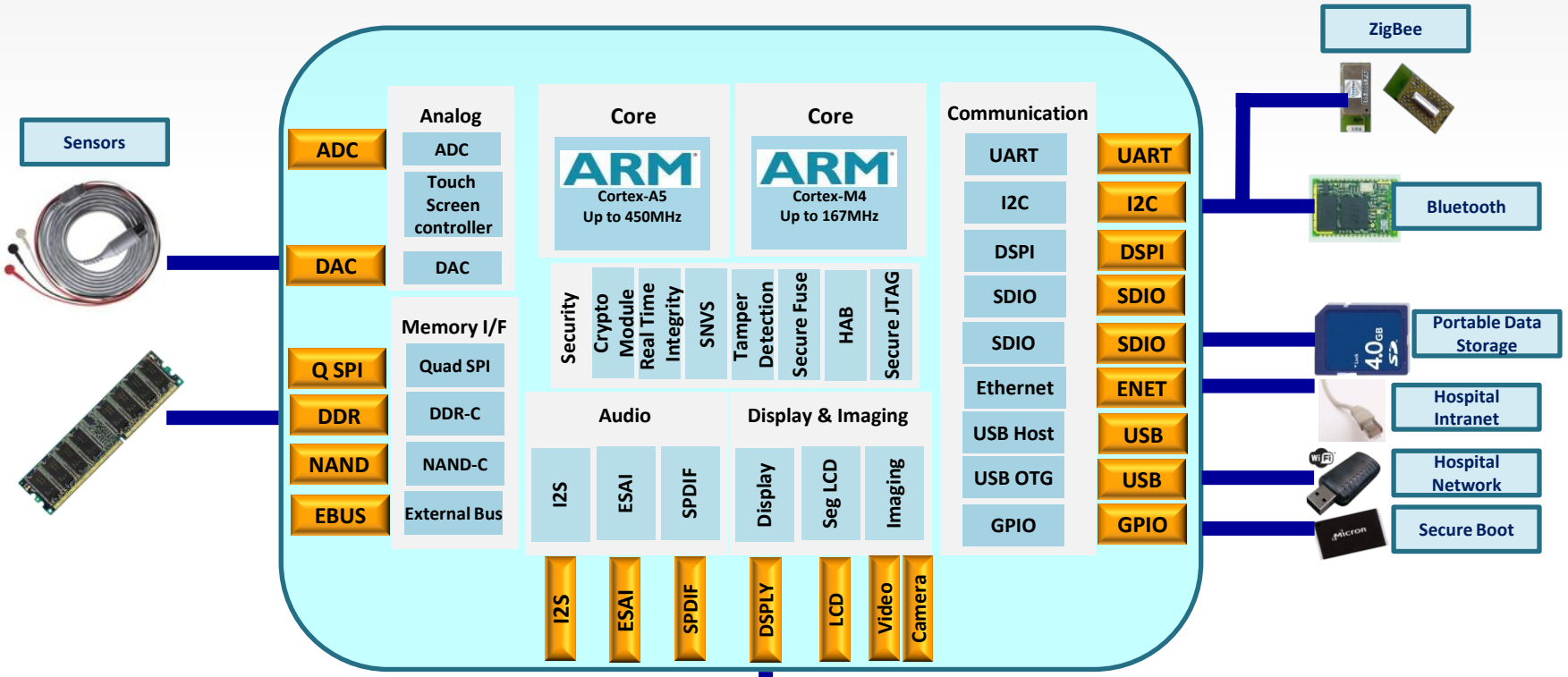
Portable Hospital Monitor



A5	M4
• High Level OS i.e. Linux or Android • video and camera functions for visual monitoring • Connectivity – Ethernet, WiFi • Human machine interfaces – Display, LCD, keypad, HMI	• Real-time control – RTOS i.e. MQX – Security: Temp, Tamper – Power Mgmt – Control of I/O peripherals for connectivity options like ZigBee and Bluetooth – Audio functions

Common Feature List

- 1.5MB SRAM
- 10/100 Ethernet
- IEEE 1588 Support
- USB HOST and Device have PHY
- USB support for HS/FS/LS
- VIU can take both digital and analog inputs
- GPU for 2.5D acceleration

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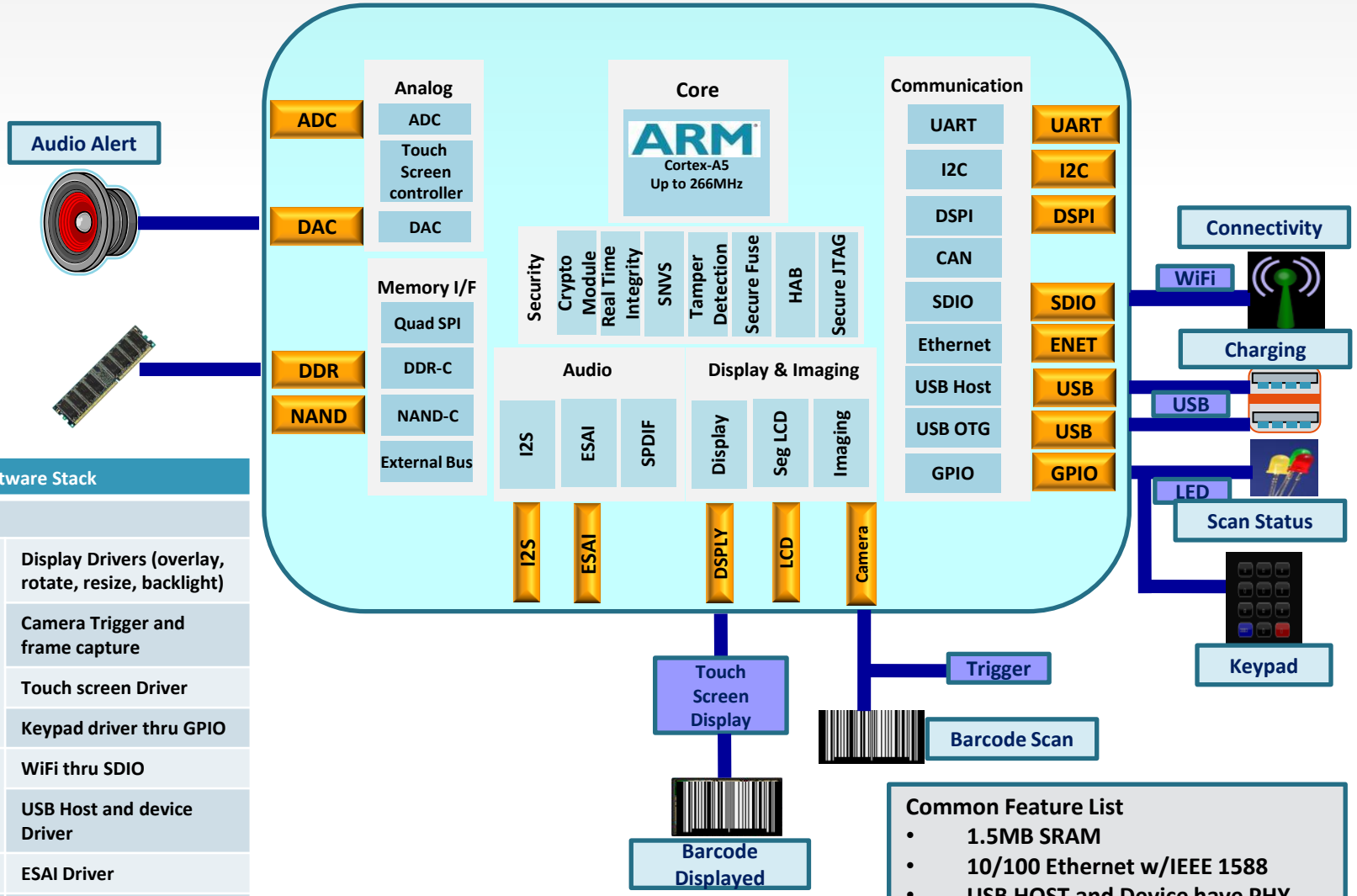
Barcode Scanner



Software Stack		
OS	Linux	
BSP	HMI	Display Drivers (overlay, rotate, resize, backlight)
		Camera Trigger and frame capture
		Touch screen Driver
		Keypad driver thru GPIO
	Connectivity	WiFi thru SDIO
		USB Host and device Driver
	Audio	ESAI Driver
	General Purpose	UART, I2C, SPI, PMIC
		A5 Kernel Bootup with Boot ROM
		DDR Drivers

Common Feature List

- 1.5MB SRAM
- 10/100 Ethernet w/IEEE 1588
- USB HOST and Device have PHY
- USB support for HS/FS/LS
- VIU - digital and analog inputs
- GPU for 2.5D acceleration

Cortex-A, Classic ARM Comparison

	ARM9	ARM11	Cortex-A5	Cortex-A8	Cortex-A9
Architecture	ARMV5	ARMV6	ARMv7 + MP	ARMv7	ARMv7 + MP
Multi-Core Capable	**No**	**Yes**	**Yes**	**No**	**Yes**
Pipeline and Machine	5-stage	8-stage	8-stage, Single issue, In-Order	13-stage, Dual Issue, in-order	8-Stage, Dual issue, Out of Order
Frequency Range (40nm)	366MHz	483MHz	300-950+MHz	600-2000 MHz	600-1900+ MHz
Power Efficiency (DMIPS/mW)	**4.5**	**3.9**	**14.4**	**4**	**8**
DMIPS/MHz	**1.1**	**1.26**	**1.6 per CPU**	**2.0**	**2.5 per CPU**

Source: ARM™ Presentation

Vybrid Controller Solutions

Vybrid VF3xx Family

Single Chip solution with dual XiP Quad SPI, Dual Ethernet and L2 Switch for appliance and energy control

Core

Up to 266 Hz ARM Cortex-A5 with TrustZone

HMI

TFT LCD up to XGA resolution

Segment LCD

Memory

32 KB I and D L1 Cache

512 KB L2 cache

On Chip: up to 1 MB SRAM . ECC support on 512 KB

NAND flash controller with 32b ECC

Analog

2 x 12-bit ADC (12-ch), 2 x 12-bit DAC

Communication

4 x UART, 2 x CAN, 3 X SPI, 2 X I2C

Ethernet MAC with IEEE 1588

USB2.0 OTG with PHY

Audio

3 x SAI for full-duplex serial interfaces like I2S, AC97

Enhanced serial audio interface (ESAI)

Video

Video Interface unit with parallel camera interface

Security

Tamper detect, high assurance boot

True RNG

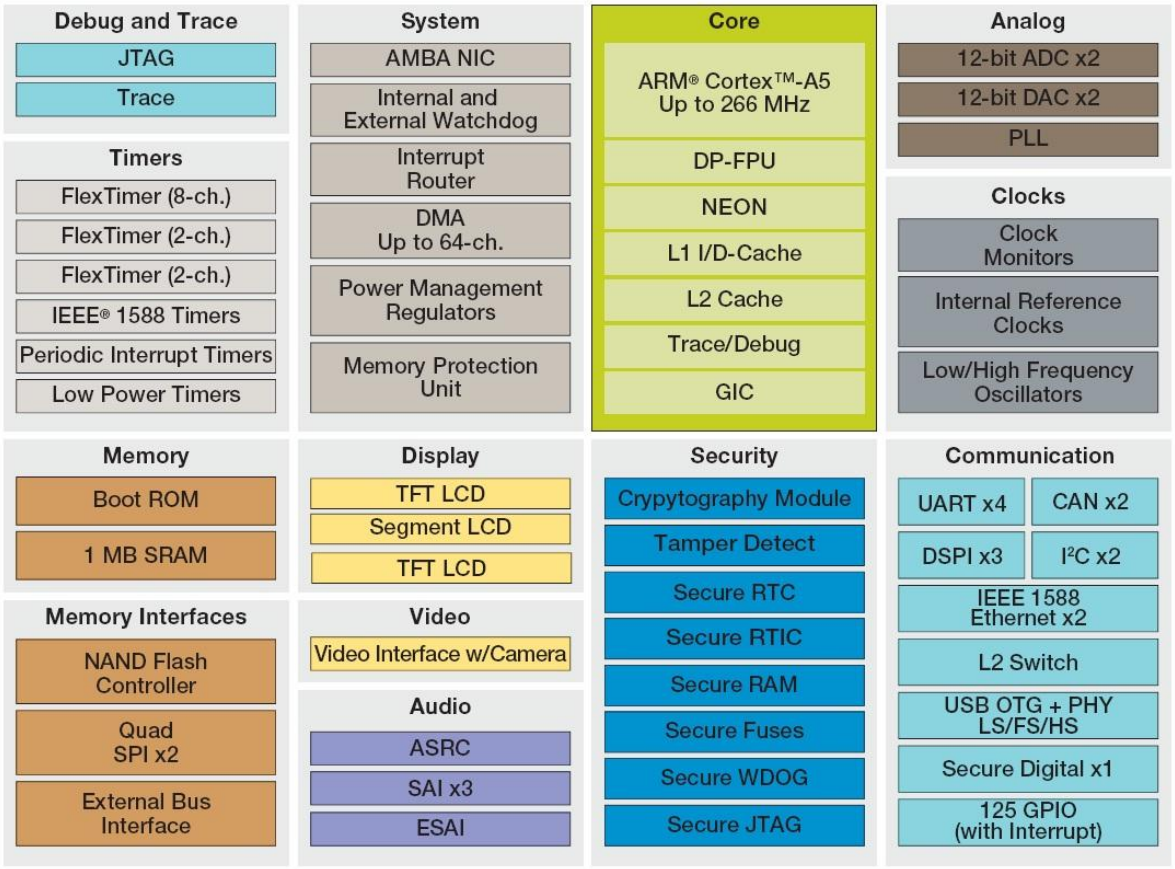
Power Management

Internal regulator (PMIC)

Package

176-pin LQFP , 364 BGA

Spec'ed to Freescale Industrial standards (-40 to 85C)



Vybrid VF5xx Family

Single Chip solution with Dual Ethernet and L2 Switch for Automation and Control

Core
Up to 450MHz ARM™ Cortex-A5 with TrustZone

HMI
TFT LCD up to XGA resolution

Memory
32KB I and D L1 Cache
512KB L2 Cache
On Chip: up to 1.0MB SRAM . ECC support on 512KB
On Chip: LPDDR2/DDR3 DRAM controller
NAND Flash Controller

Analog
2 x 12-bit ADC(16-Ch), 2 x 12-bit DAC

Communication
6 x UART, 2 x CAN, 4 X SPI, 4 X I2C
2 Ethernet MAC with IEEE1588 and L2 Switch
USB2.0 HOST and OTG with PHY

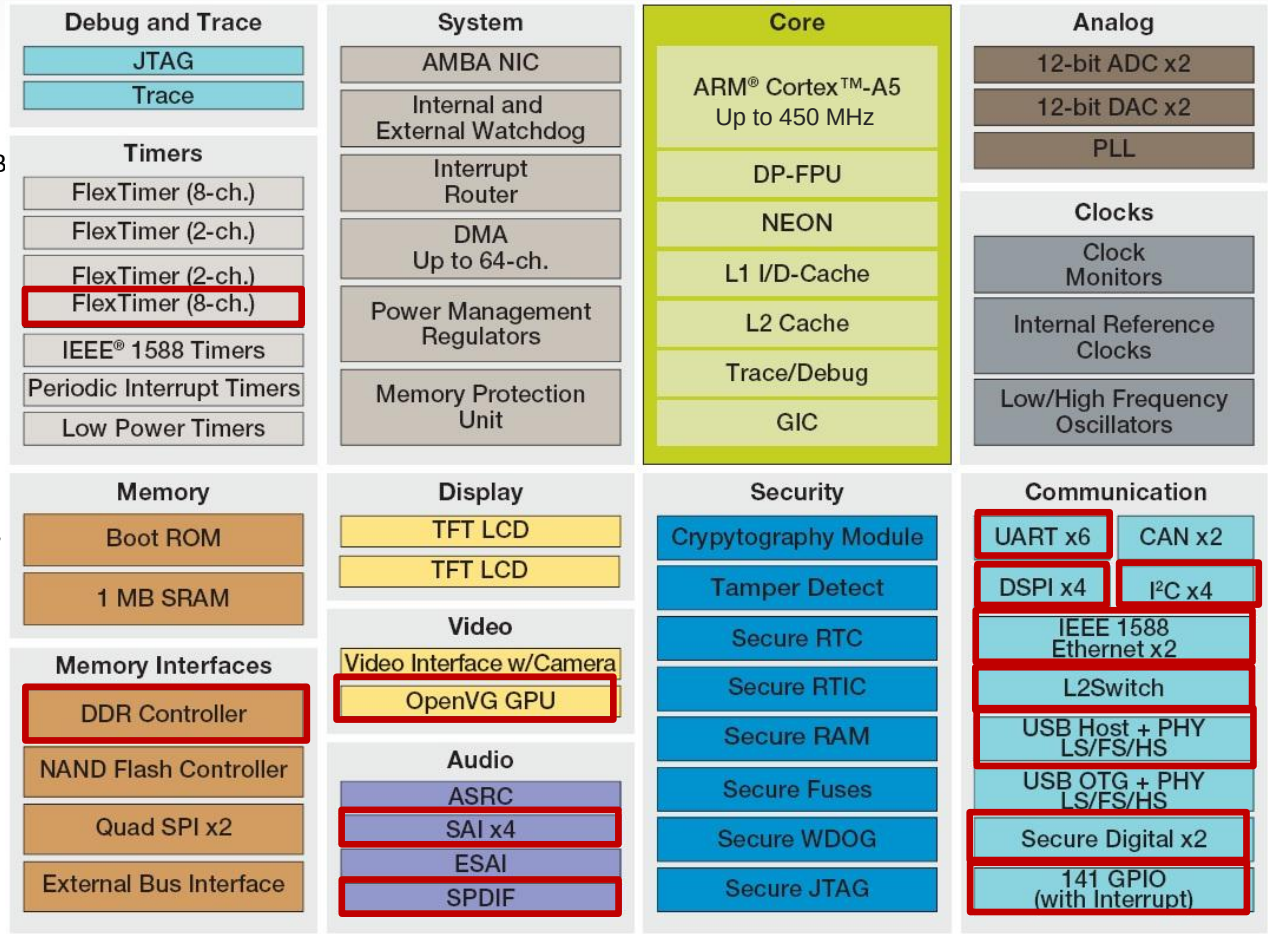
Audio
4 x SAI for full-duplex serial interfaces like I2S, AC97
ESAI – Enhanced Serial Audio Interface
SPDIF

Video
Video Interface unit with parallel camera interface
OpenVG GPU

Security
Tamper Detect, High Assurance Boot
True RNG

Power Management
Internal regulator (PMIC)

Package
17x17 0.8mm pitch 364-pin MAPBGA
Spec'ed to Freescale Industrial standards (-40 to 85C)



Changes from previous family

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Changes from previous family

Vybrid VF6xx Family

Dual heterogeneous core solution with dual XGA display, GPU for portable systems

Core
Up to 500MHz ARM™ Cortex-A5 with TrustZone
Up to 167MHz ARM™ Cortex-M4

HMI
Dual TFT LCD up to XGA resolution

Memory
32KB I and D L1 Cache for A5, 16KB I and D for M4
512KB L2 Cache and 64KB TCM for M4
On Chip: up to 1.0MB SRAM . ECC support on 512KB
On Chip: LPDDR2/DDR3 DRAM controller
NAND Flash Controller

Analog
2 x 12-bit ADC (16-Ch), 2 x 12-bit DAC

Communication
6 x UART, 2 x CAN, 4 X SPI, 4 X I2C
1 Ethernet MAC with IEEE1588
Dual USB2.0 HOST and OTG with PHY

Audio
4 x SAI for full-duplex serial interfaces like I2S, AC97
ESAI – Enhanced Serial Audio Interface
SPDIF

Video
Video Interface unit with parallel camera interface and
analog input
OpenVG GPU

Security
Tamper Detect, High Assurance Boot
True RNG

Power Management
Internal regulator (PMIC)

Package
17x17 0.8mm pitch 364-pin MAPBGA
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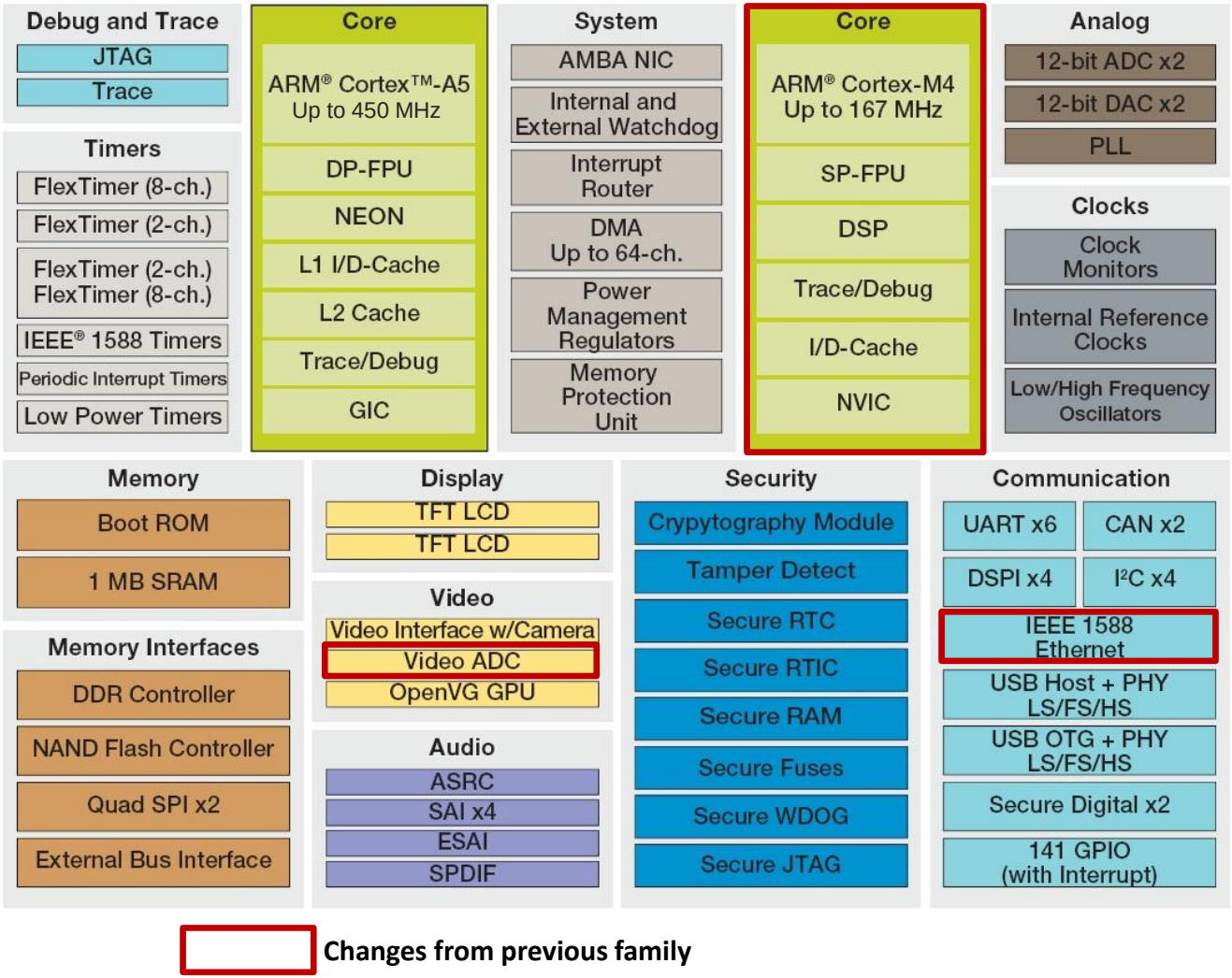

Changes from previous family

Vybrid Key Differentiators

- **Hetrogeneous Dual core architecture for real time apps**
  - Integrates Cortex M4 for real time applications
  - Supports Dual OS (Linux on Cortex A5 and MQX on M4)
  - No need for external ASICs /FPGA for deterministic real time applications

- **Integrated Power Management**
  - Core supply generated on-chip.
  - No complicated external PMIC required.
  - Simple LDO to drive IO supply.
  - Single Supply operation for LQFP packages without DRAM.

- **(config 1) 1.5 MB on-chip SRAM**
  - Support for Dual WQVGA(480x272) without external memory(e.g. DRAM)
  - Support for Single WVGA (800x480) without external memory
  - 512K ECC supported on SRAM

- **(config 2) 1.0 MB on-chip SRAM with 512K L2 Cache**
  - 512K ECC supported on SRAM

Vybrid Key Differentiators

- **Quad SPI Flash Interface**
  - Support for Dual QuadSPI
  - Support Execute-In-Place (XIP)
  - Upto 160MB/s peak bandwidth (limited by external Memory bandwidth)
  - Lower cost alternative to NOR/NAND Flash

- **Integrated Video ADC**
  - Supports direct analog Video input (NTSC/PAL)
  - Up to 4 Video Inputs

- **Unique Security capabilites**
  - Trusted platform with High Assurance Boot(HAB)
  - Support for Encrypted boot
  - Support for hardware PKI
  - Anti-tamper capabilities for physical security

Vybrid Power Modes

(Preliminary)

Typical Power Modes in an embedded system	Cortex A5/M4 Power Modes	Vybrid Extended Power Modes	Recovery Time	"Typical" Idd Range
Run	Run	RUN	-	Starting @ <320uA/MHz *
► 24 Mhz Operation , PLL bypass, Peripherals OFF		LPRUN	-	20-25mA
► 32Khz/128 Khz Operation, PLL bypass, Peripherals OFF		ULPRUN	-	8-10mA
Wait	Sleep	WAIT		6-8 mA
Stop	DeepSleep	Stop	1.5 – 7 us	4-6 mA
Power Gate modes with Wakeup capability				
► Enables complete shut-down of core logic, including WKUP, further reducing leakage currents in all low power modes ► Supports 16 external input pins and 8 internal modules as wakeup sources ► Wakeup inputs are activated in LPSTOP modes		LPSTOP3	400us	80-100 uA
		LPSTOP2	400us	40-45 uA
		LPSTOP1	400us	35-40 uA
		VBAT	N/A	7-8uA

* *All modules OFF, A5@500Mhz,M4@167Mhz at TYP condition*

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  - Booting
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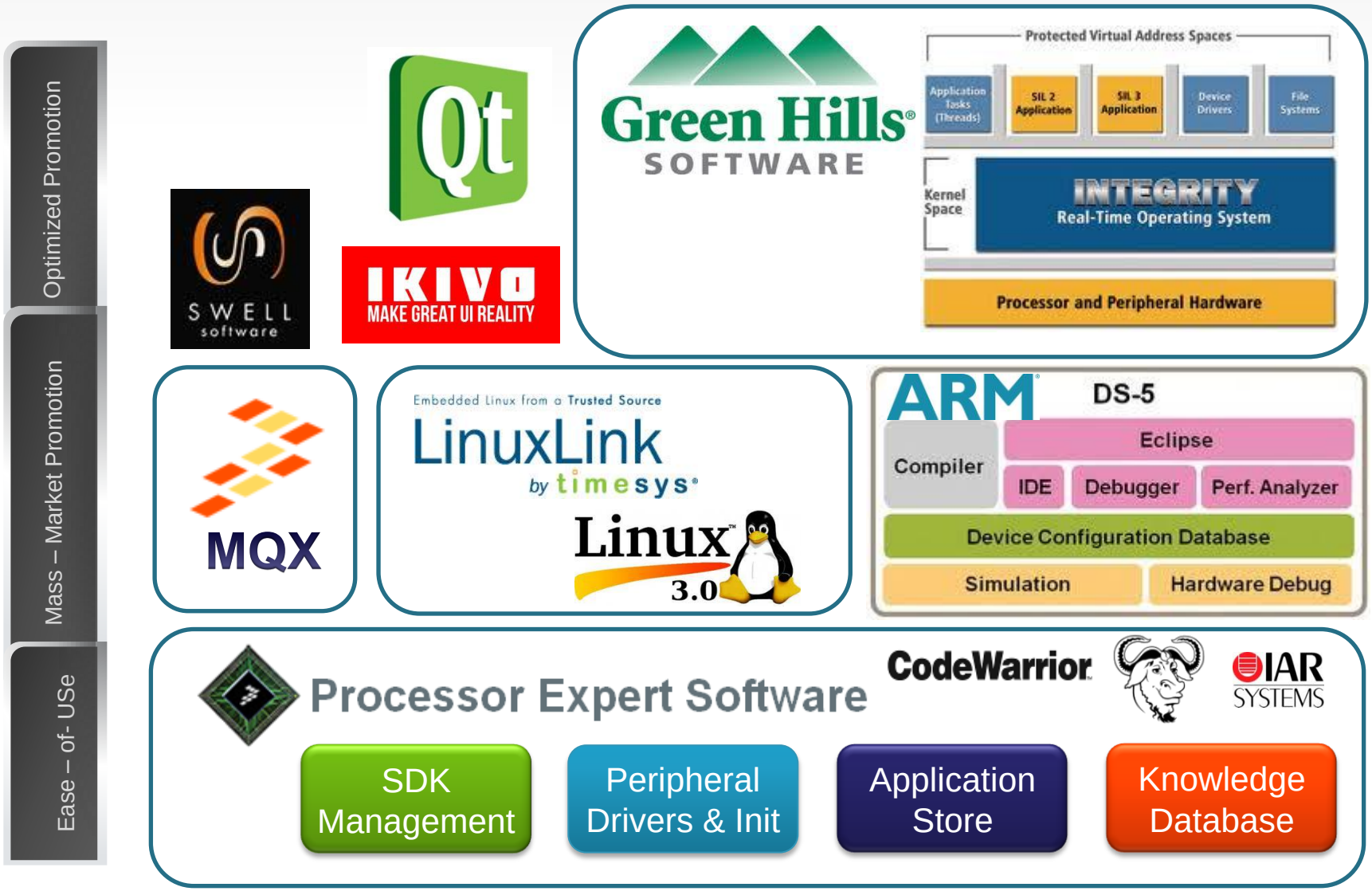
rid - Enablement Landscape



Vybrid Solution Approach: LinuxLink – Tower – MQX

Flexible LinuxLink Software Development Platform

Modular Freescale Tower System

- Modular
- Cost-effective
- Easy-to-use

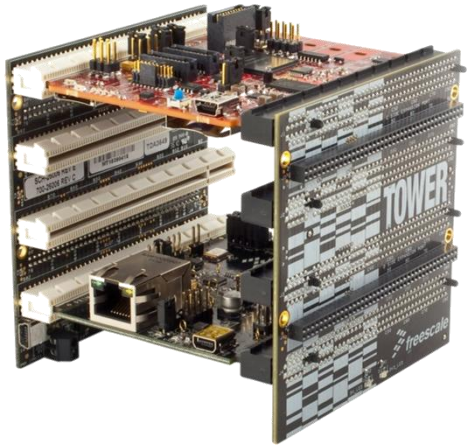
Where would you like to begin?

- Boot Linux On My Board
- Build Custom BSP/SDK
- Build an Application

Complete & custom Linux-based solution

Linuxlink cloud development allows customers to rapidly deploy pre-built or custom BSP/SDKs for Tower or other hardware platforms.

Vybrid Tower System – Leveraging the industry's most scalable development tool



TARGET: $199 Module, $269 Kit

- Integrated secure USB-JTAG Debuger (OpenSDA / CMSIS-DAP / MSD)
- Execute – in – place flash (Spansion)
- Single board computer and fully Tower compatible
- Battery back-up
- High Speed ETM Trace Port
- DDR3 / NAND / microSD
- Dual HS USB ports
- Tower PI (TWRPI) socket for radio/sensors
- Integrated FSL MMA8451Q

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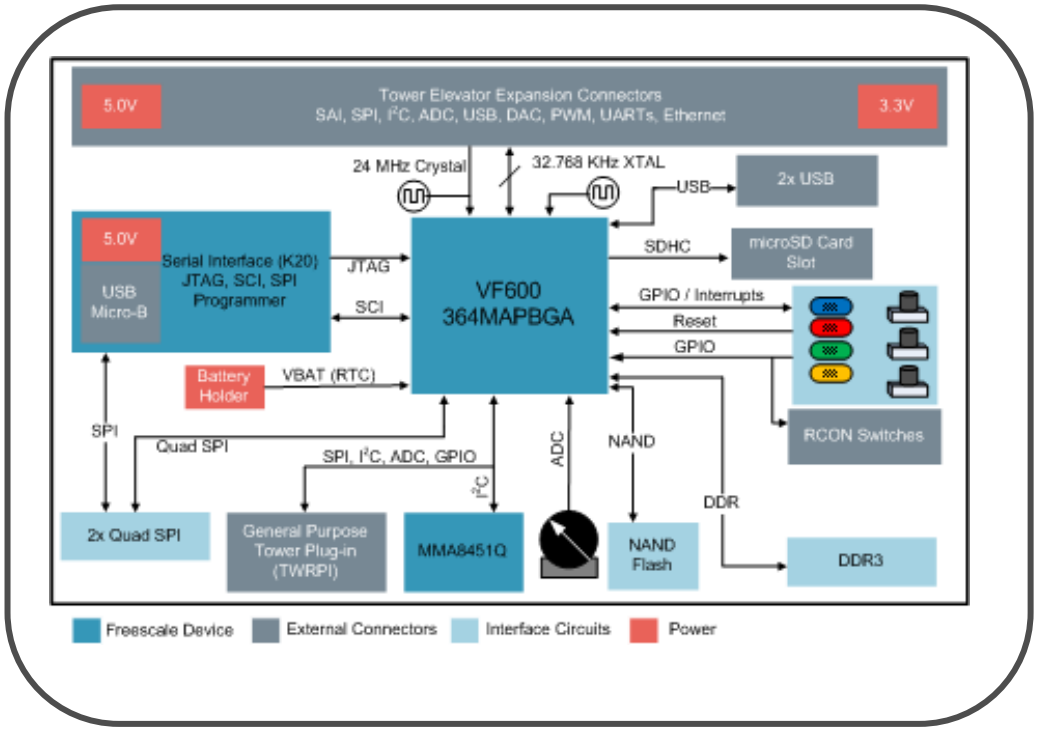
TWR-VF600 Vybrid Controller Solution Tower Board for Industrial Applications

Features:

- VF600 364 BGA
- New Serial Interface debugger with SPI programming
- Dual USB on-board
- Test points for tamper detect
- Memories
  - DDR3
  - Dual Quad SPI
  - NAND
- Standard Tower Features
  - TWRPI socket
  - Accelerometer (MMA8451Q)
  - Potentiometer
  - MicroSD Socket
  - LED's and push button switches
- Compatible Modules (non-inclusive)
  - TWR-SER2 for Dual Ethernet
  - TWR-LCD-RGB for DCU
  - TWR-Dock

TWR-VF600



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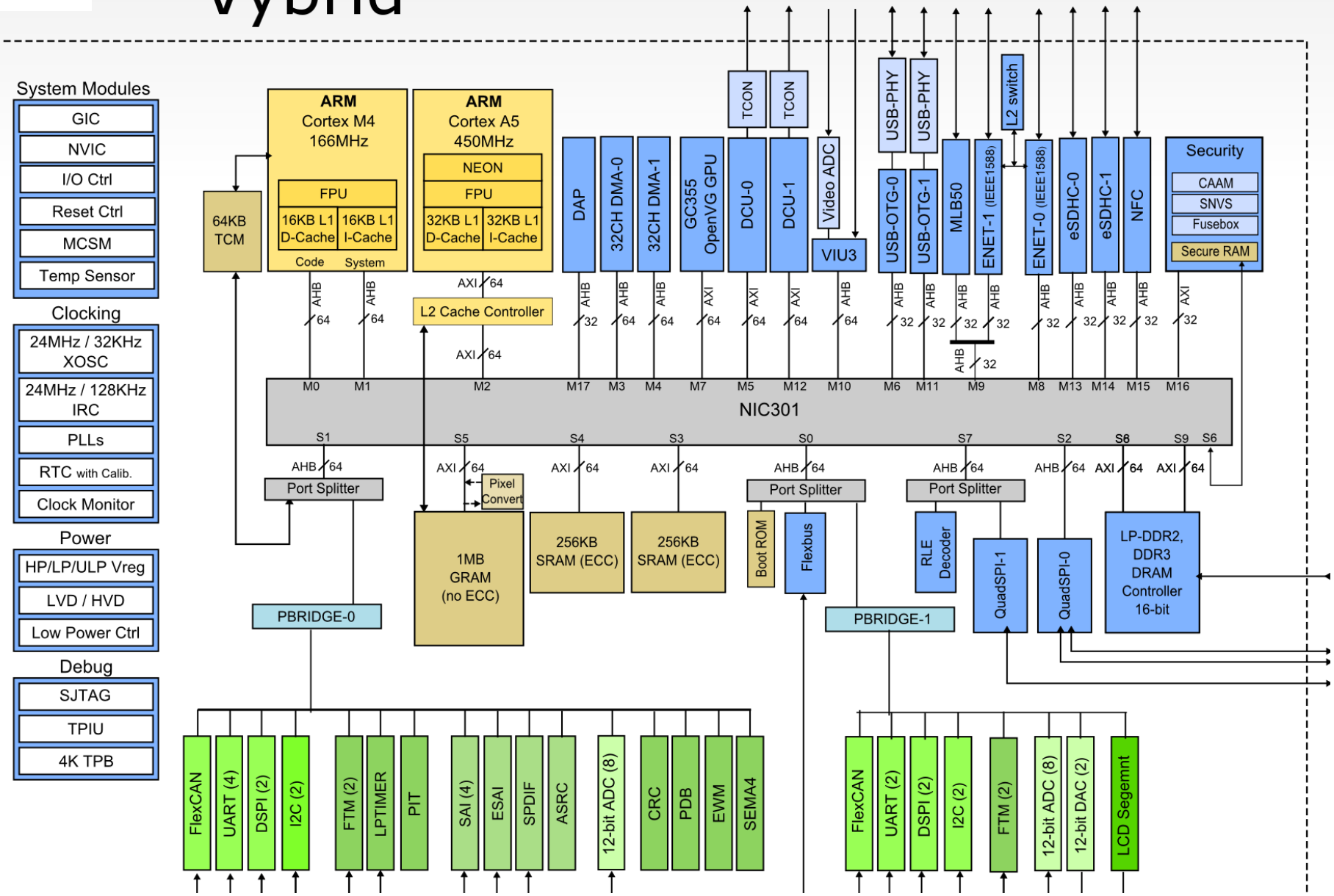
Vybrid Architectural Overview

- Unique heterogeneous architecture with A5 + M4
- Ability to segment tasks that need predictable latencies (M4) and graphical and connectivity tasks (A5)
- Secure boot and cryptographic algorithm acceleration for sensitive applications like payment systems
- Multimedia hardware IP that offloads pixels processing
- Error Correction Code (ECC) on-chip SRAM, DDR controller and NAND flash controller

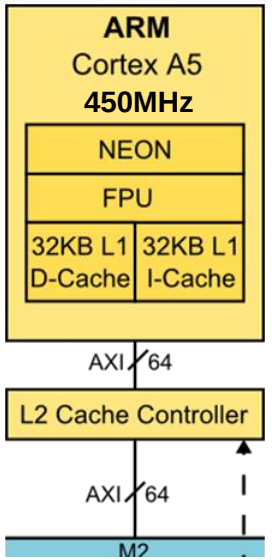
Vybrid



CortexA5 Features

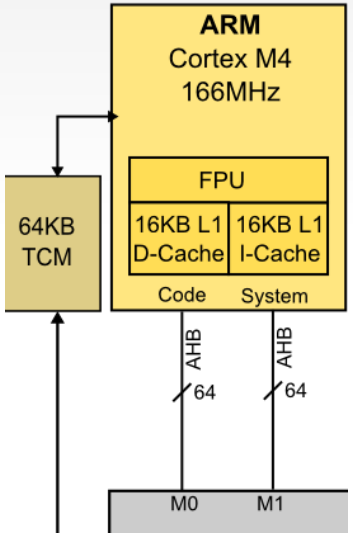
- ARM Cortex-A5 processor core
- Supports ARMv7-A instruction set architecture
  - Includes FPU (VFPv3-D16) definition
    - Single & Double precision, add, sub, mult, div, mac, sqrt
  - NEON Media Processing Engine (MPE)
    - Extends FPU capability with advanced SIMD instructions for media and signal processing functions over 8, 16, 32bit integer and 32bit floating point data types
- 8-stage single issue pipeline implementation operating at 450MHz
  - 1.57 DMIPS per MHz integer performance
  - 4-stage load/store pipeline
  - 5-stage FPU/MPE pipeline
- Processor-local Memories
  - 2 way set-associative 32 Kbyte Instruction Cache with 32 byte line size
  - 4 way set-associative 32 Kbyte Data Cache with 32 byte line size
  - Optional 512K L2 Cache
  - Standard CA5 Memory Management Unit

64-bit AXI System Bus Interface supporting multiple outstanding transactions



Cortex M4 Features

- Cortex-M4 Real-Time Control Processor
  - Operating at 1:1 clock ratio compared to platform
    - Core frequencies = 133.3 – 166.7 MHz
- 3-stage pipeline provides 1.25 DMIPS per MHz performance
  - Includes single precision FPU, DSP & SIMD ISA extensions
- 16K Code + 16K System Caches with 32-byte cache line
- 64 Kbytes of Tightly-Coupled Memory split equally across TCM{L,U}
- Modified Harvard 64-bit AHB system bus interface
  - 64-bit AHB backdoor port to TCMs
- CoreSight debug and trace system
- Nested Vector Interrupt Controller (NVIC)



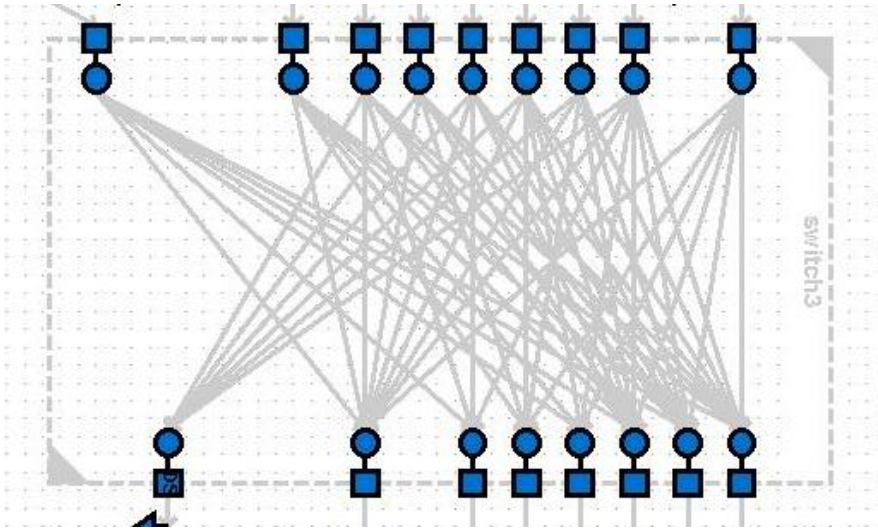
Memory Map

- Two Cortex cores share an ISA and common memory map
  - 4GB address space is effectively accessible from either core
- Memory coherency is wholly managed by software

CM4 Start	System Addresses CA5, Sys Start	Size [Mbytes]	Region Description
0x0000_0000	0x0000_0000	8.00	Boot ROM
0x0080_0000	Reserved	248.00	CM4 DDR code alias
0x1000_0000	Reserved	128.00	CM4 QuadSPI0 code alias
0x1800_0000	Reserved	112.00	CM4 FlexBus code alias
0x1f00_0000	Reserved	8.00	CM4 OCRAM code alias
0x1f80_0000	0x1f80_0000	8.00	CM4 TCML (code)
0x2000_0000	0x2000_0000	256.00	QuadSPI0
0x3000_0000	0x3000_0000	240.00	FlexBus
0x3f00_0000	0x3f00_0000	4.00	OCRAM - sysRAM
0x3f40_0000	0x3f40_0000	4.00	OCRAM - gfxRAM
0x3f80_0000	0x3f80_0000	8.00	CM4 TCMU (data)
0x4000_0000	0x4000_0000	0.44	IPS0
0x4007_0000	0x4007_0000	0.06	SecureRAM
0x4008_0000	0x4008_0000	0.50	IPS1
0x400f_f000	0x400f_f000	0.00	GPIOC
0x5000_0000	0x5000_0000	256.00	QuadSPI1
0x7800_0000	0x7800_0000	32.00	RLE
0x7a00_0000	0x7a00_0000	32.00	QuadSPI1 Rx buffer
0x7c00_0000	0x7c00_0000	32.00	QuadSPI0 Rx buffer
0x7e00_0000	0x7e00_0000	8.00	gfxRAM- RGB565 view
0x7e80_0000	0x7e80_0000	8.00	gfxRAM-ARGB1555 view
0x7f00_0000	0x7f00_0000	8.00	gfxRAM-ARGB4444 view
0x8000_0000	0x8000_0000	1536.00	DDR
0xe000_0000	Reserved	512.00	CM4 PPB
	0xe000_0000	512.00	DDR (CA5 only)

Network InterConnect

- Cores interface to Network InterConnect (NIC) bus fabric
  - Provides hardware interconnect matrix between masters & slaves
  - Vybrid configuration supports 18 masters + 10 slaves
  - Simultaneous multi-master transactions



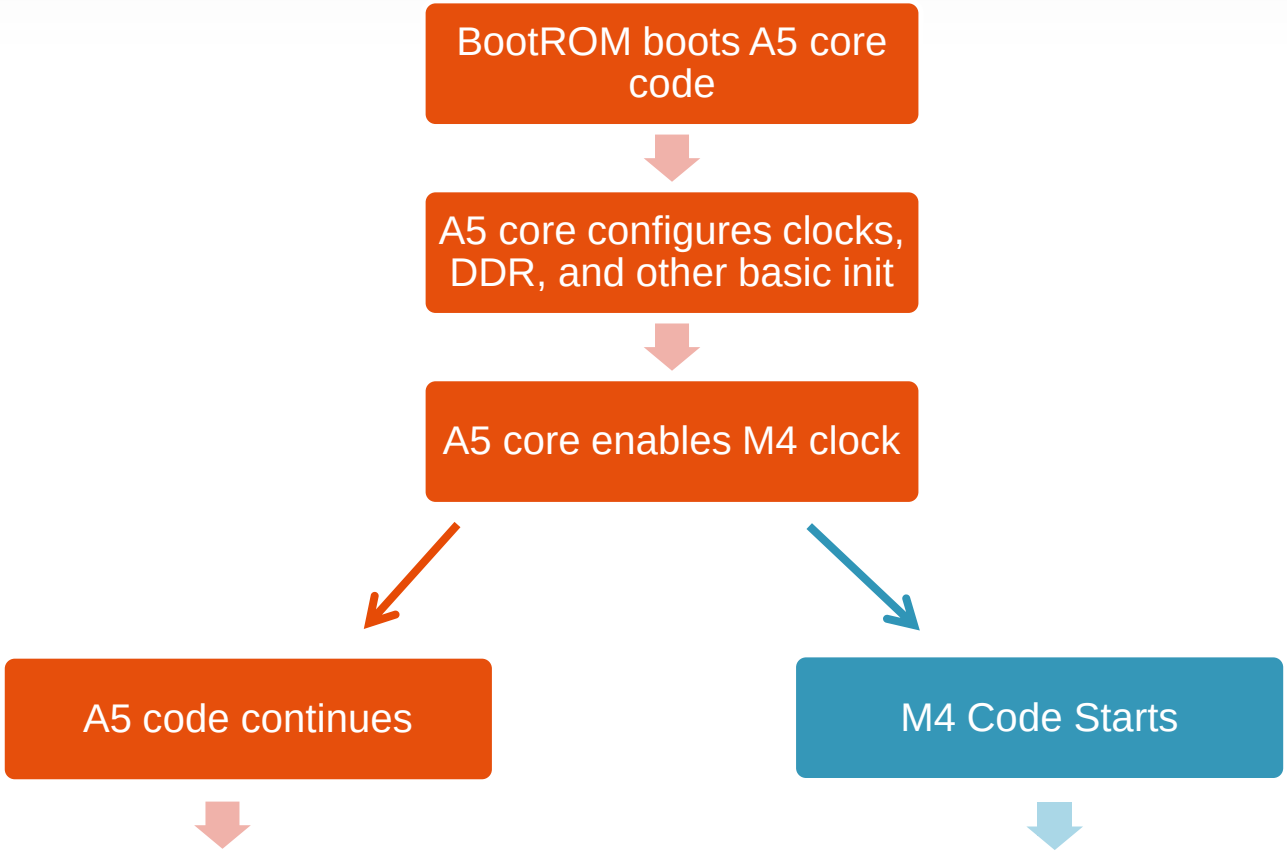
Memory Protection

- Two layered security subsystem includes:
  - Central Security Unit (CSU)
    - The CSU supports access checking based on *reference attributes for the individual slave ports of the NIC system bus switch fabric* and slave peripherals.
  - Multiple instances of AMBA TrustZone Address Space Controllers (TZASC).
    - The TZASCs provide access checking based on *memory address space regions.* In addition to the basic access controls provided by the logic associated with the CSU, Vybrid also includes 9 instances of TZASCs. This access control mechanism covering memory regions is supported on the 3 OCRAM controllers (2x OCRAM_sys, OCRAM_gfx), the 2 DDR ports, the CM4's backdoor TCM port, the 2 QuadSPIs and the FlexBus.

Vybrid Multi-core Support

- Hardware support for basic multi-core requirements
  - Peripheral interrupt steering
  - Directed CPU interrupts for inter-processor communication
  - Hardware Semaphores

Dual Core Startup



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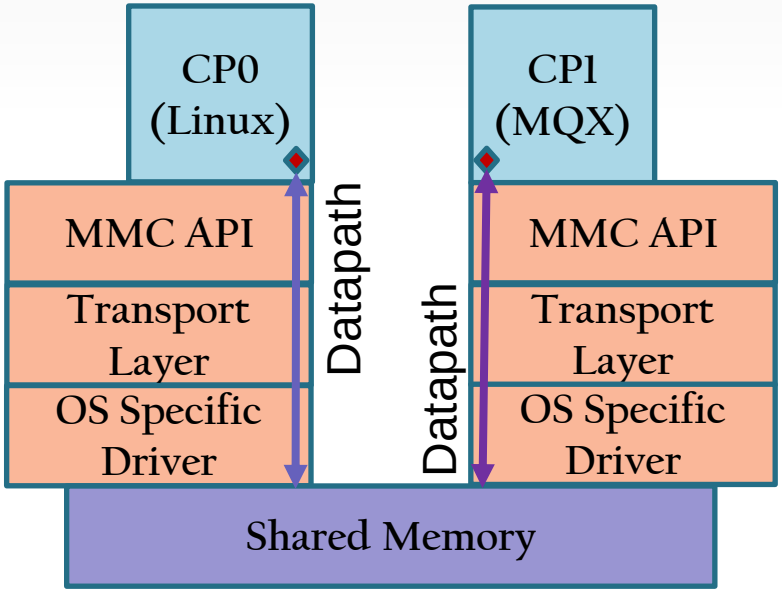
Enabling M4 Core – Code Example

```
/* Set starting point for M4 code */
/* Must be odd address since M4 is thumb */
  SRC->GPR2 = (unsigned int)0x3f040411;

/* Enable M4 core */
  CCM->CCOWR = 0x15a5a;
```

Multi-Core Communication (MCC) Software

- MCC implementation
  - CP0 = CA5 running Linux
  - CP1 = CM4 running MQX
- MMC takes place between transport layers of 2 MCAPI implementations via shared memory
- Communication is transparent to application layer
- Implemented like a socket or message queue



Controlling Multi-Core Access to Shared Resources: HW Semaphores

- 16 Hardware Semaphores
  - Used to control access to shared data structures and resources
  - Simple "lock/unlock" mechanism via a *single write access*
  - 3-state implementation
    - if gate = 0b00, then state = unlocked
    - if gate = 0b01, then state = locked by processor 0
    - if gate = 0b10, then state = locked by processor 1
  - Optional interrupt notification to indicate when the gate is unlocked
  - Secure reset mechanisms are supported to clear the contents of individual gates and/or notification logic

HW Semaphore Rules

1. All writes to shared data values or shared hardware resources must be protected by a "gate" variable.
2. Once a processor locks a gate, accesses to the shared data or resources by other processes/processors must be blocked. **This must be enforced by software.**
3. The processor that locks a particular gate is the only processor that can open (unlock) that gate.

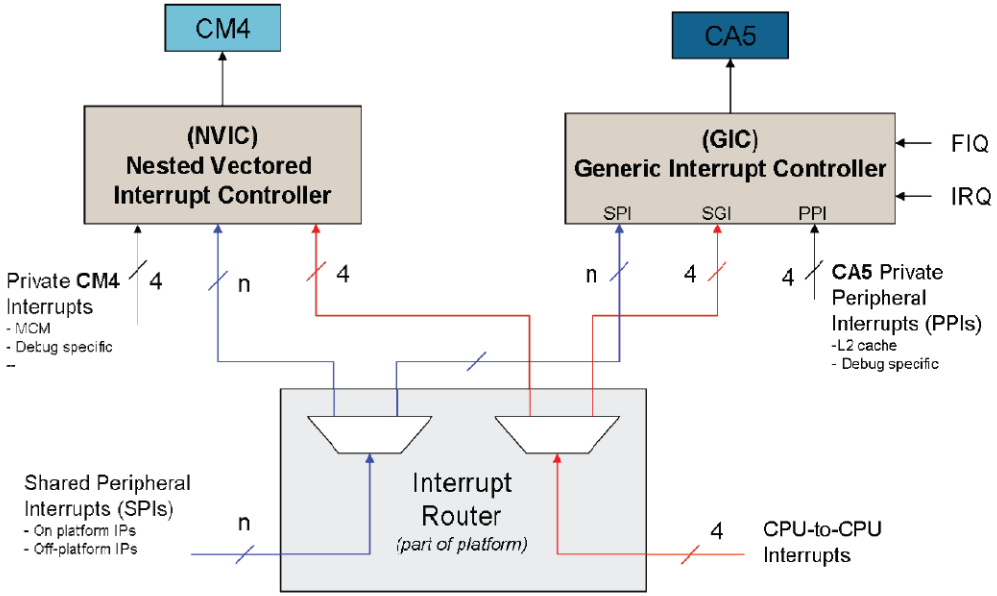
HW Semaphores: Simple Coding Example

```
/* Attempt to lock the gate for this processor. spin-
  wait in this loop until gate ownership is obtained
*/
do {
   /* write gate with processor_number + 1 */
    gate[n] = locked_value;
   /* read gate to verify ownership was obtained */
    current_value = gate[n];
} while (current_value != locked_value);
```

Alternatively, if lock failed, perform other tasks until interrupt signals that resource is unlocked.

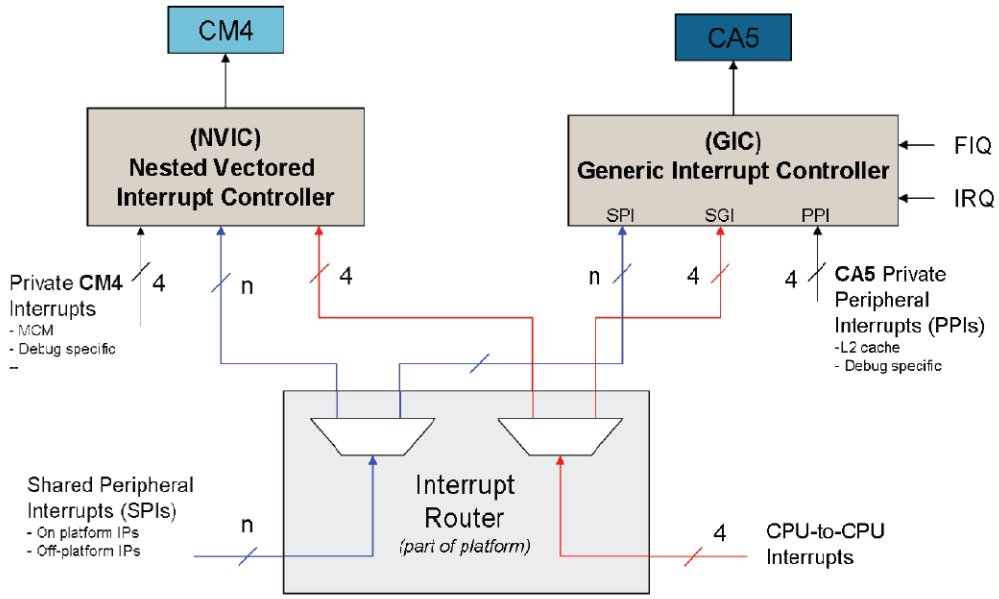
Interrupt Handling

- The two processors use different interrupt controllers
  - A5 core: ARM® Generic Interrupts Controller (GIC)
  - M4 core: ARM® Nested Vectored Interrupt Controller (NVIC)
- Each processor uses its own vector table



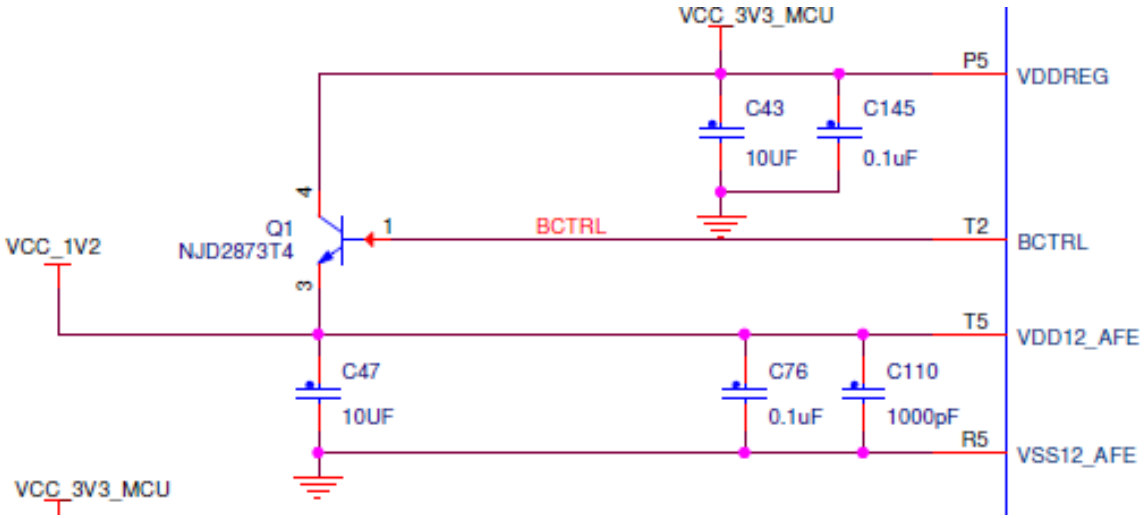
ybrid Controller Solutions
Interrupt Router + Controllers

- Interrupt (IRQ) Router
  - Interrupts can be routed to *neither, either, or both cores* under SW control
  - 8 directed interrupts
    - 4 CPU-to-CPU interrupts
    - Semaphore IRQ, private CPU debug IRQ, CA5 L2, CA5 Performance Monitor
  - 104 shared peripheral IRQs

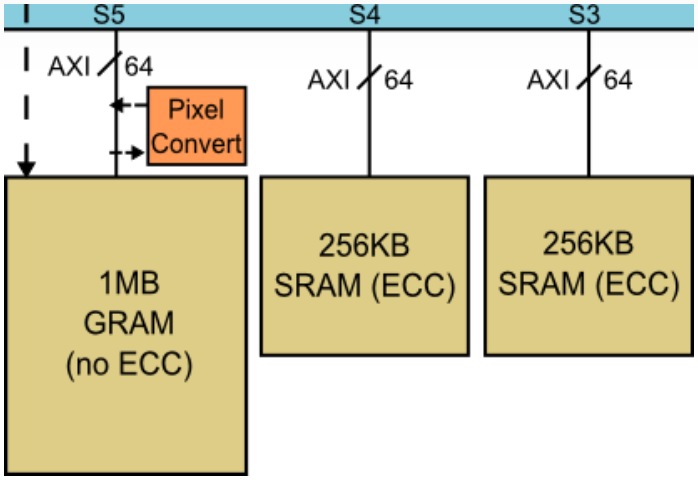


System Power

- Simple power supply – No PMIC required
- Only two levels of power sequencing
  - Controlled by Vybrid via NPN ballast transistor
- Need regulators for:
  - 3.3V for main power
  - 1.5V/.75V for DDR
  - 5V for USB Host



On-Chip Memories



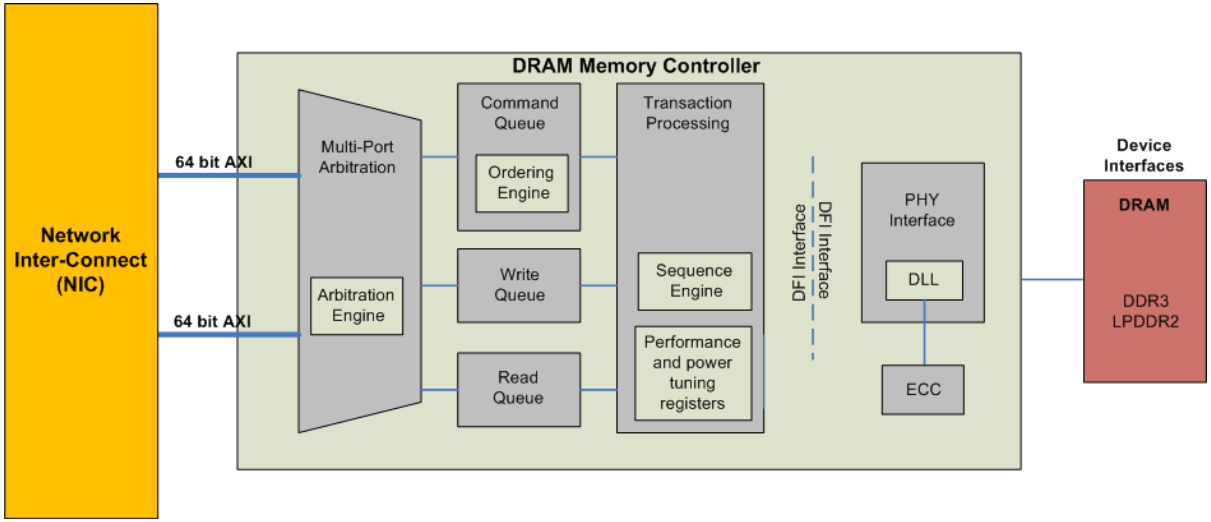
- **On-Chip Memory Implemented:**
  - 512KB SRAM with ECC split into 2 independent blocks of 256kBytes
  - 1Mbyte Graphics RAM (GRAM) no ECC

- **Graphics RAM**
  - 1MB GRAM shown, but can be 512KB or 1MB depending on configuration
  - Pixel converter function to minimize graphics memory footprint

- **Code & Data integrity with Error Correction Codes**
  - ECC has Single-bit correction & Multi-bit detection
  - 64-bits data to 8-bit ECC syndrome

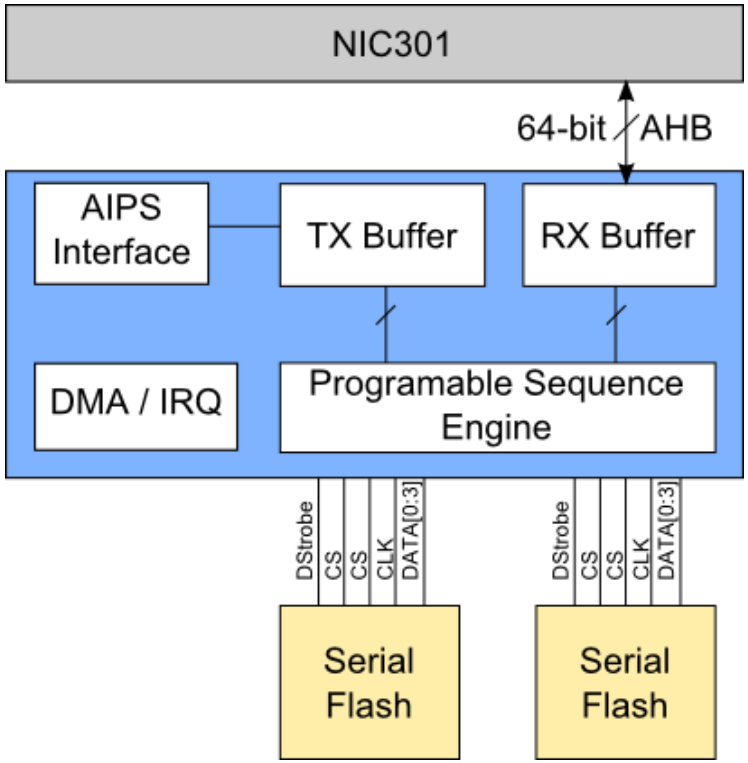
DDR Memory Controller (DDRMC)

- Compliant to JEDEC Specifications.
- Supports 8-bit and 16-bit DRAM memories
- Supports Two port 64-bit AXI application side interface
- Support for Synchronous and Asynchronous mode
- Clock frequencies from 100 MHz to 400 MHz supported
- Supports up to 8GB components
- Supports LPDDR2 and DDR3
  - Support for LPDDR2-S2 , S4
  - Supported LPDDR2 grades: LPDDR2- 800 and lower
  - Supported DDR3 grades : DDR3- 800
- ECC support (only for 8-bit DRAM interface)
- Advanced bank look-ahead features for high memory throughput.
- Full initialization of memory on memory controller reset
- User configurable arbitration schemes between two ports



Vybrid Controller Solutions Quad SPI Features

- **Dual QuadSPI architecture supports:**
  - 2 external Serial Flashes per QuadSPI module
  - Up to 104 MHz SDR and Up to 80 MHz DDR Serial Flash
  - Programmable Sequence Engine for compatibility to any Serial flash
  - XIP (Execute-In-Place)
  - Supports up to 4 chip selects
- QuadSPI can control 2 x 4-bit serial flashes :
  - Individual Flash mode
  - Parallel mode enabling ‘octal flash’ with data recombination internally in QuadSPI
- Up to 80 MHz clock (160 MByte/sec peak bandwidth)
- Flexible Receive (RX) Buffering Scheme:
  - Sub-buffers allocated to specific masters.
  - Master prioritisation
  - Pre-fetch capability
  - Suspend & resume for lower priority masters



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  - Audio and Video
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Vybrid BOOT Interfaces

- Various Boot Interfaces Supported
  - *Quad SPI (QSPI[0:1])**
  - *NOR Flash (FlexBus)**
  - Serial Flash (I2C[0:3]/DSPI[0:3])
  - SD/eSD/MMC/eMMC (ESDHC[0:1])
  - Nand Flash (NFC)
  - FlexCAN[0:1] (using Serial Download Protocol)
- Serial Download Interfaces
  - USB0 (HID Device)
  - UART[0:3]

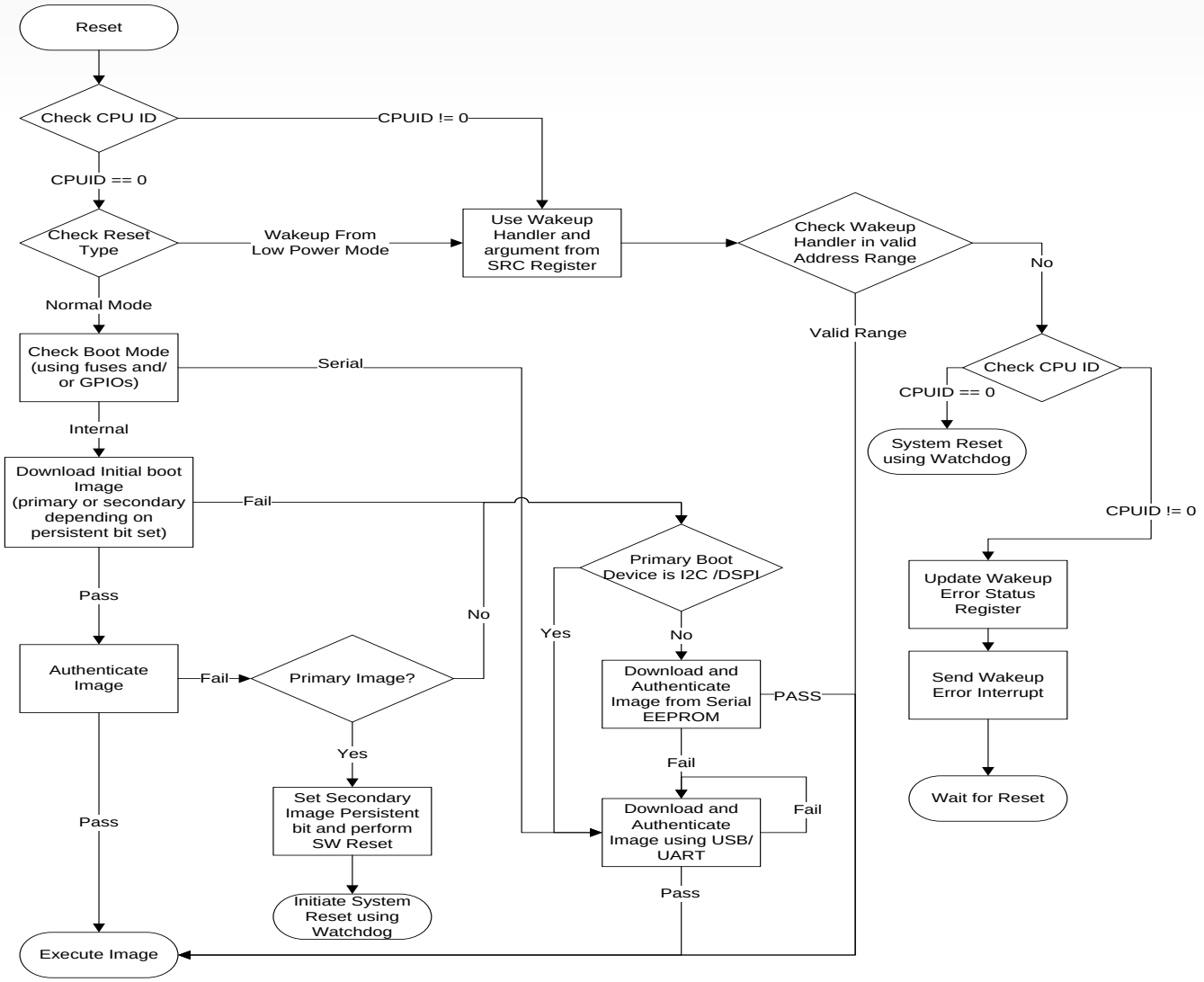
**Option to run from device directly*

Boot Modes

- Boot Interface selected by one of 3 sources
  - Fuse Settings
  - Serial Downloader
  - Reset Configuration (RCON) Boot

	BOOTMOD_1 (PTE0)	BOOTMOD_0 (PTE1)
Boot from Fuses	0	0
Serial Downloader	0	1
RCON Boot	1	0
Reserved	1	1

Vybrid High Assurance Boot - Boot Flow Diagram



Recovery BOOT

- Allows booting from I2C/DSPI flash memory interface (programmable by Fuse) in case BOOTROM is unable to download/execute image from Primary Boot interface.
- EEPROM_RECOVERY Enable Fuse is used.
- Configurations of Recovery Device is read from BOOT_CFG[4].
- Recovery BOOT feature is supported for all interfaces except USB, UART, Serial-ROM (I2C/DSPI)

Redundant Boot

- Supported on NFC and ESDHC interfaces only.
- Allows BOOTROM to download and boot from Redundant image in case primary image fails to boot.
- Also, provides a feature for device firmware upgrade.
  - Firmware upgrade s/w is present as a redundant image in the device.
  - Main Application can set PERSIST_SECONDARY_BOOT bit in Persistent Registers and issue a Watchdog Reset.

BOOTROM Application Download Procedure

- Step by Step Procedure used by BOOTROM
  1. Download first 4 KB from Boot Interface to 0x3F04_0000
  2. Authenticate IVT (Image Vector Table)
  3. Execute DCD (Device Configuration Data)
  4. Copy the initial image to destination memory pointed to by “start” pointer in Boot Data Structure
  5. Download rest of the image from Boot Interface to memory
  6. Execute CSF (Command Sequence File) *“csf” pointer in IVT*
  7. Jump to Application entry point (“entry” pointer in IVT) if success

BootROM Notes

- The secondary (M4) core is not enabled by the BootROM. It must be enabled by user software

- Important to keep in mind that the BootROM may modify default register reset values
  - CA5 Clock at 264 MHz
  - Registers modified depend on boot interface
    - UART0 by default modified

U-Boot Bootloader:
Features currently supported on Vybrid

- Available driver for NOR, Serial Flash (SPI), SD Card.
- Ethernet support – PING, TFTP
- Image format – flat binary, ELF and old uImage
- Can boot MQX, Linux Kernel, Standalone Program, and run Script Files
- Hush Shell scripting (if…then…else…fi, for…do…done, etc)
- Debug monitor – memory display, modify, copy, compare, etc
- File system support – FAT16/32, EXT2, JFFS2
- Cortex A5 core only
- Instruction Cache

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Seven PLLs

- PLL1 – PLLSYS
- PLL2 – 528MHz
- PLL3 – USB1 480MHz
- PLL4 – Audio
- PLL5 – ENET*
- PLL6 – Video
- USB2 PHY PLL – USB2 480MHz

*(Only RMII is supported by the Ethernet module)

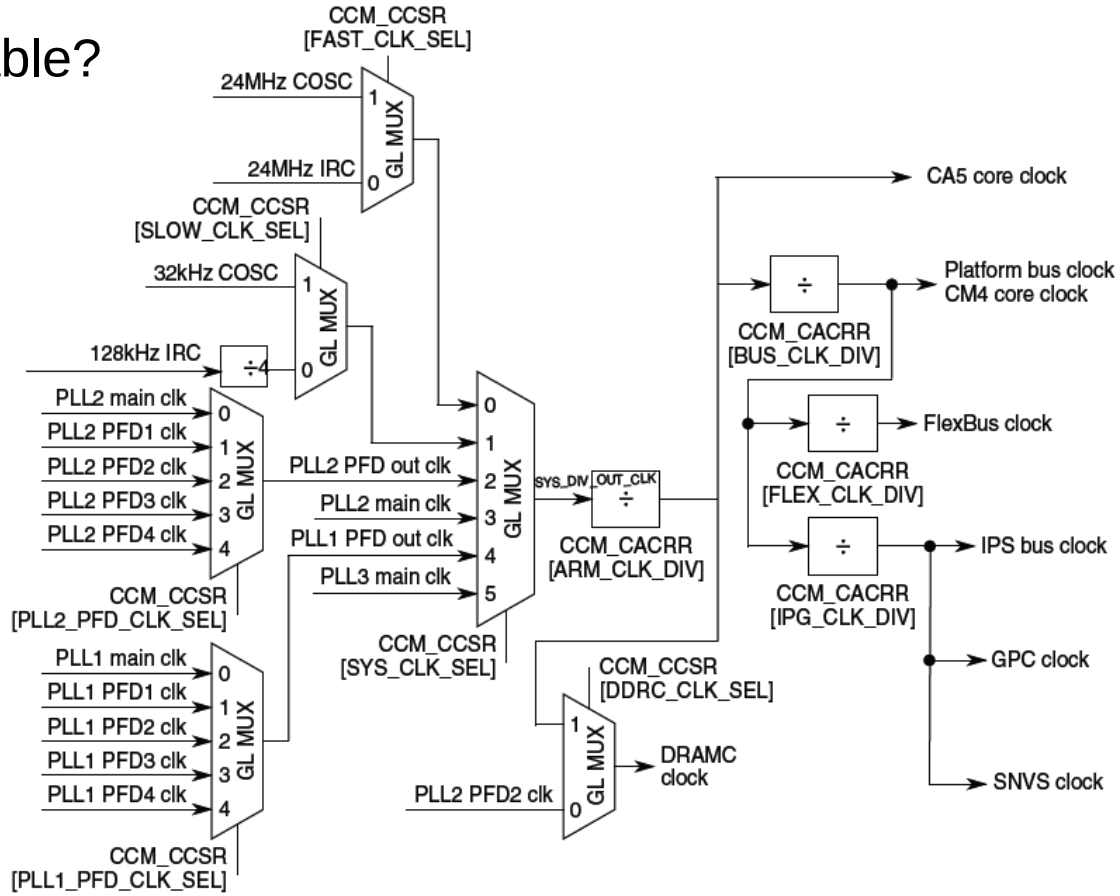
Clock Sources

- Fast
  - 24MHz - Internal Reference Clock (IRC)
  - 24MHz - External Crystal Oscillator
- Slow
  - 128kHz - Internal Reference Clock (IRC)
  - 32kHz - External Crystal Oscillator
- 1KHz - Internal Low Power Osc. (LPO) - used as PORT glitch filter
- External Audio clock
- External Ethernet clock

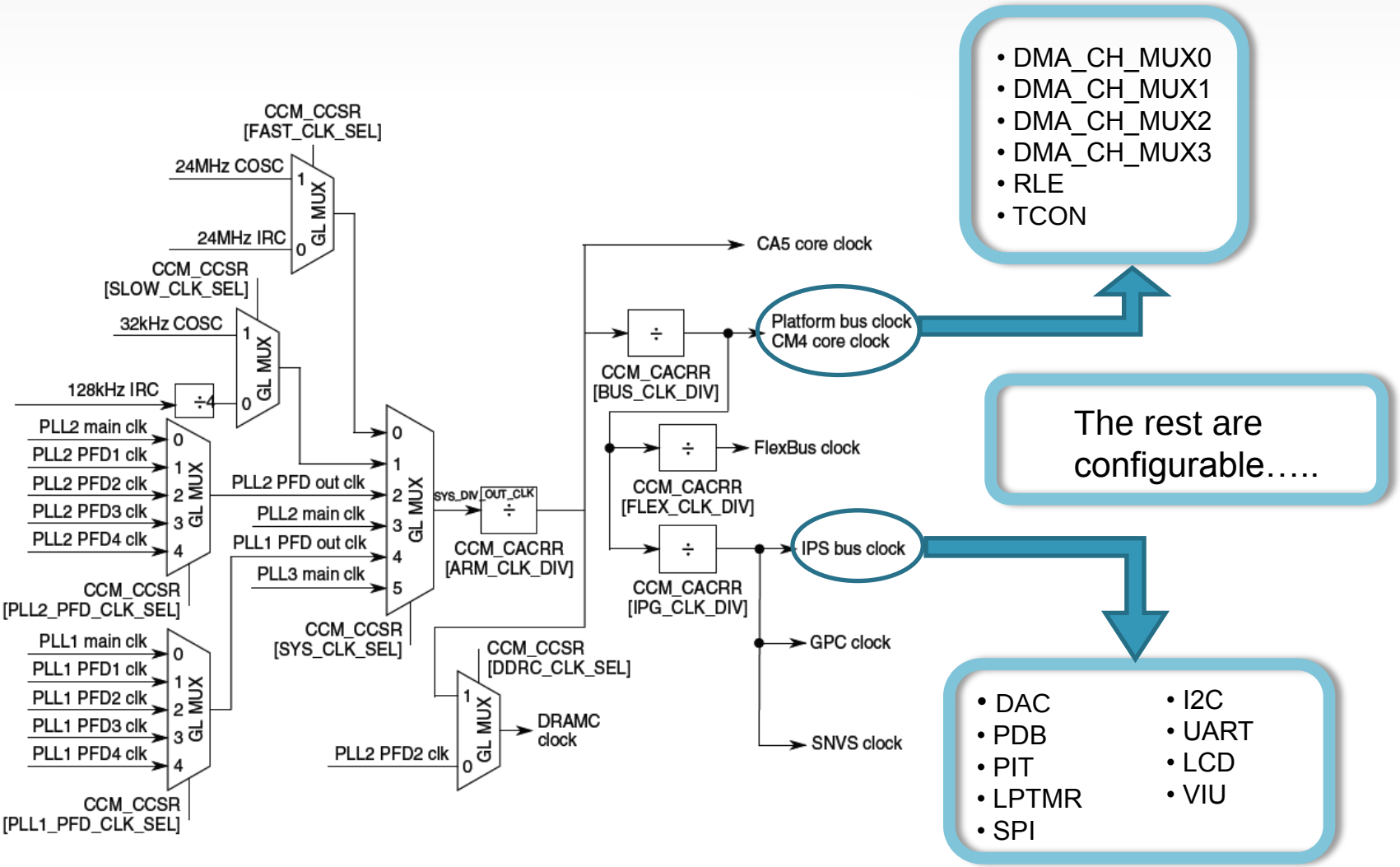
System Clock Tree - Sources

System Clock sources: PLL1-3, 24MHz, 32kHz

- What PLLs are available?
  - PLL1 (480-528 MHz)
  - PLL2 (480-528 MHz)
  - PLL3 (480-528 MHz)
- What PFDs?
  - PLL1 (1-4)
  - PLL2 (1-4)
    - Primary Fractional Dividers



System Clock Tree - Peripherals



- DMA_CH_MUX0
- DMA_CH_MUX1
- DMA_CH_MUX2
- DMA_CH_MUX3
- RLE
- TCON

The rest are configurable…..

- DAC
- PDB
- PIT
- LPTMR
- SPI
- I2C
- UART
- LCD
- VIU

Module Clocking

- Vybrid module clocking:
  - Configurable (set in CCM)
  - IPS Bus Clock
  - Platform Clock

Configurable Clocks *	IPS Clock	Platform Clock
DCU	DAC	M4 Core
QuadSPI	PDB	eDMA
ESAI	PIT	SEMA4
ESDHC	LPTMR	FlexBus
GPU	SPI	
NFC	I2C	
SPDIF	UART	
VADC	LCD	
SAI	VIU	
Ethernet		
SNVS		
FlexCAN		
SWO		
Trace		

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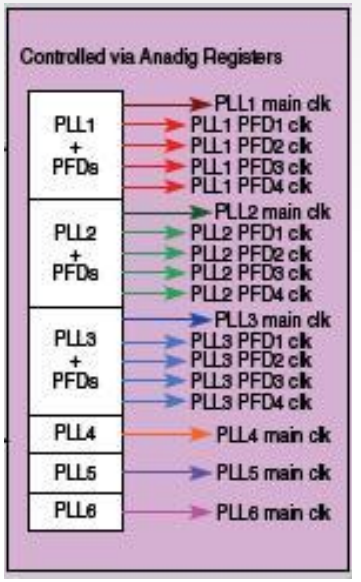
PLL Features

PLL	Alias	Frequency Range	PFD Support?	Spread Spectrum Support?	Dither Support?
PLL1	Sys PLL	480-528MHz	Yes	Yes	Yes
PLL2	528MHz PLL	480-528MHz	Yes	Yes	Yes
PLL3	USB1 PLL	480-528MHz	Yes	No	No
PLL4	Audio PLL	650MHz-1.3GHz	No	Yes	Yes
PLL5	ENET PLL	50 MHz	No	No	Yes
PLL6	Video PLL	650MHz-1.3GHz	No	Yes	Yes

Additional PLL options



PFD – Primary Fractional Dividers interpolate the VCO of the PLL it is connected to and effectively produces a frequency output of Fvco * (18/N) (where N is a user defined value between 12 and 35)

- **Supported by PLL 1-3**

$$\text{PFD Output Frequency} = \text{PLLOutput Frequency} * \left(\frac{18}{\text{frac}}\right)$$

Updates much faster than the PLL (“on the fly”) and can provide significant power savings in Run mode.

Vybrid Power Modes

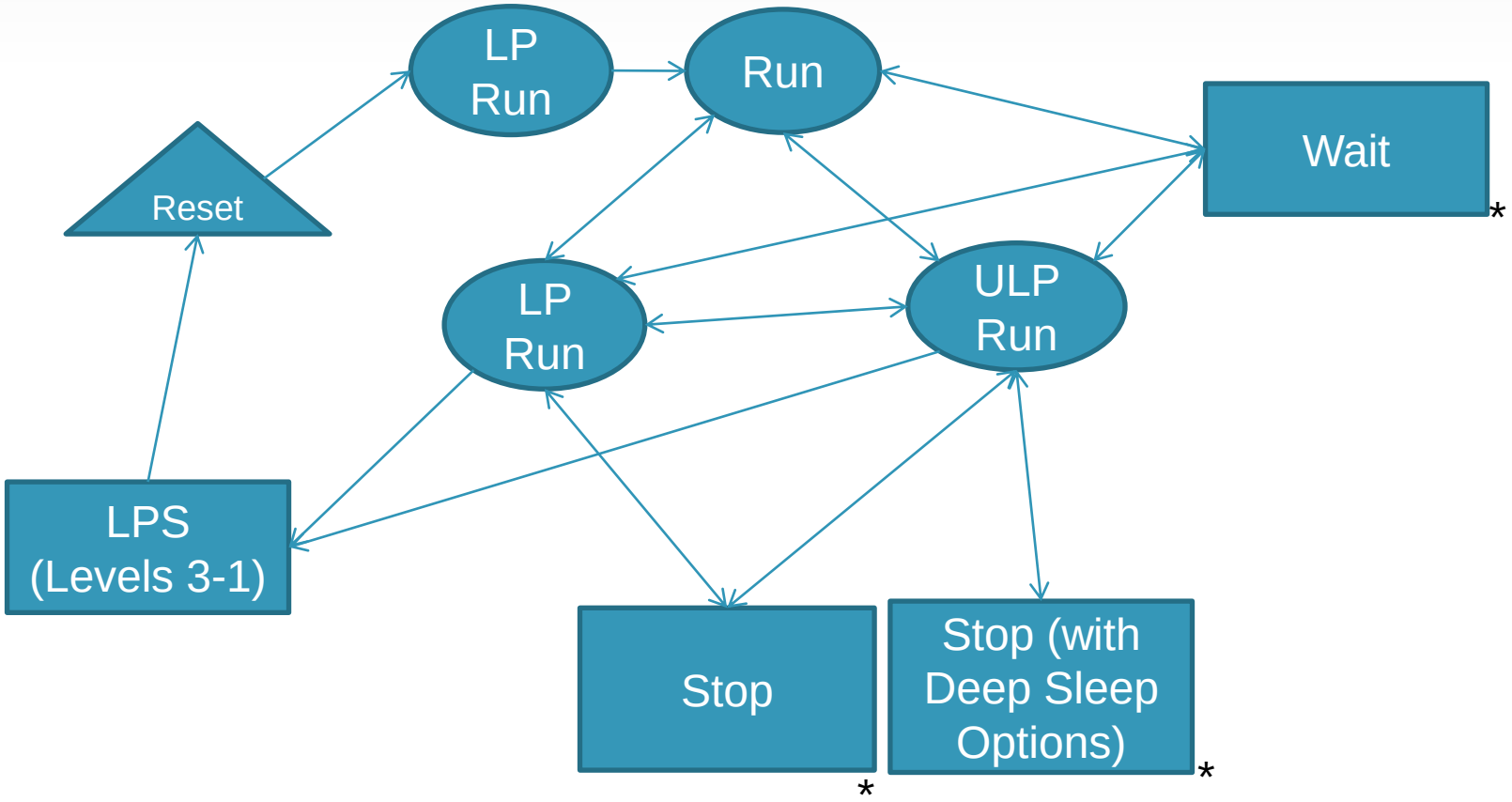
- Run Mode
  - High frequency using PLLs, all peripherals operational
- Low Power Modes
  - Low Power Run (**LPRUN**) Mode – PLLs OFF, Sys clock is 24 MHz
  - Ultra Low Power Run (**ULPRUN**) Mode – PLLs OFF, Sys clock is 32 kHz
  - **WAIT** Mode – Both the CA5 and CM4 cores are halted
  - **STOP** Mode – Cores halted, Peripheral clocks are gated off, Optional Regulator Power down, Deep Sleep option
- Power Gated Modes
  - **LPSTOP[3-1]** - Peripheral clocks are gated off, power domains are de-energized, and some (or all) SysRam is lost

Vybrid Power Modes – Preliminary Power Numbers

Typical Power Modes in an embedded system	Cortex A5/M4 Power Modes	Vybrid Extended Power Modes	Recovery Time	"Typical" Idd Range
Run	Run	RUN	-	Starting @ <320uA/MHz *
► 24 Mhz Operation , PLL bypass, Peripherals OFF		LPRUN	-	20-25mA
► 32Khz/128 Khz Operation, PLL bypass, Peripherals OFF		ULPRUN	-	8-10mA
Wait	Sleep	WAIT		6-8 mA
Stop	DeepSleep	Stop	1.5 – 7 us	4-6 mA
Power Gate modes with Wakeup capability				
► Enables complete shut-down of core logic, including WKUP, further reducing leakage currents in all low power modes ► Supports 16 external input pins and 8 internal modules as wakeup sources ► Wakeup inputs are activated in LPSTOP modes		LPSTOP3	400us	80-100 uA
		LPSTOP2	400us	40-45 uA
		LPSTOP1	400us	35-40 uA
		VBAT	N/A	7-8uA

* *All modules OFF, A5@500Mhz,M4@167Mhz at TYP condition*

Power Management Diagrams**



* - The mode which you exit to will be the mode you entered this low power mode from.
** - This diagram applies to Normal Boot process only

LP Modes: Dynamic Power Saving Modes

Note: Even though some of these features are listed as off in STOP, there may be a way to configure them to continue running.

Lower Power Consumption →

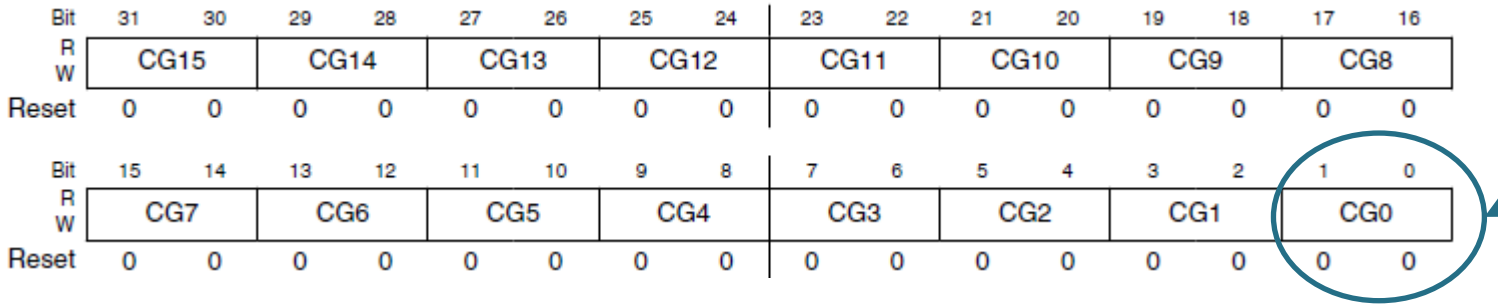
Features	LP Run	ULP Run	STOP
Platform	On	On	On
Peripherals	Option	Option	Off
PLLs	Option	Option	Off
FXOSC	Option	Off	Off
FIRC	Option	Option	Option
SXOSC	Option	Option	Option
SIRC	Option	Option	Option
RAM1	On	On	On
RAM2	On	On	On
IO	On	On	Retained
HP-Reg	On	Option	Option
LP-Reg	On	On	On
ULP-Reg	On	On	On

Peripheral Clock Options in STOP & WAIT mode

- Two bit field determines peripheral clock in WAIT or STOP Mode
  - 0b00 = Clock is off during all modes.
  - 0b01 = Clock is ON in RUN mode, OFF in WAIT and STOP
  - 0b10 = Clock is ON during all modes, including STOP mode
  - 0b11 = Clock is on during all modes, except STOP mode

e.g., CCM_CCGR0: FlexCAN0

CCM_CCGRx Register definition



STOP Mode – Additional Power Savings

Disable unused PLLs

Enable Well Bias Mode – reduce leakage current

Power down Power Regulator (HPREG)

Deep Sleep – periphery power down, maintain memory contents, outputs pulled low

Power Gated Modes in LPS1-3 Modes

Lower Power Consumption →

Features	LPS3	LPS2	LPS1
Platform	Off	Off	Off
Peripherals	Off	Off	Off
PLLs	Off	Off	Off
FXOSC	Off	Off	Off
FIRC	Option	Option	Off
SXOSC	Option	Option	Option
SIRC	Option	Option	Option
RAM1 (16k)	On	On	Off
RAM2 (48k)	On	Off	Off
IO	Lost	Lost	Lost
HP-Reg	Off	Off	Off
LP-Reg	Off	Off	Off
ULP-Reg	On	On	On

Power Gated Modes – Options

Power 64K, 16K, or 0K SRAM

Assert Standby Pin

- **For External Power Mgmt IC**

Setup Modules or Reset for Wakeup

Module Options through WKPU

- **Pins(17 total), LPTIMER, SNVS_LP, ADC0/1, or PIT**

Power Gated Modes – Power Domains

Power Domain	Description	Modules
PD1	Power-gated domain	All power gated modules in LPS modes
PD0	Always-powered domain (Modules in this domain are operating in LPStopn mode)	LPTimer, SRC, VREG_Dig, GPC, WKPU, PMU, FIRC, ADC0, ADC1, LCD
PD0_SW	Switchable PD0 domain (Modules in this domain may or may not operate in LPStopn mode)	RAM1 and RAM2
Vbat	Power domain powered by the backup power supply (coin cell battery)	128 kHz IRC, 32 kHz XOSC, Secure Non-Volatile Storage, Temperature Voltage Monitor
IO	An always-powered domain that only powers the 17 always alive pads which can be used for wakeup events	17 always powered GPIO

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  - Other Key Features: Video, Audio, Memories, Quad SPI
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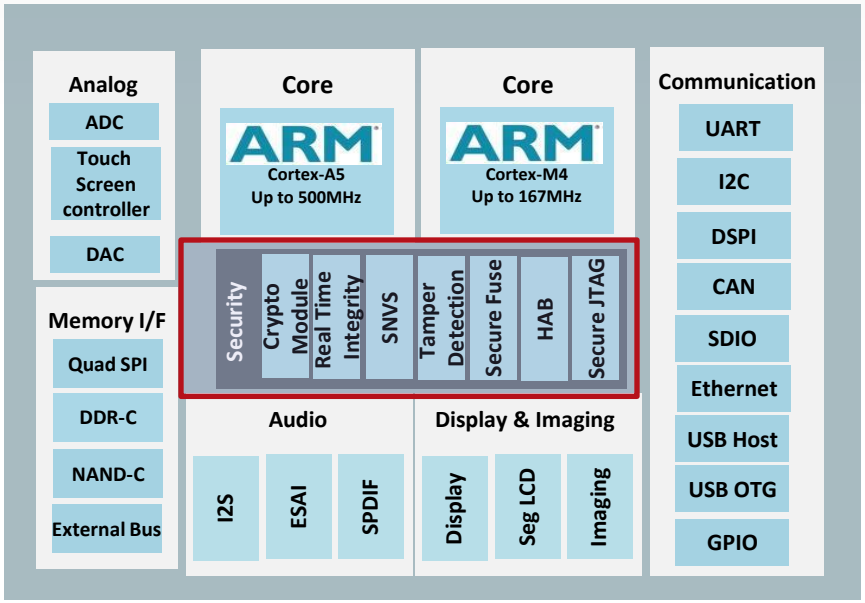
Vybrid Security



- **Hardware security accelerators**
  - Secure boot
  - Cryptographic accelerators
  - Tamper detection
  - Secure financial transactions

- **Hardware-supported security features:**
  - Secure High Assurance Boot
  - AES, DES/3DES, SHA-1, SHA-224, SHA-256
  - Run-time Integrity Checker and Security Controller (incl. Secure RAM and Security Monitor)
  - Random Number Generator (NIST SP 800-90)
  - Secure JTAG Controller (with electrical fuses)
  - Secure real-time clock
  - Universal Unique ID
  - Tamper Detection
  - ARM TrustZone

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Vybrid Security Architecture Overview

TrustZone

- Trusted execution environment for security-critical SW
  - Secure & Normal Worlds (processor modes)
  - Complemented by custom hardware firewalls

High Assurance Boot

- Security library embedded in tamper-proof on-chip ROM
- Authenticated boot: protect against unauthorized SW
  - Verify SW signature during boot
  - RSA-1024/2048 keys anchored to OTP fingerprint (SHA-256)
- Encrypted boot to protect software confidentiality
  - Decrypt SW during boot
  - AES-128/256 keys protected by HW master key (AES-256)
- Run every time Vybrid is reset
- Image Version Control (on-chip OTP-based)

Secure Storage

- Programmable TrustZone protected region within On-chip RAM
- On-chip zeroizable Secure RAM (16 KB)
- Off-chip storage protected by HW master key (AES-256)

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Vybrid Security Architecture Overview(contd..)

HW Cryptographic Accelerators

- Symmetric: AES, DES, 3DES, ARC4
- Hash & HMAC: MD5, SHA-1, SHA-224, SHA-256
- Hardware random number generator (SP800-90)
- Export control support

Secure Real-Time Clock

- Provides reliable time source
- On-chip, separately-powered real-time clock
- Protection from SW tampering

HW Firewalls

- Control access from CPU & DMA peripherals to
  - on-chip peripherals
  - on-chip memory
  - off-chip memory
- Integrated with TrustZone

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Vybrid Security Architecture Overview(contd..)

Secure JTAG

- Configurable protection against unauthorized JTAG manipulation
- Three security levels + complete JTAG disable

Physical Tamper Detection

- Tamper input signal available for:
  - Cover seal
  - Clock, voltage, temperature detectors
  - Active tamper detection
- Hardware and software tamper response

Device Configurations

- Factory: FSL-only (post-Si validation, probe/tester,…)
- Open: non-secure products
- Closed: secure products
- Field Return: test paths re-opened

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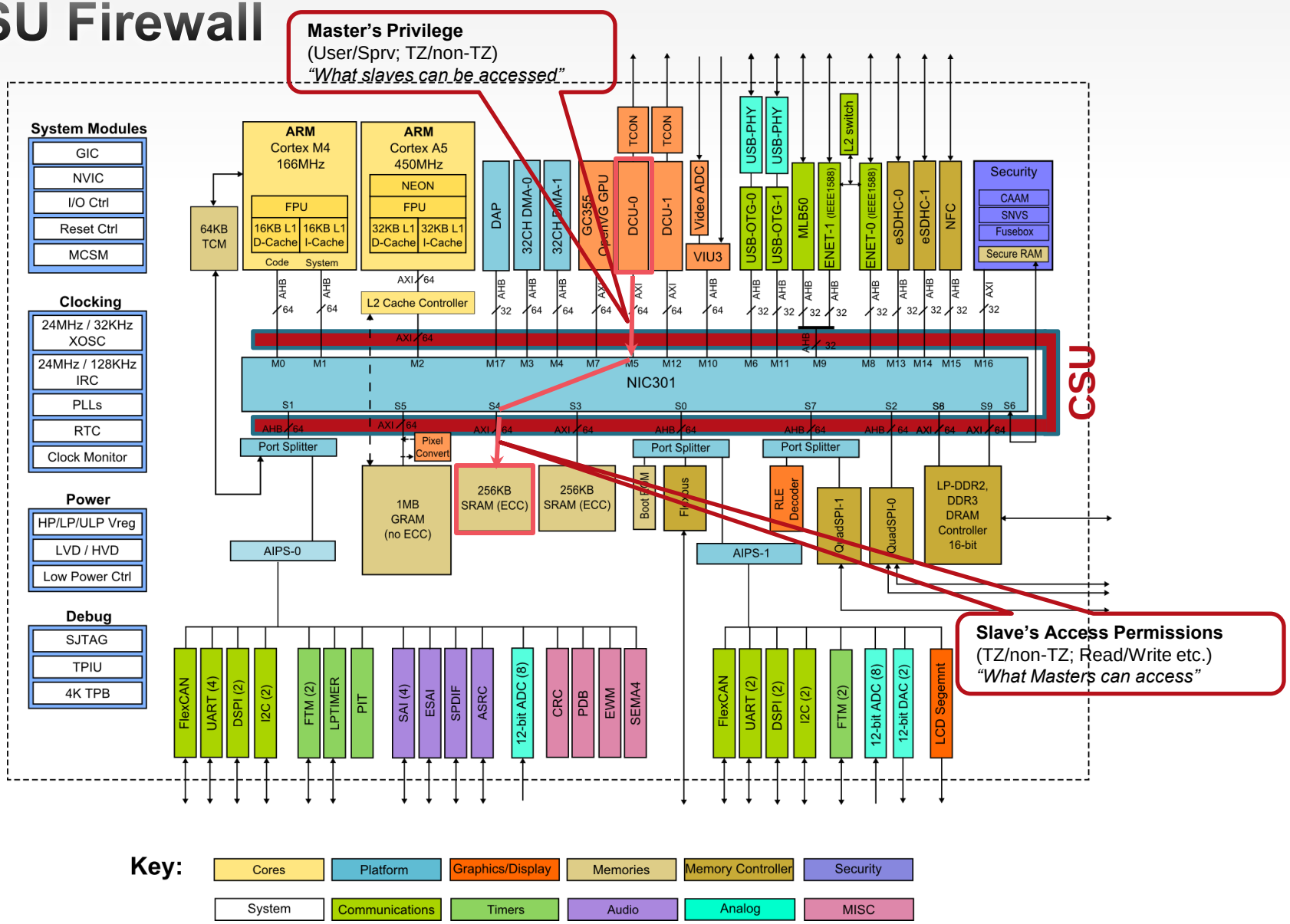
CSU Firewall



Key: Cores | Platform | Graphics/Display | Memories | Memory Controller | Security | System | Communications | Timers | Audio | Analog | MISC

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Vybrid Display Modules

- Two DCU and TCON modules
  - Output to a TFT display
- LCD Segment
  - Output to a segment LCD
- 2D Graphics Processing Unit (GPU2D)
  - Hardware acceleration of OpenVG vector graphics
- Run Length Encoding (RLE) Decoder
  - Stand-alone decoder block for decompression of images
- Pixel Converter
  - Converts 16-bit pixel data into 32-bit ARGB888 format for processing by the Cortex A5's SIMD

Display Control Unit (DCUv4): Features

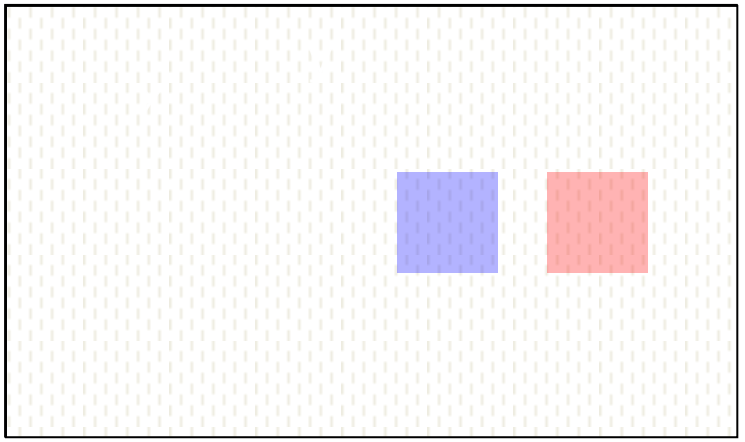
- DCU is an advanced graphics control module that directly drives an external TFT LCD
- Full RGB888 output to TFT LCD panel
- 64 graphics layers, a default background color layer and a cursor layer with integrated blinking option (66 layers total)
- Blending of each pixel using up to 6 source layers dependent on size of panel
- Programmable panel size up to SVGA (800 x 600)
- Supports multiple graphic formats in RGB and YUV format, with and without alpha and run length encoding
  - 16bpp RGB565, RGB1555, RGB4444, 24bpp RGB888 and 32bpp ARGB8888
  - Indexed colors with variable bit depths from 1 bit per pixel (bpp) to 8bpp and APAL8
  - YUV format - YCbCr422
- Gamma correction with 8-bit resolution on each color component
- Safety mode for tagging pixels on highest priority layers
- Dedicated memory blocks to store a cursor and Color Look Up Tables (CLUTs)
- Temporal Dithering

DCU Operation

- The DCU combines layers or “sprites” to create the final content
  - There are up to 66 different sources of content possible
    - 64 programmable layers that contain source graphics
    - A cursor layer
    - 1 layer as a default color for the background
  - Layers are in a fixed priority to each other
  - For each pixel position
    - the DCU fetches a pixel from the topmost layer placed there AND
    - a pixel from the next layer in the priority
    - and pixels from up to four further layers (dependent on user configuration)
  - If indexed colors are used these are converted to 32bpp before processing
  - The fetched pixels are then blended to give the display content for that position.
    - The blending attributes are determined per layer and the lowest priority pixel’s blending attributes are ignored
  - Each resulting pixel can be gamma corrected
  - The output format is 8 bits per channel(24bpp)

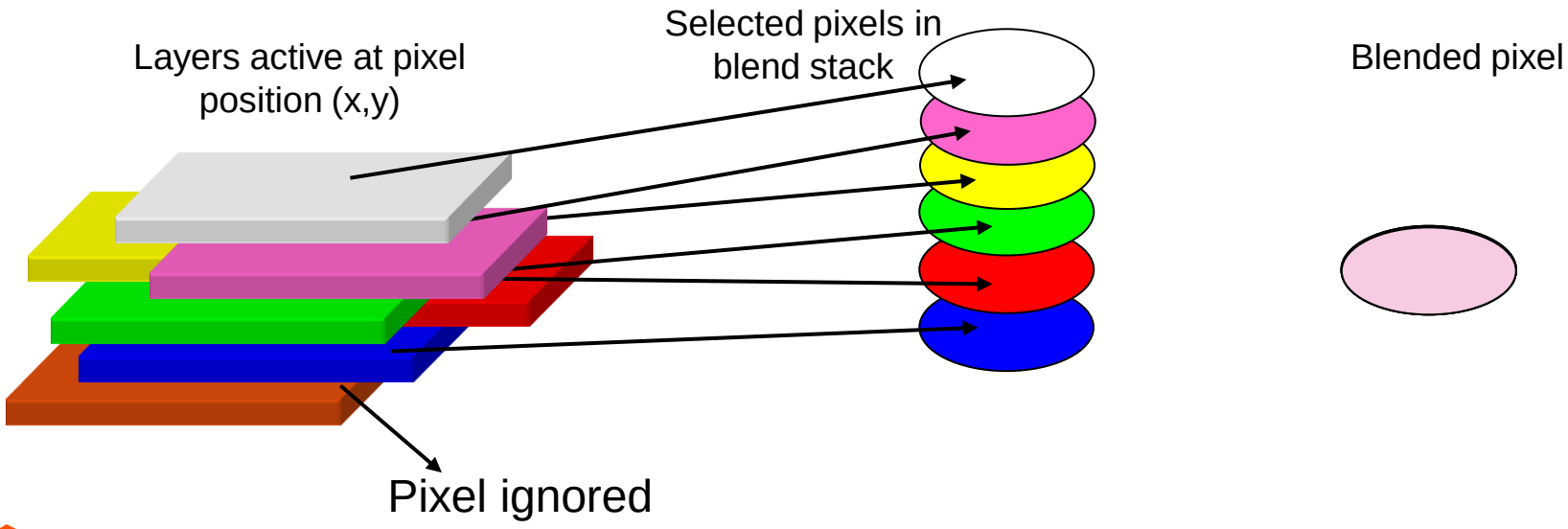
DCU: What is a layer?

- A layer is the mechanism by which graphics are displayed on the panel
- The DCU has a set of 9 registers to configure each layer
- The layer registers configure
  - Height & width of layer (pixels)
  - Signed position on panel (x,y)
  - Pointer to graphic (32-bit)
  - Graphic coding (bpp) & CLUT, blending, type, tile & safety
  - Chroma limits (max & min)
  - Tile size
  - Transparency colors



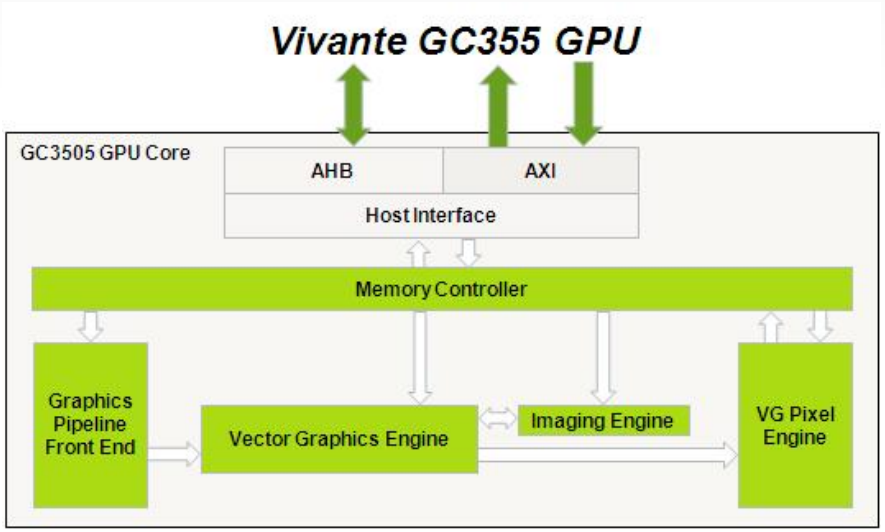
DCU: Layers & the pixel-blend stack

- At each pixel position up to six layers may be blended
  - User can globally configure the DCU to blend 2, 3, 4, 5 or 6 layers
- The blend stack determines how each pixel is blended
  - Layers below the lowest priority pixel are not visible
  - The blending settings for the lowest priority pixel are ignored



2D Graphics Processing Unit (GPU2D) Features

- Supports OpenVG 1.1
- Full fixed function hardware vector graphics GPU
- Hardware Tessellation
  - Minimum CPU involvement
- 16X FSAA
  - Photorealistic quality
  - No performance degradation
- Multi-format rendering
  - sRGB color transformation
  - Video image conversion
- High-quality vector font rendering support
- Dedicated GPU for QoS requirements



OpenVG

freescale™

Run Length Encoding (RLE) Decoder

- Standalone Decoder block for Memory-Memory decompression of RLE encoded data
- Lossless Compression
- Pixel formats supported: 8bpp, 16bpp, 24bpp, 32bpp
- Requires the CPU or DMA to push in the encoded data and then extract the decoded result
- 8x8 RxFIFO and 8x8 TxFIFO both with DMA support
- Programmable fill levels or read and write buffers
- Partial Image (Window) decode feature
- Supports compression of horizontal gradients

Video In/Picture Out on Vybrid

Analog In:
CVBS

The “Video Subsystem”

Analog Front End (AFE)

Video Decoder (VDEC)

Digital out:
YUV888

Mux

VIU

Graphics Memory

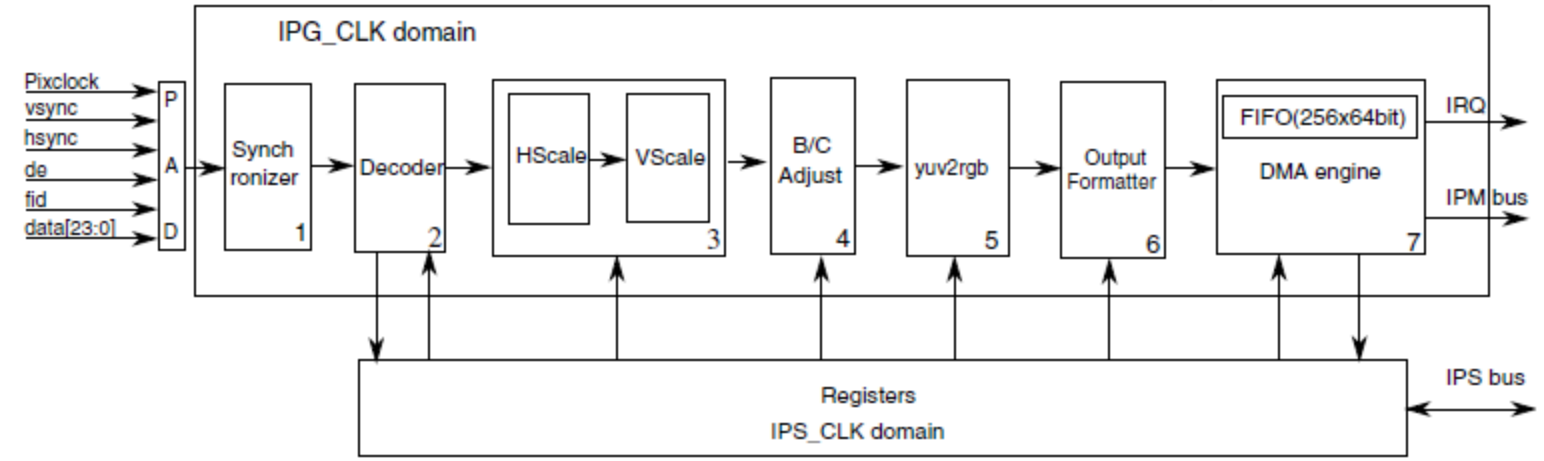
DCU

TFT LCD

Digital Path

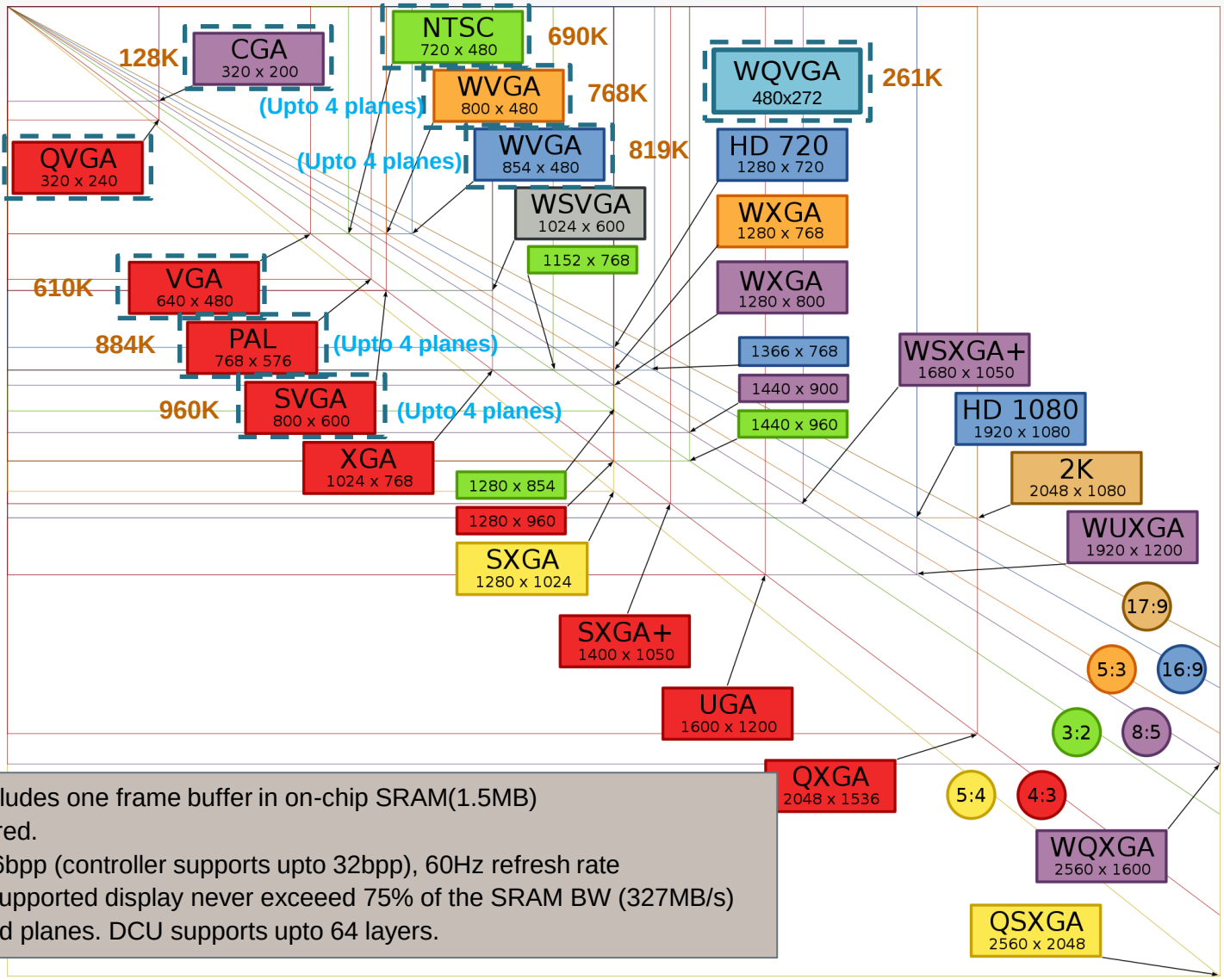
YUV888,RGBnnn,
or ITU656

Video Interface Unit (VIU3)



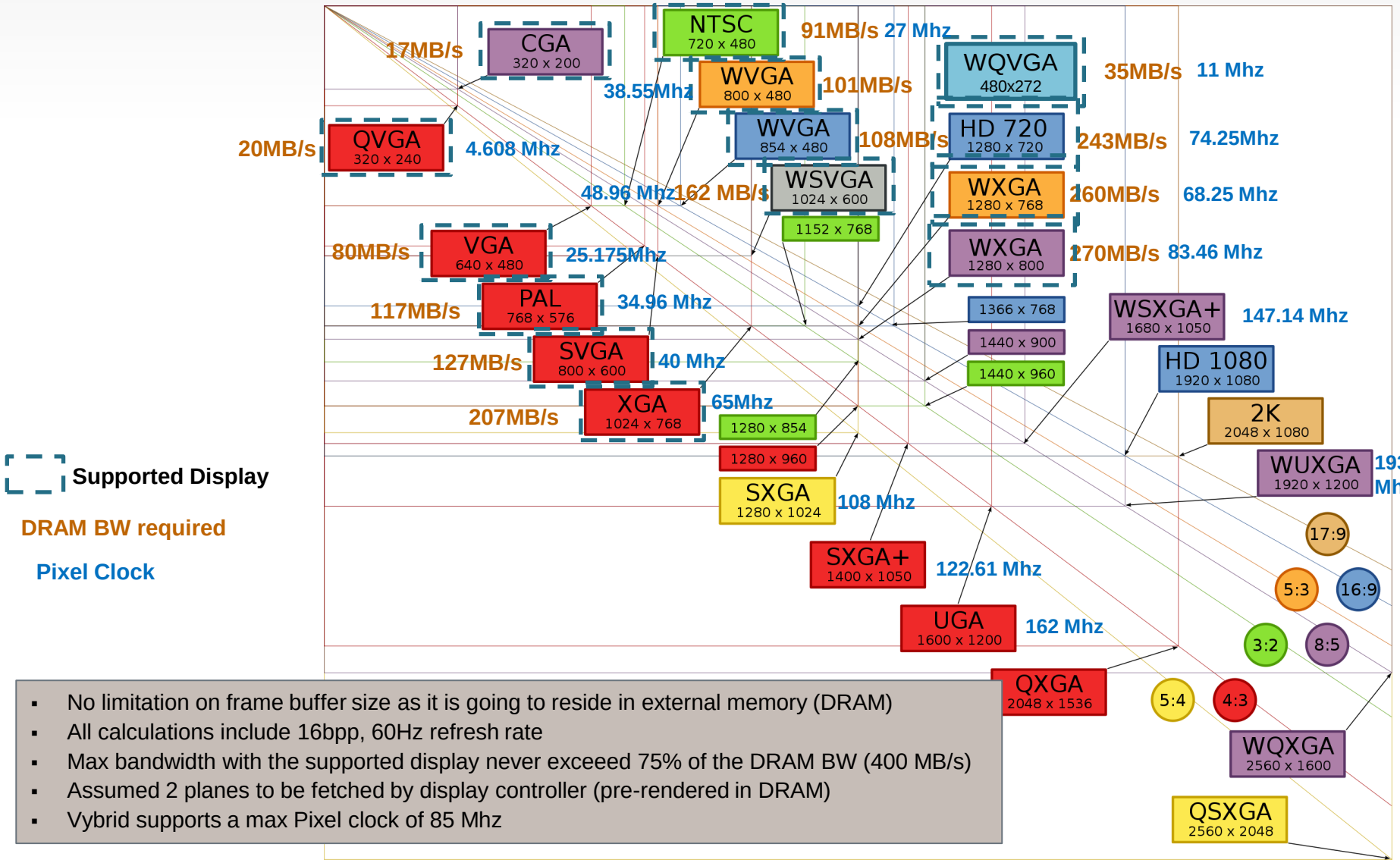
- Can be used stand-alone or in conjunction with the video AFE and decoder
- Formats supported:
  - 8-bit ITU656 video input
  - RGB888/RGB666/RGB565 parallel input
  - RGB888 input with one color component transferred per clock
- Brightness and Contrast Adjustment
- Down-scaling & Horizontal Up-scaling HW support
- Horizontal Mirroring for reverse camera adjustment
- Internal DMA engine for transferring data from FIFO to system memory

ay Resolution Supported (Vybrid:176 LQFP) with 16bpp



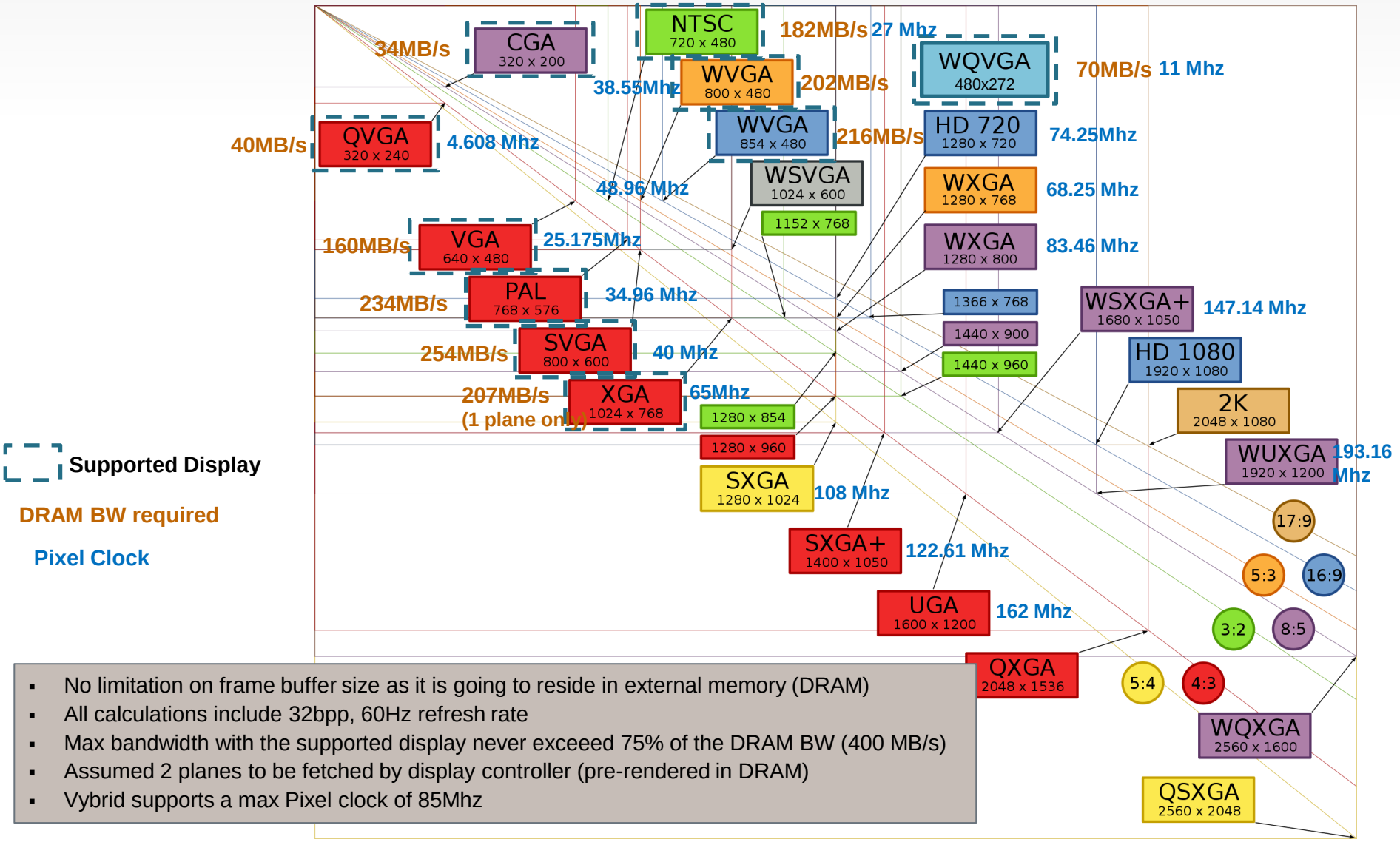
- Memory requirements includes one frame buffer in on-chip SRAM(1.5MB)
- NO external DRAM required.
- All calculations include 16bpp (controller supports upto 32bpp), 60Hz refresh rate
- Max bandwidth with the supported display never exceeed 75% of the SRAM BW (327MB/s)
- Support for upto 6 blended planes. DCU supports upto 64 layers.

ay Resolution Supported (Vybrid:364 BGA) with 16bpp



- No limitation on frame buffer size as it is going to reside in external memory (DRAM)
- All calculations include 16bpp, 60Hz refresh rate
- Max bandwidth with the supported display never exceeed 75% of the DRAM BW (400 MB/s)
- Assumed 2 planes to be fetched by display controller (pre-rendered in DRAM)
- Vybrid supports a max Pixel clock of 85 Mhz

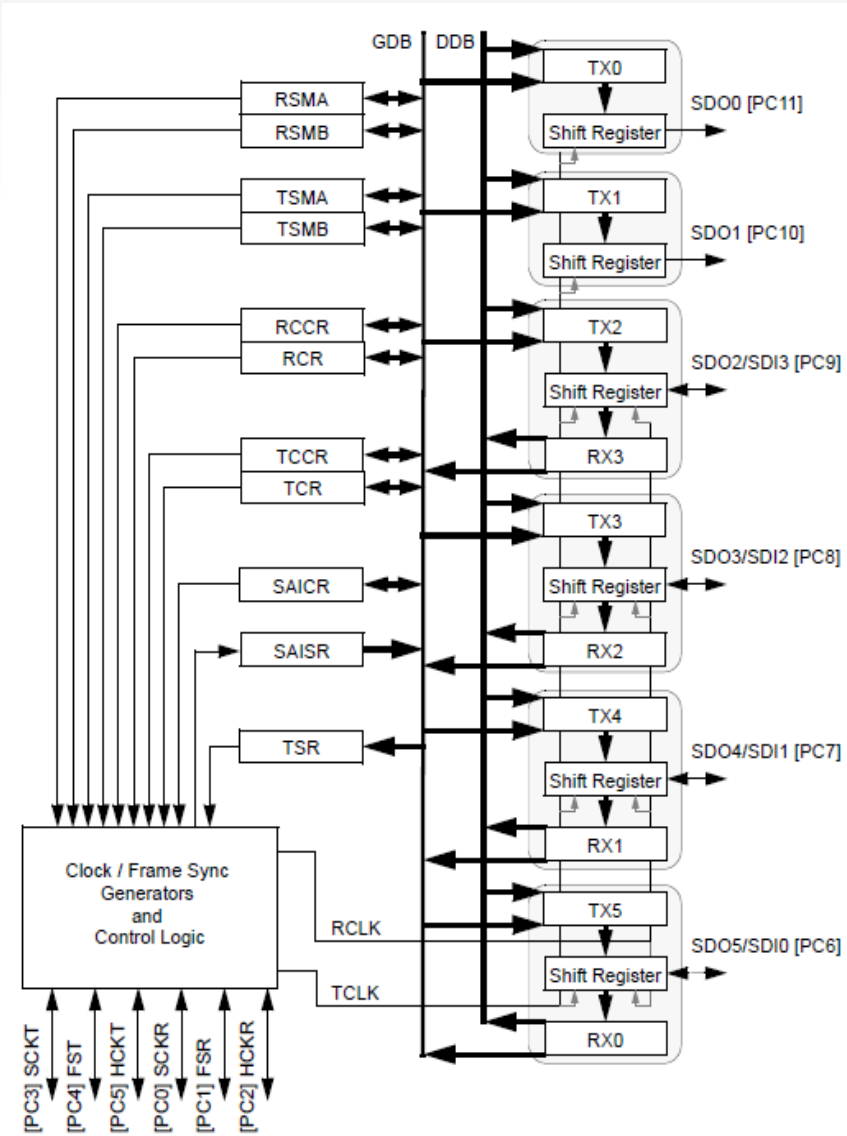
ay Resolution Supported (Vybrid:364 BGA) with 32bpp



- No limitation on frame buffer size as it is going to reside in external memory (DRAM)
- All calculations include 32bpp, 60Hz refresh rate
- Max bandwidth with the supported display never exceeed 75% of the DRAM BW (400 MB/s)
- Assumed 2 planes to be fetched by display controller (pre-rendered in DRAM)
- Vybrid supports a max Pixel clock of 85Mhz

Enhanced Serial Audio Interface (ESAI) Features

- Independent (asynchronous mode) or shared (synchronous mode) transmit and receive sections with separate or shared internal/external clocks and frame syncs, operating in Master or Slave mode.
- Two ports can operate as transmitter only, four others could be either transmitter or receiver.
- Saves pins when interfacing multiple outputs to external Audio Peripherals. Several data pins share the same bit/word clock
- Programmable data interface modes such like I2S, LSB aligned, MSB aligned
- TDM support from 2 to 32 channels per data line
- Programmable word length (8, 12, 16, 20 or 24bits)
- Flexible selection between system clock or external oscillator as input clock source, programmable internal clock divider and frame sync generation
- AC97 support
- Time Slot Mask Registers for reduced CPU overhead (for Transmit and Receive both)
- 128-word Transmit FIFO shared by six transmitters
- 128-word Receive FIFO shared by four receivers
- Wide selection of data alignment combinations when moving the 24-bit ESAI data to/from the 32-bit shared peripheral bus.



Sony/Philips Digital Interface (SPDIF) Features

- Stereo transceiver for transmission or reception of digital audio using IEC60958 standard
- Receiver
  - Input sample rate measurement
    - Used to drive internal and external components such as ESAI ports.
  - Supports the following sampling rates: 32kHz, 44.1kHz, 48kHz, 64kHz, 88.2kHz, and 96kHz
  - CD Text Support
  - CS (Channel Status) and U (User Data) bit Recovery
- Transmitter
  - One SPDIF output, IEC 60958 consumer format
  - CS bit Support
- SPDIF Receiver to SPDIF Transmitter Bypass Mode
- Low power mode - SPDIF can be disabled to save power when not in use

Asynchronous Sample Rate Converter (ASRC)

- The Asynchronous Sample Rate Converter (ASRC) converts the sampling rate of a signal associated to an input clock into a signal associated to a different output clock.
- Supports up to 10 channels split into up to 3 sampling rate conversion sets.
- Individual association of each channel to one of the sampling rate pairs.
- Designed for rate conversion between 32kHz, 44.1kHz, 48kHz and 96kHz. The useful audio signal bandwidth is below 24kHz.
- Other sampling rates in the range of 8kHz to 200kHz are also supported, but with reduced audio performance.
- Automatic accommodation to slow variations in the incoming and outgoing sampling rates.
- Linear phase.
- THD+N: -120dB
- Tolerant to sample clock jitter.
- ASRC has a disable to save power when not in use.

Introduction to Vybrid - Agenda

- Product Overview & Key Differentiators
- Software and Tools
- Architectural Details
  - General : Multi-core Communication, Semaphores, Shared Memory, Interrupts, System Power, Memory Details
  - Booting
  - Clocking and Low Power
  - Security
  - Audio and Video
- Demonstrations
- Q&A

Q&A

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