November, 2010

Networking Power Architecture Solutions

Jacques Landry

Company Overview

- **Semiconductor design and manufacturing company established in 1953**
- Focused on automotive, consumer, industrial, mobile communications, networking and enabling technologies
- Engaged with **10,000+ customers** globally; more than **100 of the top electronic manufacturers**
- **$5.7 billion** in revenue in 2007
- Headquartered in **Austin, Texas**
- **20,000+** employees in more than **20** countries

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Vision:

Global leadership in *embedded processing* and *connectivity solutions*

Leadership in chosen markets/sub-segments

- Target markets: Automotive, Consumer, Industrial, Networking, Wireless
- Target position: #1, #2 or #3 in all chosen segments

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You touch us every day.

Consumer | Industrial | Automotive | Cellular | Networking

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Focus Freescale Market Segments

IP Services


Enterprise Router


Enterprise Switch


Wireless LAN Router


IP Access Router & VPN Gateway

Access


Multi-Service Provisioning Platform

DSLAM

Multi-Service Switch Router


Carrier Core Router

NodeB (Base Transceiver Station)


Radio Network Controller

Media


IP PBX


Printer


Enterprise Media Gateway


Media Gateway

Storage


Enterprise Storage


RAID


Network Attached Storage

Industrial


Web Server


Military Aeronautics


Civil Aeronautics


Industrial Electronics


Pachinko Arcade Game


Kiosk

SOHO and Consumer

IP Set-Top Box

Media Server/Gateway


Wireless LAN Router with Broadband Modem


Integrated Access Device

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Investing in Research and Development

- More than $1.1 billion investment in research in each of the last three years
  - Materials
  - Process technologies
  - Silicon manufacturing
  - IP and product development
- More than 5,900 patent families

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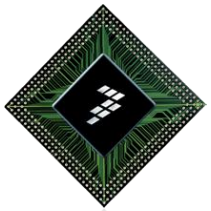
Freescale Introduces Product Longevity Program



- ►The embedded market needs long-term product support
- ►Freescale has a longstanding track record of providing long-term production support for our products
- ►Freescale is pleased to introduce a formal product longevity program for the market segments we serve
  - For the automotive and medical segments, Freescale will make a broad range of program devices available for a minimum of 15 years
  - For all other market segments in which Freescale participates, Freescale will make a broad range of devices available for a minimum of 10 years
  - Life cycles begin at the time of launch
- ►A list of participating Freescale products is available at: www.freescale.com/productlongevity

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20 Years of Communications Processing Evolution

AIM Alliance
Started 1991
First silicon 1992

PowerPC® 603e

PowerPC® 75X

Dual-core processor
MPC8641D with e600 Power cores

Dual-core with integrated content processing
MPC8572E with e500 Power core

MC68302
68K core

First PowerQUICC® communications processors
Includes Communications Processor Module (CPM)

PowerQUICC III
e500 Power core

QorIQ™
Communications Platforms

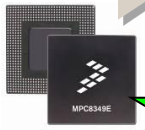
▶1989	▪ ▪ ▪	▶1994	▶1995	▶1996	▶1997	▶1998	▪ ▪ ▪	▶2002	▶2003	▶2004	▶2005	▶2006	▶2007	▶2008

QUICC® MC68360
68K core

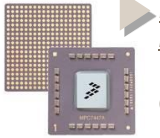
PowerQUICC II
603e Power core

Security integration with PowerQUICC line

PowerQUICC II Pro
e300 Power core



GPON processor
Integrated DSP + Power core



Power Architecture™ Host Processors
MPC7xxx
e600 core

QUICC Engine™
Next-gen CPM / dual RISC engines

In Production

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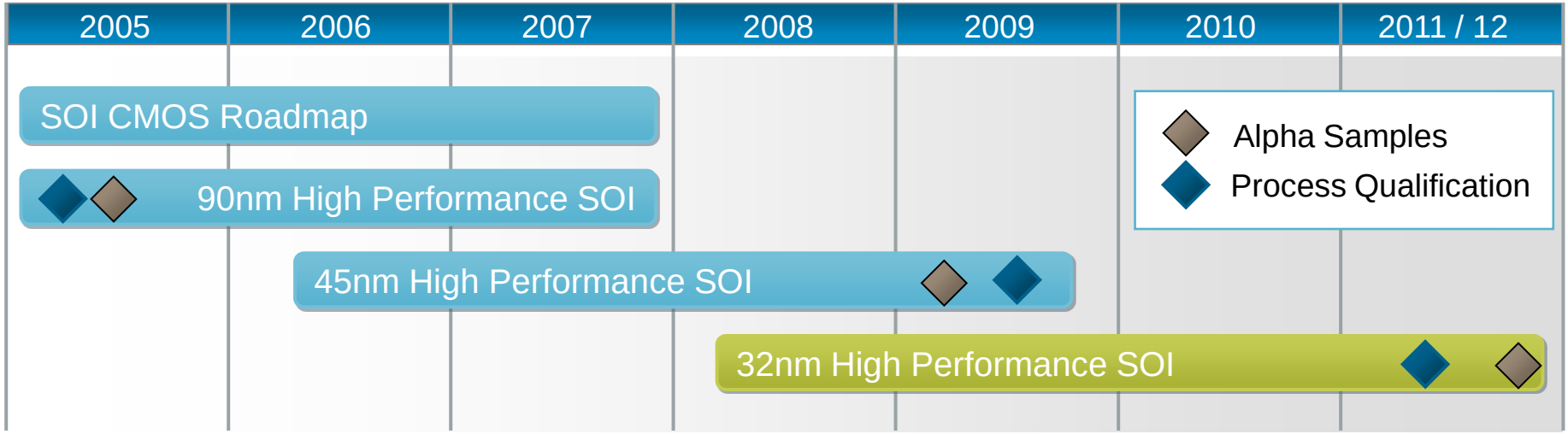
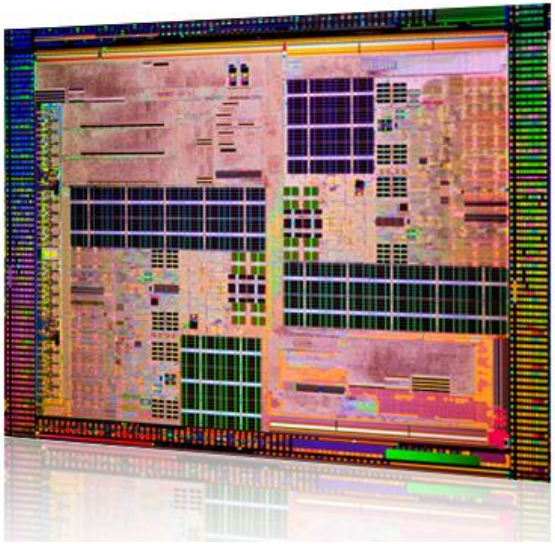
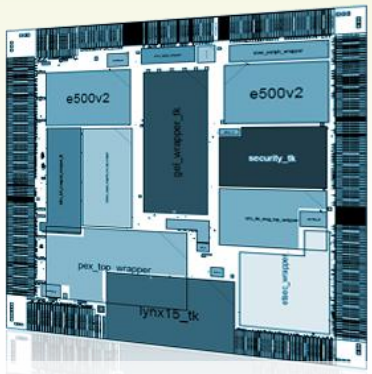
SOI CMOS Technology Roadmap



90nm Dual Core Processor

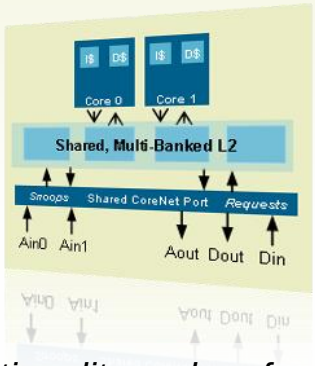


45nm Dual Core



Same functionality and performance delivered today in C90SOI is 50% lower power in 45SOI

32nm Dual Core



Same functionality and performance in 45SOI is 50% lower power in 32SOI

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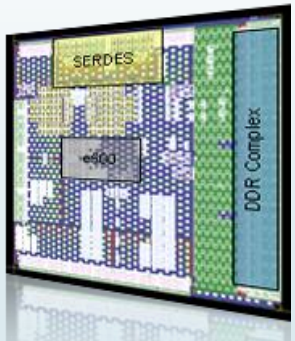
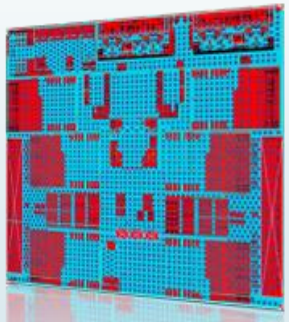
1st Wave - C45SOI Products

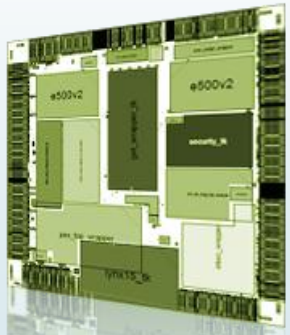
8569
Flip Chip PBGA
130M transistors
>1B vias and contacts



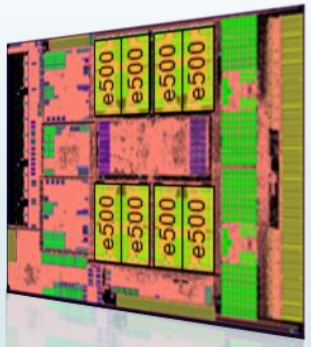
Multicore DSP 8156
Flip Chip PBGA
0.5B transistors
2.5B vias and contacts



P2020
Wire Bond TEPBGA-II
~100M transistors
>1B vias and contacts



P4080
Flip Chip PBGA
>0.6B transistors
3.4B vias and contacts



P1011 / P1020
P1012 / P1021
P1013 / P1022

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In-house Gateway Software Applications Stack

Freescale completes acquisition of Intoto to expand embedded multicore development support

AUSTIN, Texas Oct. 8, 2008 – Freescale Semiconductor has completed its purchase of privately held Intoto, Inc., a leading provider of software platform products for networking and communications equipment manufacturers. The transaction represents another milestone in Freescale's strategy to deliver comprehensive solutions for its QorIQ™ communications platforms.

freescale™ VortiQa

\vór · ti · ka\: A whirlwind of innovation

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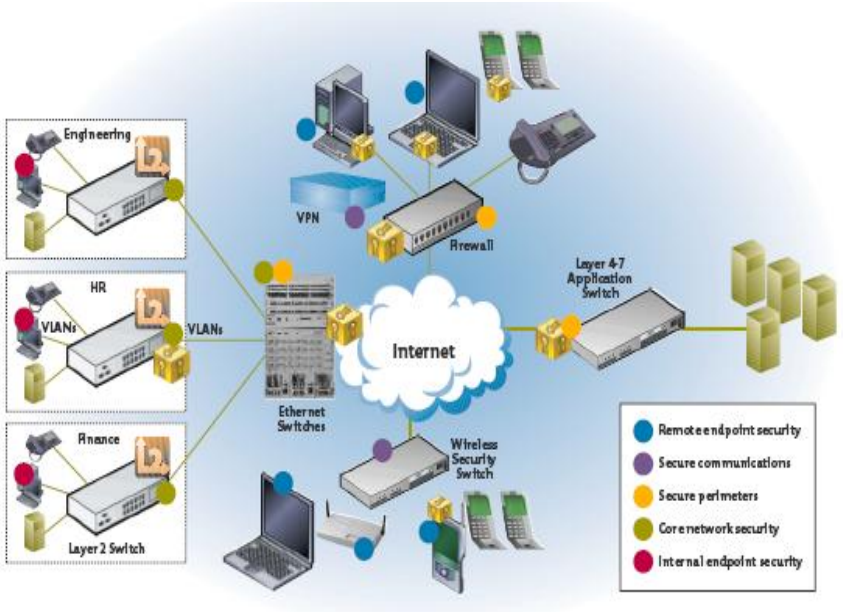
What is VortiQa Software?

- **VortiQa software**
  a new brand of Freescale software announced on June 15, 2009

  for networking equipment that helps accelerate product development and increase the pace of innovation



- Four new VortiQa product lines of **production-rea** software applications:
  - VortiQa software for service provider equipment
  - VortiQa software for enterprise network equipment
  - VortiQa software for small business gateways
  - VortiQa software for SOHO/Residential gateways

- A comprehensive **solution-centric approach** for networking applications in targeted vertical segments:
  - **Optimized for Silicon** – QorIQ™ and PowerQUICC® communications processors
  - **Software** – VortiQa software products
  - **Expanded Ecosystem** - hardware, OS, ISVs, system integrators

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VortiQa Software Products Overview

Delivers integrated networking and security functionality

freescale VortiQa

	Freescale Silicon Examples	Example Applications	Key Features
Software for Service Provider Equipment	QorIQ™ processors (P4080)	Multi-service edge routers, Switches, Wireless infrastructure, security gateway	Networking protocols L2 or L3 Stateful Packet Inspection Firewall, NAT IPSec VPN + IKEv1 + IKEv2 Stateful deep packet inspection: • P2P filtering • Protocol Anomaly • Traffic Anomaly QoS / Traffic Management Virtual Security Gateways (VSG)
Software for Enterprise Equipment	PQ2Pro, PQIII® and QorIQ™ processors (8377E, 8572E, P2020, P4080)	Enterprise UTM, security appliances, secured routers and switches	Networking protocols L2 or L3 SPI Firewall support IPSec Enterprise VPN + IKEv + IKEv2 Stateful deep packet inspection: • P2P filtering • Protocol Anomaly • Traffic Anomaly QoS / Traffic Management Anti-Virus and Anti-Spam HA Support
Software for Small Business Gateways	PQ2Pro and QorIQ™ processors (8377E, P2020)	Multi-service business gateways	Networking protocols Advanced IPSec VPN + IKE supports SPI Firewall + Advanced NAT features + Dual WAN with "Load balancing / Fail Over" Optional service provider provisioning
Software for SOHO / Residential Gateways	PQ2Pro and QorIQ™ processors (8315E, 8314E, P1020)	xDSL, PON, FTTH, and other CPE devices	Networking protocols SPI Firewall + NAT + Residential Gateway IPSec VPN Optional service provider provisioning

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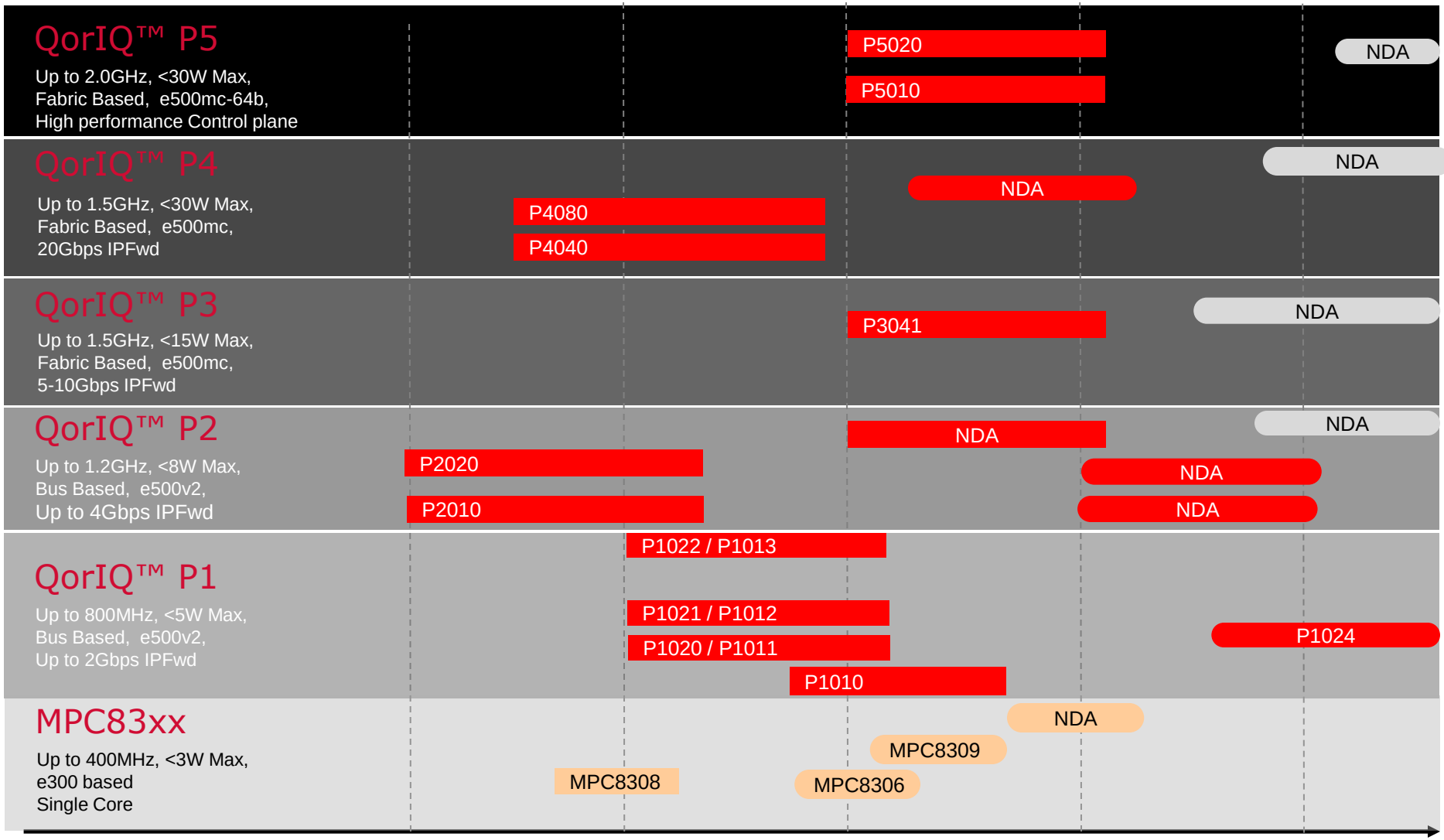
Power Architecture Processor Roadmap



Proposal | Planning | Execution | Production

Production

Sample

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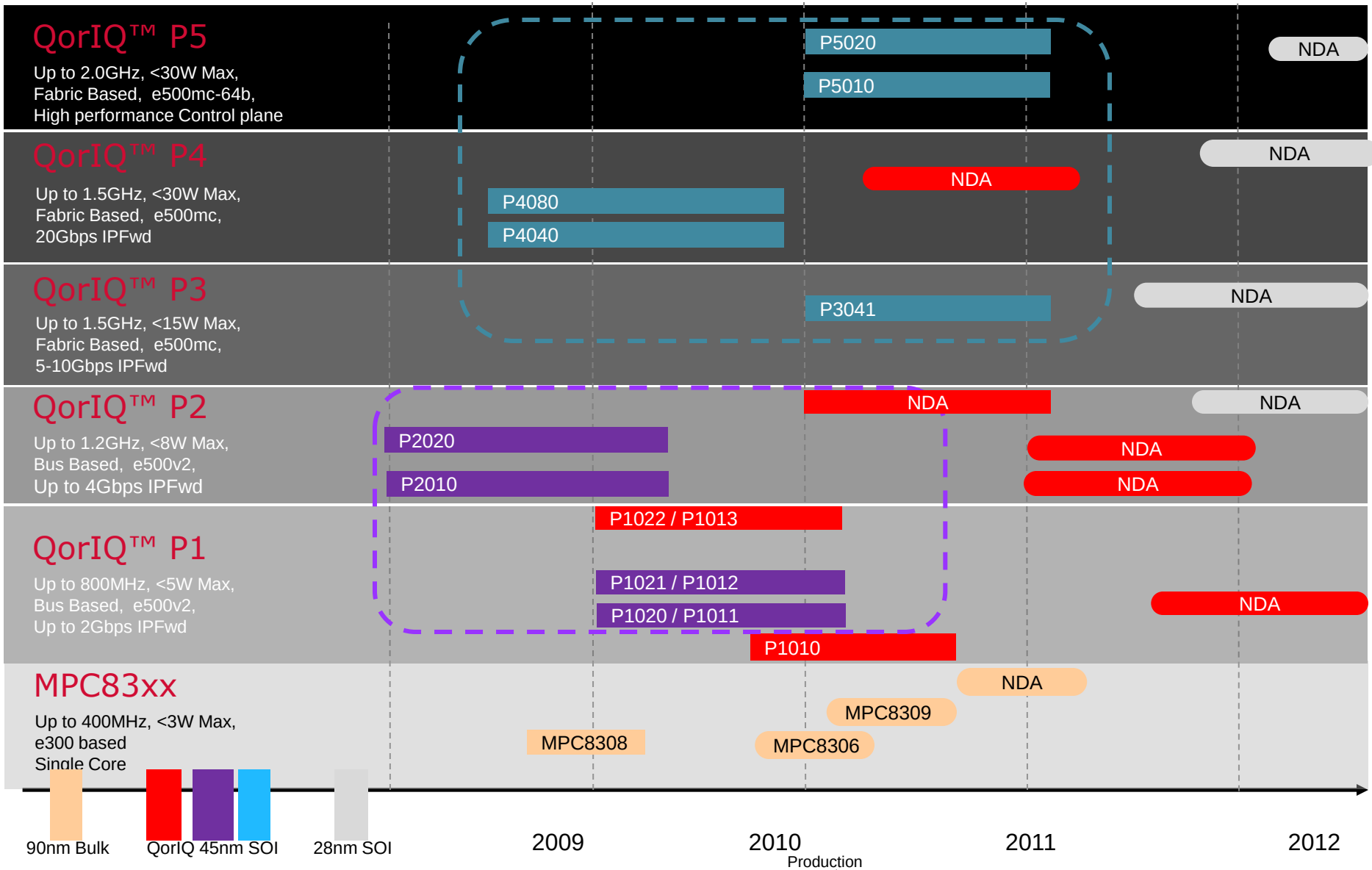
Power Architecture Processor Roadmap



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MPC8308 Block Diagram

Features

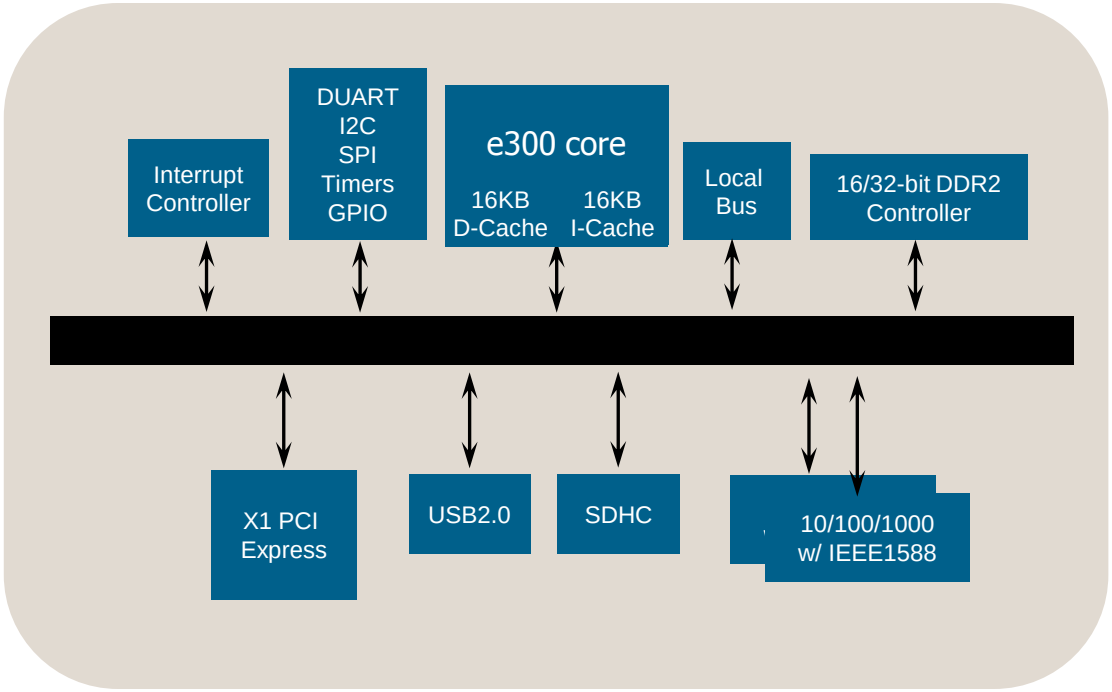
- e300 up to 400MHz
  - FPU + Dual IU
- DDR2 @ 266MHz
  - 16/32-bit (w/ ECC)
- Local Bus
  - Boot from NAND Flash support
- x2 10/100/1000
  - MII / RGMII
  - IEEE1588 support
- x1 PCI Express v1.0a
- USB 2.0 – Host / Device / OTG
- SDHC (host controller)
- Multi-channel DMA controller
- DUART, 2x I2C, SPI, GTM, RTC
- 8 dedicated GPIOs
  - Additional available based on peripherals used

Package

- 473pin MAPBGA (0.8mm pitch – 19 x 19)

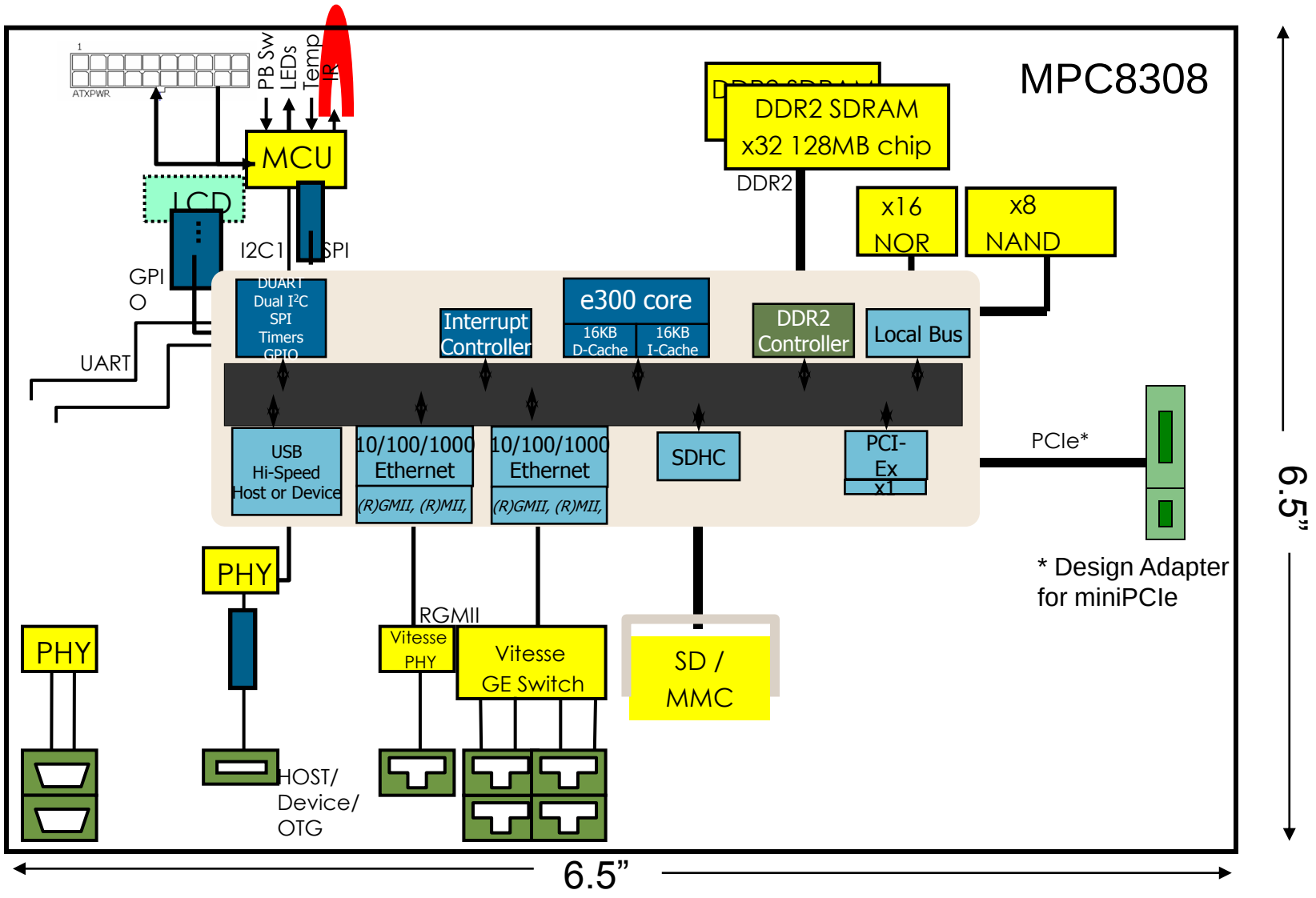
Power consumption

- ~1.5W @ 333MHz-Core, Tj 105C



No encryption engine.

(MPC8308-RDB) Mini-ITX Reference Design Board



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MPC8306S Block Diagram

Features

- e300 up to 266 MHz
  - FPU + Dual IU
- DDR2 @ 266MHz
  - 16-bit (w/o ECC)
- Local Bus
  - Boot from NAND Flash support
- x3 10/100 (/RMII/ MII)
- x2 HDLC/TDM
  - Up to 64 channels per TDM interface
- USB 2.0 – Host / Device / OTG
- DUART, 2x I2C, SPI, GTM, RTC
- 8 dedicated GPIOs
  - Additional available based on peripherals used

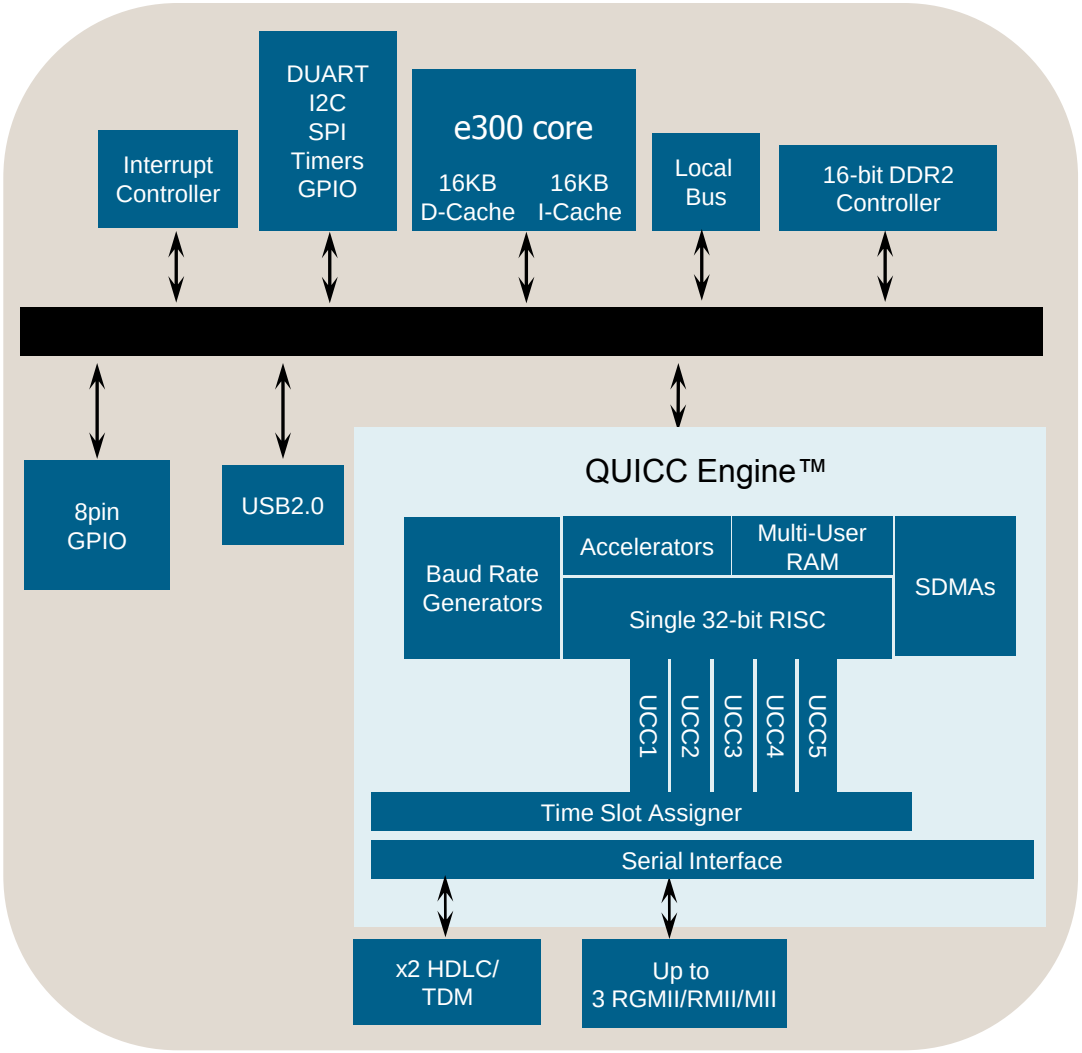
Proposed Package

- 360pin MAPBGA (4-layer; 19x19mm; 0.8mm pitch)

Power consumption

- ~1.15W (typ) @ 266MHz-Core, 200MHz-QE, Tj 25°C

No encryption engine.



MPC8306 Block Diagram

▶Features

- e300 up to 266 MHz
  - FPU + Dual IU
- DDR2 @ 266Mhz
  - 16-bit (w/o ECC)
- Local Bus
  - Boot from NAND Flash support
- Up to x3 10/100 RGMII/RMII/MII or
  - **x2 10/100/ (RMII/MII) with IEEE1588 (mux'd w/ 3rd RGMII)**
- **Profibus**
- USB 2.0 - Host / Device / OTG
- DUART, 2x I2C, SPI, GTM, RTC
- Mux'd 8 bit GPIO
  - **Mux'd 8 pins or**
  - **SDHC / x4 CAN**

▶Proposed Package

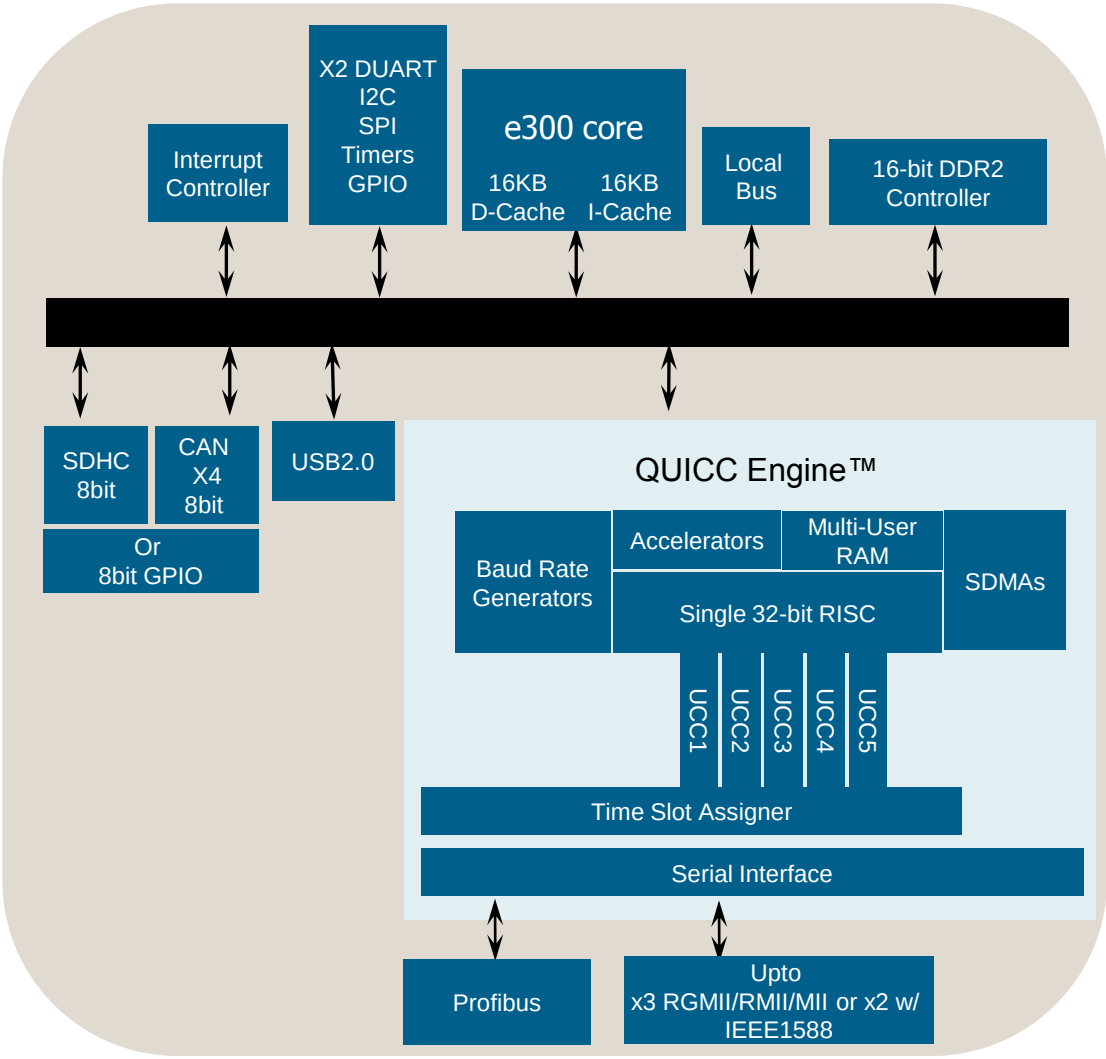
- 360pin MAPBGA (4-layer; 19x19mm; 0.8mm pitch)

▶ Power consumption

- ~1.15W (typ) @ 266MHz-Core, 200MHz-QE, Tj 125 C

No encryption engine.

Low-cost Industrial Control / Factory Automation



MPC8309 Block Diagram

Features

- e300 **up to 400MHz**
  - FPU + Dual IU
- DDR2 @ 266MHz
  - 16/**32-bit (with ECC)**
- Local Bus
  - Boot from NAND Flash support
- **32-bit PCI: up to 66 MHz (v2.3)**
- Up to x3 10/100/RMII/MII or
  - x2 10/100/ (/RMII/MII) supporting IEEE1588
- Profibus or x2 HDLC/TDM
  - Up to 64 channels per TDM
- USB 2.0 - Host / Device / OTG
- DUART, 2x I2C, SPI, GTM, RTC
- Mux'd 16 GPIO
  - MUX'd 16 pins or
  - SDHC / x4 CAN

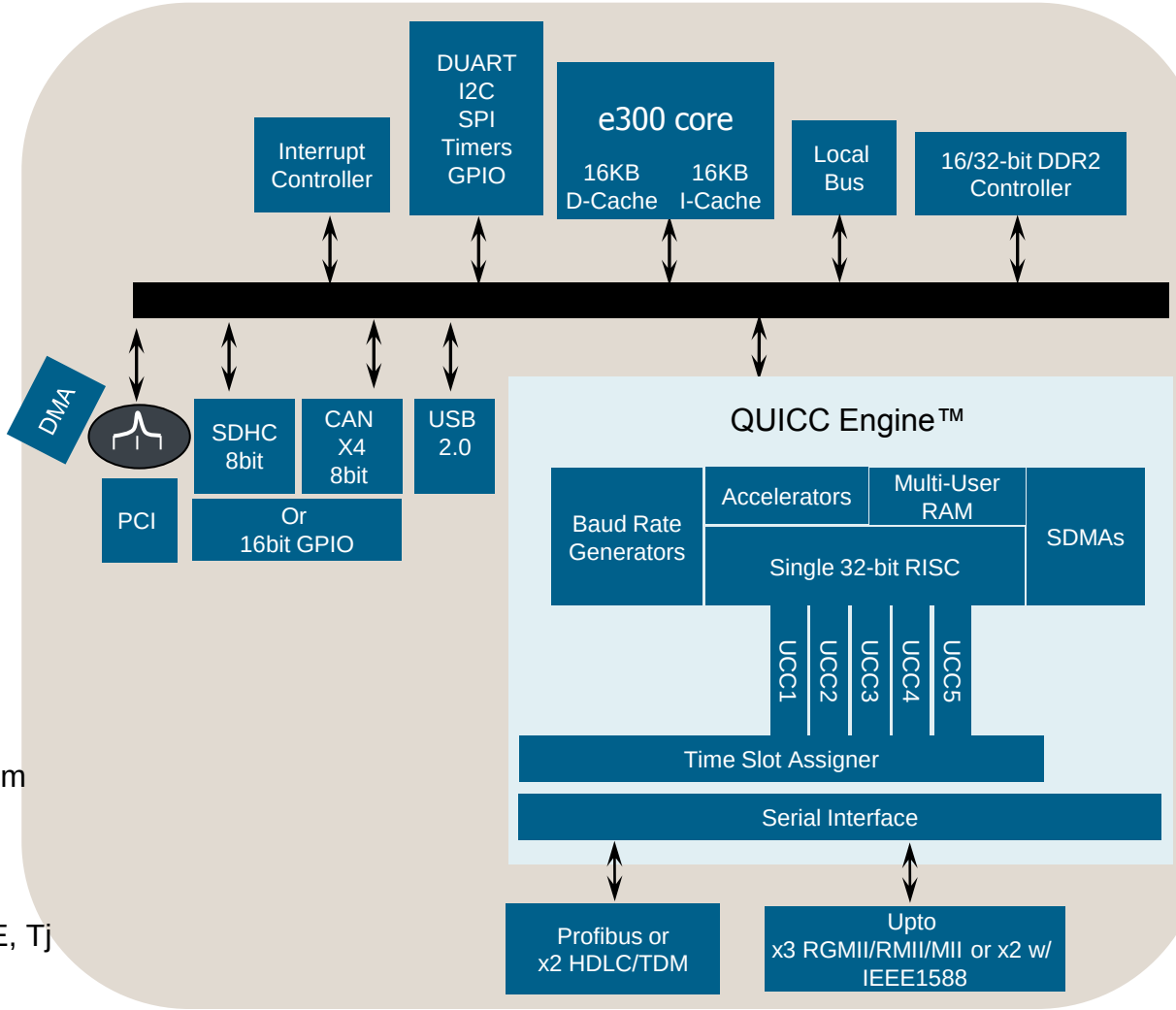
Proposed package

- 529pin MAPBGA (4-layer; 19x19mm; 0.8mm pitch)

Power consumption

- ~1.56W (typ) @ 333MHz-Core, 200MHz-QE, Tj 125°C

No encryption engine.



MPC831xE Family

MPC8313E Block Diagram and Features

CPU

e300 processor built on Power Architecture technology, to 400 Mhz rev2.1

DDR2 Memory Controller

16b/32b DDR-333 / DDR2-333

x2 10/100/1000 Ethernet MACs

Dual RGMII/RTBI/MII/RMII/SGMII

IEEE 1588 support VR 2 with rev 2.1

One High-Speed USB 2.0 (480 Mbps)

HS PHY supports host/device

Security (AES, DES, 3DES, SHA-1)

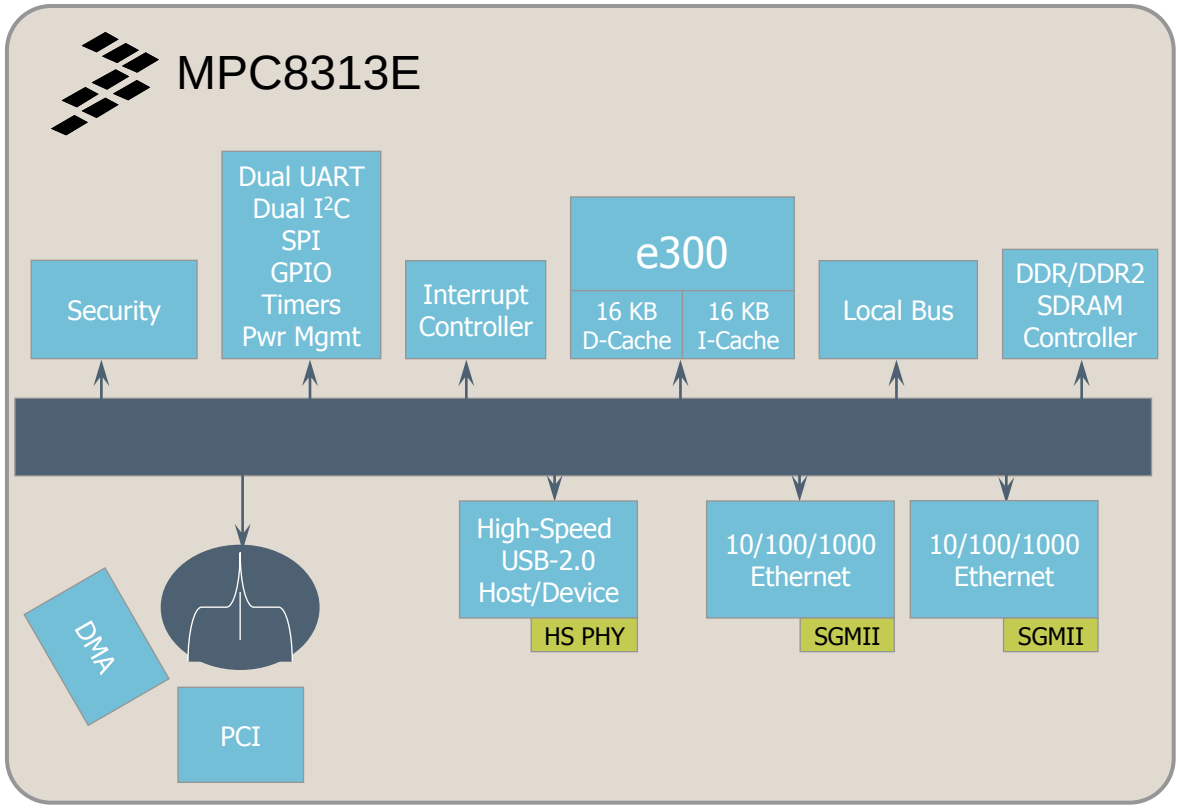
Power Management Controller

Low standby power

Technology and Package

CMOS90G, 1.0V core, 1.8/2.5/3.3V I/O

516 TEPBGAII



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New eTSEC Enhancements

Code compatible with MPC834x TSEC

Support for weighted round robin and strict priority queueing

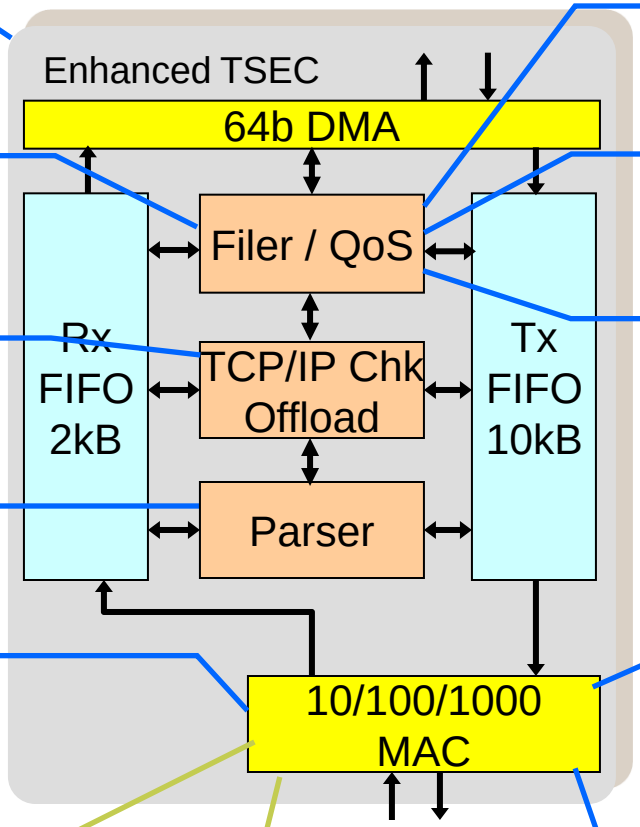
TCP/IP checksum offload for RX and TX

IPv6 and Magic Packet support

SGMII Interface Support added (8378 only)

IEEE1588 Support added

Lossless Flow Control Support



QoS support for 8 Rx and 8 Tx H/W queues

Customizable per-packet rejection

Customizable per-packet filtering/filing to 64 logical receive queues.
Examples: 802.1p, IP TOS, Diffserv classification, TCP/UDP ports, etc.

Layer 2 features:
• VLAN insertion and deletion per frame
• 2 exact-match MAC addresses

•Increased hash table address matching

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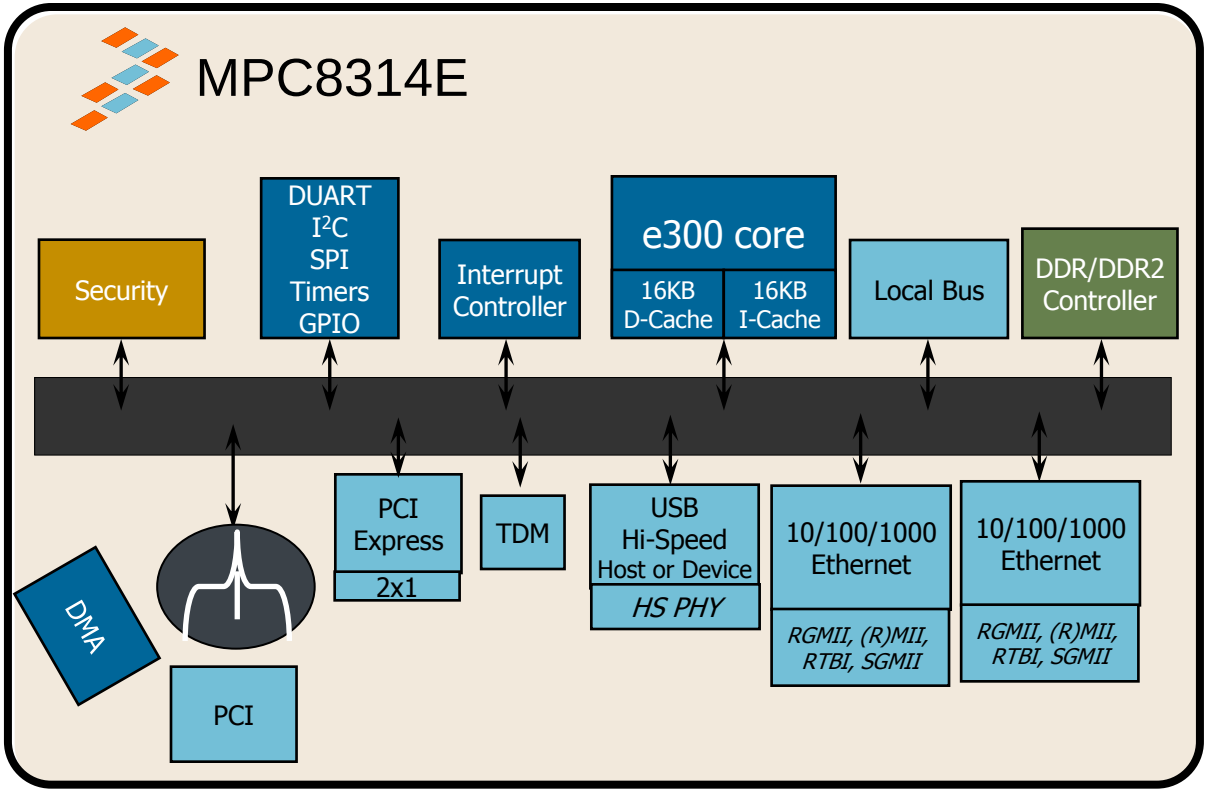
MPC8314E – Block Diagram and Features

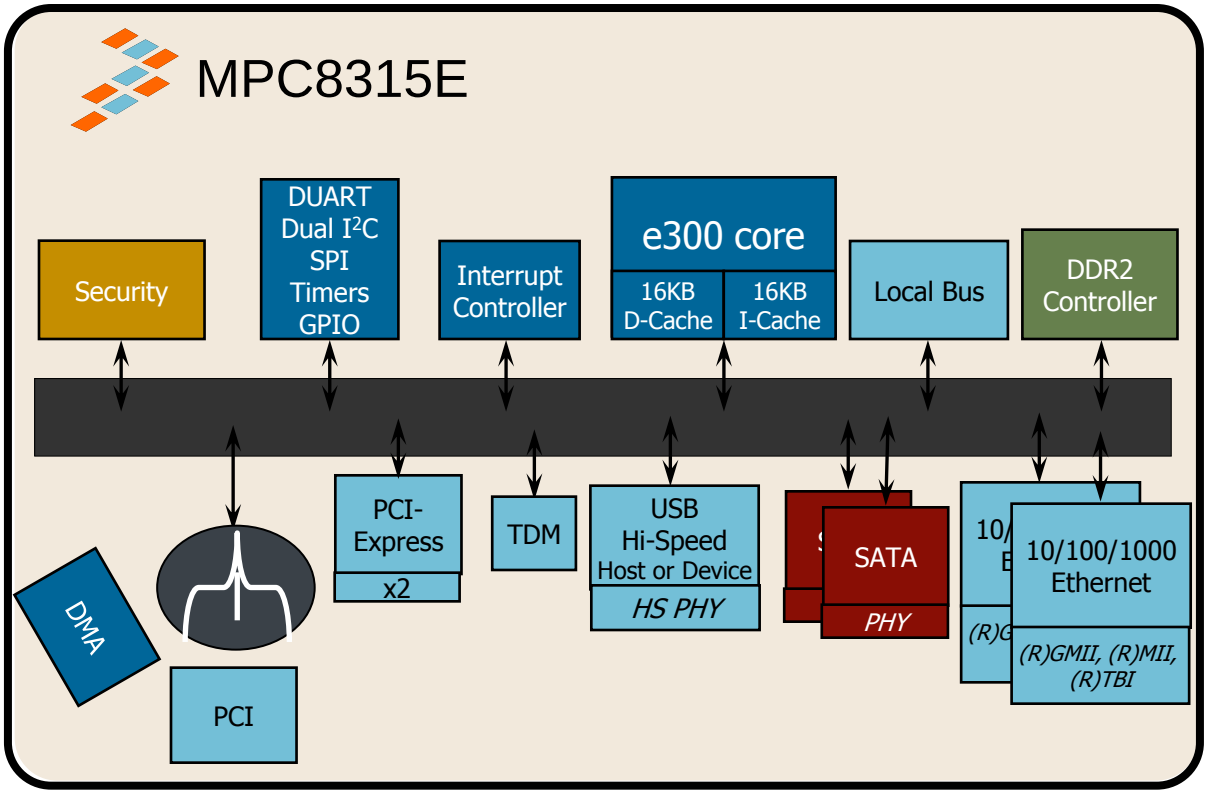
Features
- e300 processor core
  - Up to 400MHz w/FPU
  - 16KI / 16KD cache
  - 2nd ALU for 2 channel voice support
- Memory controller
  - Supports DDR & DDR2
  - 16/32-bit, 266 MHz Data Rate
- 2 x 10/100/1000 Ethernet MACs
  - Ethernet Checksum
  - 1588 Support
  - SGMII muxed with PCI Express
- 1 x PCI 2.3
  - 32bit, 66MHz
- 2 x 1 PCI Express v 1.0a
  - Muxed with SGMII
  - Root Complex, End Point
- Integrated Security Engine
  - AES, PKEU, DES, 3DES, MDEU
  - Optimized for IPSEC & DTCP-IP
- TDM
  - to connect to codec
- USB 2.0
  - HS Host/Device w/Phy
- 16 bit Local Bus
- DMA, DUART, I2C, SPI, Interrupt, GPIO
- PBGA package



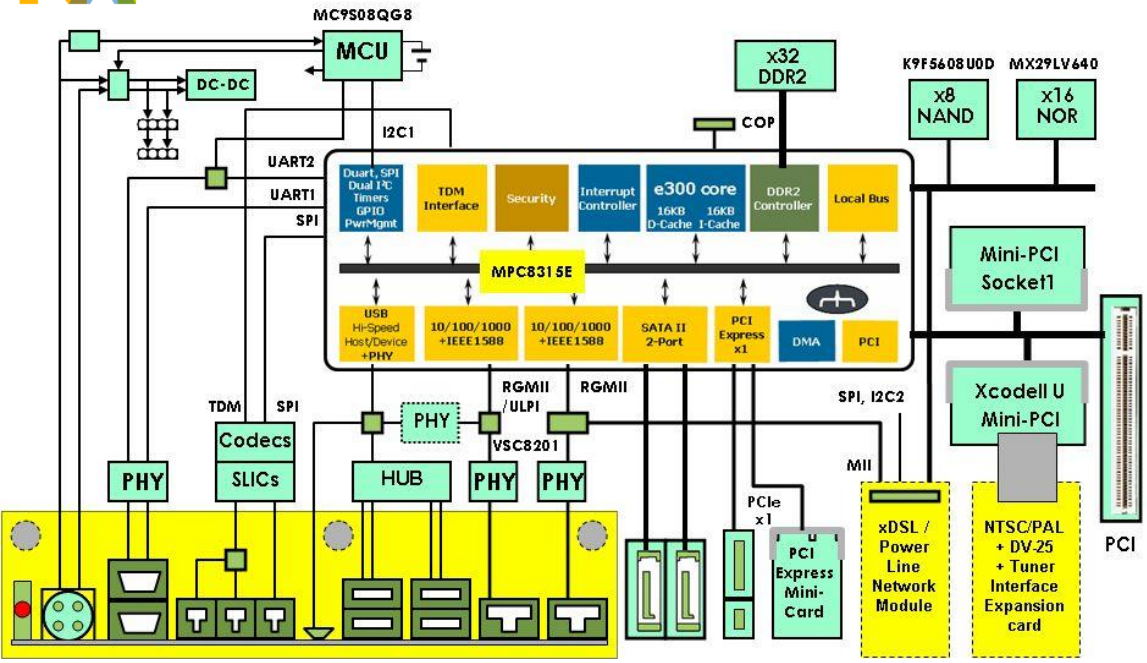
MPC8315E – Block Diagram and Features

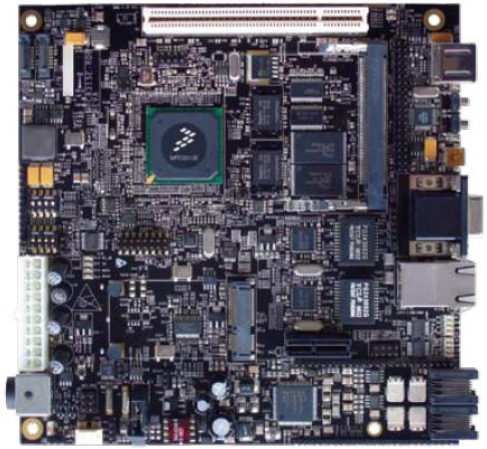
Features

- e300 processor core
  - Up to 400MHz
  - 16KI / 16KD cache
  - 2nd ALU for 2 channel voice support
- DDR2 Memory controller
  - 16/32-bit, 266 MHz
- 2x 10/100/1000 Ethernet MACs
  - Ethernet Checksum
  - 1588 Support
- PCI
  - 32bit, 66MHz PCI 2.3
- PCI-Express
  - x2 PCIE v1.0
- SATA
  - 2x SATA v2.0 w/PHY
- Integrated Security Engine
  - XOR, CRC32, IPSEC
- TDM
  - to connect to codec
- USB 2.0
  - HS Host/Device w/Phy
- Local Bus, 16bit
- DMA, DUART, Dual I2C, SPI, Interrupt, GPIO
- CMOS90G Process Technology
- PBGA package



MPC8315E-RDB board





RDB Part Numbers & Price

Part Number	SRC Price
MPC8315E-RDB	$499.00

Available Now

WIND RIVER montavista Green Hills SOFTWARE, INC. Ralink FalconStor Software mentor embedded axentra™

- **CPU**
  - MPC8315E
- **Ethernet**
  - 2 Gigabit RGMII connections directly to phys.
  - One Ethernet connection to broadband powerline capability using DS2
- **PCI Express**
  - x1 PCI Express Add-in Connector
  - miniPCI Express for WLAN
- **SATA**
  - 2 standard SATA connectors
    - eSATA will be available through SATA-eSATA connectors
- **SPI / TDM**
  - Connected to dual Legerity SLIC/SLAC
- **USB Hi-Speed**
  - Connector directly on board
  - 3 port USB Hub
- **PCI**
  - One Standard and one MiniPCI connectors
- **Memory**
  - 32-bit DDR2 for 16-bit.

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MPC8377E – Block Diagram and Features

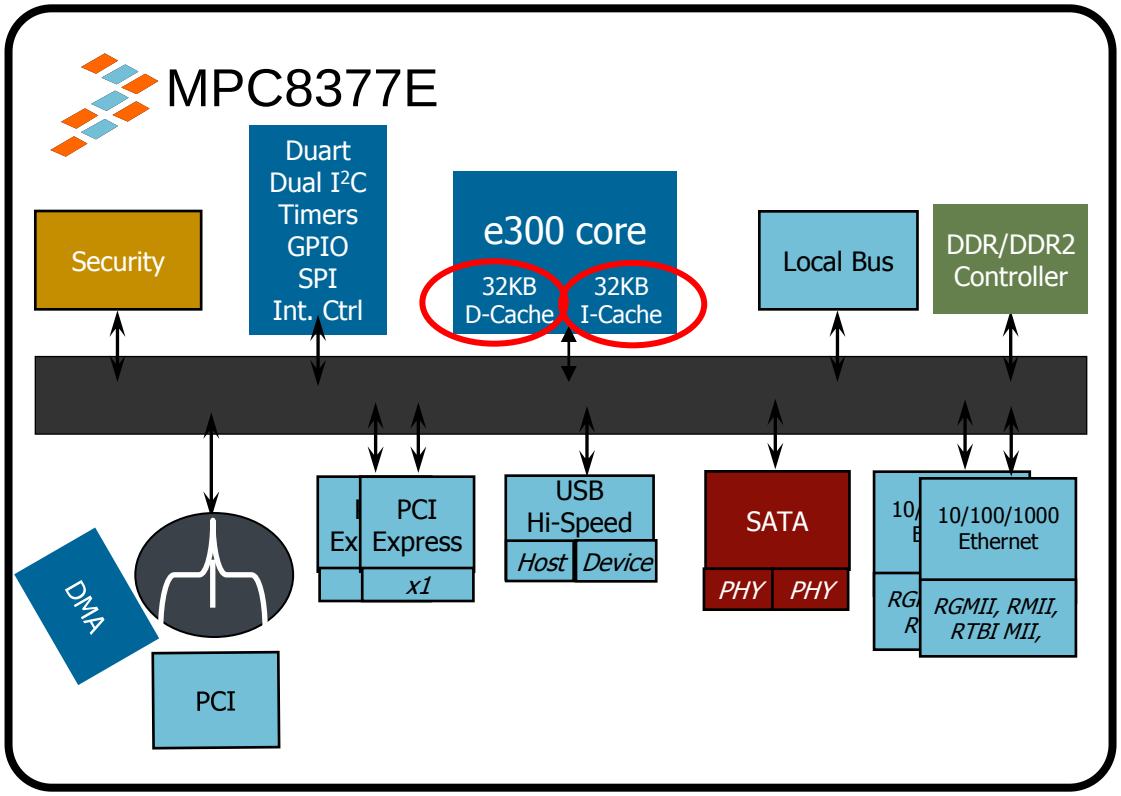
- **Features**
  - **e300 core processor**
    - **400-800 MHz w/ Floating Point**
    - 32KI/32KD cache
  - **Memory Controller**
    - Supports DDR and DDR2
    - **32/64-bit, 400MHz Data Rate**
  - **2 x 10/100/1000 enhanced Ethernet MACs**
    - RGMII, RTBI, RMII, MII
  - **1 x PCI 2.3**
    - 32 bit up to 66 MHz
    - PCI Arbiter
    - Master & Agent mode support
  - **2 x 1 PCI Express v 1.0a**

2 x SATA 3.0 Gb/S
- NCQ, Port Multiplier, Staggered Spin Up, Hot Plug

Integrated Security Engine
- AES, PKEU, DES, 3DES, MDEU, ARC4, XOR, CRC32C, RNG
- Optimized for IPSEC & DTCP-IP

One Hi-Speed USB port
- 1 port Host or Device

32 bit Local Bus w/ NAND boot support
Multi-channel DMA controller
DUART, Dual I²C, Interrupt, GPIO, SPI



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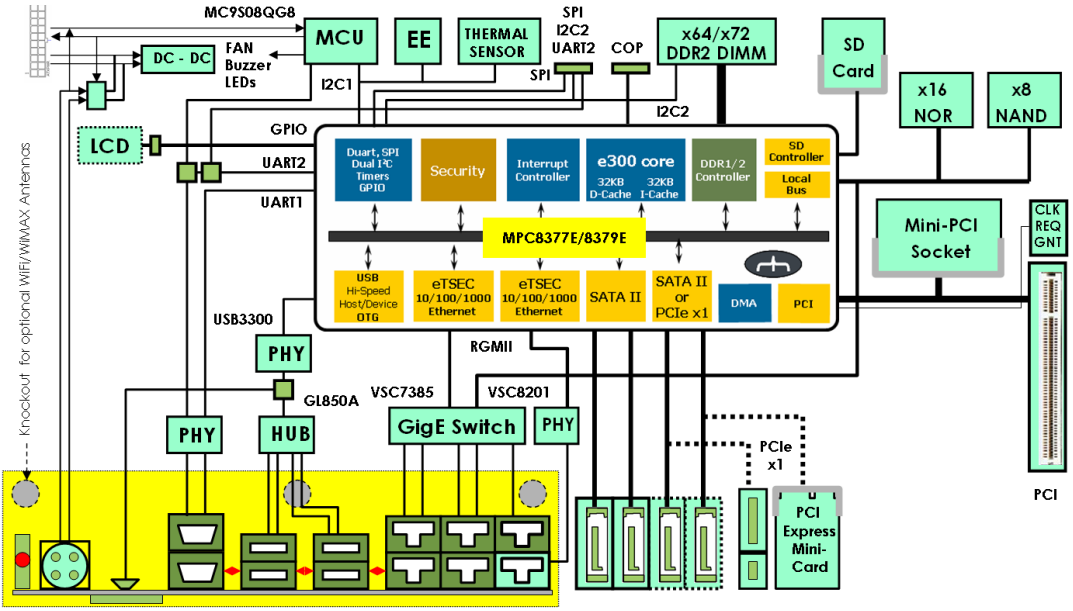
MPC8377/9 RDB Board



RDB Part Numbers & Price

Part Number	SRC Price
MPC8379E-RDB	$699.00

RDB Board Schedule

Now

Reference Design Board Features

- *CPU*
  - Freescale MPC8379E
- *Ethernet*
  - 1 Gigabit RGMII connect to Vitesse GE Phy
  - 5-Port Vitesse Ethernet Switch
- *PCI Express and PCI*
  - PCI Express Add-in Connector
  - miniPCI Express for WLAN
  - One Standard PCI connector with
  - extended for riser card
  - One Mini-PCI connector
- *SATA II*
  - 2 or 4 standard SATA connectors
- *USB 2.0 Hi-Speed*
  - 4 port USB Hub or 1-port USB OTG (jumper selectable)
  - GL850A 4 port HUB
- *Interfaces*
  - Dual UART
  - Connectors for debug connectivity
  - NAND flash and NOR flash

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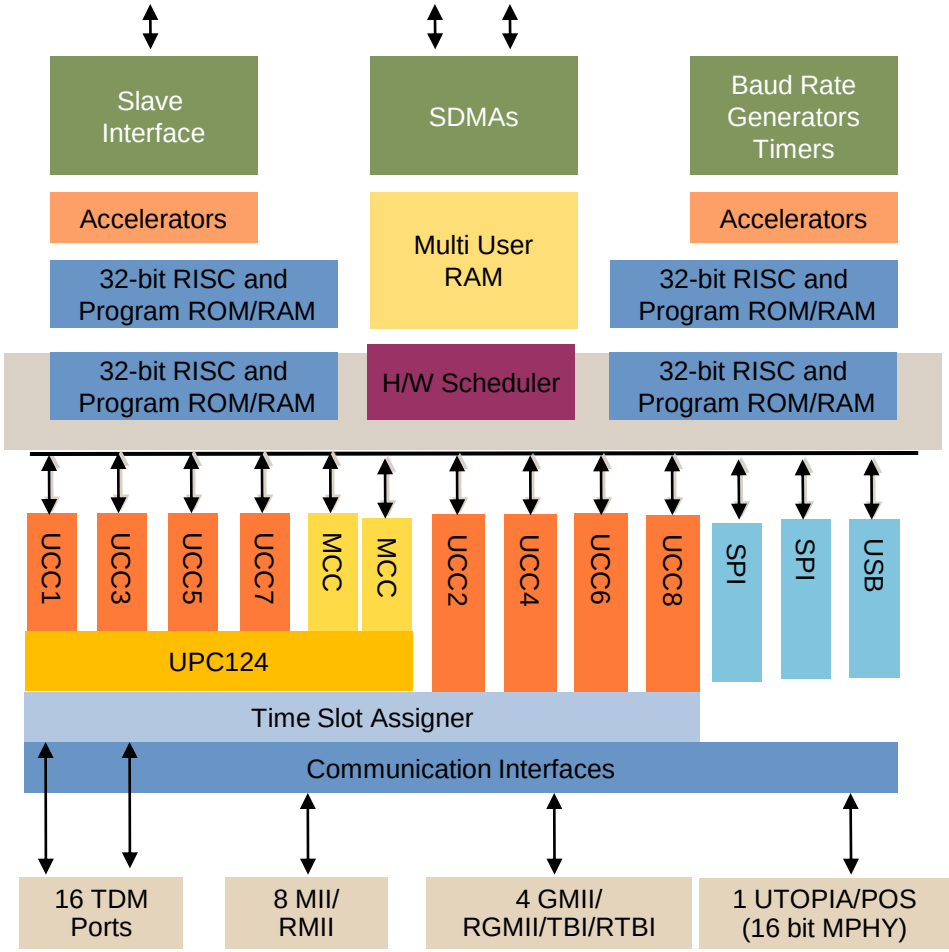
QUICC™ Engine – Architecture
Flexible, Scalable and Packet-friendly

- Asynchronous Architecture scaling from one to four RISCs at 200-667MHz.
  - Up to 2.4Gbps (Estimate) of Interworking performance,
  - Up to 3 - 4Gbps (Estimate) Layer 2 Termination performance
- Eight Unified Communication Controllers (UCCs) support virtually any interface
  - 10/100/1000 Gigabit Ethernet
  - Utopia / POS Multi-PHY Level 2 ports
  - Serial ATM
- Multi Channel Communications Controller supporting Time multiplexed protocols
  - Supports up to 16 T1/E1 interfaces
  - 256 HDLC or 128 SS7 channels on 8 TDMs
  - Serial ATM (up to 64 TC layers)
  - ML/MC-PPP

	1 RISC	2 RISC	4 RISC
MHz Range	200	200-533	200-667
IRAM Memory	8K Bytes	48K-64K Bytes	256K Bytes
MURAM Memory	16K Bytes	48K-64K Bytes	128K Bytes
ROM Memory	96K Bytes	192K bytes	N/A
Ethernet Ports	Up to 3 x 10/100	Up to 8 10/100 Up to 3 x 10/100/1000	Up to 8 x 10/100 Up to 4 x 10/100/1000
UTOPIA/POS Ports	1	2	1
TDM ports	4	8	16
IEEE1588 Support	No	Yes (8360 only)	Yes
IPV4 Forwarding Performance at 128B frames, 1x32b DDR @ 266Mhz, QE @ 200Mhz	254 Mbps		
IPV4 Forwarding Performance at 128B frames, 2x32b DDR @ 266Mhz, QE @ 500Mhz		1.2Gbps	
IPV4 Forwarding Performance at 128B frames, 1x64b DDR @ 667Mhz, QE @ 667Mhz			2.4Gbps (Estimate)



Comprehensive CodeWarrior™ & 3rd-Party Enablement Ecosystem

Portfolio of QUICC Engine Protocols Royalty and NRE Free

Protocols

- ATM AAL 0/1/2/5
- IMA over TDM / UTOPIA / Channelized
- Serial ATM (ATM TC sublayer)
- 10/100/1000 Ethernet and VLAN
- Multi-Link PPP, Multi-Class PPP, PPP-Mux
- HDLC
- BISYNC
- SS7
- Ethernet in the First Mile (EFM)
- IP Header Compression
- USB

Interworking and Switching

- ATM-to-TDM Interworking for AAL0/AAL1
- AAL2 CPS Switching
- ATM to Ethernet Interworking
- Ethernet to Ethernet Interworking
- L2 Fast Ethernet Switch
- PPP to Ethernet Interworking
- PPP to ATM Interworking*
- Enhanced Multi-Service Platform (EMSP)

Classification and Transformation

- Parsing for multi-field classification
- Hierarchical lookups
- Tables: Hash, Index, CAM Emulation, LPM*
- Flexible header manipulation

Quality of Service

- Ethernet / IP:
  - Combined strict priority and WFQ scheduling
  - Rate limiting / shaping
  - Lossless flow control
  - WRED*
- ATM Traffic Management:
  - TM 4.1 UBR, CBR, GFR, VBR
  - Per-flow ATM scheduler for 64K VCs
  - Hierarchical frame and cell based scheduling
  - Policing
  - Congestion Control

*Planned

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MPC8323E – Block Diagram

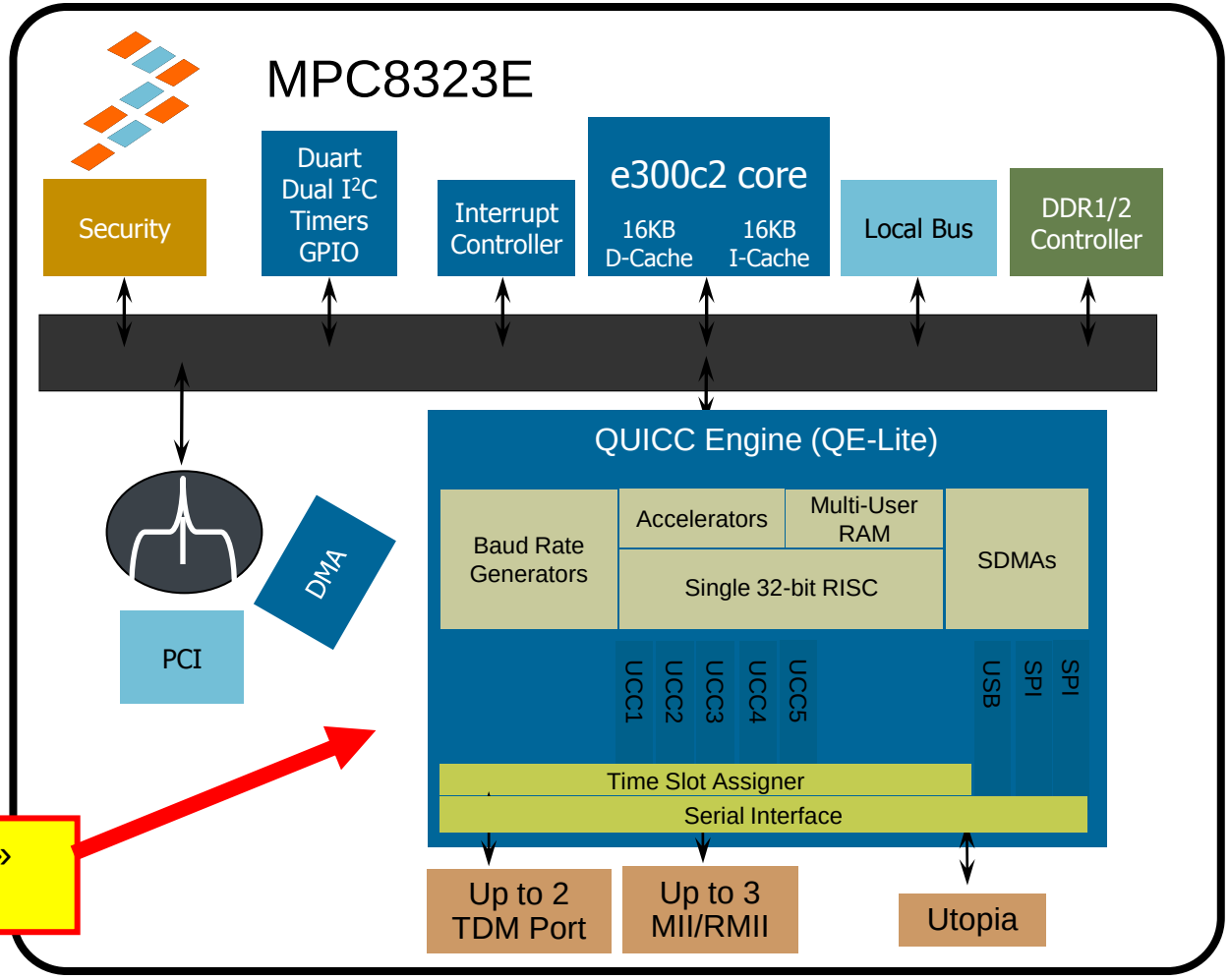
Features

- Integrated e300 processor core
  - Up to 333MHz, NO FPU
  - 16K-I / 16K-D cache
- DDR1/2 Memory controller
  - 32-bit, 266 MHz
- Local Bus, 16 bit
- PCI 32 bit
  - 33 MHz PCI 2.2
  - Master and Agent mode
- QUICC Engine Lite
  - 1 micro engine (200 MHz)
  - 5 UCCs (Utopia, 10/100, TDM w/QMC)
  - USB 2.0 FS/LS, SPI
- DUART, Dual I^2C, Interrupt, GPIO
- HW Encryption

Technology/Power

- 90nm
- 516 PBGA package
- 2W Estimate

Microcode « ethernet to ethernet » available



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MPC8360E – Block Diagram and Features

Integrated e300c1 processor core

- 266 - 667 MHz
- 32K I/D cache

DDR1/2 Memory controller

- 1 x 32/64-bit or
  2 x 32-bit 266/333 MHz

Integrated 32-bit PCI

- Up to 66 MHz PCI 2.2
- Host & Agent mode support

Local Bus

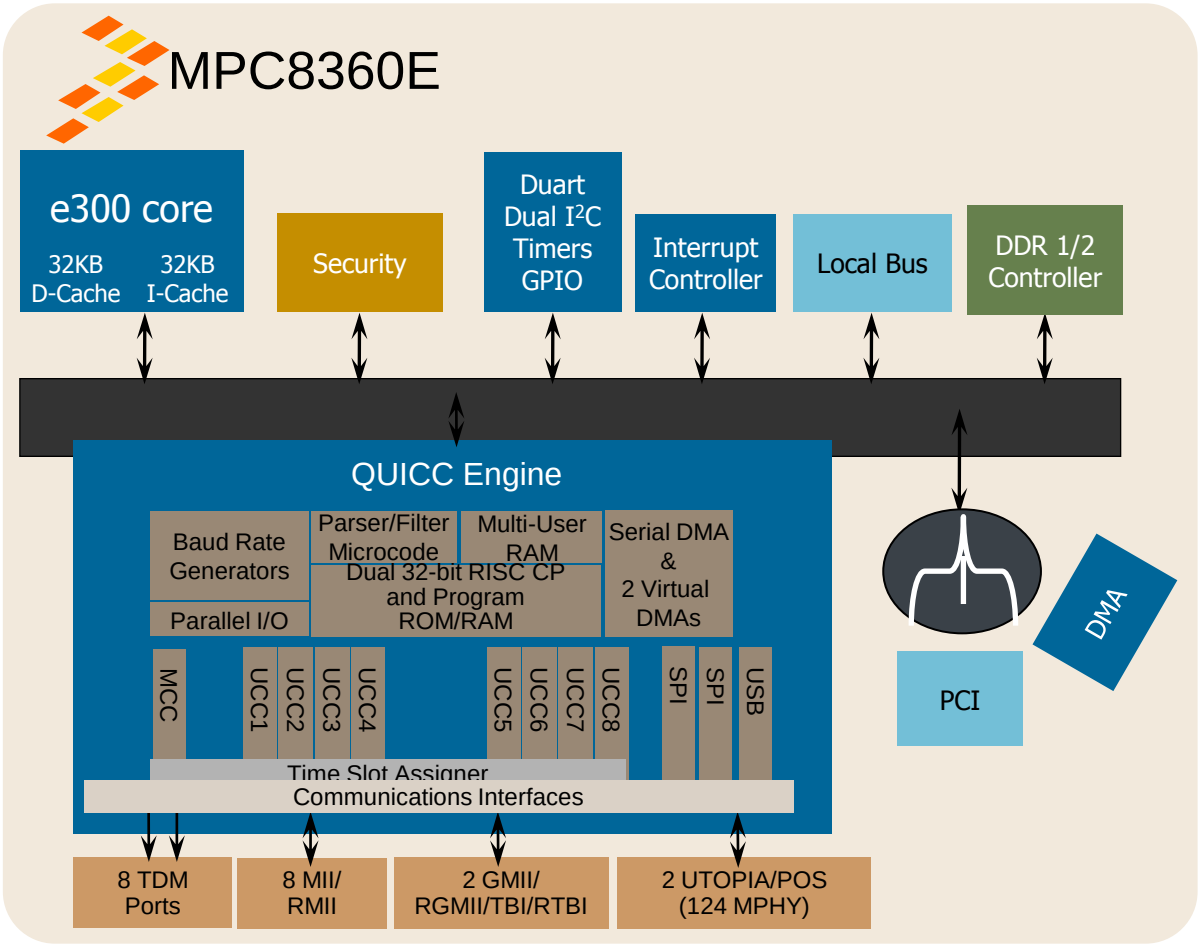
Integrated Security SEC 2.4

QUICC Engine

- 2 micro engines (300 - 500 MHz)
- 8 UCCs (Two UL2/POS, Two GMII, 8 MII, 4 port L2 switch, 8 TDMs)
- MCC (256 HDLC channels)
- Dual SPI
- USB Low/Full Speed
- Multi-channel DMA controller
- DUART, Dual I²C, Interrupt, GPIO
- Clear channel T3/E3
- IEEE1588
- System Interrupt Visibility

Technology:

- 130nm
- 1.2V core, 3.3/2.5V I/O
- 740 TBGA (37.5x37.5) 1mm pitch



Production

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MPC8358E – Block Diagram and Features

Integrated e300c1 processor core

- 266 - 400 MHz
- 32K I/D cache

DDR Memory controller

- 1 x 32/64-bit 266 MHz

Integrated 32-bit PCI

- Up to 66 MHz PCI 2.2
- Host & Agent mode support

Local Bus

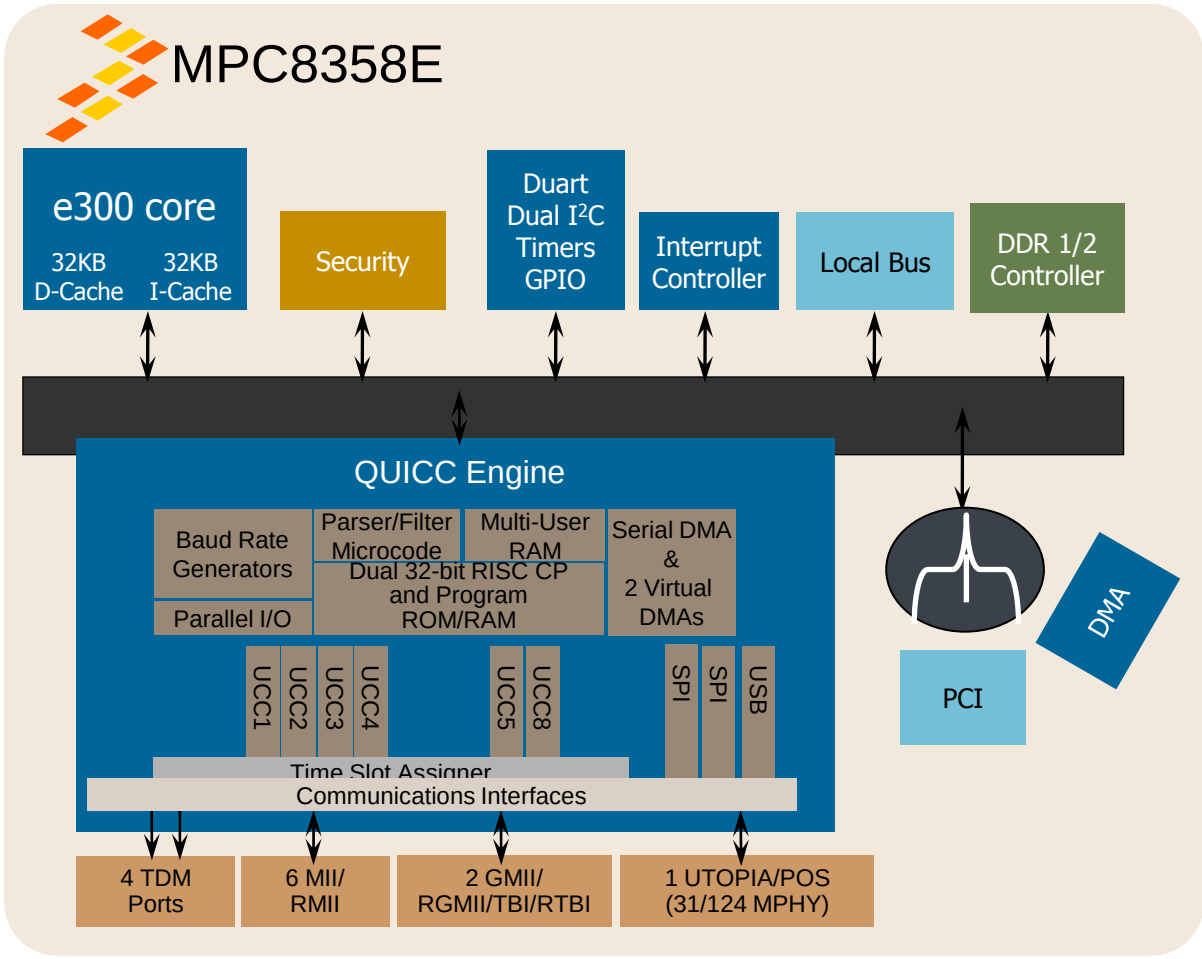
Integrated Security SEC 2.4

QUICC Engine

- 2 micro engines (200 - 400 MHz)
- 6 UCCs (One UL2/POS, Two GMII, 6 MII, 4 port L2 switch
- QMC for TDM support
- Dual SPI
- USB Low/Full Speed
- Multi-channel DMA controller
- DUART, Dual I²C, Interrupt, GPIO
- Clear channel T3/E3
- IEEE1588
- System Interrupt Visibility

Technology:

- 130nm
- 1.2V core, 3.3/2.5V I/O
- 740 TBGA (37.5x37.5) 1mm pitch
- 668 PBGA (29x29) 1mm pitch



Production

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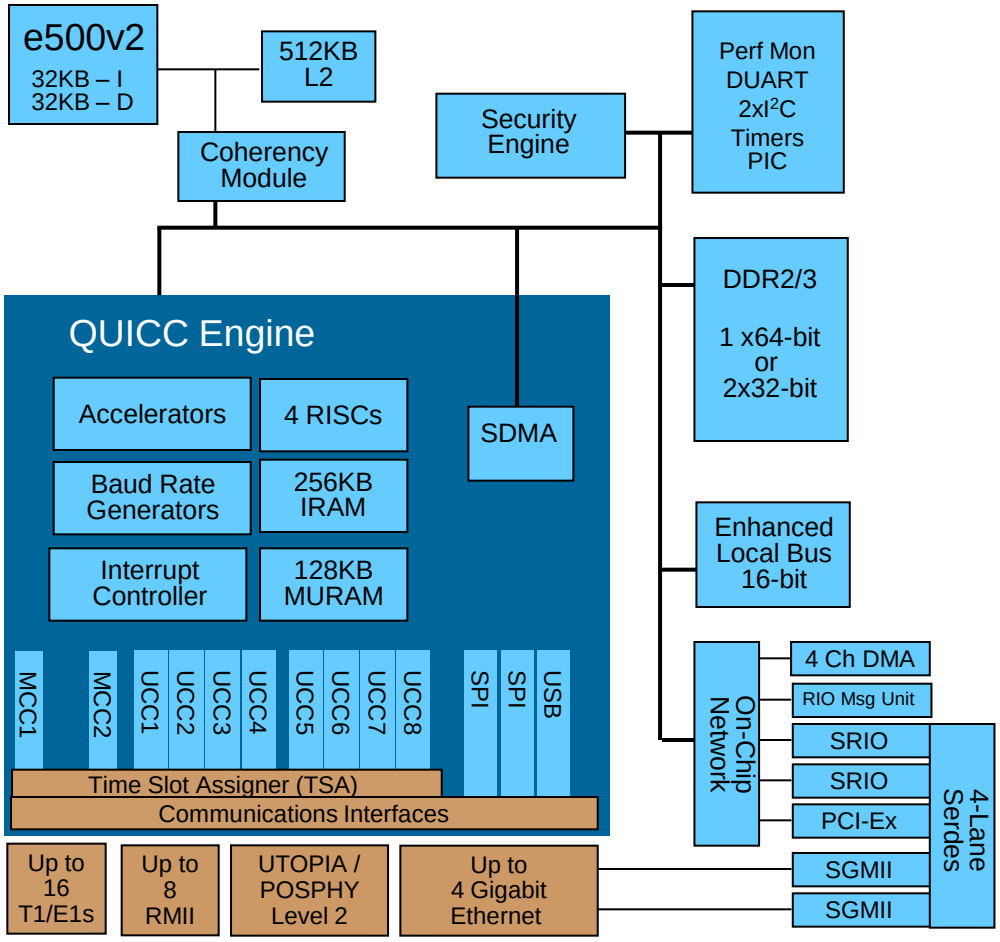
MPC8569E Product

MPC8569E



- e500 PowerPC 1.33 GHz
  - 512KB L2 Cache w/ ECC
  - 36bit physical addressing
  - Double Precision Floating Point
- System Interfaces
  - 64b or 2x32-bit DDR2/3 w/ ECC
  - 800 Mbps/pin data rate
  - 16-bit Local Bus for SRAM/Flash
  - Timers, DUART, 2xI²C, GPIO, SPI
  - USB 2.0 Full Speed
- High Speed Serial Interfaces
  - Dual SGMII
  - Dual x1 Serial RapidIO or PCI-Ex
- QUICC Engine
  - 667 MHz (4 RISCs)
  - Maximum of 8 Ethernet interfaces, one per UCC:
    - 4 x Gigabit Eth (up to 2 w/SGMII)
    - Up to 8 x 10/100 Ethernet
  - Multi-PHY UTOPIA/POS-PHY L2 (16-bit)
  - IEEE1588 Support v2
  - 16 x T1/E1 (512 x 64kbps channels)
- Security Engine
  - ARC4, 3DES, AES, RSA/ECC, RNG, XOR, Single pass SSL/TLS, Kasumi
- Four-channel DMA
- 45nm SOI process technology
- Target <7W Power (@ 800MHz e500)

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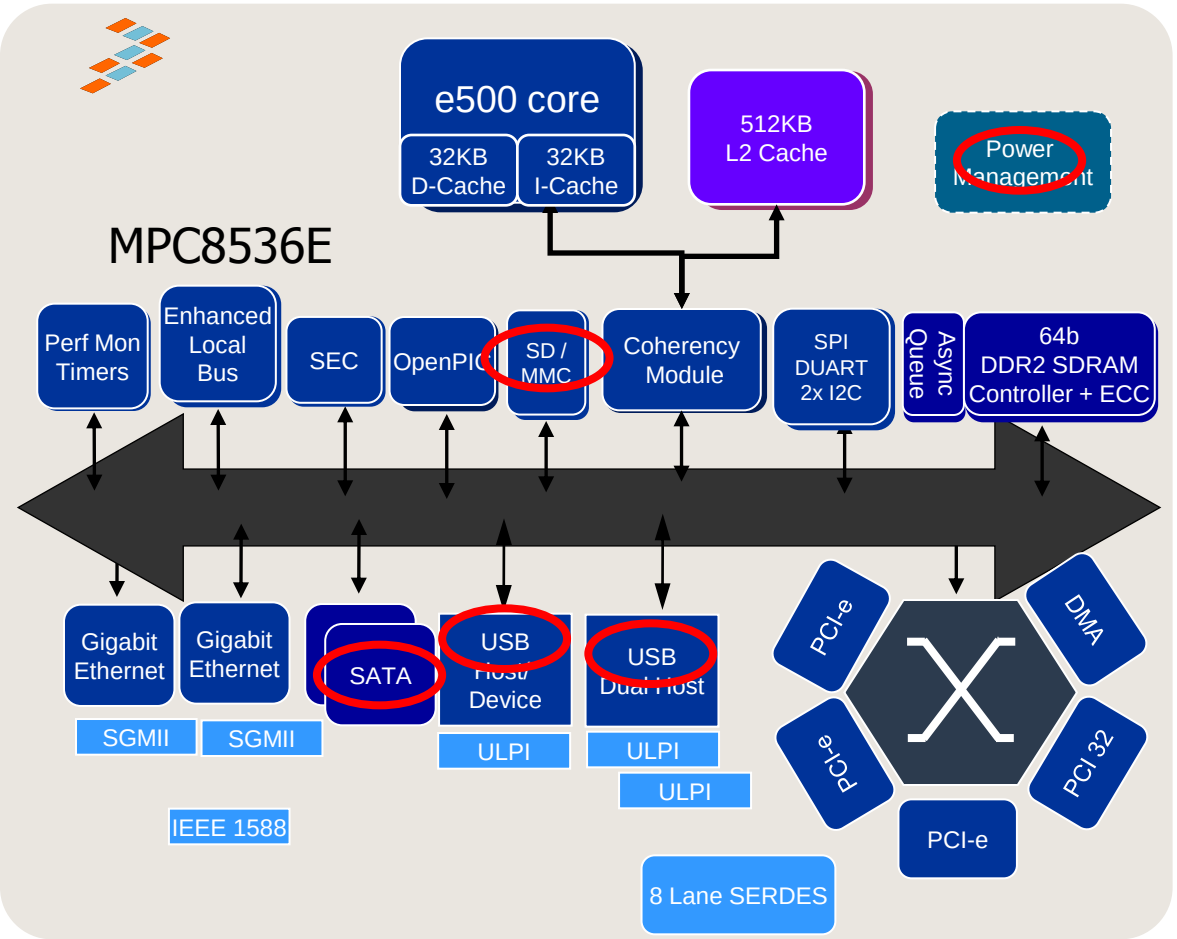
MPC8536E Block Diagram



- **e500v2 PowerPC core up to 1.5 GHz**
  - 512KB L2 Cache w/ECC
  - 36 bit physical addressing
  - DP-FPU, SPE
- **System Unit**
  - 64/32b DDR2/3 up to 533 MHz data rate w/ECC
  - Integrated Security Engine
  - USB 2.0 High Speed Host/Device
  - USB 2.0 Dual Host Controller
  - SD/MMC Flash Interfaces
  - SPI & Enhanced Local Bus
  - SATA
  - Dual 10/100/1000 Ethernet Controllers
  - High Speed Interconnect
    - Triple PCI Express
    - PCI
  - Dual SATA
  - IEEE-1588
- **Advanced Power Management Controller**
  - Nap, Doze, Sleep, Deep Sleep (@0.95W @ 35C)
  - Power off to core and cache
  - Wake on LAN,/USB/GPIO/timer/external signal
  - Isolated Power Planes
- **Low Power Dynamic Operation** (typical power estimate)
  - CPU/Platform
  - 800/400 – @ 4.5W
  - 1000/500 – @ 5.2W
  - 1500/500 – @ 6.7W

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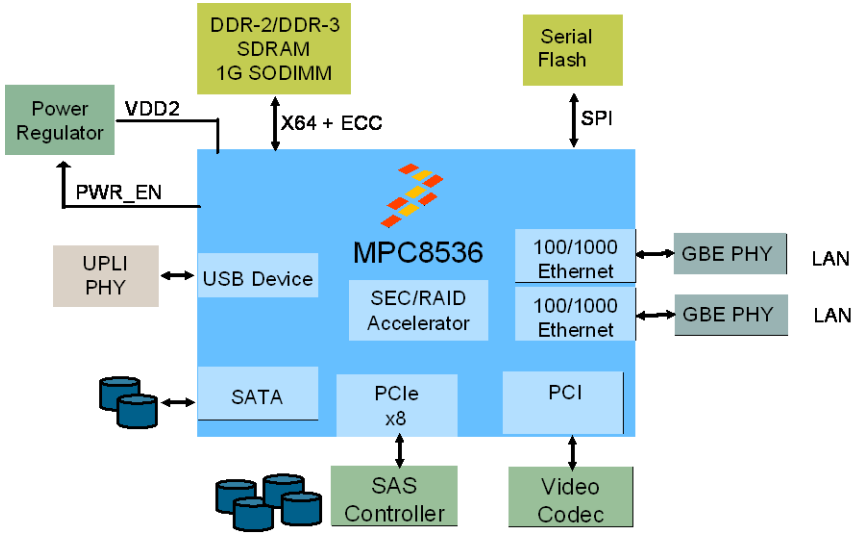
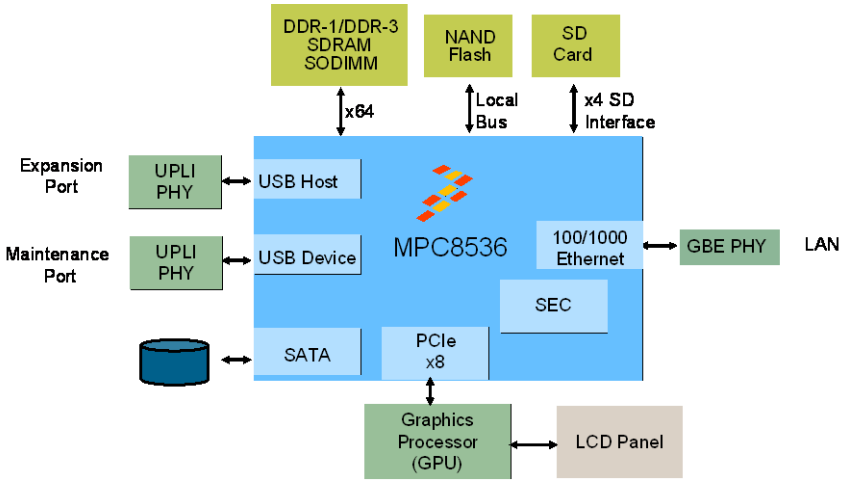
Applications targeted

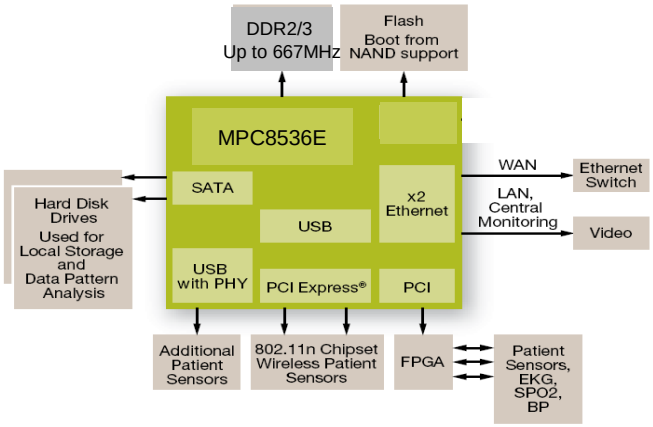


Network Storage

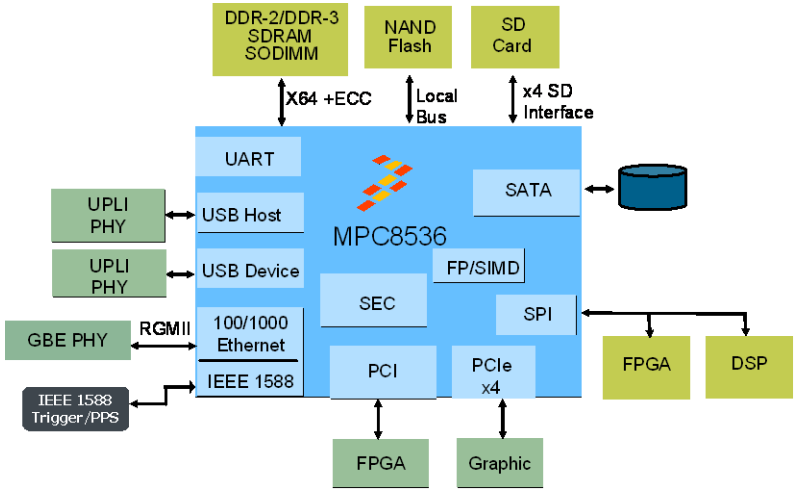


POS/Kiosk/Digital Signage/Avionic

Patient monitoring / Diagnostic equipment



Industrial Controls & Instruments



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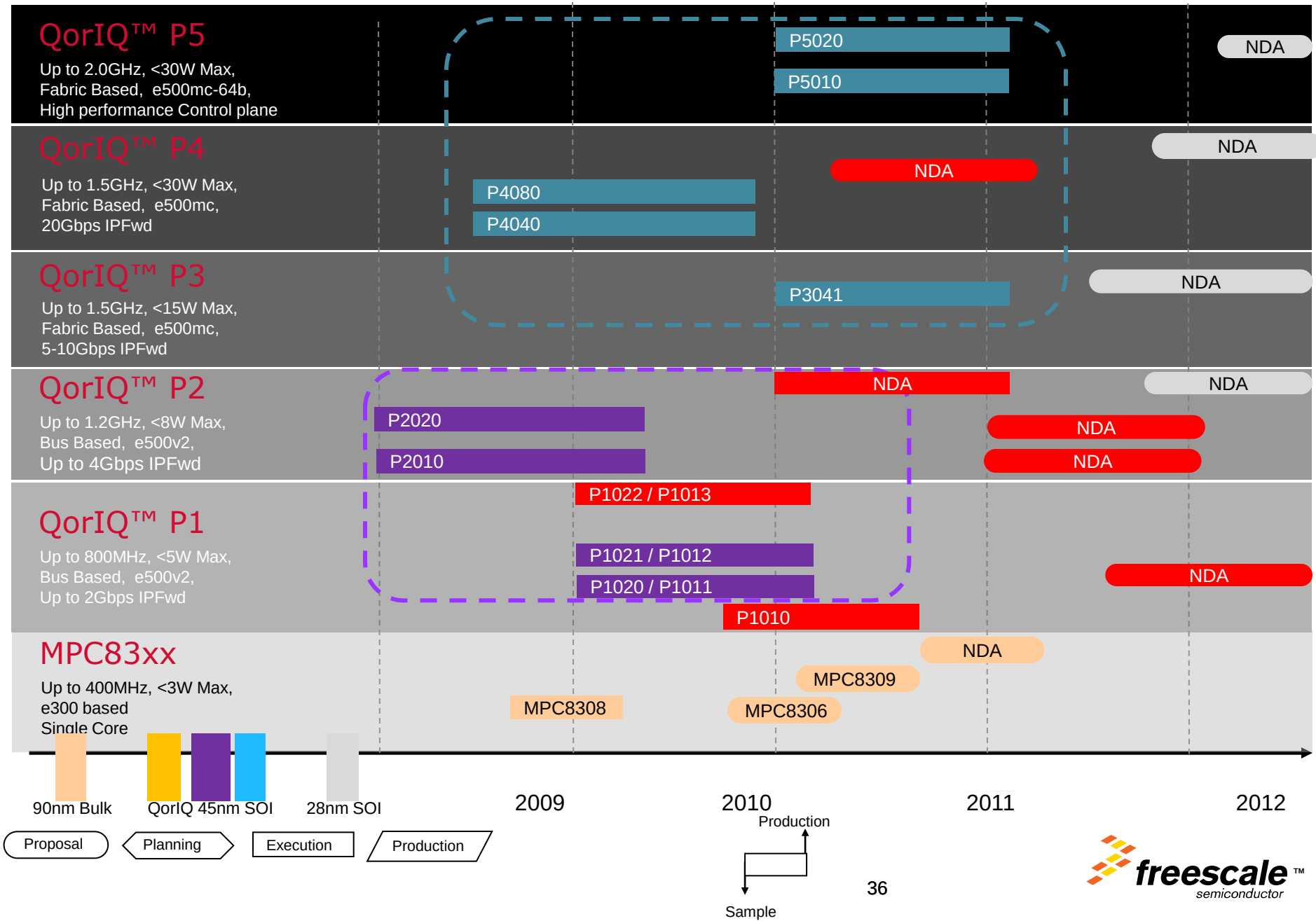
Power Architecture Processor Roadmap



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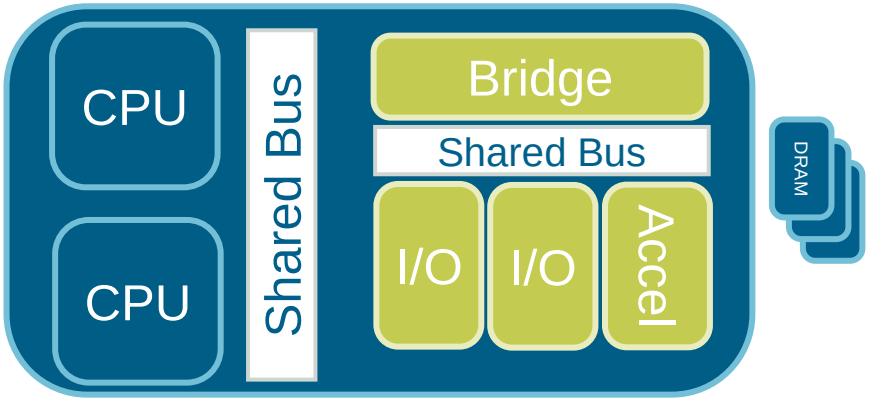
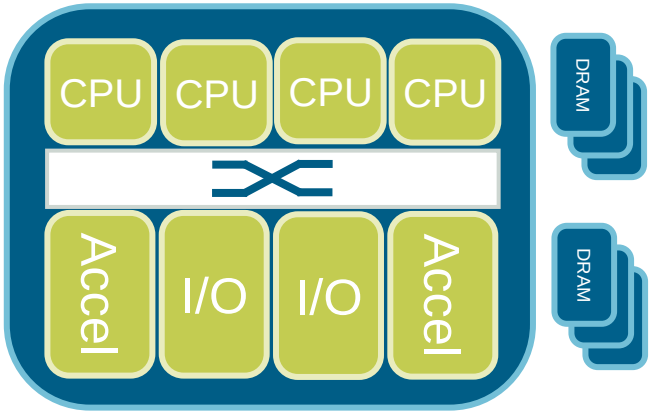
Freescale's Multicore System Architecture



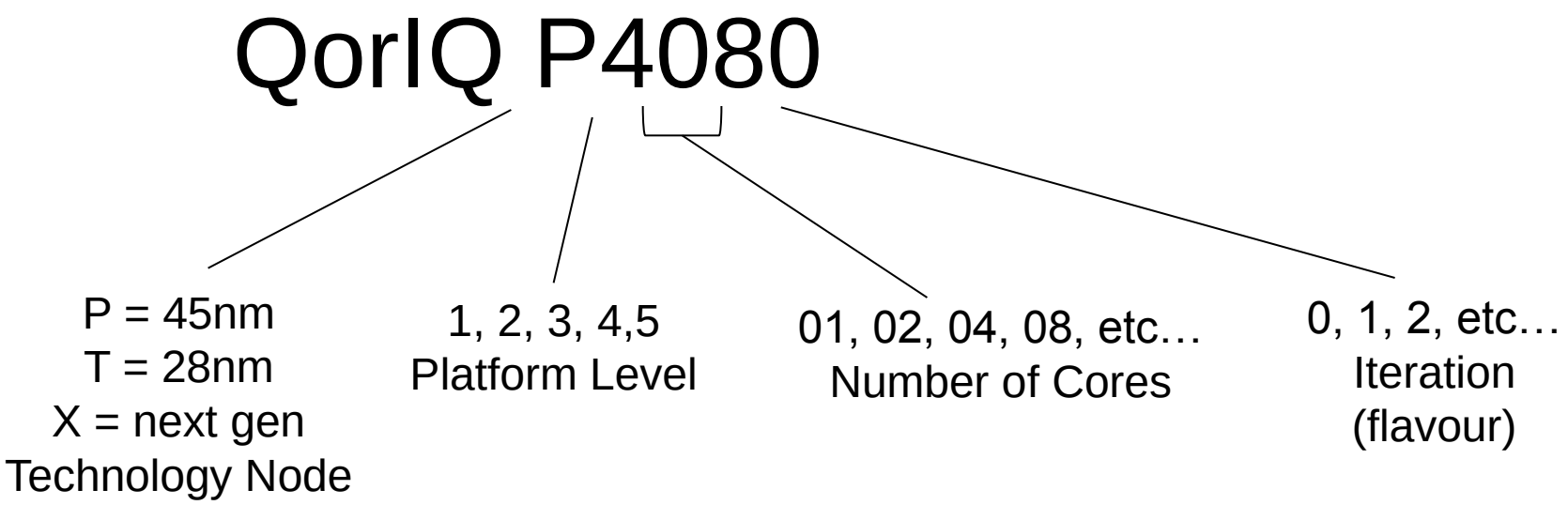
PQ/P1/P2



Multicore

Embedded Challenge	Bus Architecture	Fabric Arch	Comments
Core performance	Power Architecture e500 and e600 cores	Power Architecture e500 core w Front and backside cache	Moving to e500 cores across the family, common ISA from 4 to 30 watts
System Performance	Classic interrupt shared BUS architecture	Point to point Cross-bar Fabric	Balanced architecture between cores/IO/accelerators
Embedded Power Budgets	<4 to 30 Max Power	<4 to 30 Max Power	Year on Year improvement System Performance within embedded Pwr
Trusted computing and Virtualization	Software based virtualization	Hardware/software Virtualization/Trusted Computing	Highest level of Secure Boot and anti-threat protection in the industry
Quick time to market	Simple debug	Multiple flows with multiple points of failure	Advanced hardware debug support and software modeling capabilities

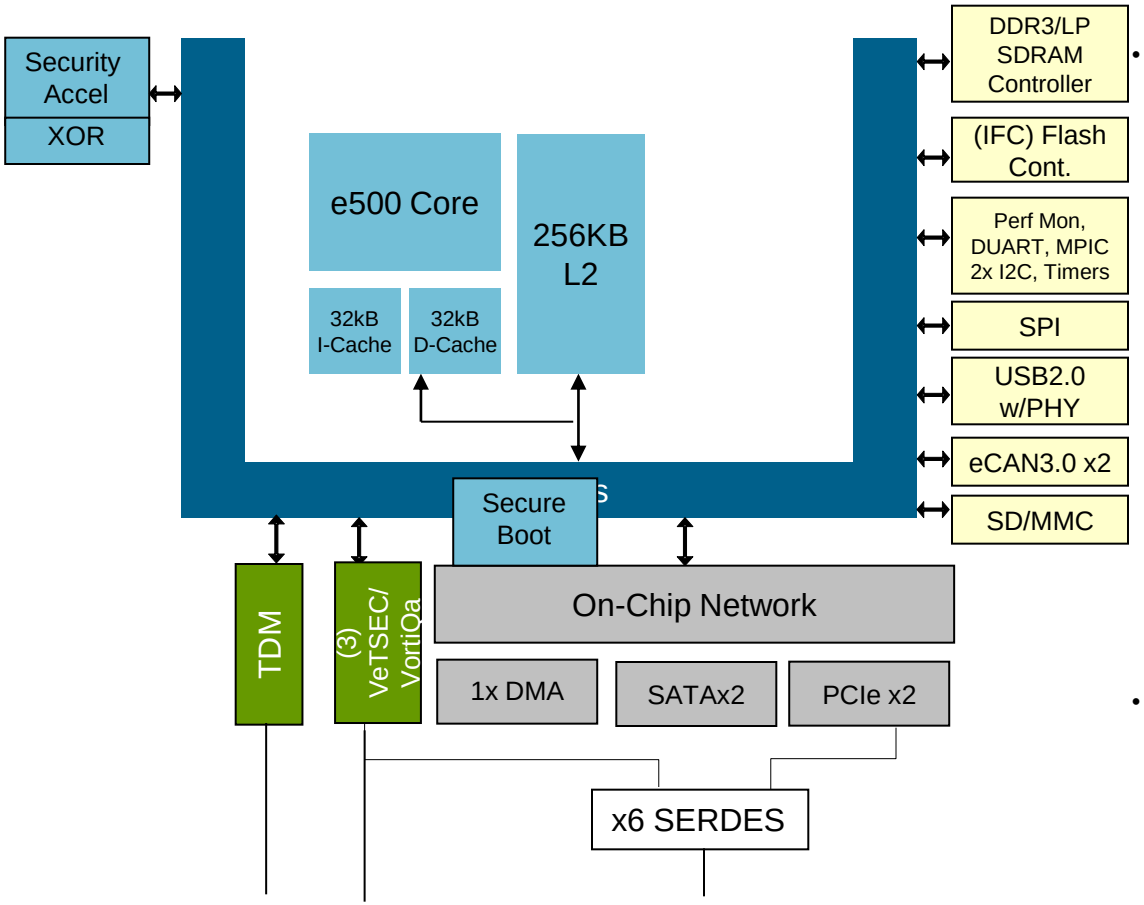
QorIQ part numbering



P1 Platform Part numbers

Dual Core	Single Core
n/a	P1010
P1020 ⟶	P1011
P1021 ⟶	P1012
P1022 ⟶	P1013
n/a	P1014

QorIQ™ P1010 Block Diagram



- e500 v2dp, 533 - 800 MHz
  - 256KB Frontside L2 cache w/ECC, HW cache coherent
  - 36-44 bit physical addressing
- System Unit
  - 16/32-bit DDR3, 800 MHz data rate w/ECC
  - Integrated SEC 4.x Lite Security Engine with Secure Boot
  - Flash Controller supporting NOR, SLC and MLC based NAND devices
  - One USB 2.0Controllers Host/Device support with Integrated PHY
  - SD/MMC card controller supporting booting from Flash cards
  - VortiQa based data path acceleration with (3) 10/100/1000 Ethernet Controllers w/ Jumbo Frame support, SGMII interface, IEEE1588v2 Support
  - Two PCI Express 1.0a Controllers operating up to 2.5Gbps
  - Two SATA Controller, 3.0 Gb/S
  - Two eCAN3.0 Controllers
  - 4x UARTs, 2x I2Cs
- Process & Package
  - 45nm SOI
  - 425-pin TEPBGA I (19mmx19mm, 0.8mm pitch)
  - <3W power consumption

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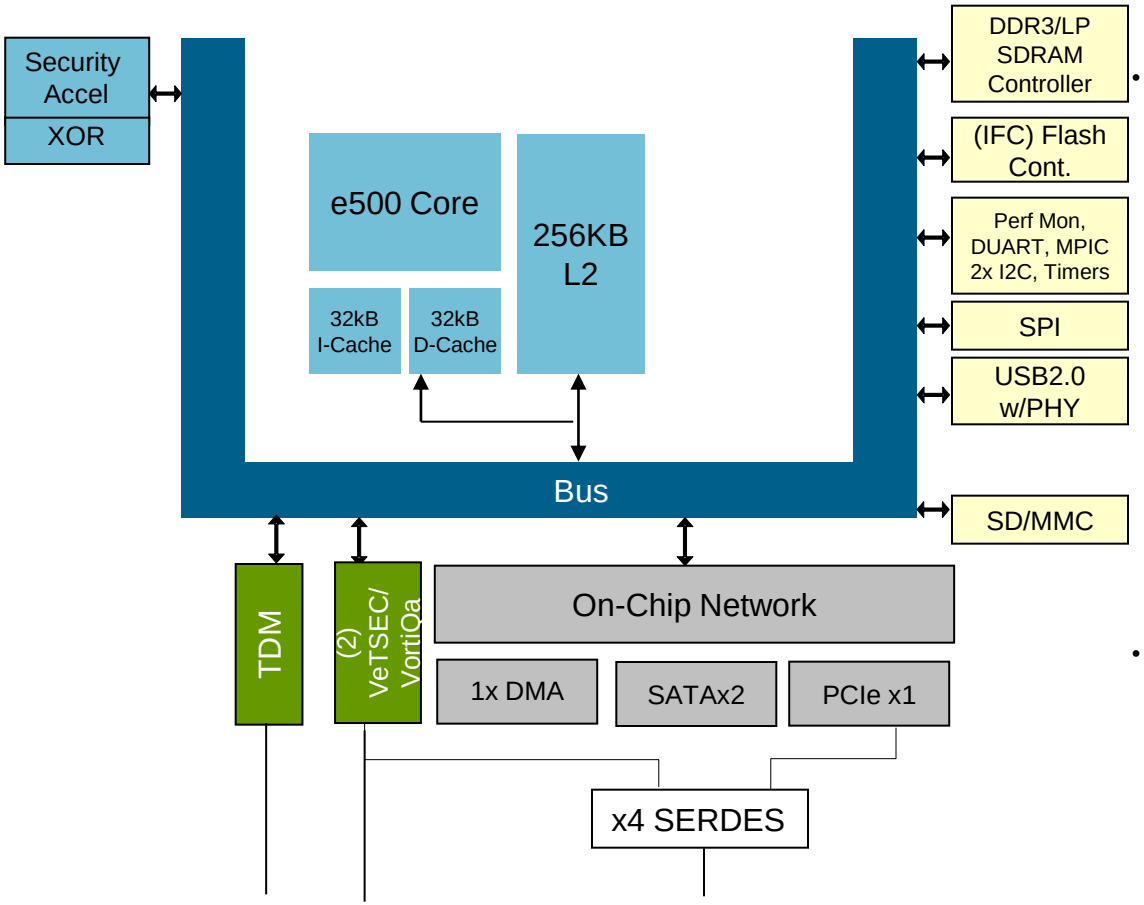
QorIQ™ P1014 Block Diagram



- e500 v2dp, 533 - 800 MHz
  - 256KB Frontside L2 cache w/ECC, HW cache coherent
  - 36-44 bit physical addressing
- System Unit
  - 16-bit DDR3, 800 MHz data rate w/ECC
  - Integrated SEC 4.x Lite Security Engine
  - Flash Controller supporting NOR, SLC and MLC based NAND devices
  - One USB 2.0Controllers Host/Device support with Integrated PHY
  - SD/MMC card controller supporting booting from Flash cards
  - VortiQa based data path acceleration with (2) 10/100/1000 Ethernet Controllers w/ Jumbo Frame support, IEEE1588v2 Support
  - One PCI Express 1.0a Controllers operating up to 2.5Gbps
  - Two SATA Controller, 3.0 Gb/S
  - 4x UARTs, 2x I2Cs
- Process & Package
  - 45nm SOI
  - 425-pin TEPBGA I (19mmx19mm, 0.8mm pitch)
  - <3W power consumption

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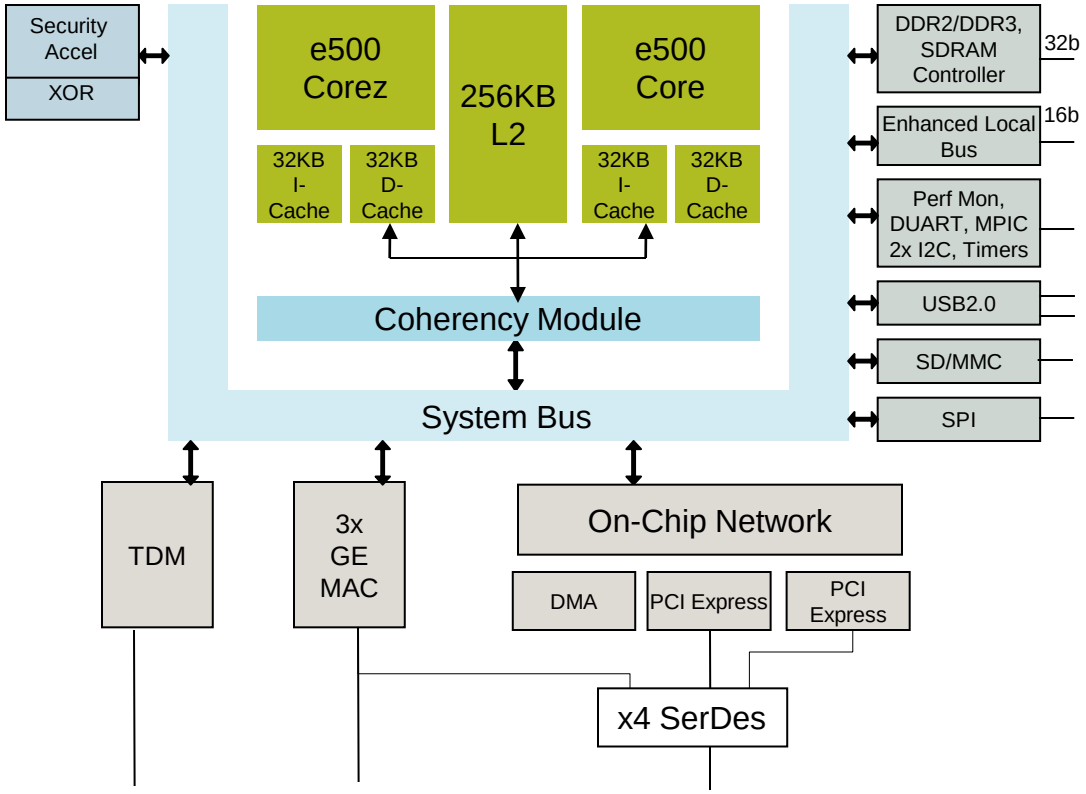
Dual-Core P1020



Samples Q1-10, Qualification Q4-10

Top speed bin probably 667MHz for extended temp.
VOIP for P1020 family will be provided by D2

- Dual e500 Power Architecture™ core
  - 533 – 800 MHz
  - 256KB Frontside L2 cache w/ECC, HW cache coherent
  - 36 bit physical addressing, DP-FPU
- System Unit
  - 32-bit DDR2/DDR3 with ECC to 800MHz datarate
  - Integrated SEC 3.3 Security Engine
  - Open-PIC Interrupt Controller, Perf Mon, 2x I2C, Timers, 16 GPIO's, DUART
  - 16-bit Enhanced Local Bus supports booting from NAND Flash
  - Two USB 2.0Controllers Host/Device support
  - SPI controller supporting booting from SPI serial Flash
  - SD/MMC card controller supporting booting from Flash cards
  - TDM interface
  - Three 10/100/1000 Ethernet Controllers (eTSEC) w/ Jumbo Frame support, SGMII interface
    - Enhanced features: Parser/Filer, QOS, IP-Checksum Offload, Lossless Flow Control
    - IEEE1588v2 Support
  - Two PCI Express 1.0a Controllers operating at 2.5GHz
  - Power Management
- Process & Package
  - 45nm SOI, XX +/- XX, 0C to 125C Tj
    - with -40C to 125C Tj option
  - 689-pin TePBGAII, 31x31mm
- 5.2W Max at 800MHz

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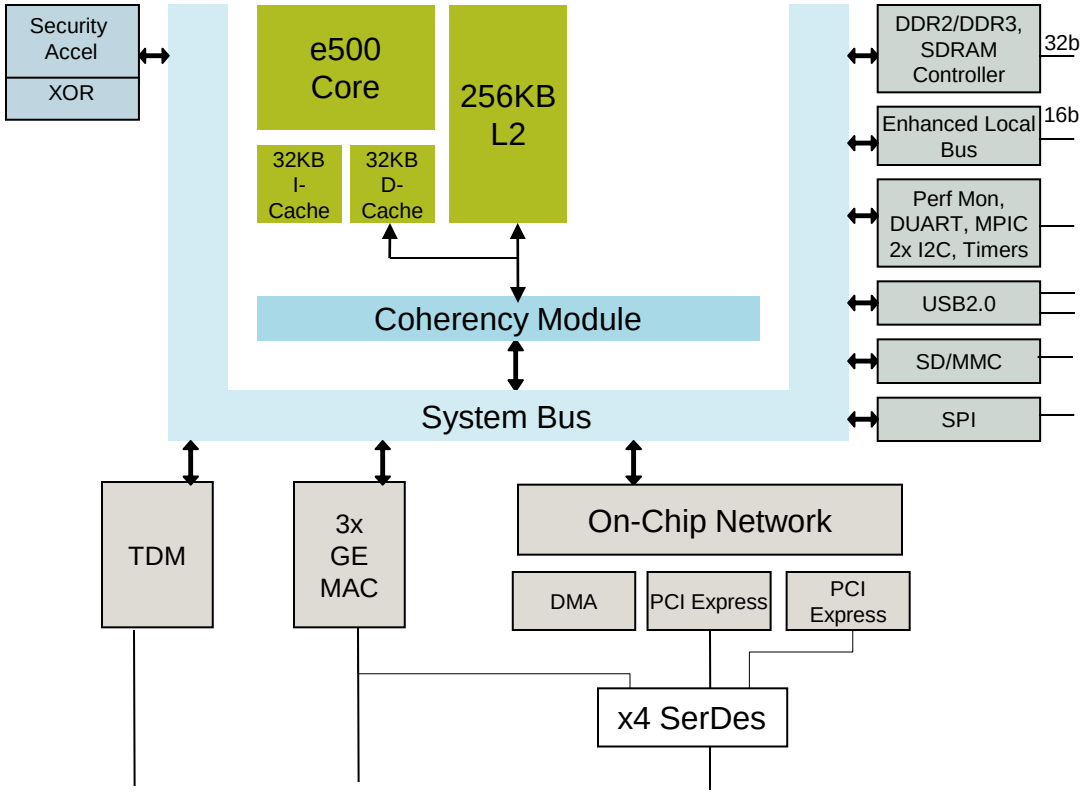
Single-Core P1011



Samples Q1-10, Qualification Q4-10

- Single e500 Power Architecture™ core
  - 533 – 800 MHz
  - 256KB Frontside L2 cache w/ECC, HW cache coherent
  - 36 bit physical addressing, DP-FPU
- System Unit
  - 32-bit DDR2/DDR3 with ECC
  - Integrated SEC 3.3 Security Engine
  - Open-PIC Interrupt Controller, Perf Mon, 2x I2C, Timers, 16 GPIO's, DUART
  - 16-bit Enhanced Local Bus supports booting from NAND Flash
  - Two USB 2.0 Controllers Host/Device support
  - SPI controller supporting booting from SPI serial Flash
  - SD/MMC card controller supporting booting from Flash cards
  - TDM Interface
  - Three 10/100/1000 Ethernet Controllers (eTSEC) w/ Jumbo Frame support, SGMII interface
    - Enhanced features: Parser/Filer, QOS, IP-Checksum Offload, Lossless Flow Control
    - IEEE1588v2 Support
  - Two PCI Express 1.0a Controllers operating at 2.5Gbps
  - Power Management
- Process & Package
  - 45nm SOI, XX +/- XX, 0C to 125C Tj
    - with -40C to 125C Tj option
  - 689-pin TePBGAII, 31x31mm
- 4.5W Max at 800MHz

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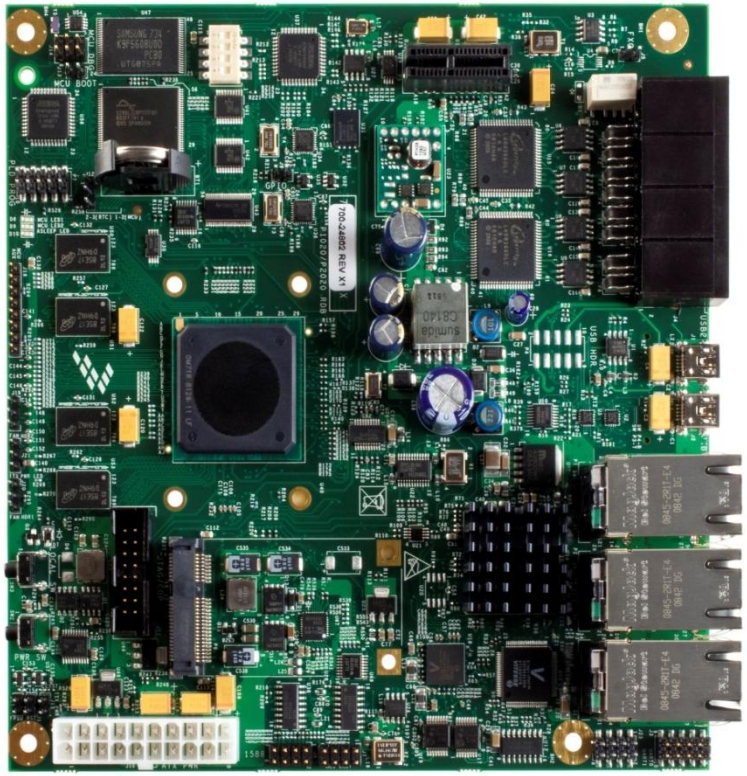
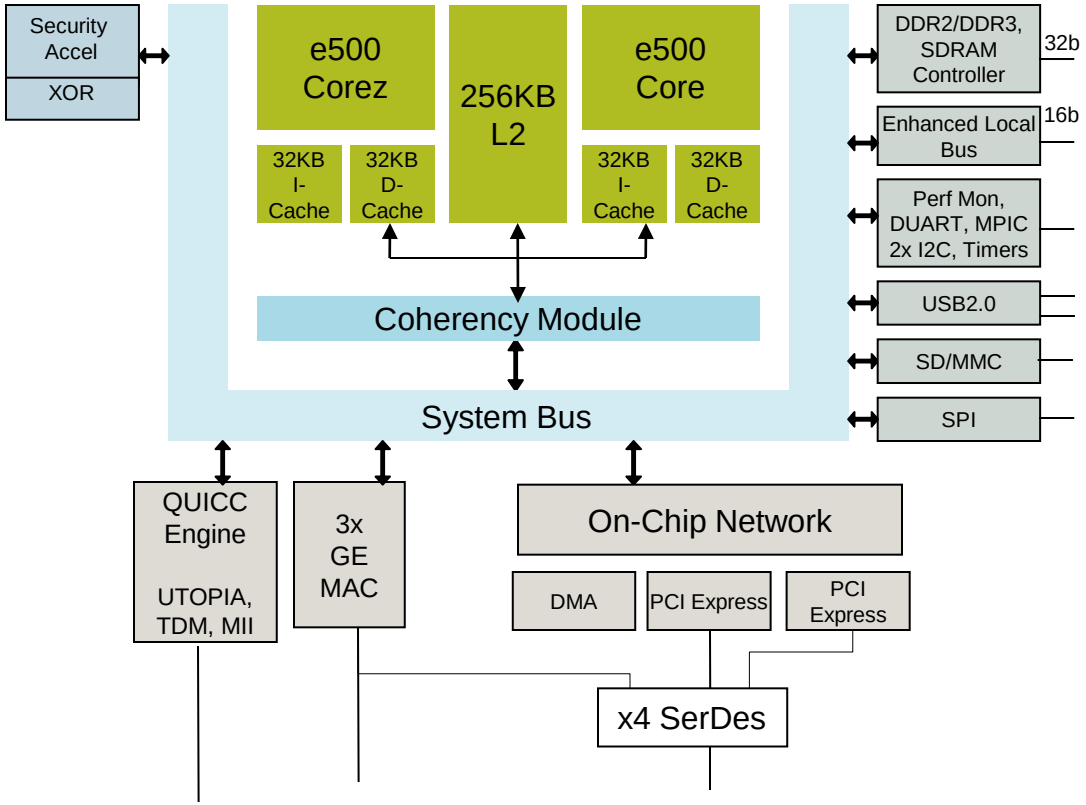
P1020 Enablement Deliverables

- **Customer Reference Design Board "RDB" that supports both P1020 and P2020 Silicon**
  - P1020 at 800 MHz
  - 32 Bits DDR2 at 667MHz data rate for P1020
  - Triple GigE supporting RGMII and SGMII
  - PCI-E x2
  - USB 2.0 for High/Full speed
  - NOR/NAND flash
  - SD/MMC Connector
  - TDM Interface with SLIC/SLAC
- **Freescale S/W**
  - Linux, U-boot, and CodeWarrior support
- **3Rd Party Tools S/W**
  - VxWorks, Green Hills, QNX & MontaVista Linux
- **3Rd Party S/W**
  - D2 Technology for VoIP solution
  - Arada for WLAN support
  - **Vortiqa for SMB solution**
- **Benchmarking**
  - Pre-silicon benchmark for VeTSEC
  - Core Benchmark (EEMBC, Dhrystone etc..)
  - SMP Optimization for IPV4, PCI-e,and IPSEC
- **Collaterals**
  - Migration Apps note form e300 to e500
  - Design Checklist
  - IBIS, BSDL & SWIFT Model
  - RDB Platform documentation
  - Training materials



QorIQ™ P1021



- Dual e500 core; 533 - 800 MHz
  - 256KB Frontside L2 cache w/ECC, HW cache coherent
  - 36 bit physical addressing, DP-FPU
- System Unit
  - 32-bit DDR2/DDR3, 800 MHz data rate w/ECC
  - Integrated SEC 3.3 Security Engine
  - Open-PIC Interrupt Controller, Perf Mon, 2x I2C, Timers, 16 GPIO's, DUART
  - 16-bit Enhanced Local Bus supports booting from NAND Flash
  - USB 2.0Controllers Host/Device support
  - SPI controller supporting booting from SPI serial Flash
  - SD/MMC card controller supporting booting from Flash cards
  - Three 10/100/1000 Ethernet Controllers (eTSEC) w/ Jumbo Frame support, SGMII interface
    - IEEE1588v2 Support
  - QUICC Engine for protocol off load and legacy interfaces
    - TDM interfaces with HDLC support
    - UTOPIA-L2 interface for ATM support
  - Two PCI Express 1.0a Controllers operating up to 2.5Gbps
  - Power Management
- Process & Package
  - 45nm SOI, 0.95V+/-50mV, -40C to 125C Tj
  - 689-pin TePBGAII
- 5.2W Max at 800MHz

BACK

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P1021/P1012 QUICC Engine Feature Overview

- Protocols and Interfaces
  - ATM
  - Serial ATM
  - HDLC/Transparent (bit rate up to 70Mbps)
  - HDLC BUS (bit rate up to 10Mbps)
  - Asynchronous HDLC (bit rate up to 2Mbps)
  - UART
  - BISYNC (bit rate up to 2Mbps)
  - Two TDM interface supporting 64 multichannel, each running at 64Kbps
  - Up to two 10/100Mbps Fast Ethernet via RMII / MII
- ATM Controller
  - Full duplex Segmentation And Reassembly (SAR)
  - AAL5, AAL0 protocols TM4.1, CBR, VBR, UBR, UBR+ traffic types
  - 64K external connections
  - Inverse Multiplexing ATM capability (IMA)
  - ITU-T I.610 based OAM handling
  - One UTOPIA-L2, 8-bit interface (no MPHY support)
- Time Slot Assigner and two TDM Interfaces
  - Independent Rx and Tx routing RAM with 512 routing entries each
  - Time slot assigner with bit or byte resolution

P1021 Enablement Deliverables

- **Customer Modular Design System Board "MDS"**
  - P1021 at 800 MHz
  - 32 Bits DDR3 at 800MHz date rate
  - Triple GigE supporting GMII and SGMII
  - PCI-E x2
  - USB 2.0 for High/Full speed
  - NOR/NAND flash
  - SD/MMC Connector
  - TDM Interface with SLIC/SLAC
  - QE Interface:
    - UTOPIA
    - T1/E1 Framers
    - Two 10/100 MII Ethernet I/F
- **Freescale S/W**
  - Linux, U-boot, and CodeWarrior support
  - CW Utilities drivers support (Bare-board drivers)
- **3Rd Party Tools S/W**
  - VxWorks
  - Green Hills
  - MontaVista
- **Benchmarking**
  - QE based use cases for ATM and TDM.
- **Collaterals**
  - MDS Platform documentation
  - Training materials

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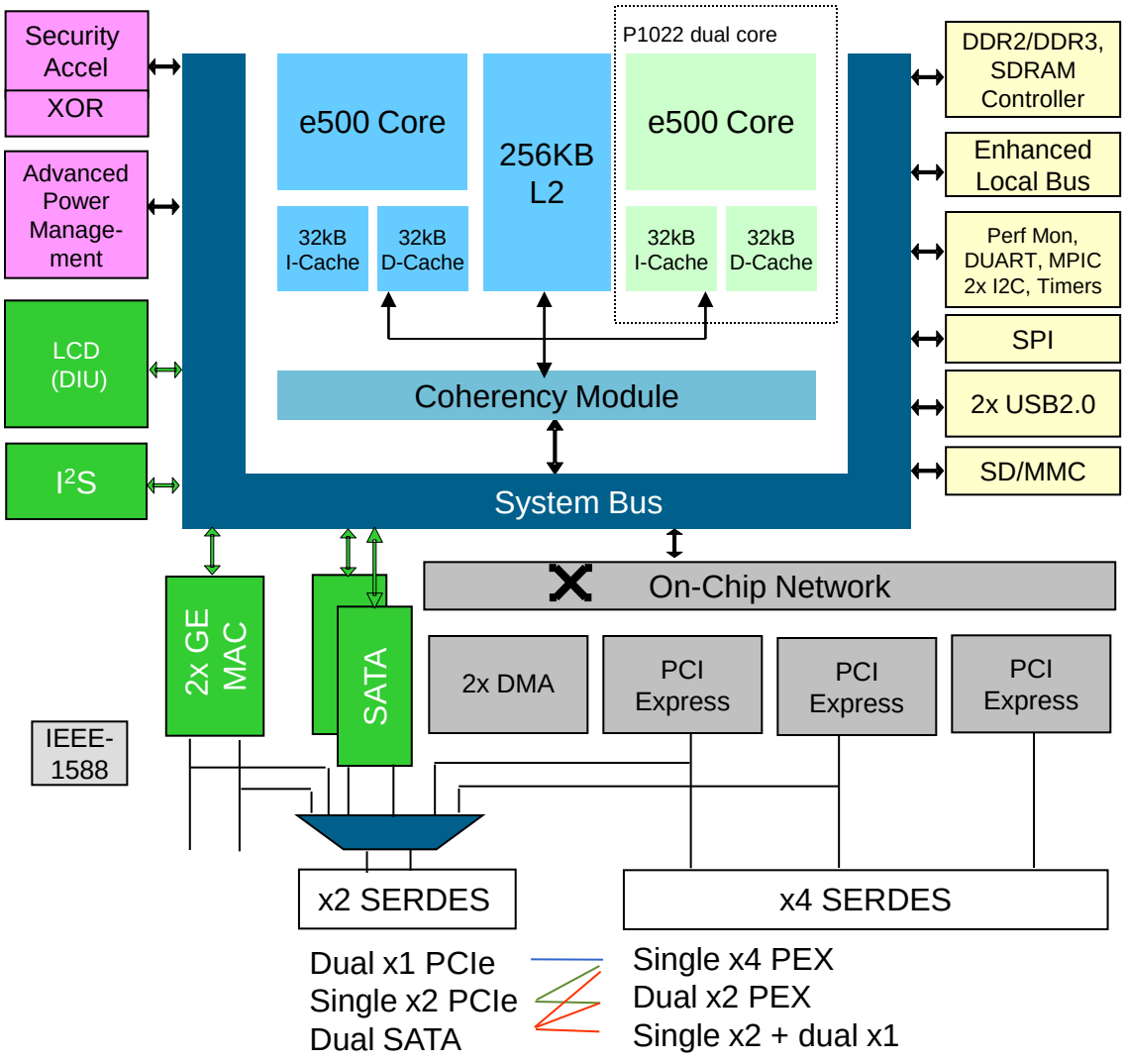
P1022/13 Block Diagram



- Scalable performance for Media Application Processing
  - Up to 1.0GHz operation
  - High Speed DDR2 and DDR3 (800MHz)
  - HW math and secure networking acceleration
- Integrated system peripherals
  - Dual USB 2.0 (No PHY req'd)
  - SD/MMC
  - SATA
  - Gigabit Ethernet
  - LCD
  - Low cost PCB layout
- Open Standard High Speed Serial Interconnect
  - 3 PCI Express Controller
    - 6 lanes
  - High Speed SPI, SGMII, I2S
- Green Operation
  - Low power fanless dynamic operation = <4W typical at dual core 800MHz
  - Advanced Power Management
  - Split power planes for power-down deep-sleep operation for EnergyStar™ support
  - Programmable wake-on-packet
  - <300mW deep Sleep @35C
- Process & Package
  - 45nm, 1.0V+/-50mV, 0C-105C Tj
  - TePBGAII

Key Values for P1022/13

High Performance PowerQuicc™ III Processor with advanced energy management for green embedded processing with system level integration

High Performance

Scalable Single and Dual Core Processing & High Speed Interconnect

Core Performance
- 500MHz to 1.0GHz e500v2 cores

HW Acceleration
- 64 bit SIMD
- DP Floating Point
- Security Acceleration

Memory
- 256KB L2 Cache
- DDR 2/3 Memory interface

High Speed Interconnect
- Triple PCI Express
- eLocal Bus

Low System Cost

System Peripheral Integration

Cost saving through Integration
- GbE
- USB 2.0
- SD/MMC
- SPI
- LCD
- IEEE1588
- SATA
- DUART
- I2C

Low Cost PCB
- Routable in 4 signal layers

Low Cost Boot Modes
- NAND Flash
- High speed serial Flash
- Removable SD/MMC

Energy Efficiency

Best in Class Power/Energy Efficiency

Low Power
- 0.95V Operation
- Fanless in many applications
- @4W typical at 800MHz
- @ 200mW Deepsleep

Advanced Energy Management
- Run and Jog active modes
- Packet-lossless Deepsleep
- Programmable wake-on-packet filter
- JOG mode

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P1022 Deep Sleep Details

- While in Deep Sleep
  - DDR mostly in self-refresh
    - Exits self-refresh when packets must be written to DDR
    - DDR IOs powered but tri-stated, termination isolated
  - Ethernet controller Rx filer classifies inbound packet types
    - Uninteresting packets dropped
      - Network management, etc
    - Packets type of interest to printer but do not cause wake-up are written to DDR

- Deep Sleep is exited when a wake-up event occurs
  - Ethernet controller Rx filer classifies an inbound packet type as immediate wake-up
    - Wake-on-LAN (i.e. magic packet)
    - TCP packet targeting printer
      - TCP SYN packet that starts print job
      - Proprietary status requests
    - User definable
  - Rx timer expiration
    - Special timer begins counting only after an inbound packet is written to memory
      - Dropped packets do not start counter
      - Keeps SoC in Deep Sleep longer in lightly loaded networks
    - Causes wake-up to respond to accumulated inbound requests
      - ARP Request (“Who has…, Tell…”)
      - ICMP Ping Request
      - SNMP get-request
  - Tx timer expiration
    - Causes wake-up to issue printer initiated traffic such as network keep alive messages
      - ARP Request (Presumably keep-alives)
      - ARP Response (“xx.xx.xx.xx is at xxx”)
      - ICMP Ping Response
      - SNMP get-response
      - NETBIOS (Presumably keep-alives)

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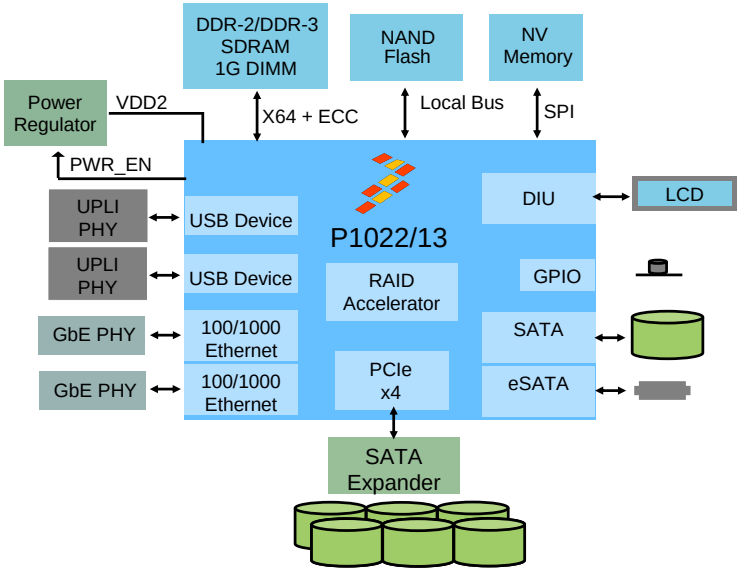
P1022/13E Target Applications (Storage)

Target Market

Storage Centric	Apps	Key Feature / Benefits
NAS Security DVR Media Server	 Network Attached Storage  Network DVR  Media Player/Server	Scalable High Speed Dataplane processing High Speed Line Rate GbE Networking High Speed Memory Advanced Energy Management Low power fanless operation Broad range of 3rd party embedded OS supported Integrated SATA and RAID Acceleration Low BOM Cost

Usage Block Diagram



Required Enablement

- Low cost development system
- 60MB/s IOZone performance benchmark
- Mulit-bay storage reference design
- 3rd Party Optimized Storage Stack Supplier
- Storage optimized Linux BSP
- Optimized Storage Applications
  - •DLNA
  - •JAVA
  - •Streaming server
- HW Video Codec Partner
- ODM supplier partner
- Demo Applications
- Power management reference drivers

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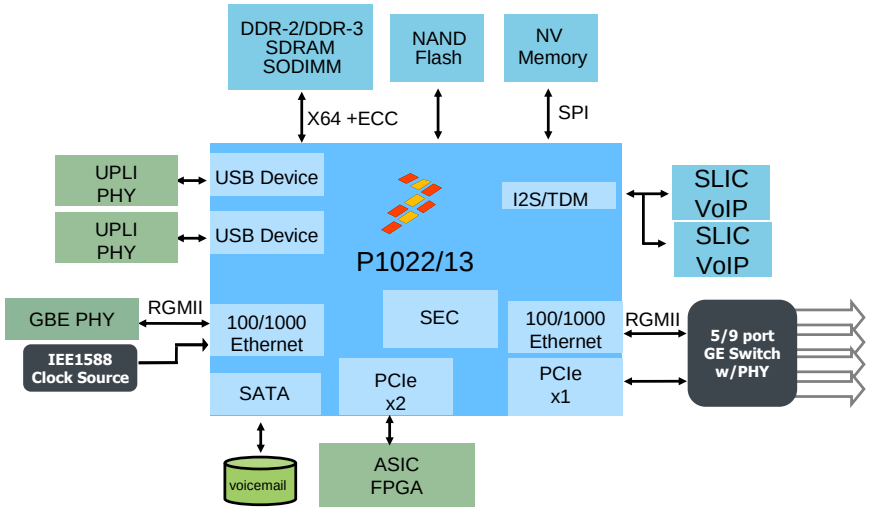
P1022/13E Target Applications (Communications)

Target Market

Communications	Apps	Key Feature / Benefits
Router Line Card Controller Wireless Access Point Access controller VPN Appliance	 Wireless AP  SMB Router  Linecard Controller  IP-PBX	Scalable High Speed Control plane processing High Speed Line Rate GbE Networking Secure Networking Low power fanless operation Broad range of 3rd party embedded OS supported Integrated SATA and RAID Acceleration Long product life-cycles

Usage Block Diagram



Required Enablement

- Reuse of existing PQ3 eco-system
- Networking Benchmarks
- Network optimized
- VoIP codec on e500v2
- Optimized Security Stack
- 802.11n driver support
- IEEE 1588 Stack – Open Source and 3rd party

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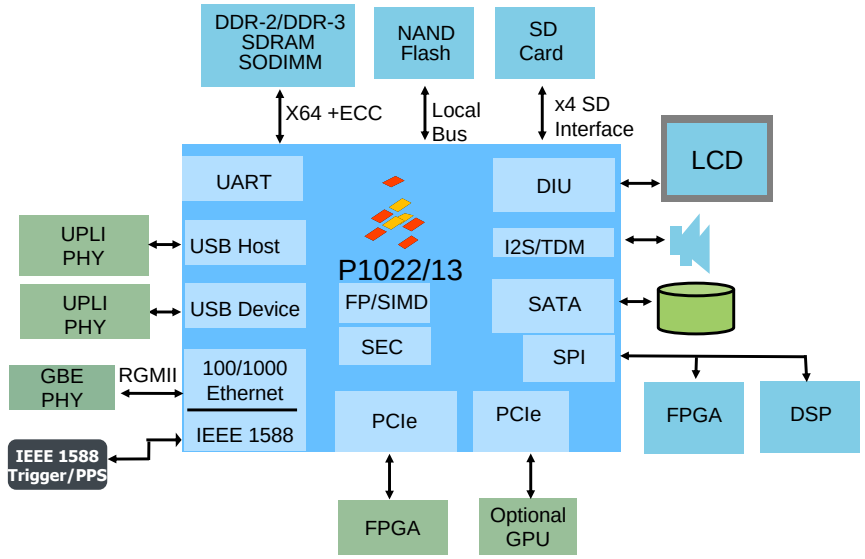
P1022/13E Target Applications (Industrial)

Target Market

Industrial	Apps	Key Feature / Benefits
Test and Measurement Instrumentation controller EPOS Mil/Aerospace Digital Signage/Gaming Medical Instrument		Low power high performance CPU HW DP Floating Point Integrated SIMD co-processor UI support through LCD controller or PCI Express interconnect to GPU and FPGA Advance energy management for EnergyStar Long product life-cycles Broad range of 3rd party embedded OS supported

Usage Block Diagram



Required Enablement

- Low Cost ComExpress Dev System
- 3rd party Computer Board Suppliers
- Graphic Supported OS's
- Open GL ES support on Linux and VxWorks
- HW Embedded Floating Support on 3rd party OS
- HW Floating Point Math Libraries Creation
- IEEE 1588 Stack – Open Source and 3rd party
- Optimized Media Player Applications
  - •JAVA VM, Flash Player, HTML Brower
  - •SW Video Decode
  - •HW partner for HD Video Decode

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Product at a Glance – P1

	P1010	P1011	P1020	P1012	P1021	P1021	P1022	P1013
CPU	Single e500V2 533 - 800 MHz 32K I/D Cache	e500V2 Up to 800 MHz 32K I/D Cache	Dual e500V2 533 - 800 MHz 32K I/D Cache	e500V2 533 - 800 MHz 32K I/D Cache	Dual e500V2 533 - 800 MHz 32K I/D Cache	Single core e500V2 533 - 800 MHz 32K I/D Cache	Dual e500V2 533 - 1000 MHz 32K I/D Cache	e500V2 533 - 1000 MHz 32K I/D Cache
L2 Cache	256KB	256KB	256KB	256KB	256KB	256KB	256 KB	257 KB
FPU	36 Physical addressing and DP-FPU	36 Physical addressing and DP-FPU	36 Physical addressing and DP-FPU	36 Physical addressing and DP-FPU	36 Physical addressing and DP-FPU	36 Physical addressing and DP-FPU	36 Physical addressing and DP-FPU	36 Physical addressing and DP-FPU
DDR I/F Type/Width	DDR3, 16-32-bit	667 MHz DDR2/3 32-bit	667 MHz DDR2/3 32-bit	667 MHz DDR2/3 32-bit	667 MHz DDR2/3 32-bit	667 MHz DDR2/3 32-bit	DDR2/3, 32-bit	DDR2/3, 32-bit
DDR Speed (Max)	800 Mhz	800 MHz	800 MHz	800 MHz	800 MHz	800 MHz		
10/100/1000 Ethernet (with IEEE1588v2)	3 w/Jumbo Frame, SGMII	3 w/Jumbo Frame, SGMII	3 w/Jumbo Frame, SGMII	3 w/Jumbo Frame, SGMII	3 w/Jumbo Frame, SGMII	3 w/Jumbo Frame, SGMII	2 w/Jumbo Frame, SGMII	2 w/Jumbo Frame, SGMII
PCI-express	x2 PCIe	2 controllers w/ 4 SERDES	2 controllers w/ 4 SERDES	2 controllers w/ 4 SERDES	2 controllers w/ 4 SERDES	2 controllers w/ 4 SERDES	3 PCIe controllers w/ 6 SerDes	3 PCIe controllers w/ 6 SerDes
QUICC Engine				> TDM w/ HDLC > UTOPIA-LW for ATM	> TDM w/ HDLC > UTOPIA-LW for ATM	> TDM w/ HDLC > UTOPIA-LW for ATM		
USB2.0	Rev 2.0 w/phy	2 Host/Device	2 Host/Device	x1 Host/Device	x1 Host/Device	x1 Host/Device	2 Host/Device	2 Host/Device
SATA	3.0 Gb/s							
TDM	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Accelerators	SEC 4.X	SEC3.3	SEC3.3	SEC3.3	SEC3.3	SEC3.3	SEC3.3	SEC3.3
eCAN	2							
LCD							Yes	Yes
Power (Est Max)	<3.0W	4.5W	5.2W	5.2W	4.7	4.2	5.8	
Process Node	45 nm SOI	45 nm SOI	45 nm SOI	45 nm SOI	45 nm SOI	45 nm SOI	45 nm SOI	45 nm SOI
Package	388 PBGA	689-TePBGAII	689-TePBGAII	689-TePBGAII	689-TePBGAII	689-TePBGAII	689 TePGA	689 TePGA

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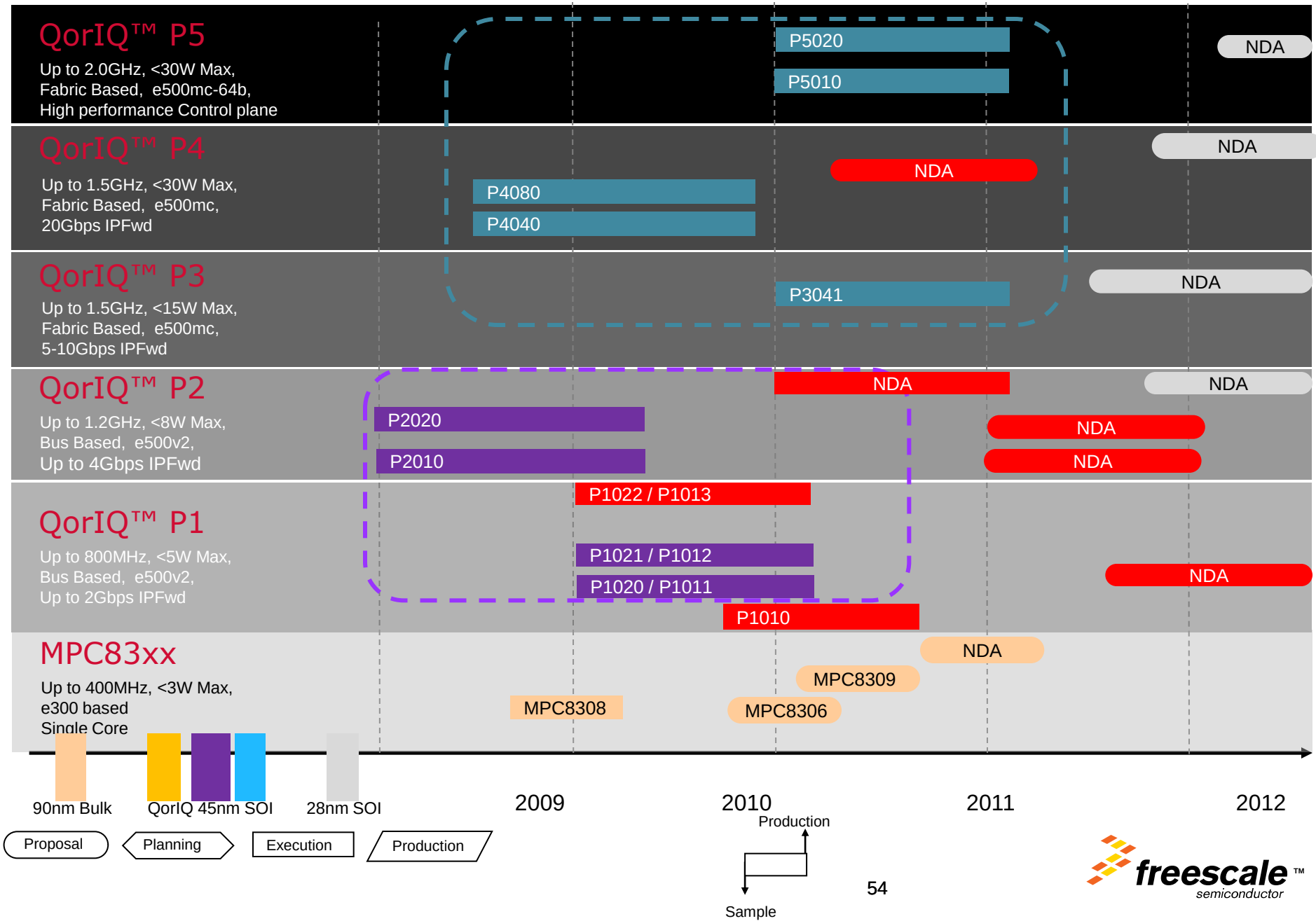
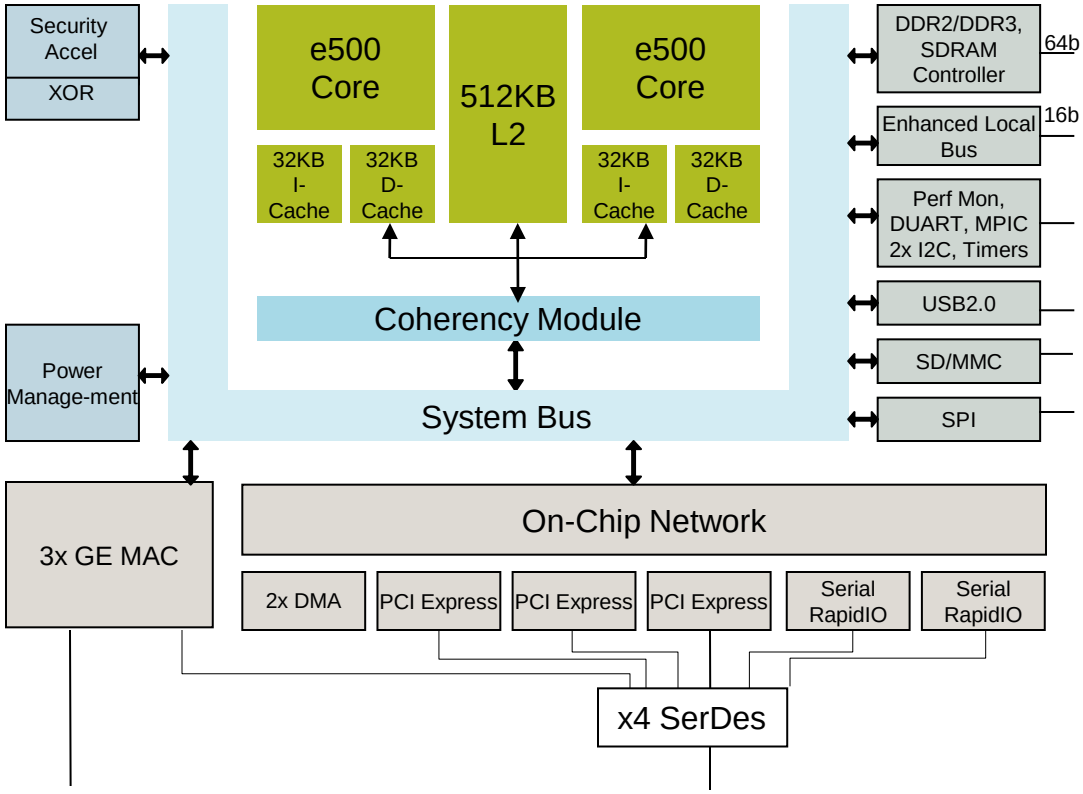
Power Architecture Processor Roadmap



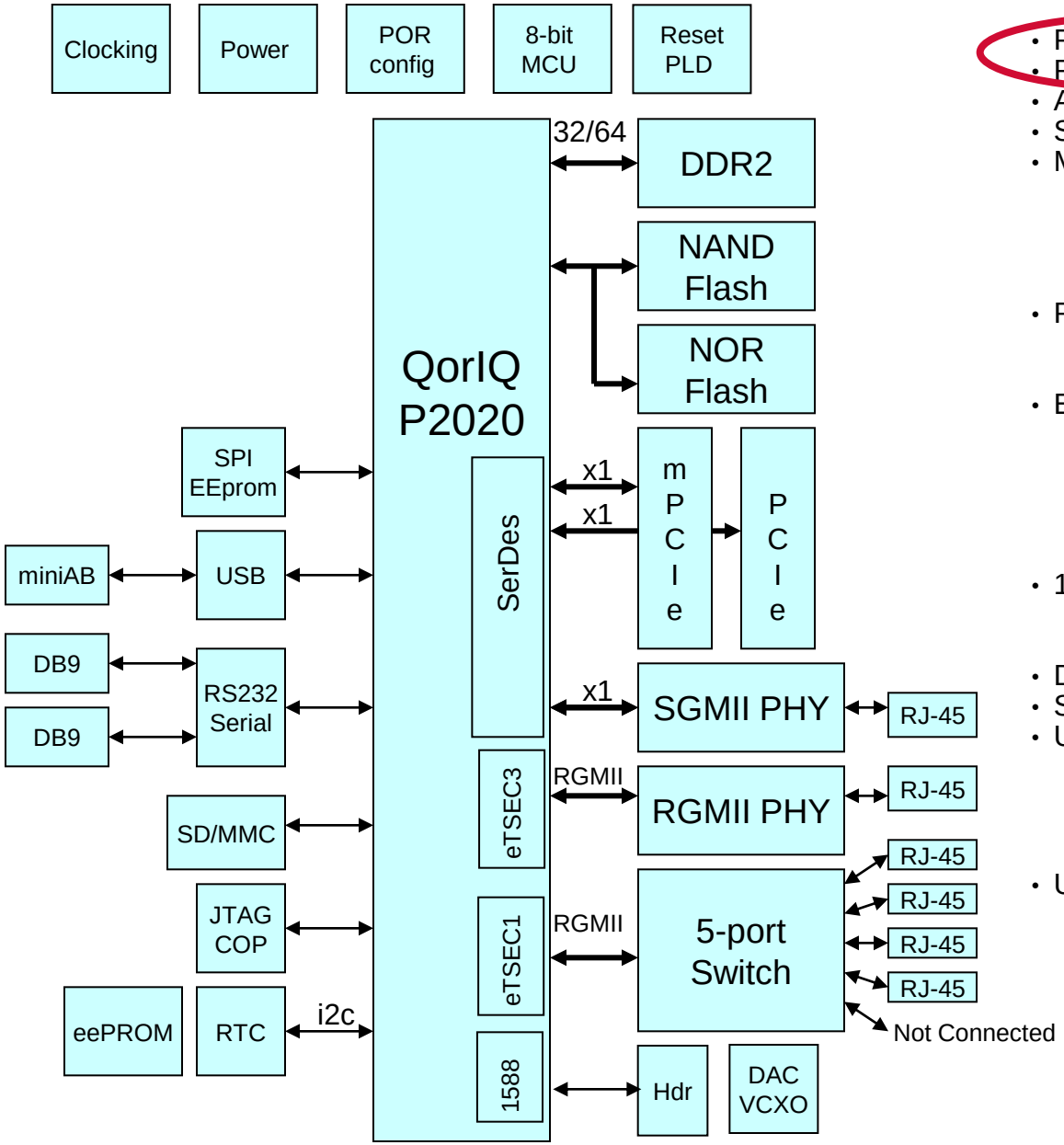
Dual-core P2020 Block Diagram



Samples May 09, Qualification Q3-10

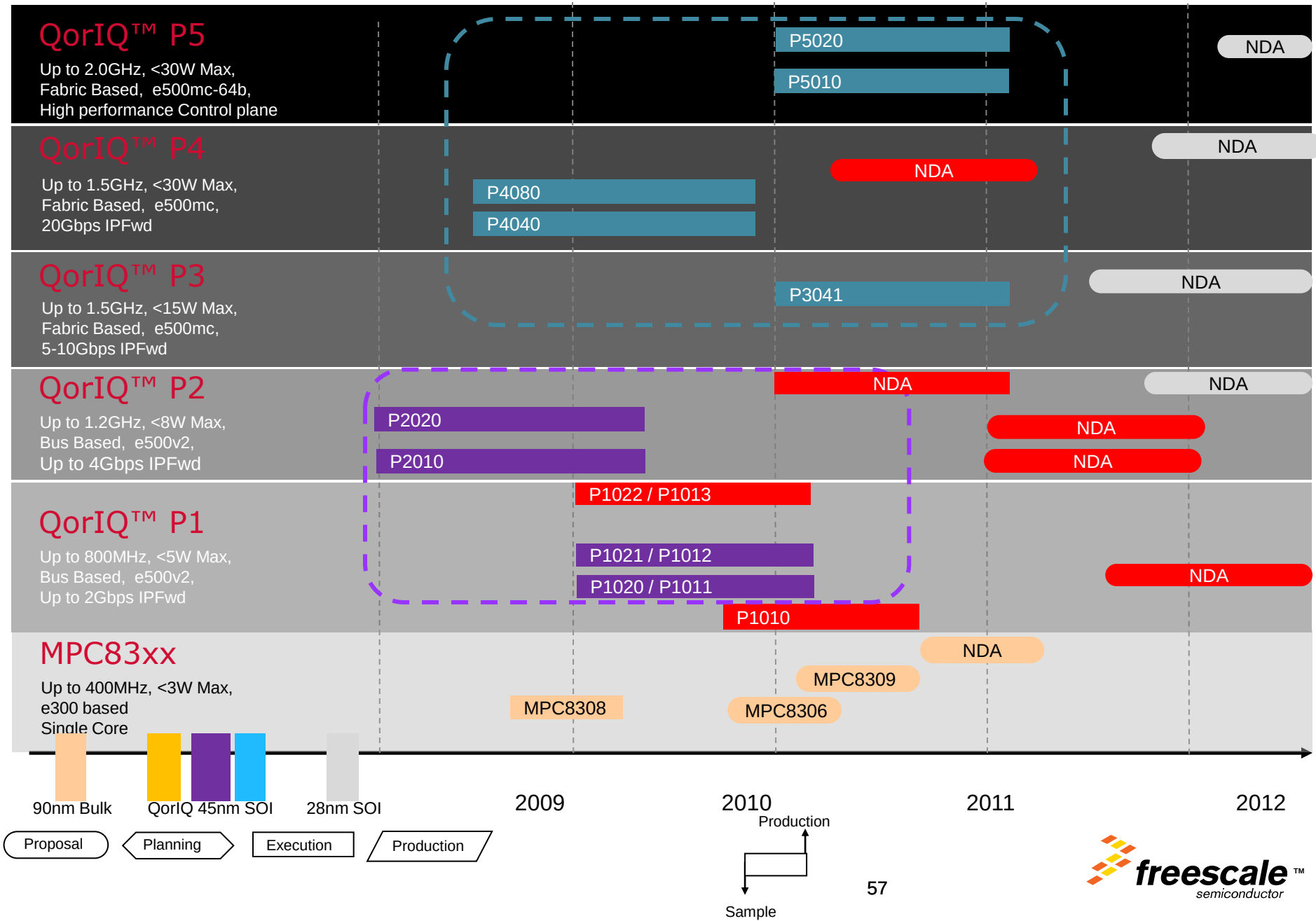
- Dual e500 Power Architecture™ core
  - 800 - 1200 MHz
  - 512KB Frontside L2 cache w/ECC, HW cache coherent
  - 36 bit physical addressing, DP-FPU
- System Unit
  - 64/32b DDR2/DDR3 with ECC to 800MHz datarate
  - Integrated SEC 3.1 Security Engine
  - Open-PIC Interrupt Controller, Perf Mon, 2x I2C, Timers, 16 GPIO's, DUART
  - 16-bit Enhanced Local Bus supports booting from NAND Flash
  - One USB 2.0 Host Controller with ULPI interface
  - SPI controller supporting booting from SPI serial Flash
  - SD/MMC card controller supporting booting from Flash cards
  - Three 10/100/1000 Ethernet Controllers (eTSEC) w/ Jumbo Frame support, SGMII interface
    - Enhanced features: Parser/Filer, QOS, IP-Checksum Offload, Lossless Flow Control
    - IEEE 1588v2 support
  - Two Serial Rapid I/O Controllers with integrated message unit operating up to 3.125GHz
  - Three PCI Express 1.0a Controllers operating at 2.5GHz
- Process & Package
  - 45nm SOI, 1.05V +/- 50mV, 0C to 125C Tj
    - with -40C to 125C Tj option
  - 689-pin TePBGAII, 31x31mm
- 8W Max at 1.2GHz

Mini-ITX Reference Design Board



- P/N: P2020RDB-PA
- Price: 595$
- Availability: Now
- SW: Linux BSP
- Memory
  - DDR2 – 1GB
  - NOR Flash – 16Mbyte (128Mbit device)
  - NAND Flash – 32MByte
  - SPI ROM – 16MByte
- PCIe
  - One standard PCIe connector (x1)
  - One mini PCIe connector (x1)
- Ethernet
  - Six 10/100/1000 ports as follows:
  - 4-ports from L2 switch connected to eTSEC1
  - 1 SGMII PHY connected to eTSEC2
  - 1 RGMII PHY connected to eTSEC3
- 1588
  - Clock input from DAC / VCXO circuitry
  - Accessible via test header
- Dual I2C
- SD/MMC card slot
- USB
  - Option #1 -Mini AB connectors on IO Panel (default)
  - Option #2 –Type A connectors (front panel)
- UARTs: Two DB9 connectors

Power Architecture Processor Roadmap



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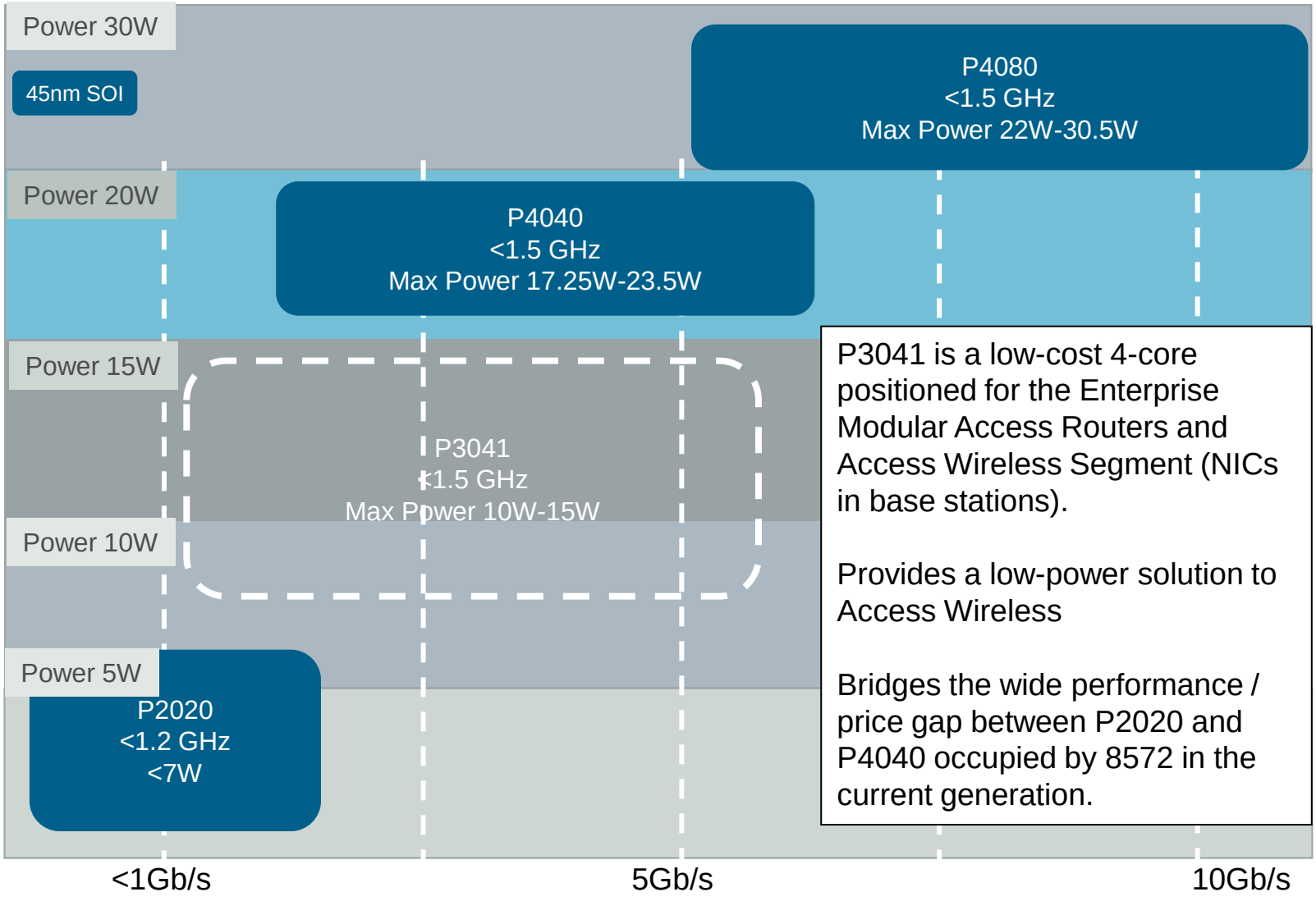
Multicore Solutions in 45nm



P3041 is a low-cost 4-core positioned for the Enterprise Modular Access Routers and Access Wireless Segment (NICs in base stations).

Provides a low-power solution to Access Wireless

Bridges the wide performance / price gap between P2020 and P4040 occupied by 8572 in the current generation.

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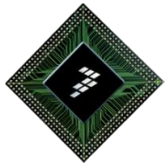
QorIQ™ P4080 Multicore News



It's a smarter approach to multicore. Freescale's Multicore Platform

►Innovative Multicore Microarchitecture for unprecedented computing efficiency, performance and scalability.

- On-chip coherency fabric
- Back-side cache per CPU core
- On-demand application acceleration

►Multicore Simulation Environment for accurate, fast code development and debugging.

- Fully tap the capabilities of the multicore platform
- Debug software not hardware
- Dynamic, real-time debug with non-intrusive capture

►45-nm Process Technology for industry-leading power-to-performance solution.

- Provides highest instructions-per-cycle (IPC) and frequency for given milliwatt/area

Introducing

- Eight e500mc cores
- CoreNet™ scales to 32 cores
- PCI Express® 2.0, 10GbE
- PME 2.0, SEC 4.0
- Data path acceleration
- Trust/secure boot
- Hypervisor
- Standardized debug
- Virtualization with real applications
- High-performance SoC
- Advanced technology
- Tier one partnerships
- Outstanding ecosystem

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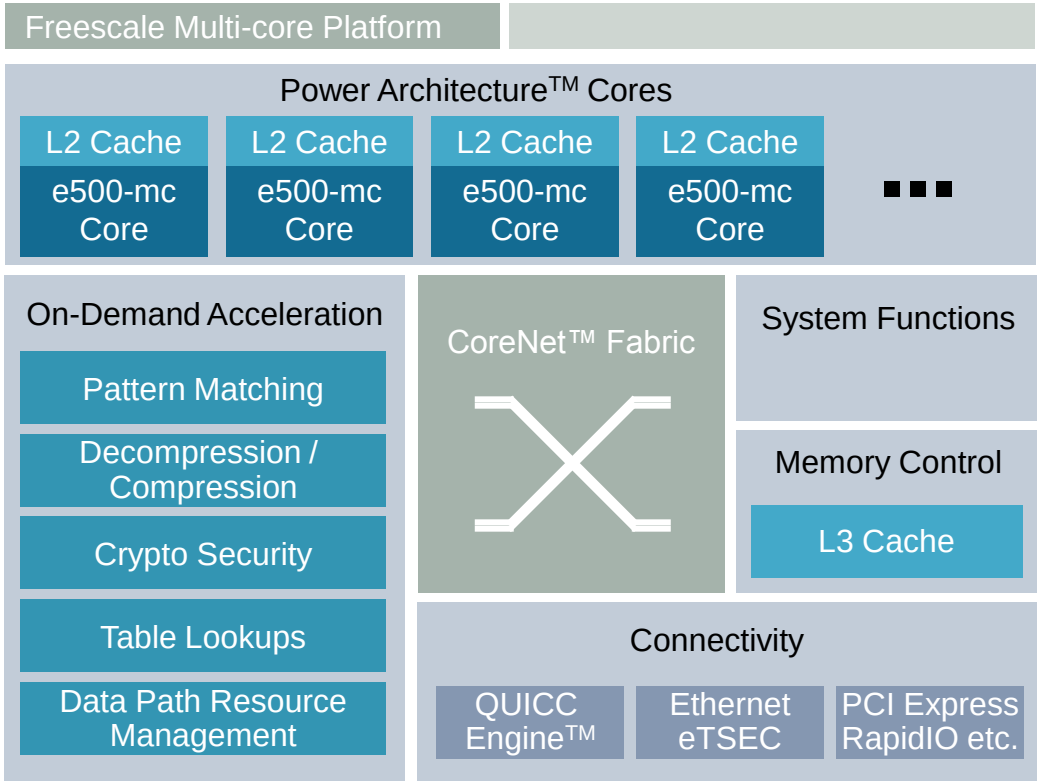
Freescale's Multicore Platform



- **►CoreNet™ Fabric for concurrent, non-blocking, hardware-based 100% cache-coherent platform connectivity**
  - **Eliminates shared bus contention and supports dramatically higher address issue bandwidth to "feed" multiple cores**
  - **Scales to support more than 32 cores**
  - **Can support heterogeneous cores**
- ►Tri-level Cache Hierarchy
  - Power Architecture™ cores with back-side L2 caches
  - Multiple L3 shared caches
  - Multiple memory controllers
- **►On-demand Application Acceleration**
  - **Offers performance advantages over pure core processing cycles, enables lower power implementations and reduces silicon area / cost**

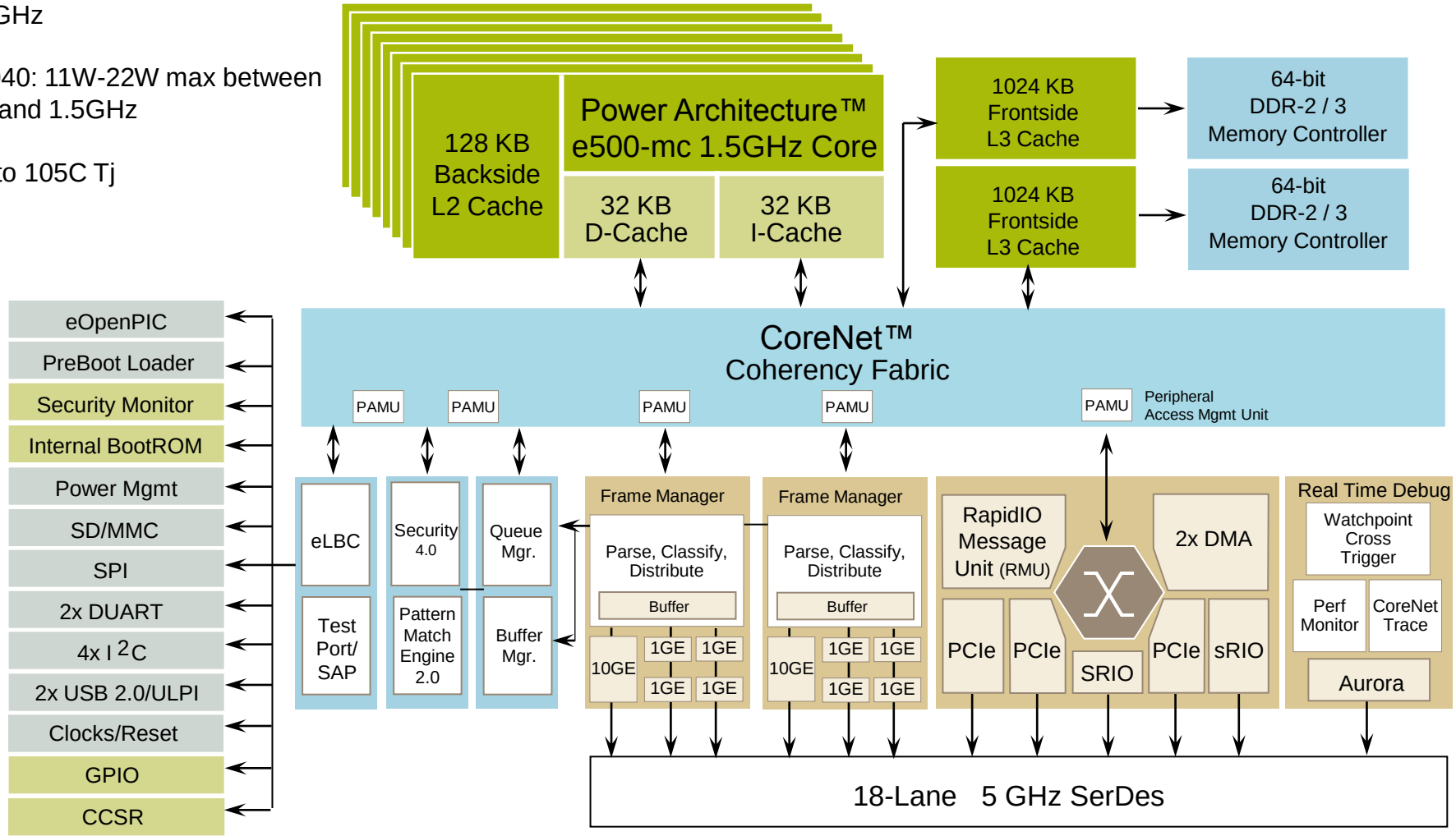
►Expected to enable 2-3 times improved system performance

QorIQ™ P4 Series P4080 Block Diagram

P4080: Under 30W max at 1.5GHz

P4040: 11W-22W max between 1.2 and 1.5GHz

0C to 105C Tj



4 core bondout called P4040. No other changes between P4080 and P4040.
3x PCIe Gen 2 controllers at 5GHz

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P4080 Designs in 2009


Military

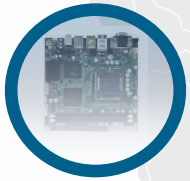

RNC


LTE eNB


Enterprise


Avionics

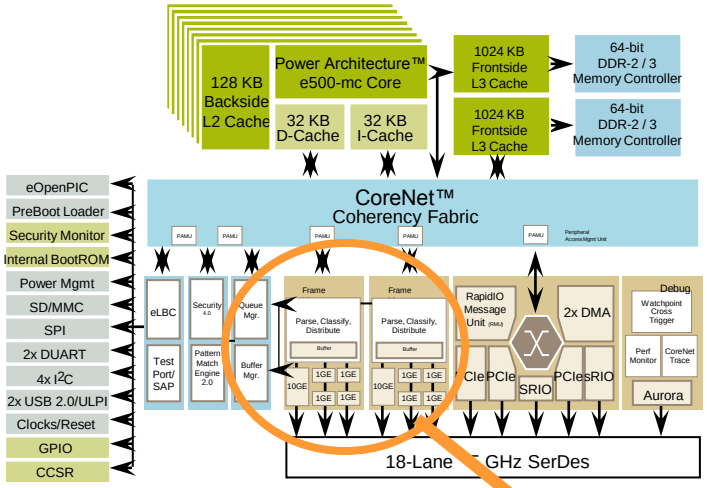

IPDSLAM


Industrial/Boards


WiMAX BTS


MGw

Data Path Acceleration Architecture - DPAA

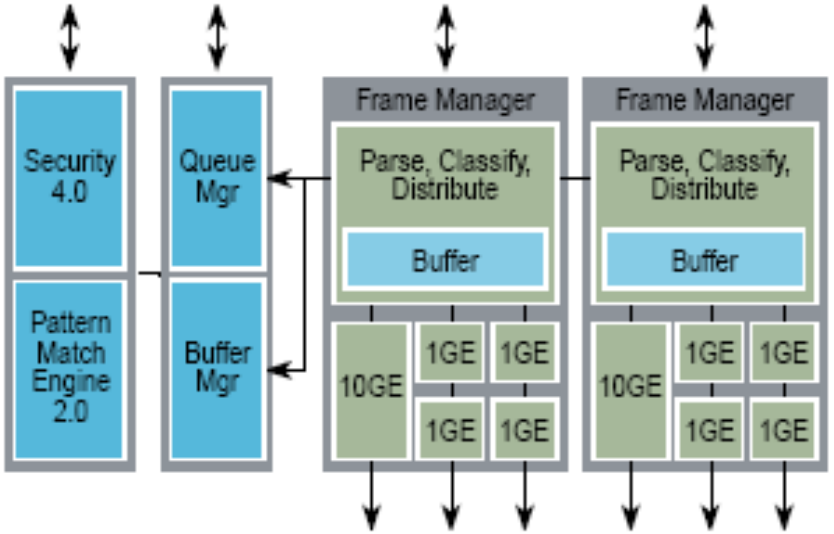


DPAA = Data Path Acceleration Architecture

Composed of:

FMan, SEC and PME for Packet processing offload acceleration Services

FMan, BMan and QMan for datapath generic services (the ''Infrastructure'')



- The purpose of the DPAA is to "make the cores work better"

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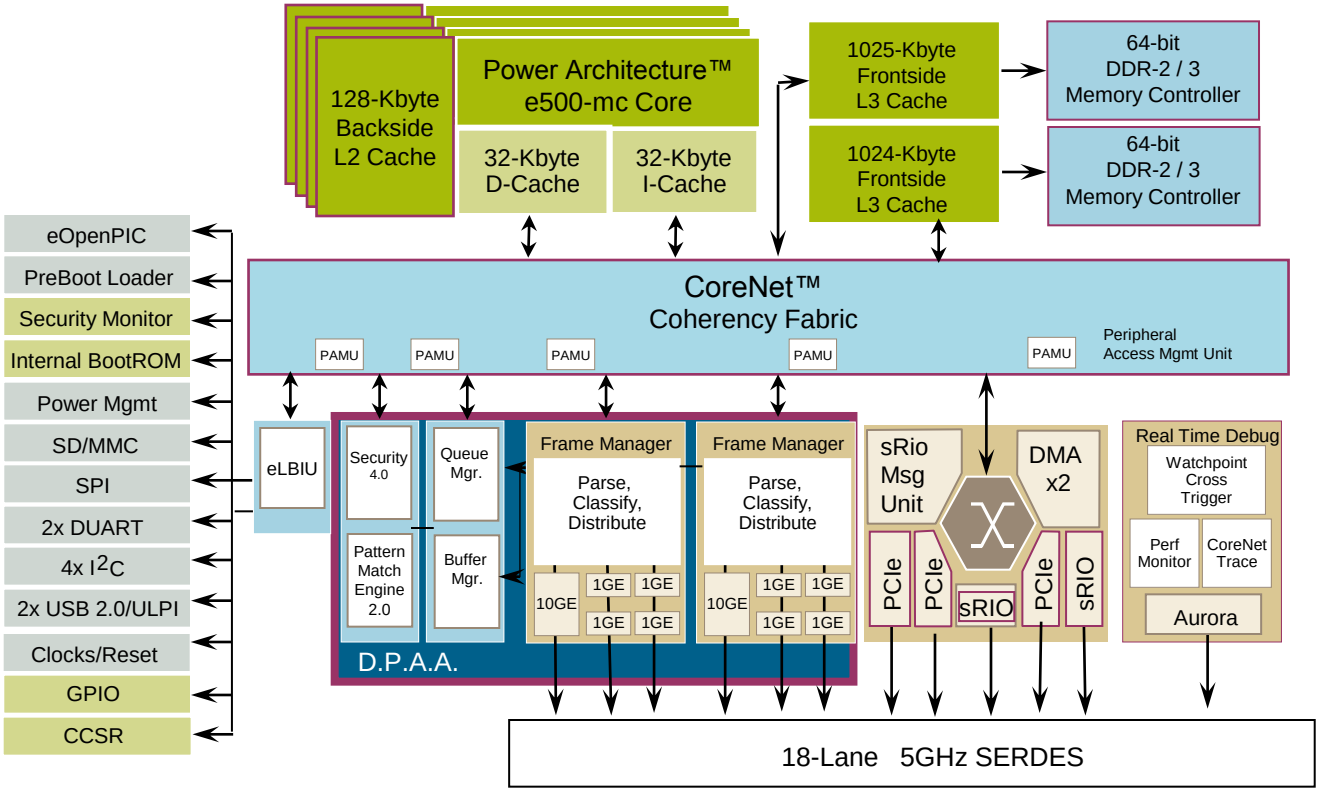
QorIQ™ P4 Series P4040 Block Diagram

Introducing

P4040
MULTICORE
PROCESSOR



- ▶Quad e500mc Power Architecture®
  - 4 cores (up to 1.5GHz)
  - Each with 128KB backside L2 cache
  - 2 MB Shared L3 Cache w/ECC
- ▶Memory Controller
  - DDR2/3 SDRAM up to 1.6 GHz
  - 32/64 bit data bus w/ECC
- ▶High Speed Interconnect
  - 3 PCIe 2.0 Controllers
  - 2 serial RapidIO Controllers
- ▶CoreNet™ Switch Fabric
- ▶Ethernet
  - 8 x 10/100/1000 Ethernet Controllers
  - 2 x 10GE Controllers
  - Classification/Policing, H/W Queuing, policing, and Buffer Management, Checksum Offload, QoS, Lossless Flow Control, IEEE 1588, SGMII/XAUI
- ▶Datapath Acceleration
- ▶Device
  - 45nm SOI Process
  - 1295-pin package, pin compat with P4080
  - 30-35% lower power than P4080

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P4080 and P4040 Estimated Power

P4080 Estimated Power

Power Designation	Tj	Pattern	Power (CPU/Platform/DDR MHz) [W] w/o IO		
			1500/800/1600	1333/667/1333	1200/600/1200
"Max" Power Supply Max	105°C	Contrived Sequence "Smoke Test"	28	24	20
"Typical" Thermal Max	105°C	Dhrystone	27	23	19
"Typical" Desktop Operation	65°C	Dhrystone	16	15	14

P4040 Estimated Power

Power Designation	Tj	Pattern	Power (CPU/Platform/DDR MHz) [W] w/o IO		
			1500/800/1600	1333/667/1333	1200/600/1200
"Max" Power Supply Max	105°C	Contrived Sequence "Smoke Test"	22	18.5	16
"Typical" Thermal Max	105°C	Dhrystone	20.5	17.5	15
"Typical" Desktop Operation	65°C	Dhrystone	13	12	11.5

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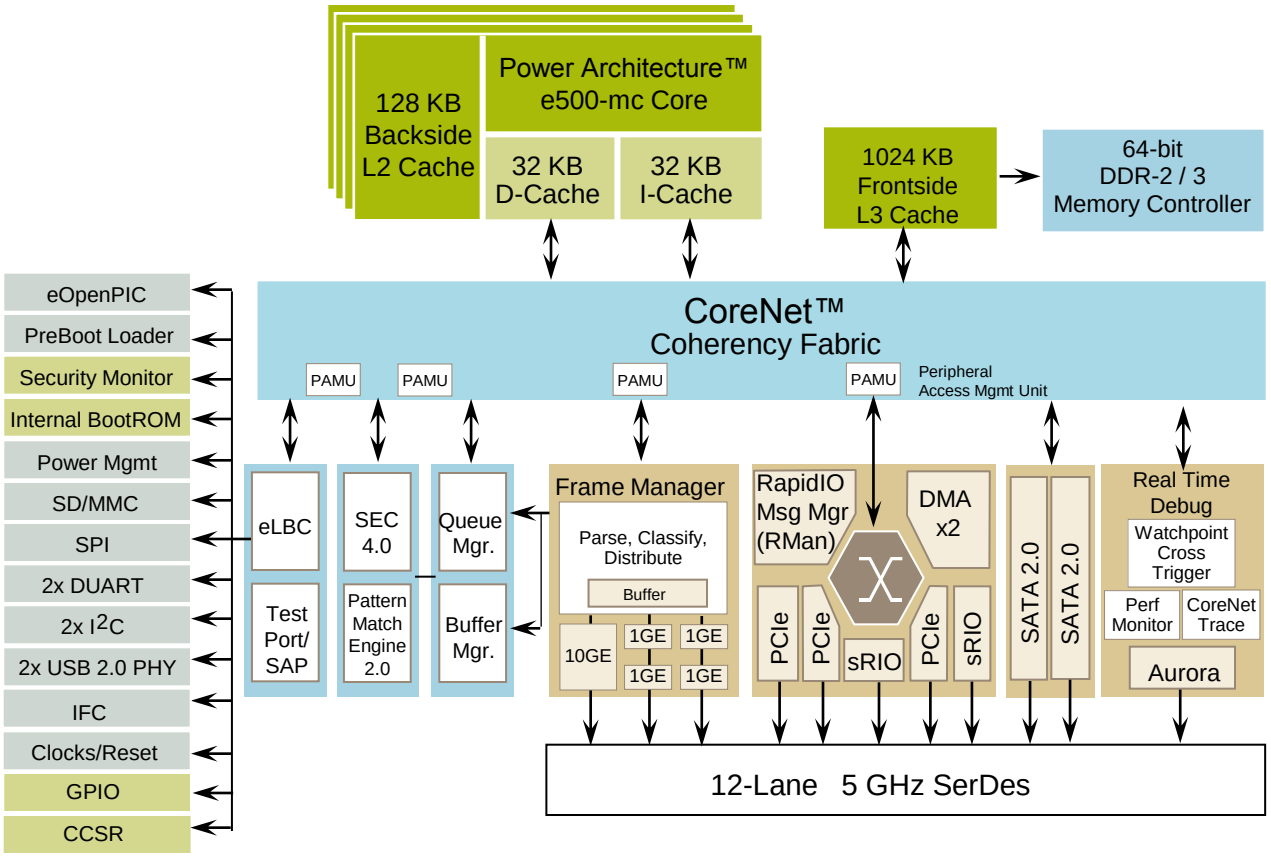
QorIQ™ P5, P4, and P3
Power Saving Clock Gating Capabilities

- Fine-grained clock gating is used throughout the CPU core and SoC platform
  - If a circuit is unused/idle during a particular clock cycle, it's clock is disabled in order to reduce the dynamic power
- Unused blocks can be disabled through software configuration, saving the dynamic power associated with each functional block
  - PCI Express
  - SRIO
  - Security block
  - PME
  - eLBC
  - DMA
  - DDR controllers
  - I2C
  - DUART
  - SERDES

P3041

0C to 105C Tj



- ▶Quad e500mc Power Architecture®
  - 4 cores (up to 1.5GHz)
  - Each with 128KB backside L2 cache
  - 1MB Shared L3 Cache w/ECC
- ▶Memory Controller
  - DDR2/3 SDRAM up to 1.3 GHz
  - 32/64 bit data bus w/ECC
- ▶High Speed Interconnect
  - 3 PCIe 2.0 Controllers
  - 2 sRapidIO 2.0 Controllers
  - Type 9 and 11 messaging
- ▶CoreNet Switch Fabric
- ▶Ethernet
  - 4 x 10/100/1000 Ethernet Controllers
  - 1 x 10GE Controllers
  - All w/ Classification/Policing, H/W Queueing, policing, and Buffer Management, Checksum Offload, QoS, Lossless Flow Control, IEEE 1588, 4 SGMII
- ▶Datapath Acceleration
  - 5Gb/s IP Forwarding, 64B packets
  - SEC 4.0: 5Gb/s IPSec, 1456B packets
  - PME 2.0: 5Gb/s IDS, 1456B packets
- ▶Device
  - 45nm SOI Process
  - 1295-pin package, pin compat with P4040
- ▶Power estimates
  - 12W at 1200MHz (typical, 105C, no I/O)
  - 15W at 1500MHz (typical, 105C, no I/O)

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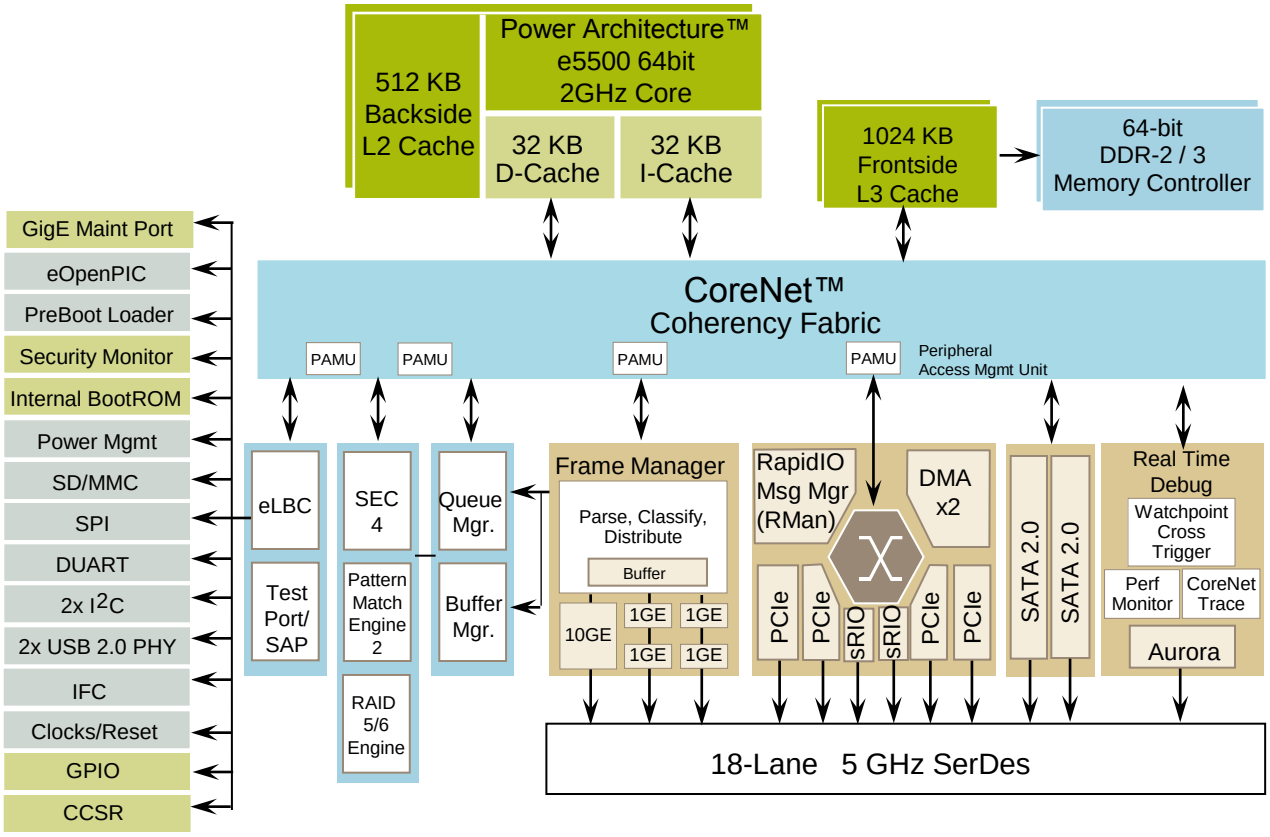
P3041 Advantages Relative to P4040

- Lower power. At 1.2GHz, the thermal max on P3041 will be about 10.5W, and P4040 will be about 14W. At 1.5GHz, the thermal max on P3041 will be about 15W and P4040 will be about 20W.
- Pricing: lower
- Dual SATA. Envisioned for usage of collecting statistics and other by-product data created by an application.
- Improved flash controller, supporting the lower cost MLC (Multilevel bit cell) flash memory in addition to the more robust but more expensive Single Level bit Cell supported by P4040.
- Includes a PHY in the dual USB ports, instead of an interface to a PHY on the P4040.
- Upgraded SRIO message unit, for improved datapath handling. Now supports Type 9 and Type 11 packets.

- P3041 is pin compatible with the P4040. A viable approach for customers is to start with the P4040 and migrate to the P3041 without needing to change the board.

P5020



- ▶Dual MC-64 Power Architecture®
  - 2 64 bit e5500 cores (up to 2 GHz)
  - Each with 512 KB backside L2 cache
  - Dual 1MB Shared L3 Cache w/ECC
  - Supports up to 64GB addressability
- ▶Memory Controller
  - Dual DDR3/3L SDRAM up to 1.3 GHz
  - 32/64 bit data bus w/ECC
- ▶High Speed Interconnect
  - 4 PCIe 2.0 Controllers
  - 2 sRIO 2.0 Controllers
    - Type 9 and 11 messaging
  - 2 SATA 3Gb/s
  - 2 USB 2.0 with PHY
- ▶CoreNet Switch Fabric
- ▶Ethernet
  - 4 x 10/100/1000 Ethernet Controllers
  - 1 x 10GE Controller (XAUI)
  - 1 GigE maintenance port
  - All w/ Classification/Policing, H/W Queueing, policing, and Buffer Management, Checksum Offload, QoS, Lossless Flow Control, IEEE 1588v2, 4 SGMII, QSGMII
- ▶Datapath Acceleration
  - SEC 4
  - PME 2
- ▶Device
  - 45nm SOI Process
  - 1295-pin package
  - ~30W max (est) at 2GHz

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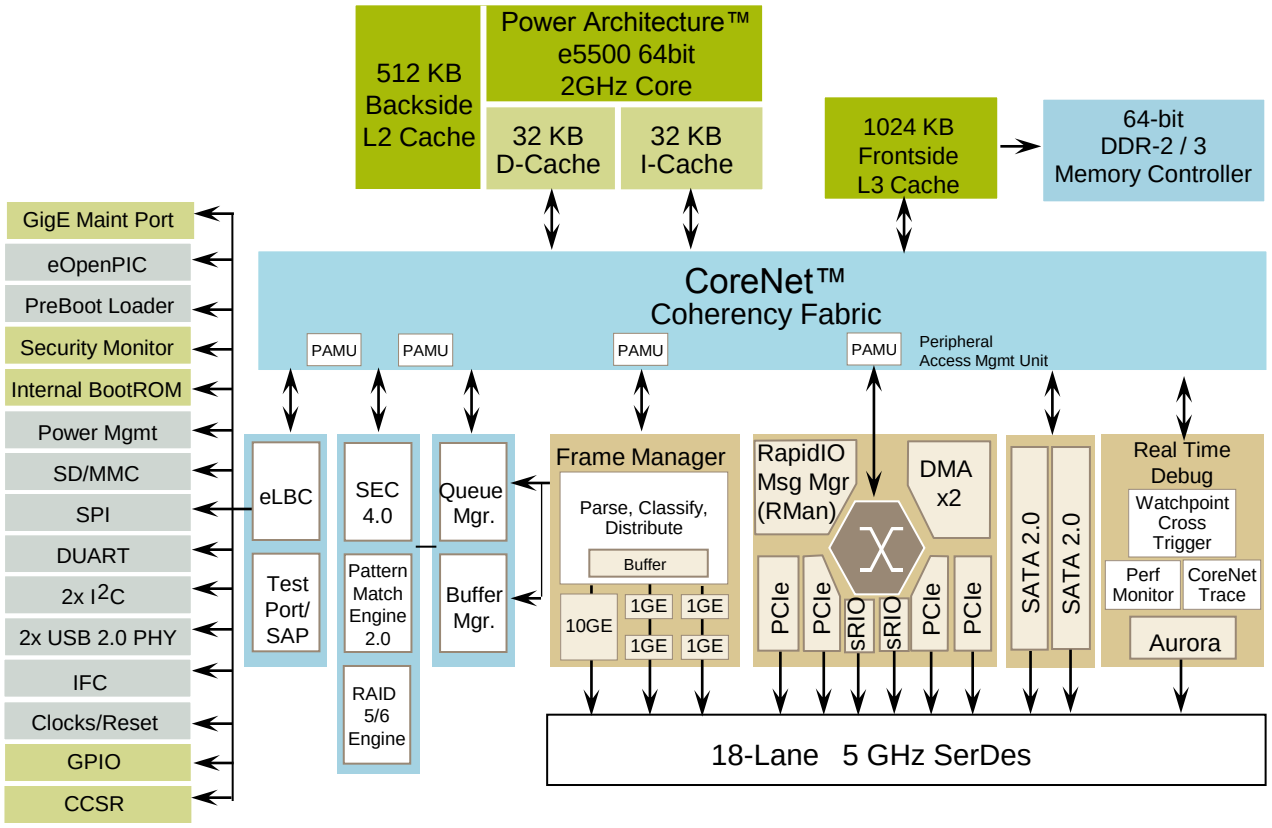
P5010



- ▶Single e500v5 Power Architecture®
  - 1 64 bit e5500 core (up to 2 GHz)
  - 512 KB backside L2 cache
  - 1MB Shared L3 Cache w/ECC
- ▶Memory Controller
  - Single DDR3/3L SDRAM up to 1.3 GHz
  - 32/64 bit data bus w/ECC
- ▶High Speed Interconnect
  - 4 PCIe 2.0 Controllers
  - 2 sRIO 2.0 Controllers
    - Type 9 and 11 messaging
  - 2 SATA 3 Gb/s
  - 2 USB 2.0 with PHY
- ▶CoreNet Switch Fabric
- ▶Ethernet
  - 4 x 10/100/1000 Ethernet Controllers
  - 1 x 10GE Controller (XAUI)
  - 1 GigE maintenance port
  - All w/ Classification/Policing, H/W Queueing, policing, and Buffer Management, Checksum Offload, QoS, Lossless Flow Control, IEEE 1588v2, 4 SGMII
- ▶Datapath Acceleration
  - 5Gb/s IP Forwarding, 64B packets
  - SEC 4: 4Gb/s IPSec, 1456B packets
  - PME 2: 5Gb/s IDS, 1456B packets
- ▶Device
  - 45nm SOI Process
  - 1295-pin package
  - ~24W max (est) at 2GHz

AltiVec Technology on the e5500 Core

- Moving the AltiVec technology to the QorIQ processor family
  - Aligns with the hardware accelerator strategy – offload processing to dedicated functions/applications
  - Utilizing the QorIQ platform power management architecture to manage power of all functions on the device
- The initial core will be e5500 + AltiVec
  - 64-bit core with next-generation Floating Point Unit (increase over e500mc)
  - AltiVec 128-bit SIMD unit which operates independent of Scalar Integer and Floating Point Units
  - Improved functionality
    - Vector Absolute Difference function – single cycle function which previously was taking multiple lines of code
    - Improved Load and Store instructions – which resolve the cumbersome alignment issues and improves performance
    - Gated clocks to minimize dynamic power
- Freescale software enablement support of internally-developed and externally-supplied libraries

Product at a Glance – P3, P4, and P5

	P3041	P4040	P4080	P5020	P5010
CPU	Quad e500MC	Quad - e500MC	Octal e500MC	Dual - e500M 64b	e500M 64b
Frequency	1.5GHz	1.5GHz	1.5GHz	2.0GHz	2.0GHz
DP FP	Yes	Yes	Yes	Yes	Yes
L2 Cache	128KB Backside per core	128KB Backside per core	128KB Backside per core	512KB Backside per core	512KB Backside per core
L3 Cache	1x 1MB w/8 way cache allocation Frontside	2x 1MB w/8 way cache allocation Frontside	2x 1MB w/8 way cache allocation Frontside	2x 1MB w/8 way cache allocation Frontside	2x 1MB w/8 way cache allocation Frontside
System Bus	Corenet	Corenet	Corenet	Corenet	Corenet
DDR I/F Type/Width	Single 64-bit DDR2/3 up to 1.33GHz	x2 64-bit DDR2/3 up to 1.6GHz	x2 64-bit DDR2/3 up to 1.6GHz	x2 64-bit DDR2/3 up to 1.6GHz	x2 64-bit DDR2/3 up to 1.6GHz
10/100/1000 Ethernet (with IEEE1588v2)	1x XAUI or x4 (SGMII) GigE	x2 XAUI or x4 (SGMII) GigE	x2 XAUI or x4 (SGMII) GigE	(2) 1x XAUI or x4 (SGMII) GigE	(2) 1x XAUI or x4 (SGMII) GigE
PCI-Exp	PEX v2.0 x16 SerDes 3 PCIe Controllers (x8, x4)	PEX v2.0 x16 SerDes 3 PCIe Controllers (x8, x4)	PEX v2.0 x16 SerDes 3 PCIe Controllers (x8, x4)	PEX v2.0 x16 SerDes 3 PCIe Controllers (x8, x4)	PEX v2.0 x16 SerDes 3 PCIe Controllers (x8, x4)
sRIO 1.2	Two Controllers Serial x4/x2	Serial x4/x1	Serial x4/x1	Serial x4/x1	Serial x4/x1
Security	SEC 4.0	SEC 4.0	SEC 4.0	SEC 4.0	SEC 4.0
Accelerators	PME2.0 Data Plane Mgmt Assist F Man, Q Man, B Man	PME2.0 Data Plane Mgmt Assist F Man, Q Man, B Man	PME2.0 Data Plane Mgmt Assist F Man, Q Man, B Man	PME2.0 Data Plane Mgmt Assist F Man, Q Man, B Man	PME2.0 Data Plane Mgmt Assist F Man, Q Man, B Man
Power (Est Max)	< 15 Watts	21	< 30W	< 30W	< 30W
Package	1295 FC PBGA	1295 FC PBGA	1295 FC PBGA	1295 FC PBGA	1295 FC PBGA
Technology node	45nm SOI	45nm SOI	45nm SOI	45nm SOI	45nm SOI
Samples	Q410	Q110	Q110	Q410	Q410
Status	Definition	Execution	Execution	Definition	Definition

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Multicore Development Environment

- **Virtualization enables partitioning of resources among System Classes**
  - Core, Memory, I/O, Accelerators
- **Supports flexible mix of SMP/AMP (control plane, data plane) as well as 3rd party services**
  - On-chip fabric enables scalable cache-coherent memory access with isolation and protection
- **Multi-Core Diagnostics supporting trace, event, and application performance analysis**
- **Hybrid simulation environment enables migration and partitioning of OSs and applications onto a full multi-core system**
  - Enables fast, accurate performance prediction and software optimization

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QorIQ™ P4080 Enablement Solution

	Simulation	Silicon
Stacks & Apps	▶Freescale VortiQa ▶LWE sample applications	
Performance Analysis	▶Hybrid model with graphical front-end	▶CodeWarrior run control & trace + profiling tools
S/W Debug	▶CodeWarrior and/or GDB	
Build Tools	▶GNU tools + LTIB*	
H/W Config Tools	▶PME config tool ▶FMAN config tool	
H/W Debug	(Model debug (via Virtutech)	▶CodeWarrior trace (via Aurora)
BSP	▶Freescale Linux & Light Weight Executive (LWE) ▶Freescale hypervisor	
Target	P4080 Simulator (simics)	P4080 Silicon

Strategic Alliances – Partner Specifics

	ENEA	Green Hills	Mentor
Freescale Devices supported	QorIQ StarCore PowerQUICC	QorIQ PowerQUICC	QorIQ PowerQUICC
Partner software products to be optimized for FSL devices	RTOS: OSE, OSEck Tools: Optima	RTOS: Integrity Tools: MULTI	Linux: Veracruz City Tools: EDGE
Alliance Term	Multi-Year, Long Term	Multi-Year, Long Term	Multi-Year, Long Term
Freescale software IP incorporated into partner products?	Yes	Yes	Yes
Multicore focus?	Yes	Yes	Yes
Expected Product Availability	Select products available now*	Select products available now*	Starting in June 2010*

* Product Roadmap available directly from Partner

Networking Ecosystem

World Class Alliances
Strategic Technology Collaboration

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e200 e300 e500 e600

SOC integrated devices
Embedded power budgets
Networking life cycles
Networking/security IP
Content Aware Packet Processing

Development and production systems
in standard industry form factors

RadiSys. THE POWER OF WE | FLEXTRONICS | Computer Systems, Inc. MERCURY | Portwell

EMBEDDEDPLANET

GDA Technologies, Inc. accelerate your innovation™

CELESTICA

freescale semiconductor | kontron

WIND RIVER | mocana™ | ClamAV | SNORT.ORG | D2 technologies

QNX SOFTWARE SYSTEMS | Linux | Green Hills® SOFTWARE, INC. | Mentor Graphics

Dimark | ARICENT | KASPERSKY lab | WIND

ENEA | virtutech | WIND RIVER | CodeWarrior

Optimize application specific stacks for continual improvement in network security solutions

Value Partners: enable faster time to market and longer time in market

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20 Years of Communications Processing Evolution

AIM Alliance
Started 1991
First silicon 1992

PowerPC® 603e

PowerPC® 75X

Dual-core processor
MPC8641D with e600 Power cores

Dual-core with integrated content processing
MPC8572E with e500 Power core

First PowerQUICC® communications processors
Includes Communications Processor Module (CPM)

PowerQUICC III
e500 Power core

QorIQ™
Communications Platforms

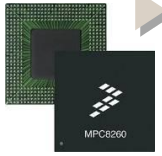
MC68302
68K core

1989	- - -	1994	1995	1996	1997	1998	- - -	2002	2003	2004	2005	2006	2007	2008

Security integration with PowerQUICC line

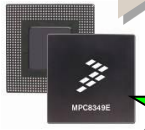
GPON processor
Integrated DSP + Power core

QUICC® MC68360
68K core

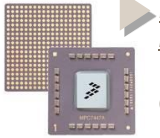


PowerQUICC II
603e Power core

PowerQUICC II Pro
e300 Power core



QUICC Engine™
Next-gen CPM / dual RISC engines



Power Architecture™ Host Processors
MPC7xxx
e600 core

★ In Production

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… the News: Freescale Introduces Product Longevity Program

- The embedded market needs long-term product support, which allows OEMs to provide assurance to their customers.

- Freescale has a longstanding track record of providing long-term production support for our products.

- We are now pleased to announce that we are introducing a formal product longevity program for the market segments we serve.
  - In the automotive and medical segments, Freescale will manufacture select devices for a minimum period of 15 years.
  - For all other market segments in which Freescale participates, Freescale will manufacture select devices for a minimum period of 10 years.

- A list of applicable Freescale products is available for quick access at www.freescale.com.

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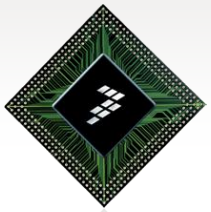

Why choose Freescale as your MPU supplier?

Industry Leading SOC Architecture

- Ever increasing System Performance .
- Balanced architecture – cores/memory subsystems/Hi-speed IO/Hardware Off load and accelerators
- High level integration of differentiated IP.

Broad and Scalable Portfolio

- Able to meet price/power/performance of a broad range of applications
- Ecosystem that provides quick time to market solutions

Sales and Service at the most critical point of contact - you

- Freescale and our distribution partners provide the largest trained sales and FAE organization in the industry
- 10 year minimum support for our devices.

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