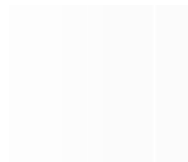


Industrial Solutions



2017 June



SECURE CONNECTIONS
FOR A SMARTER WORLD

Agenda

20 minutes

TSN and LS1028A

20 minutes

Robotics

20 minutes

Open Industrial Linux and demo



Industry 4.0 Requires Scalable Application Processing



Analyze



Automate



Monitor

Improving time to market, manufacturing flexibility, and increasing quality and efficiency will require smarter, connected businesses

Powering Industrial Applications
for over 6 decades

1 Billion Industrial Application
Processors Shipped

Legacy

Longevity

Extreme Op

Security

Complete Solutions for Industrial Processing



Example Industrial Products



**Industrial
Managed
Ethernet
Switches**

**Gateway/
Router**

**Industrial
Firewall**

**Remote
Terminal Unit
(RTU) /
Automation
Controller**

**Programmable
Logic
Controllers
(PLCs)**

**Robots
(Controllers/
PLCs)**

Industrial Protocols for Different Applications

Target Applications

- Motor drives
- Motion control
- Synchronized servos



IRT

Deterministic
 $< 1 \mu\text{s}$ jitter
 $< 1 \text{ ms}$ cycle time

Protocols



- Conveyor belts
- Picker arms
- PLCs, I/O Control
- Valves



RT

Deterministic
 Jitter matters for sync
 1 to 100 ms cycle time



- Sensors
- Data scanner
- Inventory management



NRT

Non-deterministic
 Jitter doesn't matter
 $> 100 \text{ ms}$ cycle time

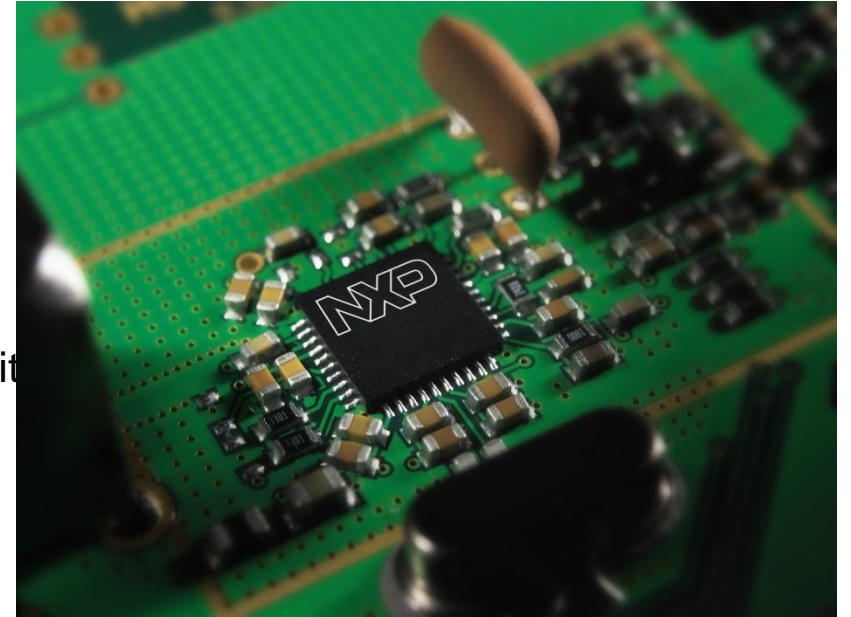


IEEE® 1588 Precision Time Protocol
 VERY jitter sensitive; cycle time does not matter



Strong Legacy in Industrial Embedded Systems

- Embedded and Automotive Heritage
- JEDEC Industrial and Consumer Certification
- Founder of Multicore for Avionics (MCFA) working group
- Secure, Trustworthy, Assured and Resilient Semiconductors and Systems (STARSS)
- NXP membership in European Horizon 2020 Cert MILS project
- Automotive AEC-Q100 Certification
- U.S. National Institute of Standards and Technology (NIST) Cryptographic Algorithm Validation Program (CAVP)
- IEEE Audio Video Bridging (AVB) Task Group
- IEEE 1588
- Time Sensitive Network (TSN)
- EtherCAT Technology Group (ETG)
- PROFI International (PI)
- Wireless Hart Zigbee



Supply Longevity



Industrial applications require product longevity

- Long product lifecycles
- Special product certification required

NXP Industrial Application Processors

- 10 and 15 year supply longevity options
- Formal program with products listed at www.nxp.com/productlongevity

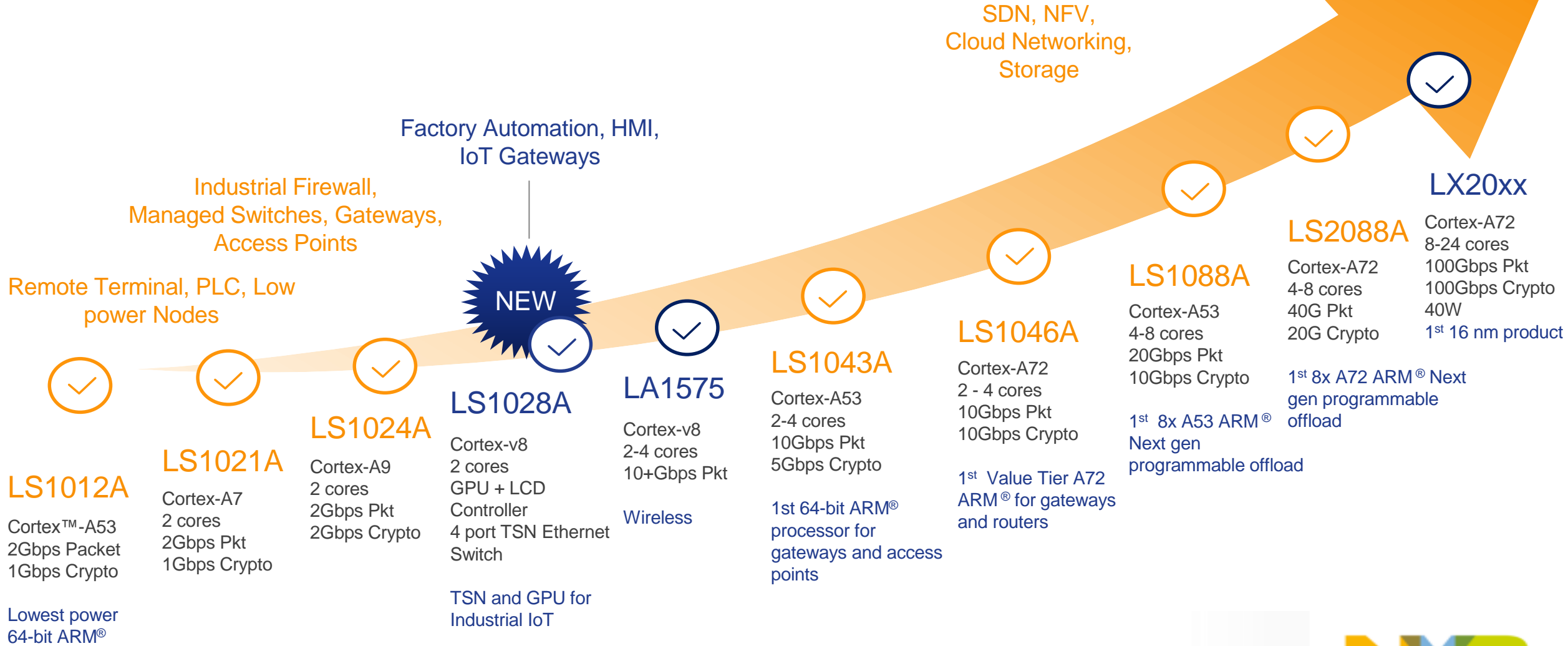


Extreme Operating Conditions

- **10 year product life** with continuous operation
- Product Life Application Notes
- Extreme **temperature conditions**
 - -40° C cold start
 - 70-85° C ambient operating conditions
 - Up to 125° C junction temperature
- Low power consumption for **fanless designs**
- Small footprint for **space-constrained designs**



QorIQ Layerscape – Leading the 64-bit ARM[®] and Multicore Innovation



TSN AND LS1028A



Time Sensitive Networking (TSN):

Extend use cases from audio/video applications (AVB) to control systems

Reduced worst-case delays

- 4 μ s or less per hop @ 1 Gbps for short messages (plus cable delays)

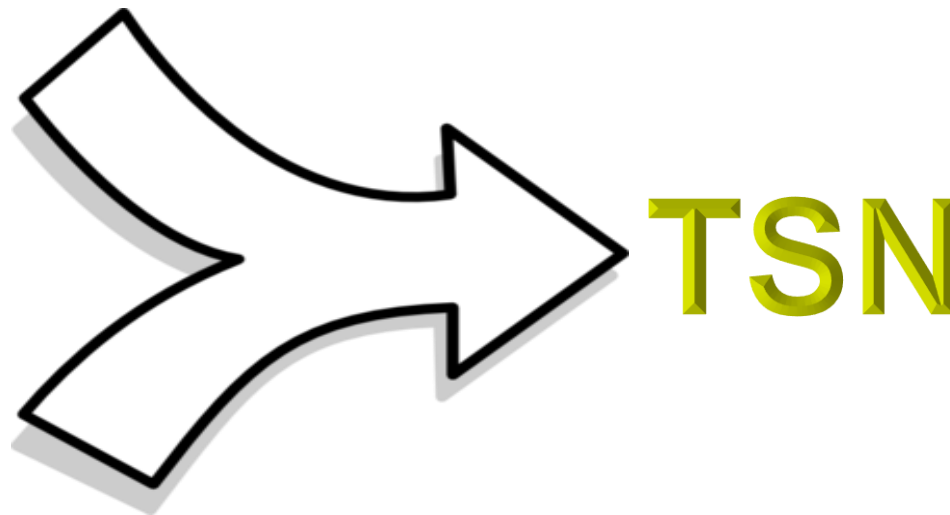
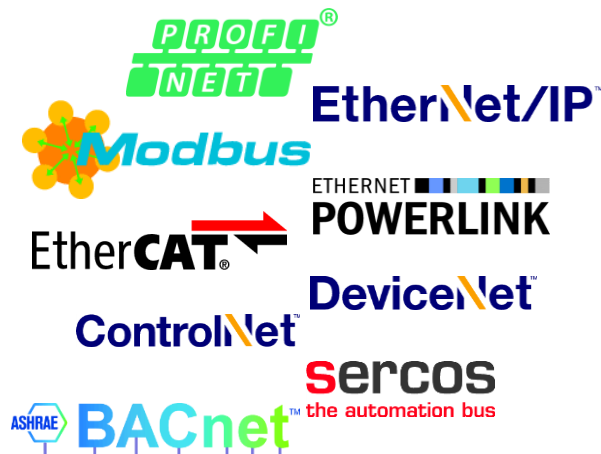
Improved robustness:

- Alternative paths with “instant” switchover
- Multiple clock sources with “instant” switchover

Scalability

- Reduced management traffic for reservations and configuration

Converged Networks



TSN

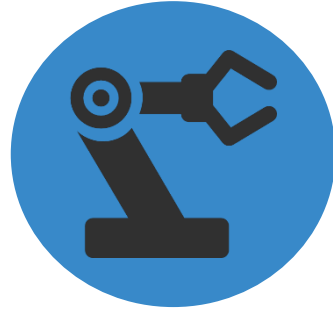


Major Markets For TSN



Automotive

- Low, Bounded Latency
- Reserved Bandwidth
- Growing Bandwidth



Industrial

- Very Low Latency
- Time Sync
- High Bandwidth
- Redundancy
- Network Convergence



Pro A/V

- Time Sync
- Bounded Latency
- Ease of Deployment



Consumer

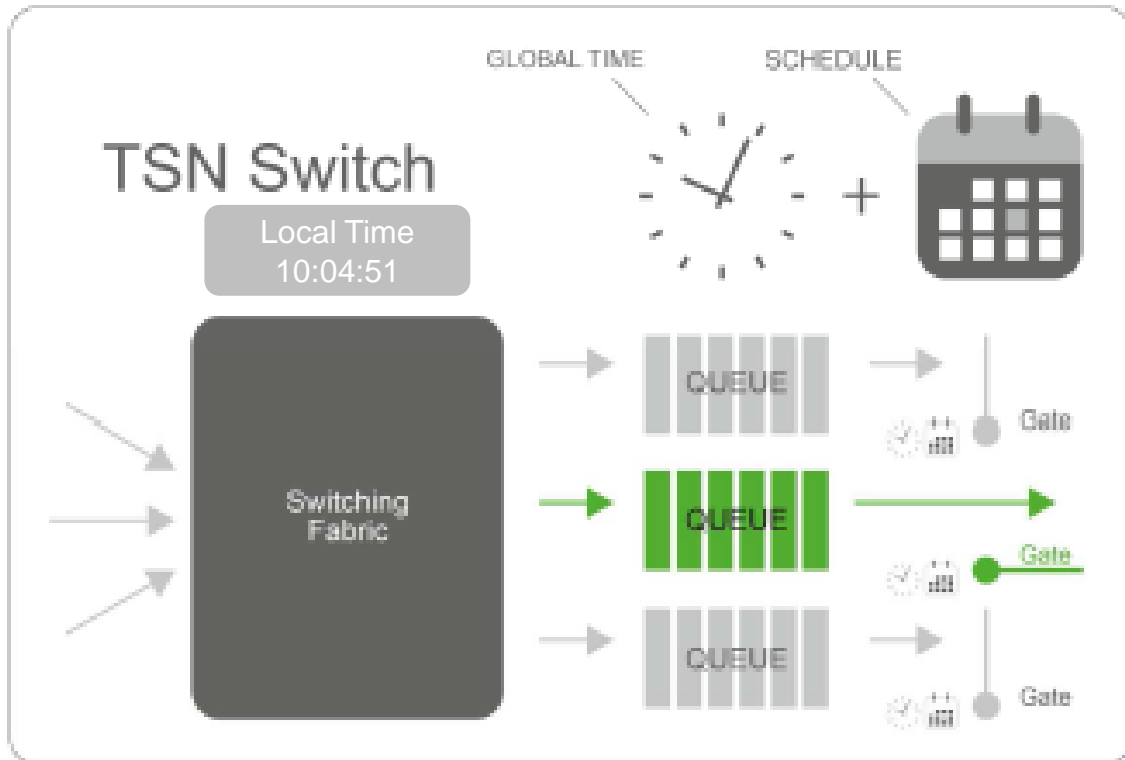
- Interoperability
- Flexibility for new media

Time Sensitive Networking Feature Plan

Standard	Description
802.1Qbv	Time-aware shaping (queue based)
802.1Qbu	Frame pre-emption
802.1CB	Redundancy (frame replication and elimination)
802.1Qcc	Enhancements and improvements for stream reservation
802.1Qch	Cyclic queuing and forwarding
802.1Qci	Per-stream filtering and policing
802.1AS	Timing and synchronization (mechanisms for faster fail-over of clock grandmasters)



802.1Qbv: TAS – Time Aware Shaping



Time Triggered transmissions from each of 8 queues

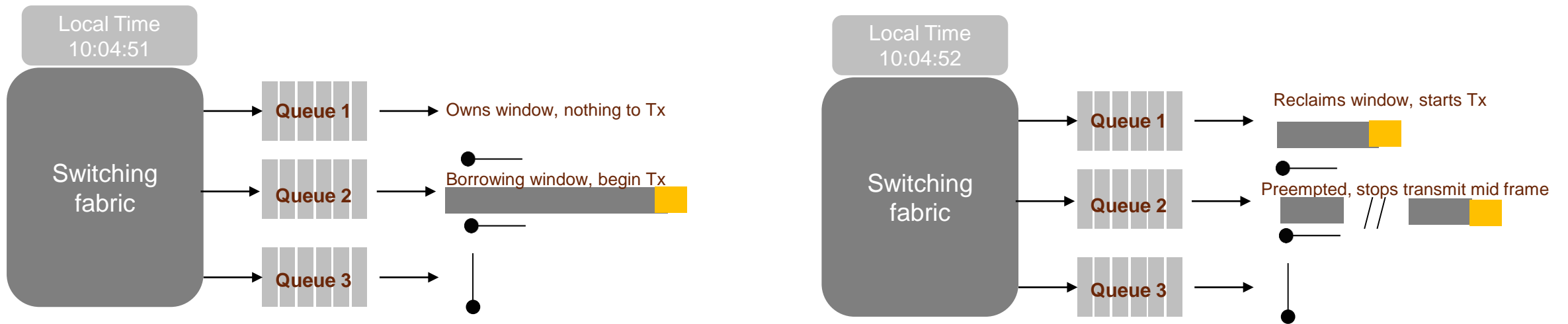
Queue selection based on priority field of VLAN tag

Reserves bandwidth for deterministic traffic throughout the network

TAS + Cut-through guarantees <2 usec latency through switches and daisy chain endpoints

802.1Qbu: Frame Pre-emption

1. Allows priority packet to interrupt best effort traffic in the middle of a frame
2. Once priority packet is finished, best effort traffic continues from the same spot

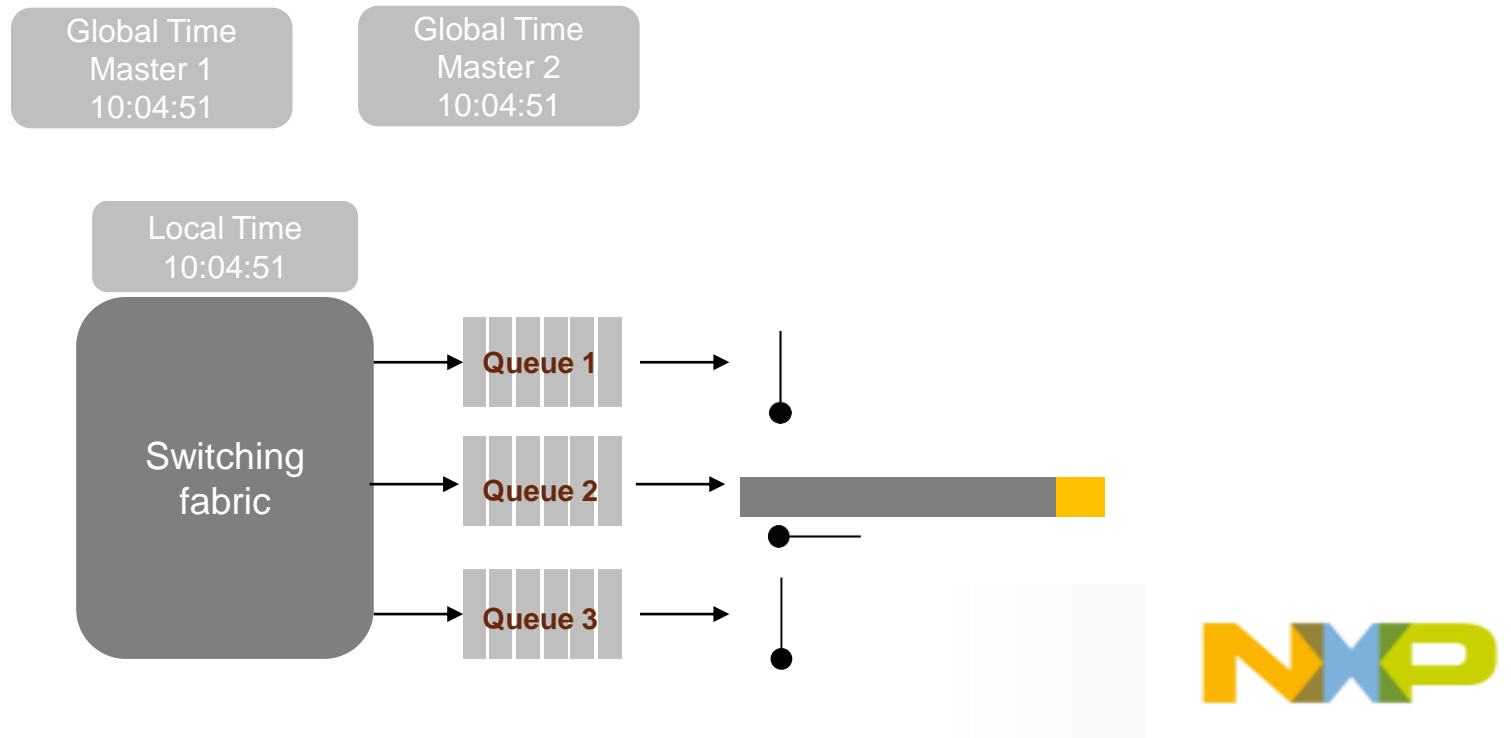


Can be used with Time Aware Shaping to increase bandwidth for best effort traffic, allow for large packet sizes

Can also be used alone, with 2 traffic classes

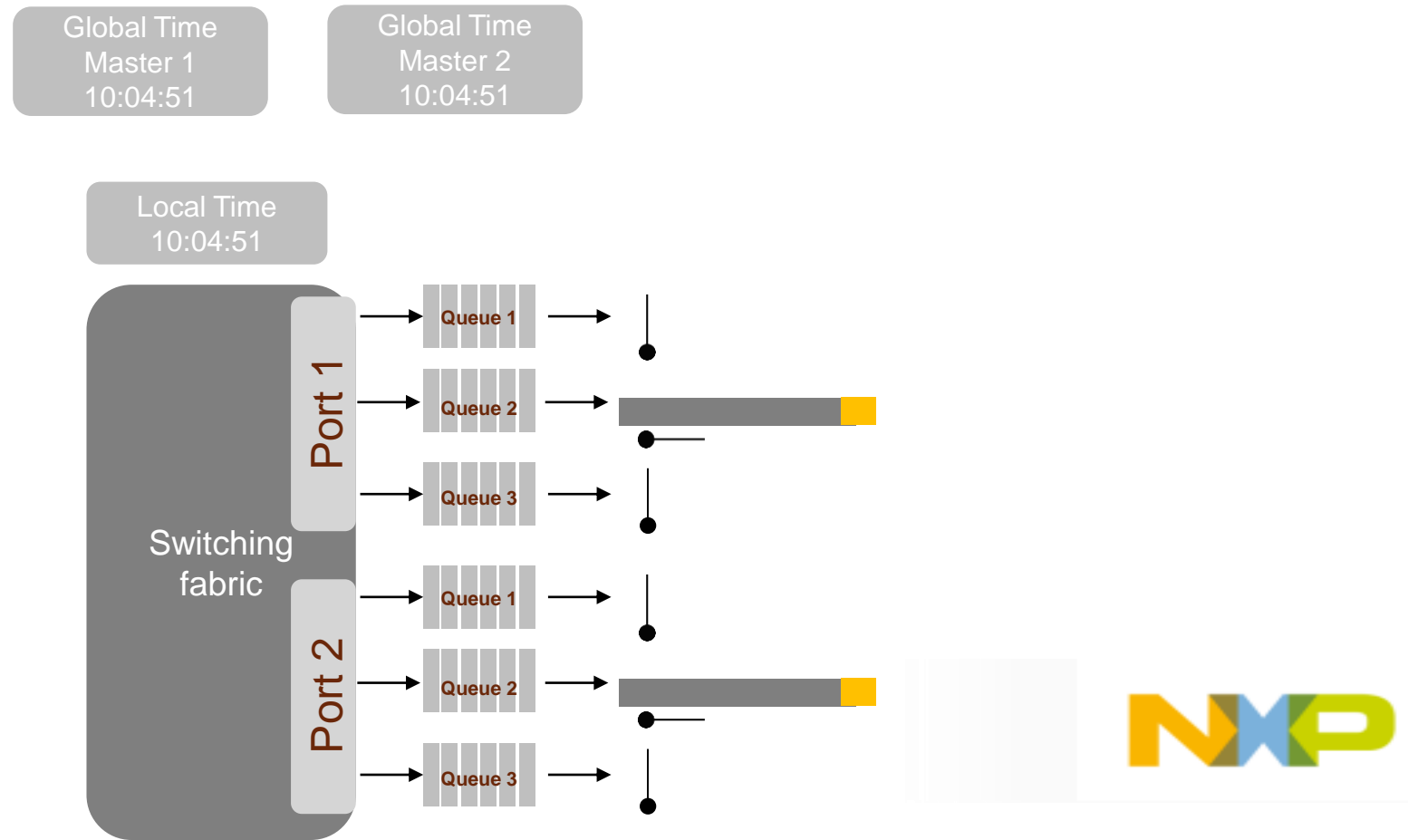
802.1ASrev: Timing and synchronization

- Defines how TSN ports & switches synchronize their clocks with other network clocks, so that sender and receiver have a shared understanding of time. 802.1AS eventually becomes a profile of IEEE 1588.
- Standardizes the use of multiple grandmaster clocks as well as the possibility to make multiple connections to these grandmaster clocks for redundancy/fail-over.
- Defines support for multiple clocks (local 1, local 2, local 3; synchronized to different masters for different purposes)



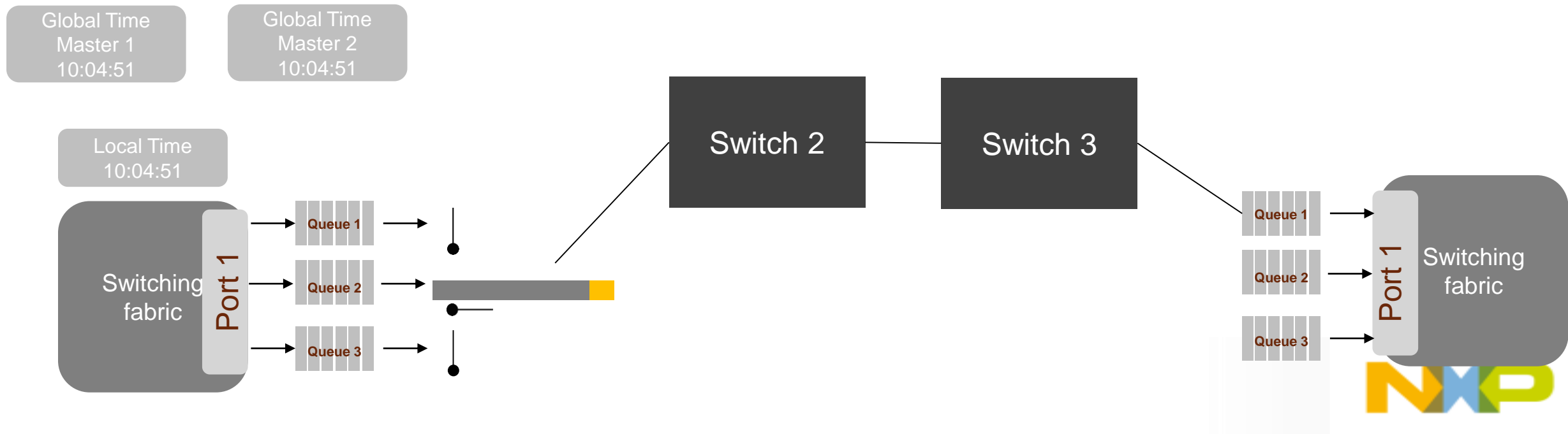
802.1CB: Redundancy (frame replication and elimination)

- From a management perspective, defines how to configure redundant transmissions of frames (presumably from different ports on a switch) to ensure that the target receives at least one copy, even if one transmission path is disrupted. Similar to HSR and PRP.
- Works with 802.1CA: Path Control & Reservation.
- Handles duplicate frames (1 from each path)

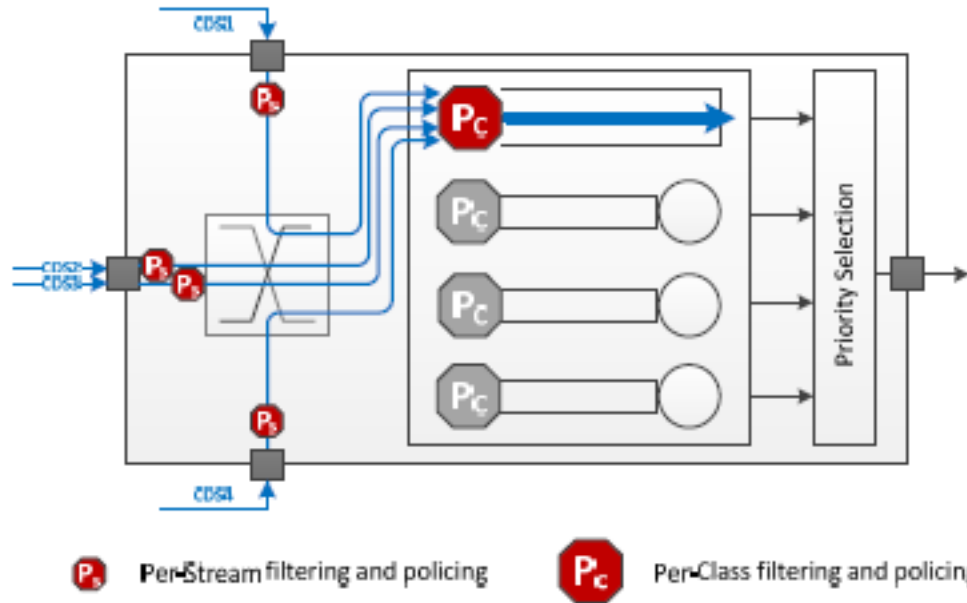


802.1Qcc: Enhancements and improvements for stream reservation

- An improved version of 802.1Qat Stream Reservation Protocol)
- Support for more streams, configurable SR (Stream Reservation) classes and streams, better description of stream characteristics, support for Layer 3 streaming, deterministic stream reservation convergence, and UNI (User Network Interface) for routing and reservations. TSN configuration can be achieved statically by a network designer, or dynamically by a network service.



802.1Qci: Per-stream filtering and policing



MEF SRTCM	Difference	Modified SRTCM
bandwidth for excessive traffic	Meaning of yellow tokens	bandwidth for jitter compensation
only from Yellow bucket	Used tokens of yellow frames	from Green and Yellow buckets
at least for a complete frame size	Range of EBS	allowing smaller than a frame size (required for edge ports)
best effort	Transmission of yellow frames	kept in highest priority

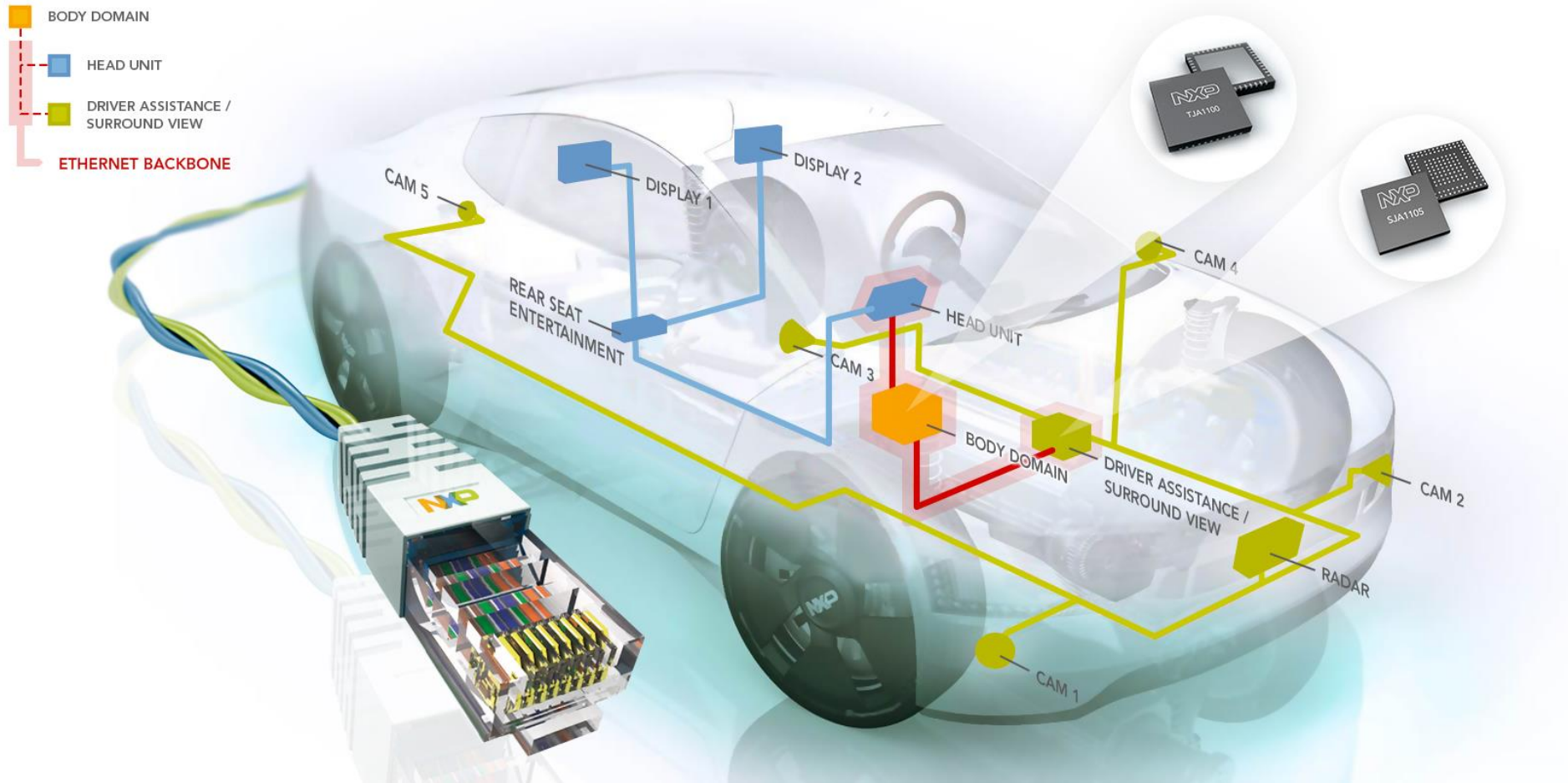
Per-stream filtering and policing

- perform per-stream bandwidth enforcement to ensure conformance with traffic contract
- detect and limit faulty stream to protect transmission of other non-faulty streams on egress
- filter out non-conformant frames, e.g. over-sized frames

Per-class filtering and policing

- perform per-class bandwidth enforcement for control-data classes on egress port

NXP and TSN



SJA1105T Automotive TSN Ethernet switch announced August, 2015

Production today

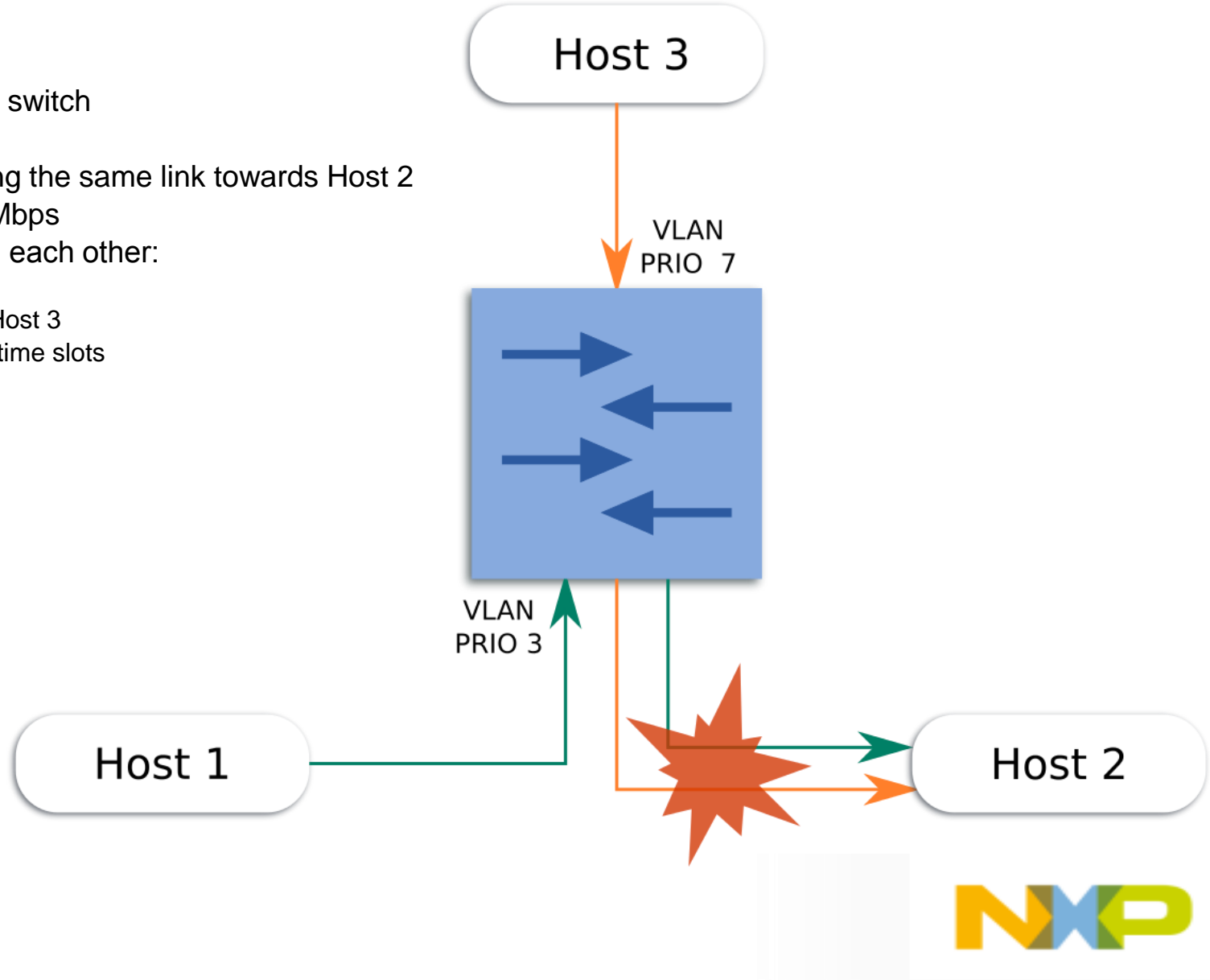
TSN, AVB, Deterministic Ethernet



TSN Demo

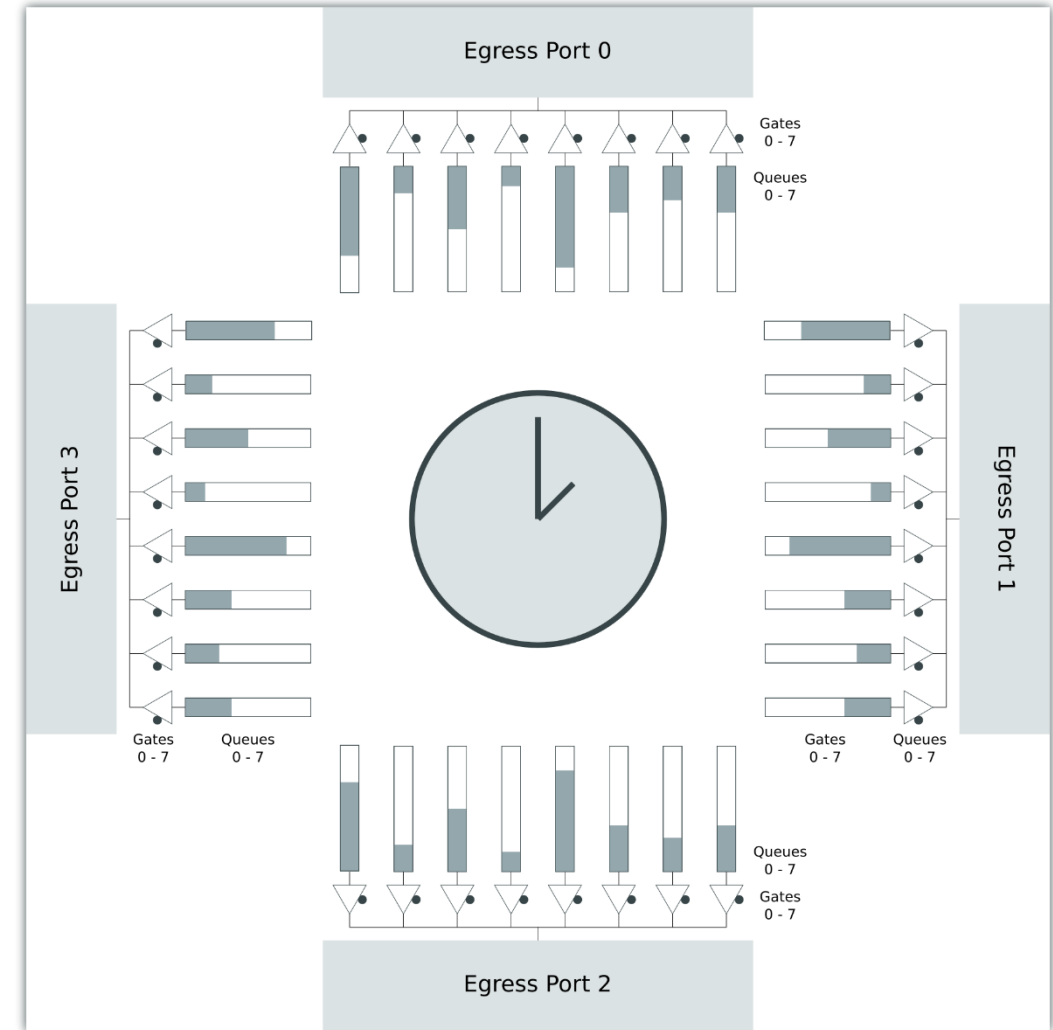
- Overview

- 3 host Linux machines connected through a switch
- 2 TCP flows competing for bandwidth
- Flows bottlenecked because they are sharing the same link towards Host 2
- Combined throughput cannot exceed 1000Mbps
- 3 approaches to isolate the flows' impact on each other:
 - *Standard* switch configuration: do nothing
 - *Ingress Policing*: rate-limit traffic coming from Host 3
 - *Time Gating*: schedule the 2 flows on different time slots



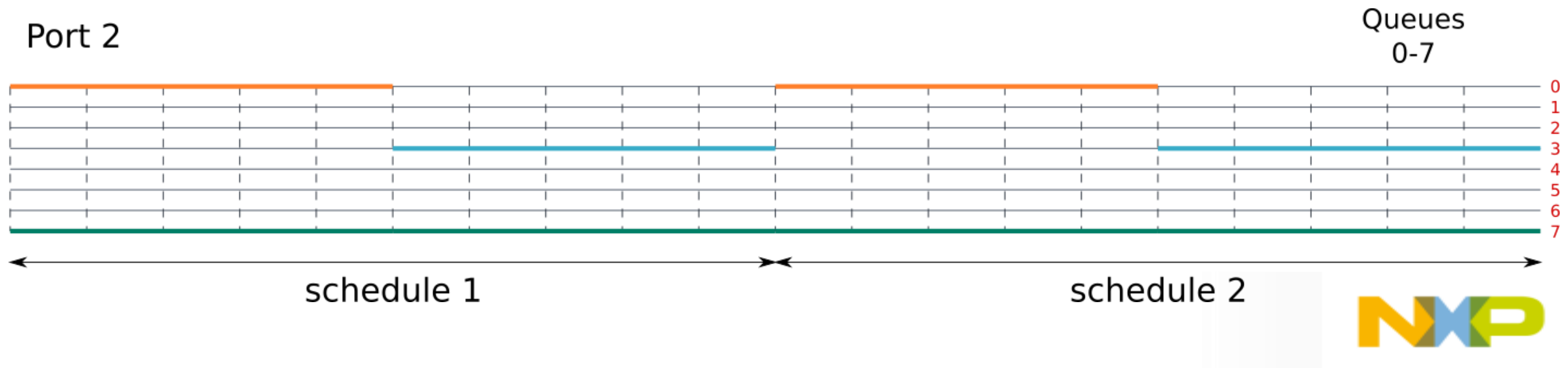
TSN Demo – Analysis: Scheduling configuration

- The Time-Aware Scheduler works by following the guidelines in 802.1Qbv
 - The 5 Egress Ports each have 8 Gates, which can be open or closed
 - Each Gate has 1 Queue associated with it
 - Whenever a Gate is open, packets from that Queue can be sent out the wire
 - An internal clock generates ticks each 200ns
 - At each tick, a new time slot can be created, where some Gates can be opened and some can be closed
- Effectively works like TDM (Time Division Multiplexing) for Ethernet

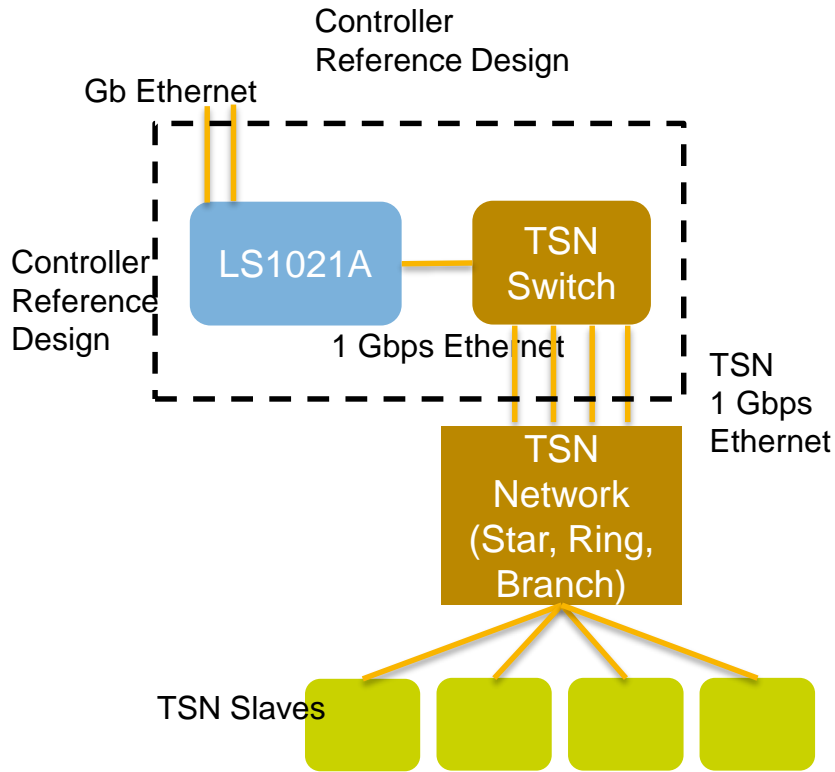


TSN Demo – Analysis: Scheduling configuration

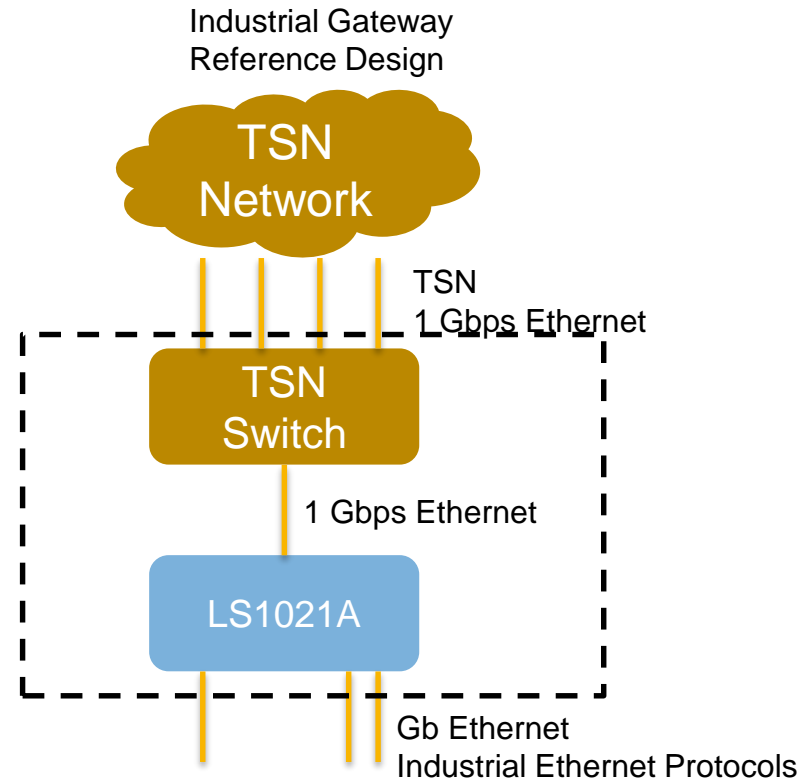
- The user defines how many clock ticks each time slot takes
 - The individual time slots are called *subschedules*
- Once the Time-Aware Scheduler goes through each time slot in a round-robin fashion, it starts over again periodically
 - A complete period of *subschedules* is called a *schedule*
- On Egress Port 2 (toward Host 2), create a subschedule for VLAN PRIO 0 and one for PRIO 3
 - Flow 1 is completely isolated from Flow 2
 - Minimal interference, best utilization of bandwidth



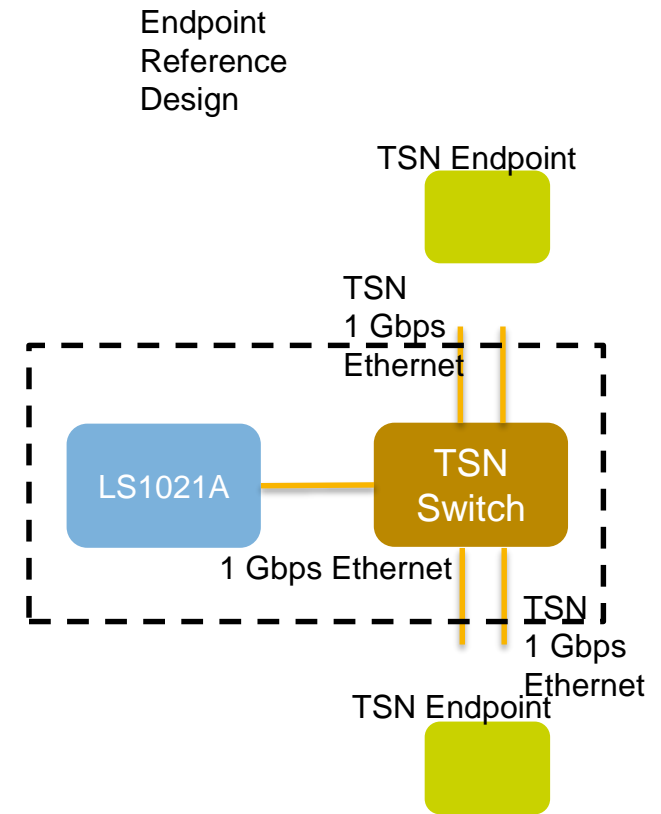
1.2 TSN Reference Design for Application Development



Applications
TSN PLCs,
Automotive Gateway



Applications
Legacy Industrial
PLC,
Industrial Gateway



Applications
Robotics controller, motor
control, synchronized audio
playback





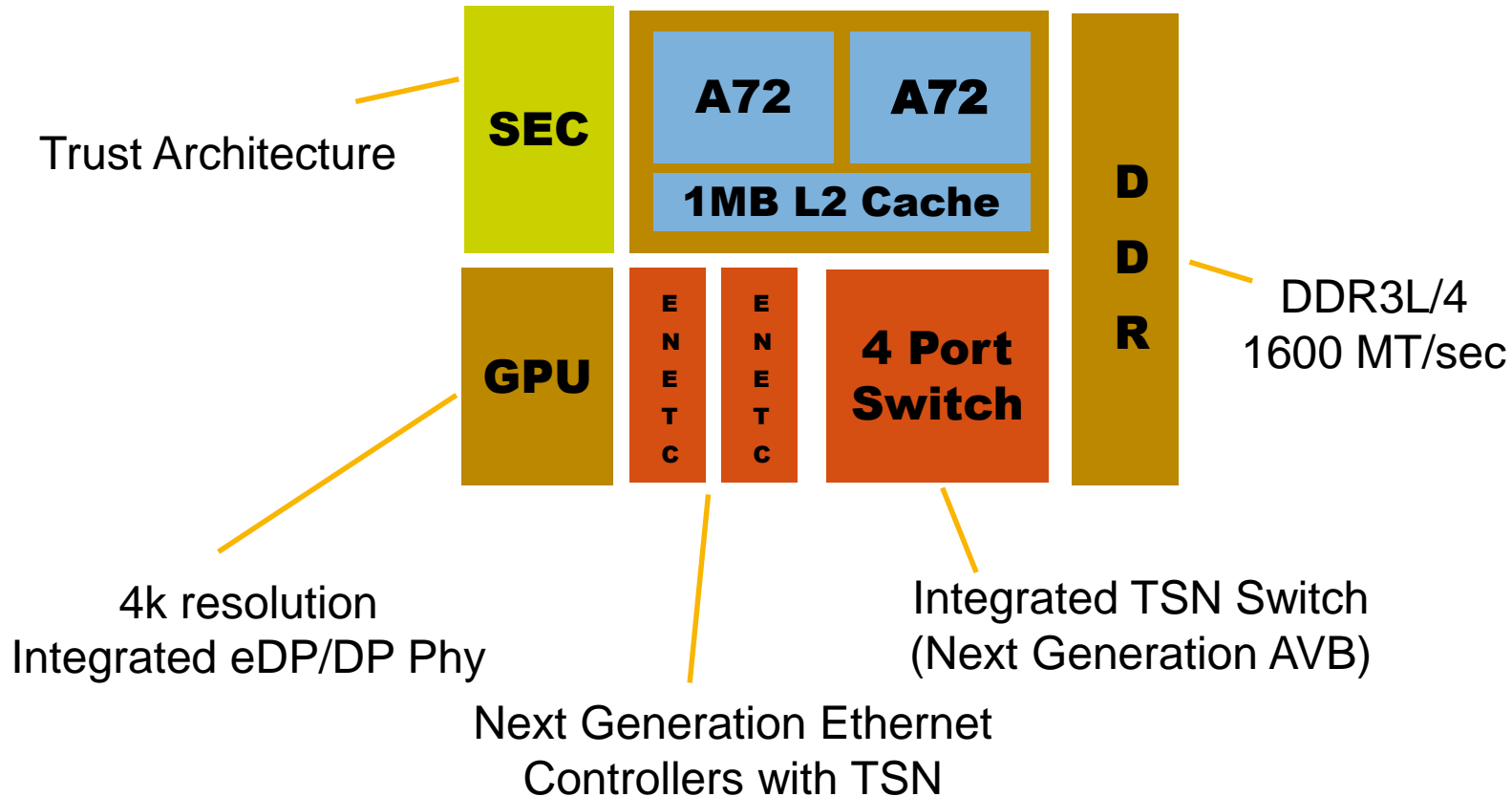
Dual Core Cortex-A72 Processor For Industrial Applications

- Highest performing ARMv8-A processor core
- Extended temperature – 125 Deg C Tj
- Integrated GPU for HMI
- Time Sensitive Networking for deterministic latency over Ethernet



LS1028

\$20 Price **5W Thermal Power** **125 Deg C Tj**



Target Markets and Customers

Industrial

- Energy Distribution
ABB, Schneider Electric
- Robotics Controllers
Kuka, Yaskawa, Fanuc
- Motion Controllers
Mitsubishi, Omron, Siemens
- HMI
Siemens, Rockwell Automation

Embedded Boards

TQ, Kontron, Advantech

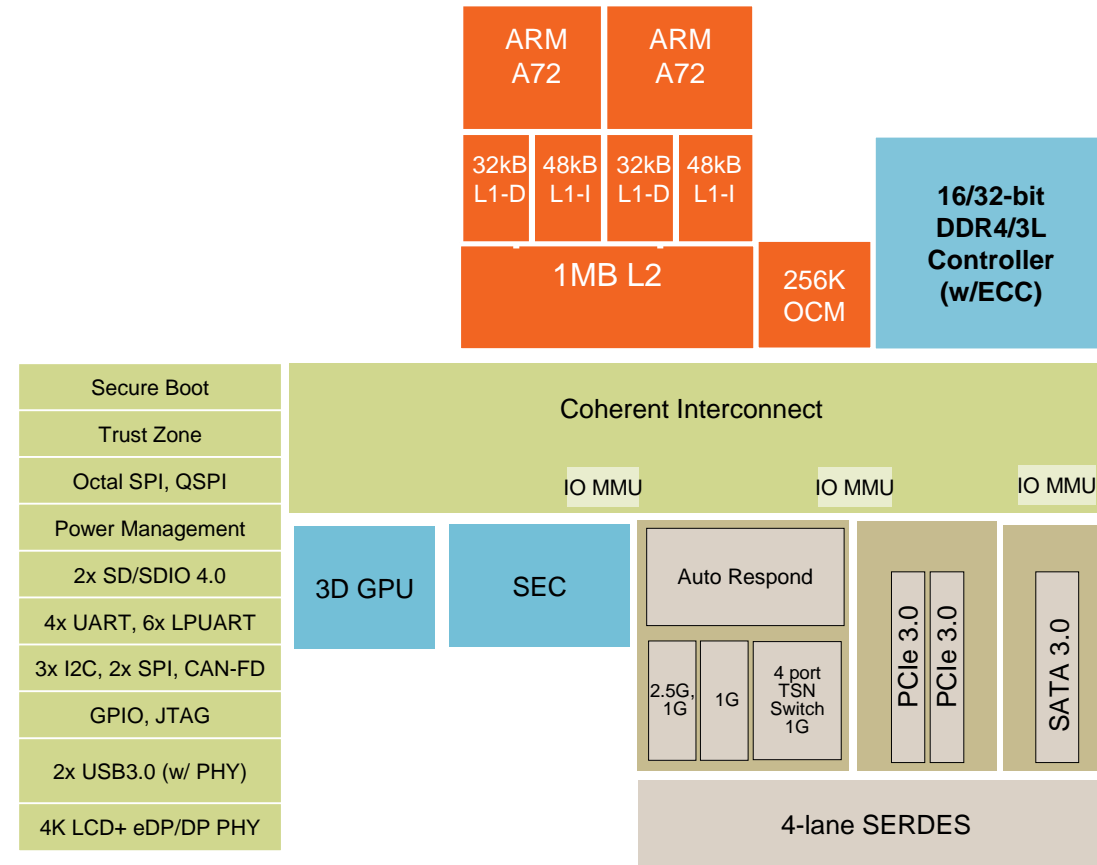
IoT Gateways

Dell, Cisco, GE



LS1028A

- **Dual ARM Cortex A72 processors**
 - Up to 1.3GHz per core w/ECC protected L1/L2
 - 32KB D / 48K I L1 cache
 - 1MB L2 cache
- **Memory Controller**
 - 16-bit(+ECC)/32-bit(+ ECC) DDR4/3L
- **High Speed Interconnect**
 - 2x PCI Express Gen3
 - 1x SATA3.0 (4 lane SERDES shared w/PCI-e)
 - 2x USB3.0 (with/PHY)
- **Ethernet**
 - 6x Ethernet, 1x 1 / 2.5 Gb, 1x 1Gb, 4x 1Gb
 - IEEE 1588 v2
 - TSN
- **Datapath**
 - SEC Acceleration
 - TSN L2 Switch
 - Auto Respond
- **Graphics**
 - 4K LCD Controller with eDP/DP Phy
 - 3D GPU
- Advanced Audio: 5xSAI, PWM
- 4x UARTs, 6x LPUART, 2x CAN-FD
- 3x I2C, 2x SPI, 2x SD/SDIO 4.0
- Octal SPI, 16 bit parallel bus
- Secure Boot, Trust Architecture
- Advanced Power Management



Package: 17 x 17mm FCPBGA, 0.75 pitch



Time Sensitive Networking Feature Plan

Standard	Description	LS1028A Support
802.1Qbv	Time-aware shaping (per-queue based)	Yes
802.1Qbu	Frame pre-emption	Yes
802.1CB	Redundancy (frame replication and elimination)	No
802.1Qcc	Enhancements and improvements for stream reservation	Yes
802.1Qch	Cyclic queuing and forwarding	No – PAR
802.1Qci	Per-stream filtering and policing	Partial Support
802.1AS	Timing and synchronization (mechanisms for faster fail-over of clock grandmasters)	Yes



TSN Chip Design Target

TSN Feature	TSN Design Target	Current Performance with Standard Ethernet
Number of hops	5-50	NA
Bandwidth	1 Gbps	1 Gbps
Jitter	+/- 500 nsec	>3 usec
Delay	<2 usec cut-through latency ¹	> 3 usec, not bounded
PTP time stamp accuracy	10 ns	40 ns

¹ Latency is measured FIFO for a packet. Latency should not vary for different packet size.



QorIQ LS1028A For Industrial Applications



✓ High Performance ARM® A72 cores

✓ Extended Temperature Support –
Deg C

125

✓
• Integrated TSN

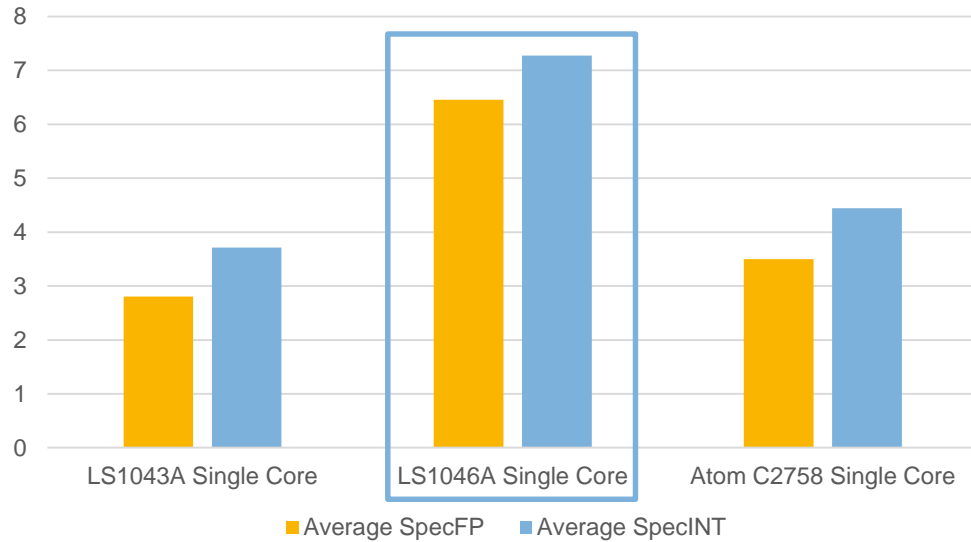
✓
• HMI



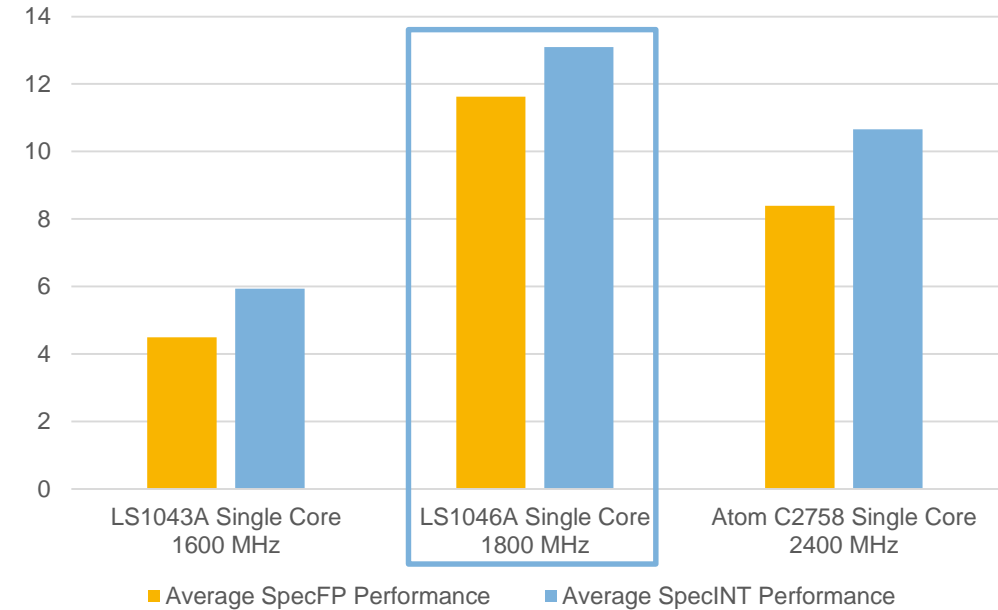
ROBOTICS

Better Per Core Performance Than Intel Atom

Normalized Single Core Performance
(Score/CPU/MHz)



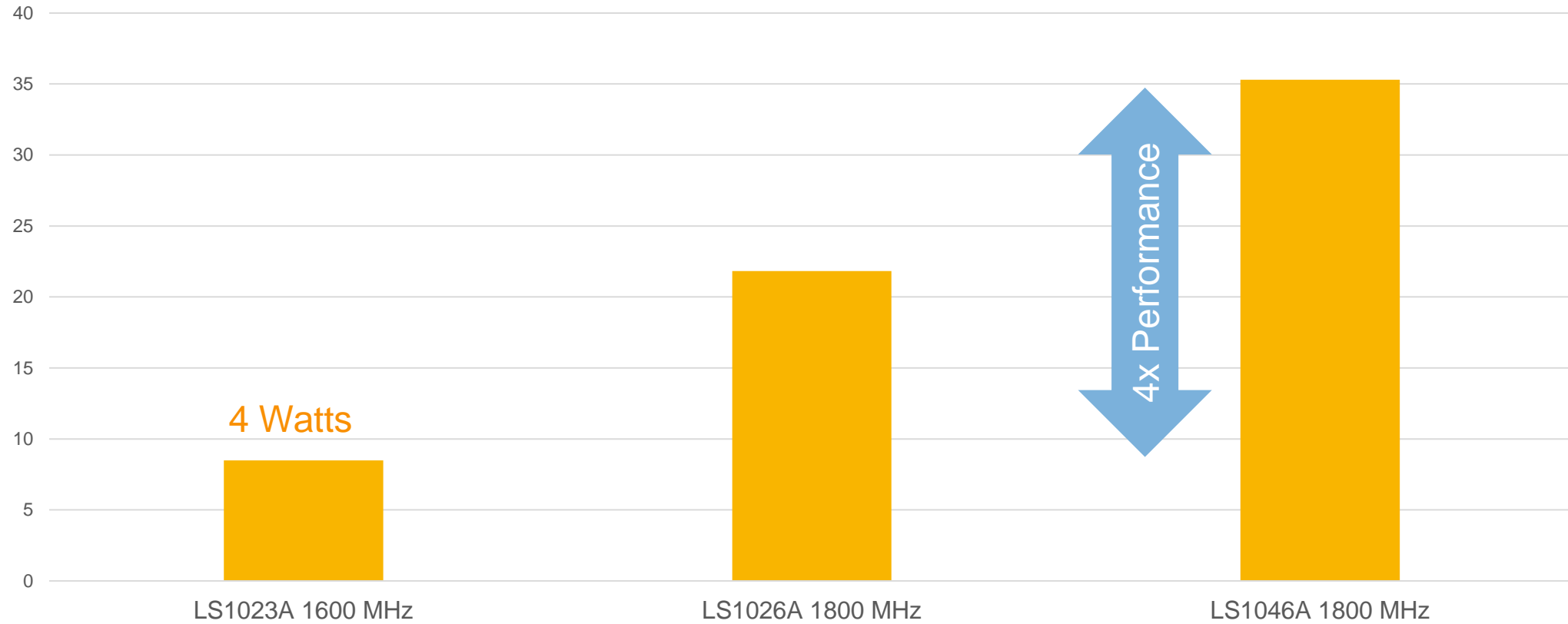
Raw Single Core Performance



LS1046A (A72) core provides superior per clock performance to Atom
LS1046A (A72) beats Atom single core performance at full clock speed
LS1043A (A53) provides similar per clock performance to Atom with superior \$/watt

Floating Point Performance Range

Average SpecFP Performance



Real Time Performance

Industrial Linux SDK with Xenomai real-time kernel

VxWorks 7 support for LS1043A Q2 2017

VxWorks 7 support for LS1046A Q3 2017

Nucleus RTOS support for LS1046A

LS1043A Measured Memory Latency

Latency @ 1.6GHz core	L1	L2	DDR
Core Clock cycles	3	13	148
ns	1.9	8	93

LS1043A DDR to PCIe Latency with QDMA

PCIe Configuration	256 Byte Transactions	Latency First Byte written to PCIe (nsec)	Average Latency Per Transaction (nsec)
PCIe Gen 2 x1	1 Transaction	471	471
	12 Transactions	6506	542
PCIe Gen 2 x2	1 Transaction	467	467
	12 Transactions	3457	288



Scalable Processing in Pin Compatible Package

4x A53 1.6 GHz
5 W Power
21,000 Coremark
½ Neon Unit

LS1043

LS1046

4x A72 1.6 GHz
14 W Power
32,000 Coremark
2 Neon Units

2x A53 1.6 GHz
4 W Power
10,500 Coremark
½ Neon Unit

LS1023

LS1026

2x A72 1.6 GHz
11 W Power
16,000 Coremark
2 Neon Units

23mm x 23mm
780 pin
FC-PBGA Package



1588 Development Roadmap

Q1 2017

- Platforms
 - LS1043A RDB
 - LS1046A RDB
 - LS1021A TSN
- Linux PTP Master/Slave Support
- Boundary Clock (LS1021A)

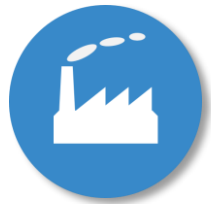
Q2 2017

- Boundary Clock (LS1043A, LS1046A)

Q3 2017

- Platforms
 - LS1021A TSN
 - LS1043A RDB
 - LS1046A RDB
- Power Profile
- Telecom Profile
- Transparent Clocking (LS1021ATSN)
- 1-step timestamping (LS1021ATSN)

Industrial Success Stories – Robotics Controller



Customer's Product

- Robotics Controller
 - Computing power: 2 X ARM A72
 - Real-time Data Calculation
 - Linux-OS (with Real Time Preempt Patches)
 - 2 Lane PCIe Endpoint
 - 1 Lane PCIe Root Complex
 - Fanless embedded system



Customer's Challenges

- Faster time to market
- Longevity of product >15 Years
- Standard ARM 64 Bit core
- Real-time system performance
- System power dissipation < 15W
- First ARM design

Industrial Success Stories – Robotics Controller



NXP's Solutions

- LS1026
 - 2 X ARM A72
 - 3x PCIe 3.0 controllers
 - IEEE 754 Floating Point Compliance
 - Linux Ramdisk loaded via PCIe
 - Linux Software Development Kit with Linux 4.x Kernel – Yocto, kernel.org and NXP.com

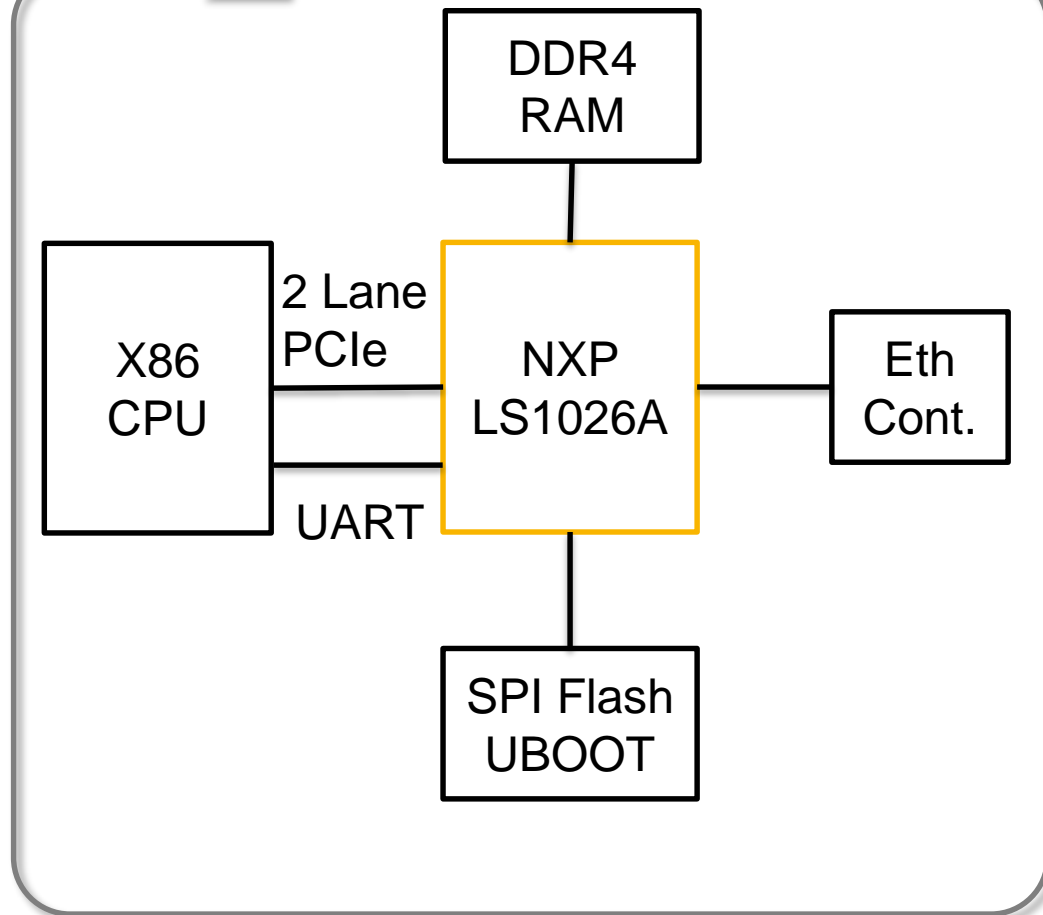
Closing the Deal

- Engage end-customer as alpha customer on LS1046/LS1026
- Provided schematics review for customer
- Regular communication in place NXP / Disty FAE and End customer during evaluation phase
- Assistance debugging PCIe Endpoint with x86 Root Complex

Industrial Success Stories – Robotics Controller



Block Diagram



Competitors

- Intel



Customer's Product

- Motion Controller
 - Computing power: 2 X ARM A53, 4 x ARM A53
 - Real-time Data Calculation
 - Real-time VxWORKS OS
 - PCIe Controller or 16 bit parallel interface to ASIC
 - Fanless embedded system



Customer's Challenges

- Faster time to market
- Longevity of product >15 Years
- Standard ARM 64 Bit core
- Real-time system performance
- Low power < 5W for SoC
- Scalable to higher compute performance

Industrial Success Stories – Motion Controller



NXP's Solutions

- LS1023A/LS1043A
 - 2 X ARM A53/4 X ARM A53
 - 3 x PCIe 2.0 Controllers
 - Integrated Flash Interface for 16 bit parallel bus
 - 2x DUART
 - 6x Integrated Gigabit Ethernet Controllers
 - eSDHC for SD card
 - Pin compatible with 4 x A72 SoC (LS1046)

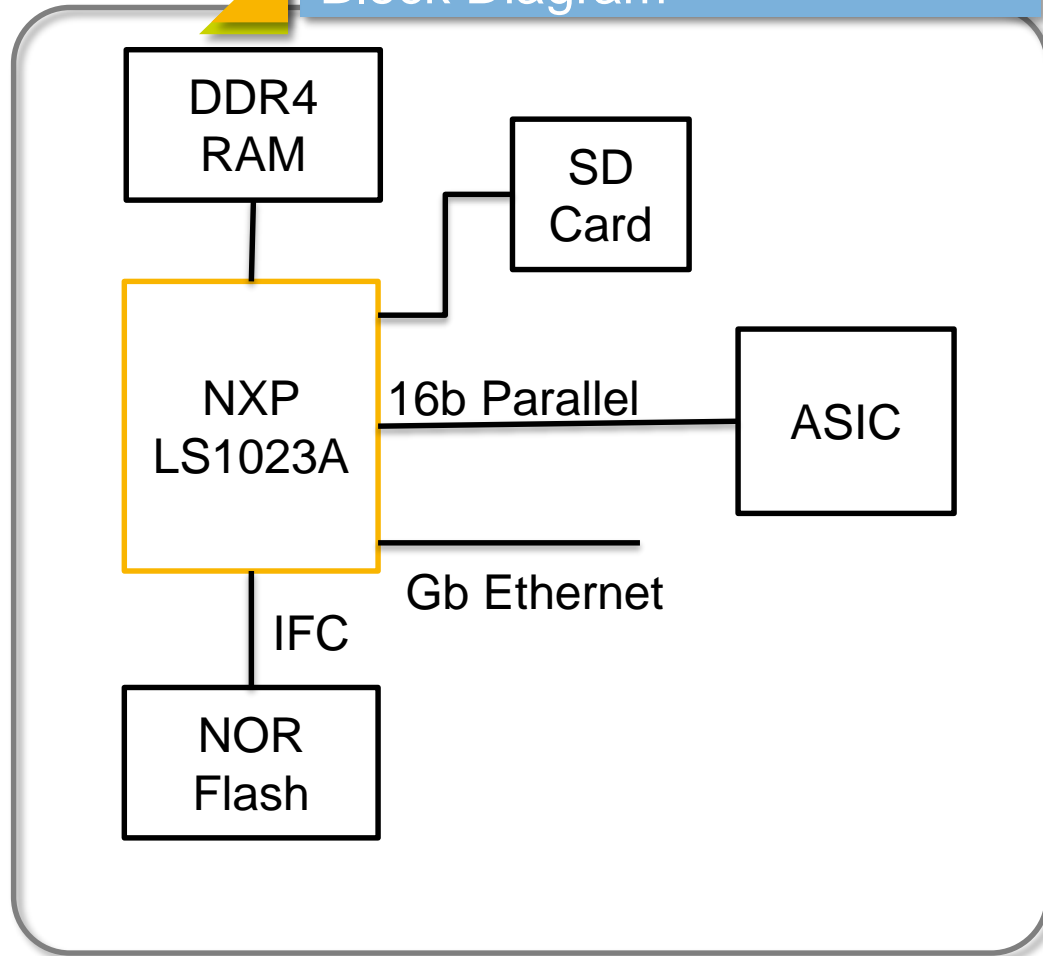
Closing the Deal

- Provided early LS1043A and LS2085A RDBs for A53 and A57 evaluation
- Delivered early LS1043A samples for prototype boards
- Close relationship with WindRiver to ensure 64-bit VxWORKS met customer schedule on the LS1043A

Industrial Success Stories – Motion Controller



Block Diagram



Competitors

- Xilinx

OPEN-IL

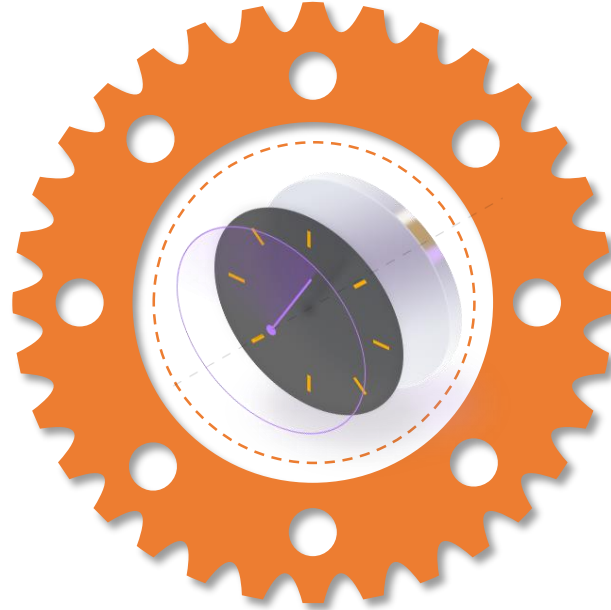


INDUSTRIAL-GRADE CONTROL



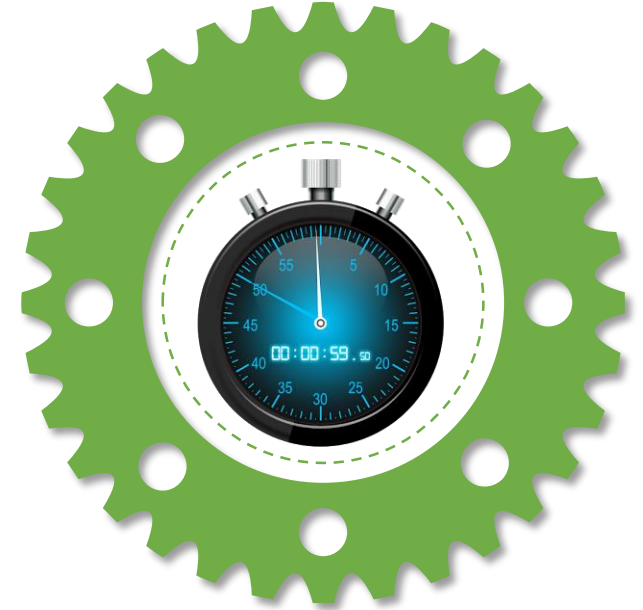
Determinism

- All industrial control networks require some level of determinism
- Determinism needs to be addressed at all levels of the network stack
- Determinism at Ethernet level is critical to industrial applications



Time Precision

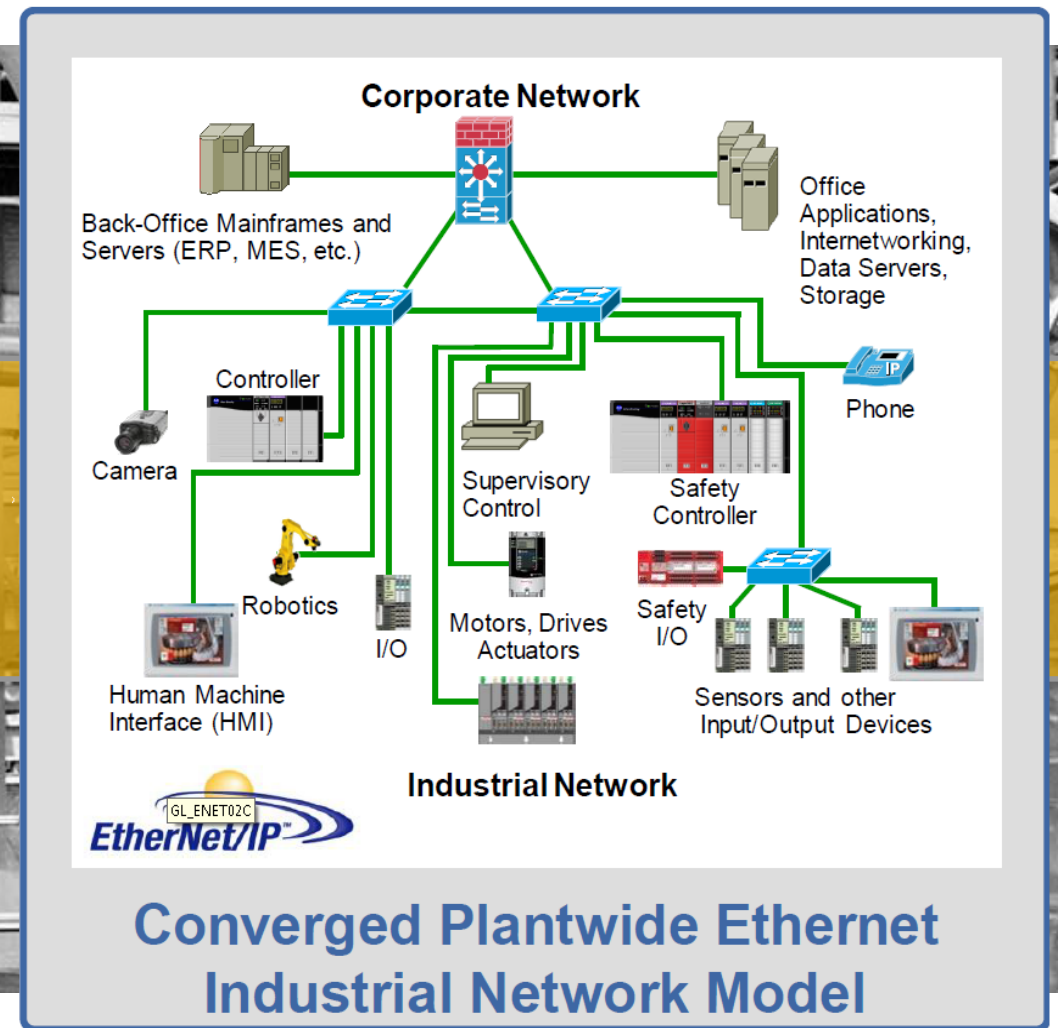
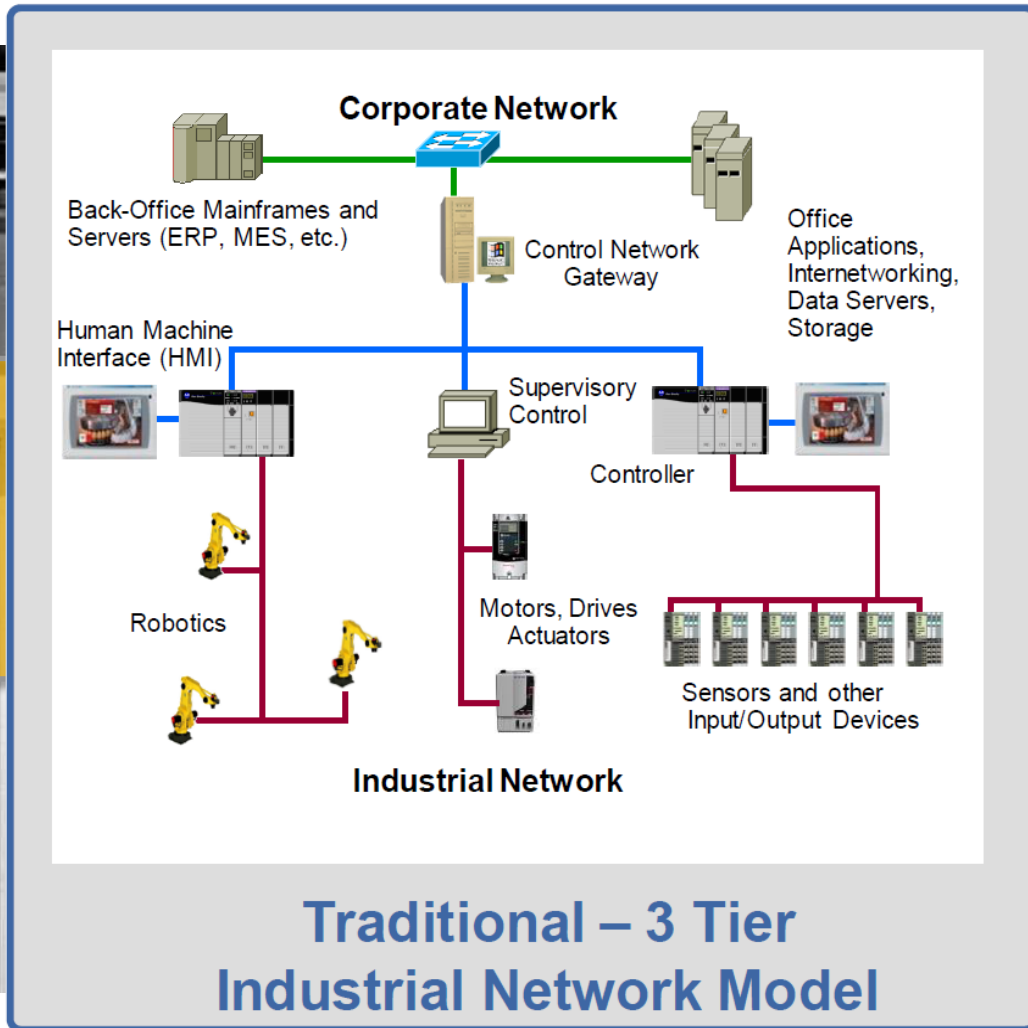
- Many emerging real-time Industrial Ethernet solutions require cycle times as low as a few microseconds
- Precise time distribution is crucial to understand sequence of events (e.g. identifying origin of a power failure)



Real Time

- Real-time error detection and recovery is key to industrial networks (e.g. DLR beacons need to be sent every 400 μ s)
- Industrial network has more strict requirements on latency and jitter (e.g. IEEE 802.1AS specified the maximum latency for PTP packets is 10ms)

MIGRATION TO ETHERNET



REQUIREMENTS FOR INDUSTRIAL SOFTWARE PLATFORM



**Open Software
Platform**



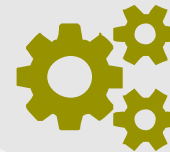
**Connectivity
and Industrial
Networking**



**Security and
Trust
Computing**



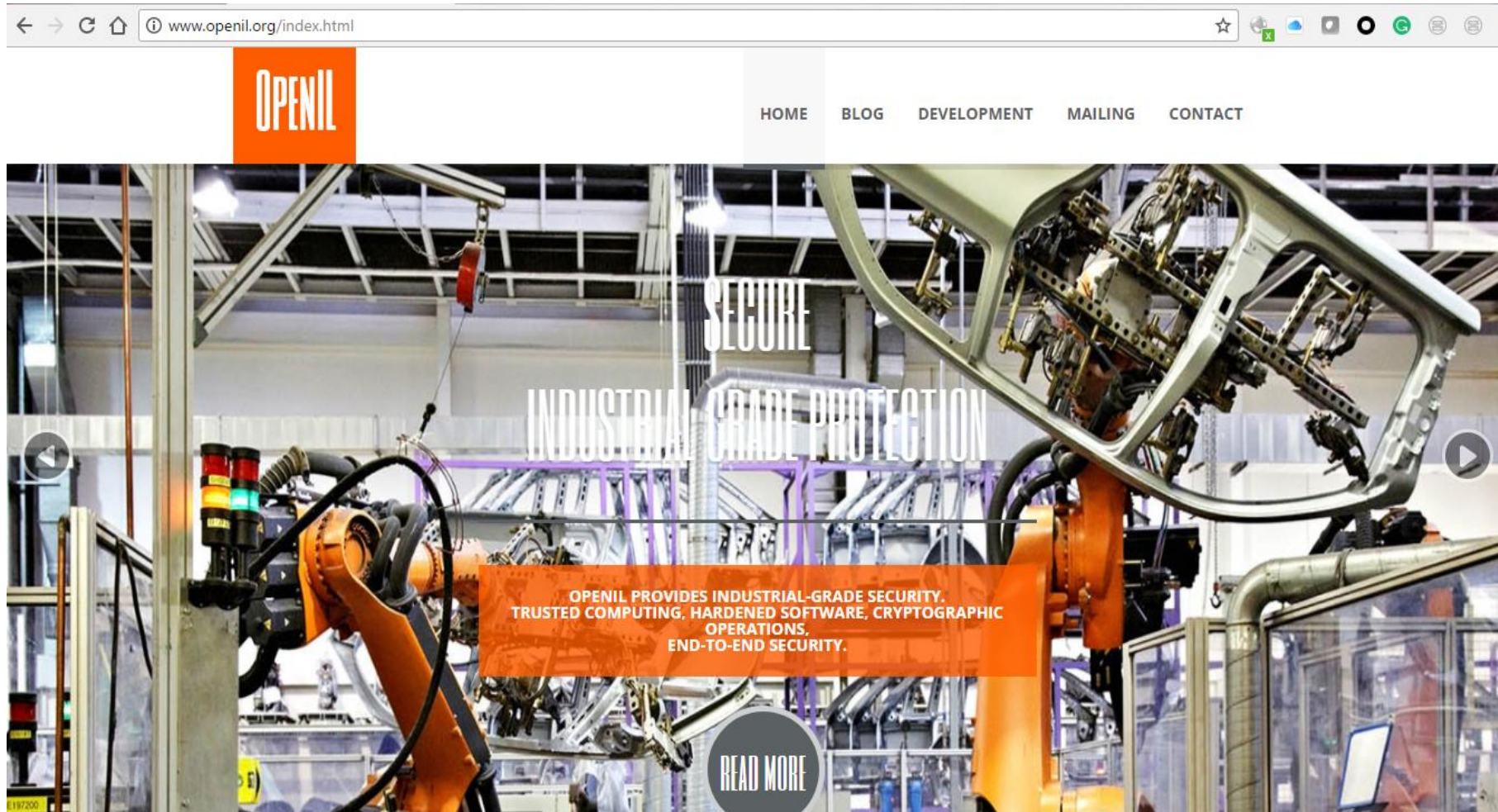
**Operation and
Platform
Manageability**



**Precision and
Determinism**



OpenIL: Open Industrial Linux



- Secure boot
- OP-TEE
- SELinux
- Secure updates
- Secure Provisioning tool



OpenIL: Open Industrial Linux

www.openil.org/index.html

OPENIL

HOME BLOG DEVELOPMENT MAILING CONTACT

PRECISE
IEEE1588 TIME DISTRIBUTION

OPENIL SUPPORTS FULL IEEE1588 PTP IMPLEMENTATION.
FULL INTEGRATED INDUSTRIAL PROTOCOLS AND APPLICATIONS.
FIELD TESTED EXTENSIVELY.

READ MORE

- IEEE1588 Boundary clock
- IEEE1588 Transparent clock
- Fast convergence
- 20ns clock offset



OpenIL: Open Industrial Linux

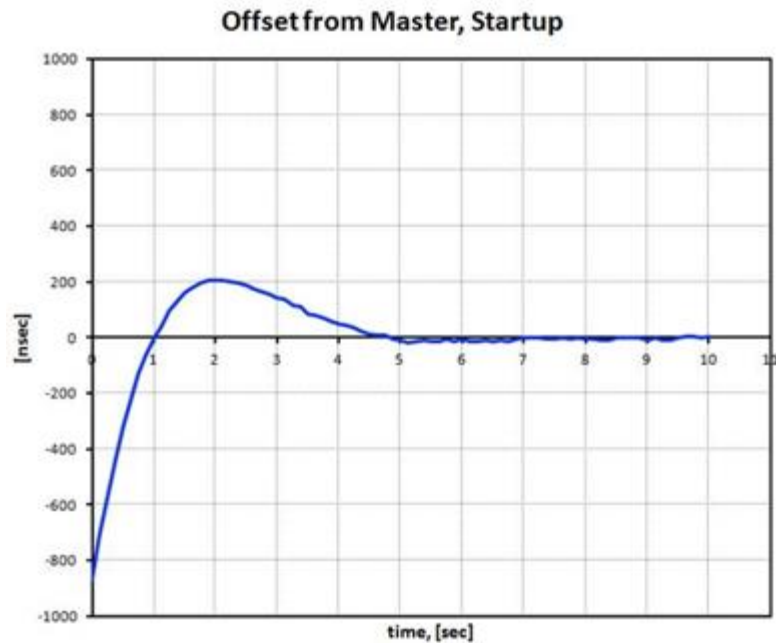


Figure 4-2 Offset from Master in Startup Stage

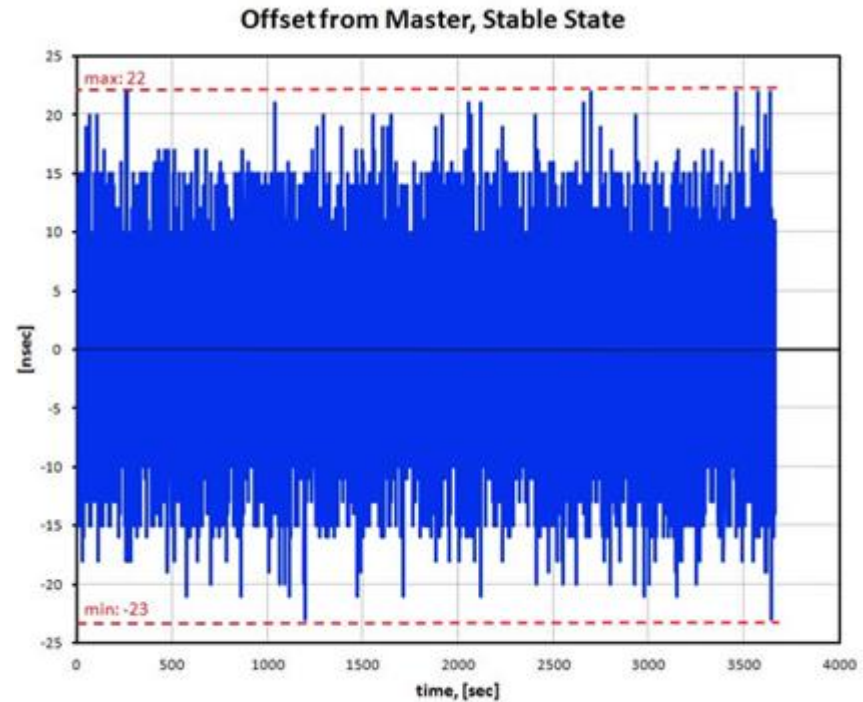


Figure 4-3 Offset from Master in Stable State

- IEEE1588 Boundary clock
- IEEE1588 Transparent clock
- Fast convergence
- 20ns clock offset



OpenIL: Open Industrial Linux

www.openil.org/index.html

OPENIL

HOME BLOG DEVELOPMENT MAILING CONTACT

REAL-TIME
ROBUST RESPONSIVE SOFTWARE

OPENIL PROVIDES TRUE REAL-TIME SOFTWARE PLATFORM.
XENOMAI REAL-TIME LINUX KERNEL, PROFESSIONALLY DEVELOPED
AUTOMATION SOFTWARE, TESTED AND VALIDATED.

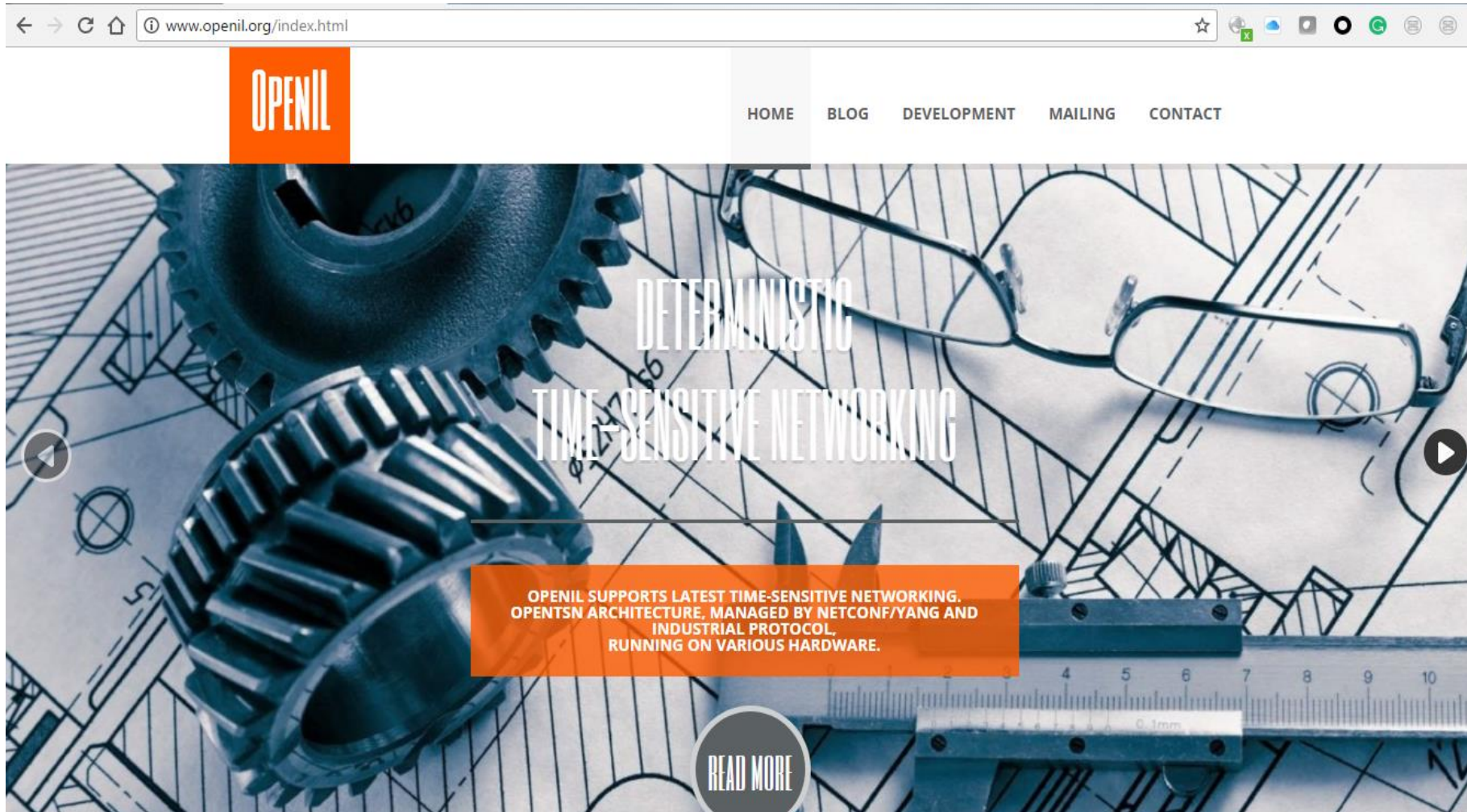
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- A72 ARM64 core
- 1.8GHz core freq
- Fast boot
- Xenomai Cobalt mode

latency min (us)	latency avg (us)	latency max (us)
0.24	0.279	0.68



OpenIL: Open Industrial Linux




- TSN support
- SJA1105 TSN switch support
- LS1028 TSN support – TSN endpoint and TSN switch
- Netconf/Yang remote configuration



OpenIL: Open Industrial Linux

GitHub, Inc. [US] | <https://github.com/openil/>



openil

Repositories People 0

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openil
OpenIL is an open source project based on Buildroot and designed for embedded industrial solution.
● Makefile Updated 4 days ago

linux
linux source code for openil
● C Updated on May 26

u-boot
U-Boot source code for openil
● C ★ 1 Updated on May 18

linuxptp
PTP IEEE 1588 stack for Linux
● C Updated on May 18

sja1105-tool
The sja1105-tool is a Linux userspace application for configuring the NXP SJA1105 Automotive Ethernet L2 switch.
● C ★ 1 Updated on May 18

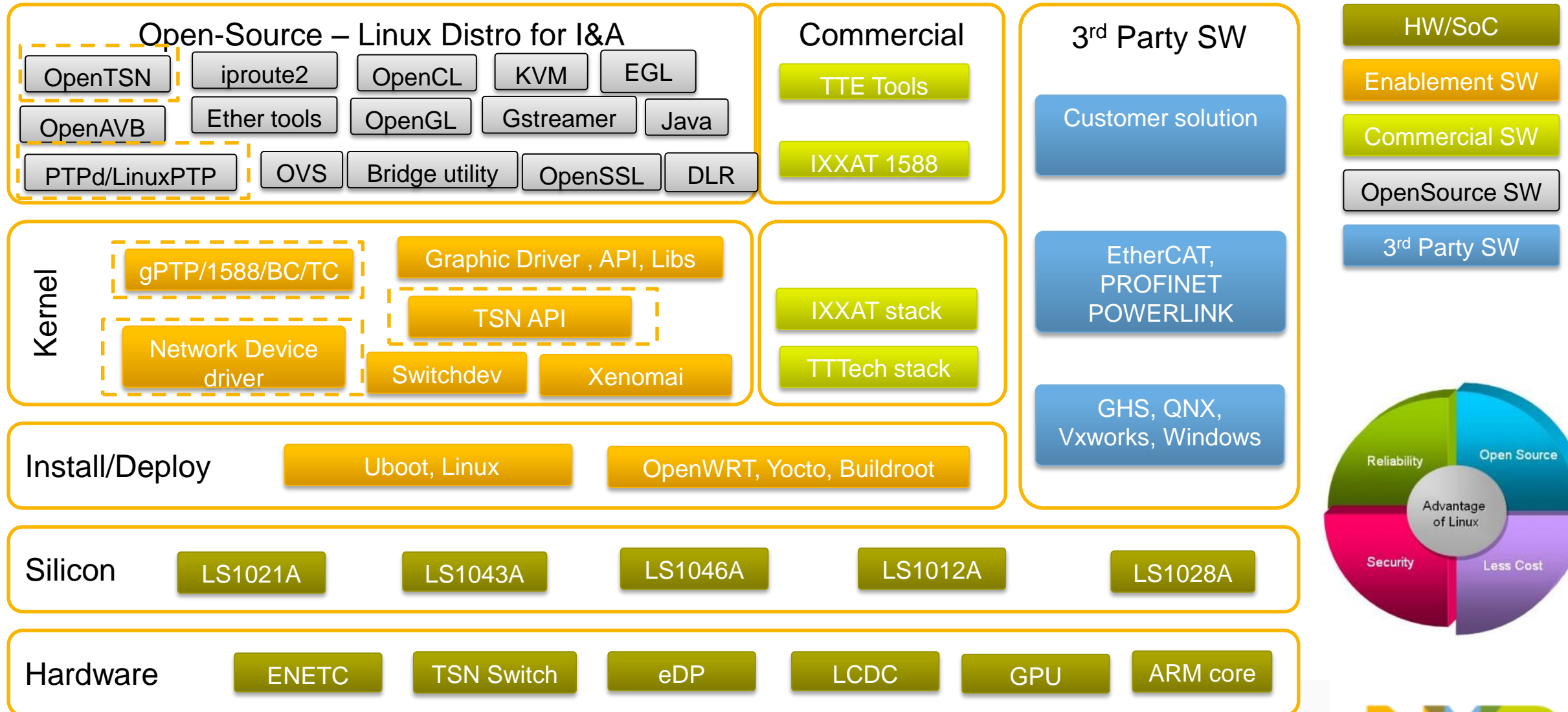
Top languages
● C ● Makefile

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- Opensource platform



INDUSTRIAL SOLUTION COMPONENTS





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