Advanced Vehicle Networking
AMF-AUT-T0502

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Content

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• Networking Protocols
• Networking future trends
• Roadmaps
• Competitive advantage
• Conclusions
Introduction: Complex Electric/Electronic System

Today:

~40 electric/electronic systems, 50-100 microprocessors, >100 sensors within modern mid-size cars

Source: Bosch
Car Network Protocols
Communication Protocols Landscape

- **LIN**
  - 20 kBit/sec
  - Event triggered
  - Master-slave
  - Single wire bus

- **LS**
  - 125 kBit/sec
  - Event triggered
  - Two wire bus

- **HS**
  - 1 MBit/sec
  - Event triggered
  - Two wire bus

- **CAN FD**
  - 1 MBit/sec - Arb
  - 8 Mbit/sec - Data
  - Two wire bus

- **MOST150**
  - 150 MBit/sec
  - Synchronous
  - Plastic fibre optical / Unshielded twisted-pair

- **MOST50**
  - 50 MBit/sec
  - Synchronous
  - Unshielded twisted-pair

- **MOST25**
  - 25 MBit/sec
  - Synchronous
  - Plastic fibre optical

- **MOST150**
  - 150 MBit/sec
  - Synchronous
  - Plastic fibre optical / Unshielded twisted-pair

- **FlexRay**
  - 10 MBit/sec
  - Time triggered
  - Fault tolerant, dependable
  - 2x2 wire

- **MOST150**
  - 150 MBit/sec
  - Synchronous
  - Plastic fibre optical / Unshielded twisted-pair

- **CAN FD**
  - 1 MBit/sec - Arb
  - 8 Mbit/sec - Data
  - Two wire bus

- **MOST50**
  - 50 MBit/sec
  - Synchronous
  - Unshielded twisted-pair
CAN FD Summary

• **Motivation**
  - Bandwidth need is on the increase
    - E.g. Future growth, functional safety
  - Increased demand for >8 byte message
    - E.g. Software authentication
  - Improve fault confinement
    - Notification of system bus degradation
  - Provide CAN upgrade path without major network re-design

• **New Features added**
  - Increase Bit Rate
    - Arbitration phase: up to 1Mbps; Data phase: up to 8Mbps
  - Increase Payload
    - Up to 64bytes
  - Error status indicator

• **Remote frames not supported**
CAN FD Summary

- **EDL** – Extended Data Length
  - EDL = recessive indicates CAN FD frame format
  - EDL = dominant indicates standard CAN frame format

- **r1, r0** – reserved bits
  - RTR replaced by r1 in CAN FD base and extended frames

- **BRS** – Bit Rate Switch
  - BRS = recessive: switch to alternate bit rate
  - BRS = dominant: do not switch bit rate

- **ESI** – Error State Indicator
  - ESI = recessive: transmitting node is error passive
  - ESI = dominant: transmitting node is error active

- **New DLC-coding and CRC**
## CAN FD Summary

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>CAN 2.0</th>
<th>CAN FD</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum payload length [bytes]</td>
<td>8</td>
<td>64</td>
<td></td>
</tr>
<tr>
<td>Payload bandwidth for functional messages</td>
<td>16</td>
<td>68</td>
<td>Approx four times higher functional bandwidth</td>
</tr>
<tr>
<td>[bytes/ms at 50% bus utilization]</td>
<td>11-bit ID, 0.5 Mbit/s, 8 bytes payload</td>
<td>11-bit ID, 2 Mbit/s payload, 0.5 Mbit/s arbitration, 32 bytes payload</td>
<td></td>
</tr>
<tr>
<td>Detection of bit errors and/or degradations</td>
<td>Medium</td>
<td>Good</td>
<td>Improved detection and self diagnostics</td>
</tr>
<tr>
<td></td>
<td></td>
<td>error status indicator flag, enhanced CRC polynomials</td>
<td></td>
</tr>
</tbody>
</table>

- Note: Max payload bandwidth for CAN FD >>68 if full 64bytes used and data bit rate 8Mbps. Can achieve up to approx 10x improvement
CAN FD Summary

• **Use Case 1: Fast SW Download**
  
  **Standard data rate** – 500 kb/s
  
  **FD data rate** – 2 Mb/s
  
  - Time to transmit 4 standard CAN message with 8 data bytes and 15% stuff bits - 1021 μs
  
  - Time to transmit 1 CAN FD message with 32 data bytes and 15% stuff bits - 229 μs
  
  - CAN FD message allow greater transfer data rates than CAN2.0. Thus, reducing re-programming time

• **Use Case 2: Longer message support - Avoid Splitting of long messages**
  
  - Secure 8 Byte CAN message by additional MAC (Message Authentication Code)
  
  - Example (2): Transmission of acceleration sensor data in x,y,z-direction
Communication Protocols Landscape

bit rate [bits/s]

- **Lin**: 20 kBit/sec
  - Master-slave
  - Single wire bus

- **LIN**: 20 kBit/sec
  - Event triggered
  - Fault tolerant
  - One/two wire bus

- **CAN FD**: 1 MBit/sec
  - 8 Mbit/sec
  - Two wire bus

- **HS CAN**: 1 MBit/sec
  - Event triggered
  - Two wire bus

- **LS CAN**: 125 kBit/sec
  - Event triggered
  - Two wire bus

- **MOST25**: 25 MBit/sec
  - Synchronous
  - Plastic fiber optical

- **MOST50**: 50 MBit/sec
  - Synchronous
  - Unshielded twisted-pair

- **MOST150**: 150 MBit/sec
  - Synchronous
  - Plastic fiber optical

- **Ethernet**: 100 MBit/sec
  - Synchronous
  - Twisted-pair

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  - Time triggered
  - Fault tolerant, dependable
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- **Ethernet**: 100 MBit/sec
  - Twisted-pair
Ethernet Summary

- Widely used network standard (IEEE 802.3) for LANs
- Several speed grades:
  - 10 baseT, 100 baseT, 1000 baseT....
- Auto qualified Physical layer based on Unshielded twisted pair (TP) wire
- Multiple Phy to MAC Interfaces
  - MII, MII_Lite, RMII, GMII, RGMII, ....
- Duplex and Half duplex communication
- Ethernet already established in vehicle
  - Diagnostics, Ethernet camera
  - Ethernet AVB being introduced
- Broad offering of software stacks, tools, expertise makes use of Ethernet cost attractive
**Type II Format**

- Original format – Ethertype defines payload encapsulation
- 802.2 Header in payload to define frame type
- Optional 802.1Q VLAN Tag after MAC SA
- Preamble and Start of Frame are identified by PHY
- Inter frame gap is enforced by PHY
- PHY detects and informs MAC of collisions
Ethernet (Layer 2)

• EtherType field used to identify higher layer protocols in payload
  - 0x0800 = IPv4
  - 0x86DD = IPv6
  - 0x0806 = ARP
  - 0x8100 = VLAN
  - ..................

• CRC 32 validated over MAC header and payload
Ethernet AVB Summary

- IEEE 802.1 Audio/Video Bridging (AVB) standards enable time-synchronized low latency streaming services through 802 networks.
  - Ensures interoperability between devices using AVB
- AVB technology allows network to reserves the necessary bandwidth and resources
  - Ensure that the signal reaches its destination in a precisely pre-determined amount of time synchronized across all outputs.
  - Aim is to minimise the amount of buffering to keep costs down
- Four IEEE 802.1 AVB standards form the foundation of AVB technology
  - IEEE 802.1AS (PTP): “Timing and Synchronization for Time-Sensitive Applications in Bridged Local Area Networks.”
  - IEEE 802.1Qat (SRP): “Virtual Bridged Local Area Networks - Amendment 9: Stream Reservation Protocol (SRP).”
  - IEEE 802.1Qav (Qav): “Virtual Bridged Local Area Networks - Amendment 11: Forwarding and Queuing for Time-Sensitive Streams.”
  - IEEE 802.1BA: “Audio/Video Bridging(AVB) Systems”
AVB Ethernet stack summary

- IEEE 802 Ethernet Driver
  - Low level driver for MAC
- IEEE 802.1AS (PTP)
  - Used to synchronise network nodes to a common time reference
    - Defines clock master selection (BMCA) and negotiation algorithms
    - Link delay measurement, and compensation
    - Clock rate matching and adjustment mechanisms.
  - Specifies use of IEEE 1588
- IEEE 802.1 QAT (Bandwidth reservation)
  - Stream reservation protocol (SRP).
    - Used to guarantee QoS by ensuring end to end bandwidth availability before an AV stream starts.

AVB Ethernet stack summary

• IEEE 802.1 QAV (Shaping)
  - Queuing and forwarding protocol to ensure asynchronous Ethernet traffic does not interfere with steaming AVB traffic.
    • Allows bridges to provide guarantees for time-sensitive (i.e. bounded latency and delivery variation), loss-sensitive real-time audio video (AV) data transmission (AV traffic).
    • Standard uses the timing derived from IEEE 802.1AS

• IEEE 1722 AVTP (Time sensitive streaming)
  - AVTP specifies methods to transport audio/video data and timing information so that audio/video content sent by a Talker can be reproduced.

IEEE 1722.1

- IEEE P1722.1 defines the higher layer protocol for IEEE P1722 based devices. It specifies an application procedure for the AVB network systems. This standard covers:
  - Service discovery – Identifies other 1722.1 capable nodes
  - device enumeration
  - connection management
  - Connects/disconnects virtual links between media sources/sinks
  - device control protocols:
Future trends
Future Trends

- Cross-domain car communication
  E.g. increasing safety enabled by data interaction between active safety and advanced driver assistance functions
- Networking of Cars and Environment
  Car2car communication for efficient organization of traffic flow
- More comfort and safety features in the car
  - Camera’s, TFT displays, connectivity, functional safety
  - Example for average car
    - ~40 electric/electronic systems
    - 50-100 MCUs
    - >100 sensors
- Memory and performance on the increase
  - Modern car up to 50Mbyte (excludes infotainment)
Future Trends

• Move to integrate more functions into larger “domain controllers”
  - Reduce costs, integration complexity and wiring harness weight

• High bandwidth backbone interconnect network needed
  - Manage the network complexity to reduce the development effort and increase fault tolerance and robustness of the network
  - Higher demand on bandwidth and quality of service
Future Trends

- **Ethernet for Automotive**
  - Ethernet already introduced into vehicle
  - Cost of Ethernet reducing
  - Increased bandwidth options (scalability)
  - Possible to stay below electromagnetic compatibility (EMC) emissions limit with low cost UTSP
  - Ethernet is a well-known and mature network structure
  - Many developers have Ethernet experience
  - Simple integration of consumer devices
  - Availability of hardware, software and low-cost and freeware tools
Roadmap
<table>
<thead>
<tr>
<th></th>
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<tbody>
<tr>
<td><strong>Entry BCM</strong></td>
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<tr>
<td>MPC5604/3/2/B/C</td>
<td>z0, 64MHz, Up to 512k Flash, 48k RAM CAN, LIN</td>
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<tr>
<td>MPC5602/1D</td>
<td>z0, 48MHz, Up to 256k Flash, 16k RAM CAN, LIN</td>
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<tr>
<td><strong>Mid-High BCM</strong></td>
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<tr>
<td>MPC5607/6/5/B</td>
<td>z0, 64MHz, Up to 1.5M Flash, 96k RAM CAN, LIN</td>
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<tr>
<td>MPC5646/5/4B</td>
<td>z0, 120MHz, Up to 3M Flash, 192k RAM, Flex, Security, CAN, LIN</td>
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<tr>
<td>MPC5646/5/4B</td>
<td>z4, 120MHz, Up to 3M Flash, 256k RAM, Flex, Ether, Security, CAN, LIN</td>
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<tr>
<td><strong>Integrated Gateways</strong></td>
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<tr>
<td>MPC5668E</td>
<td>z6+z0, 116MHz, Up to 2M Flash, 598k RAM Flex, Ether, MLB, CAN, LIN</td>
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<tr>
<td>MPC5668G/E</td>
<td>z6+z0, 116MHz, Up to 2M Flash, 598k RAM Flex, Ether, MLB, CAN, LIN</td>
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</tr>
<tr>
<td>MPC5748/7/6G</td>
<td>z4+z4+z2, 160MHz, 3M-6M Flash, Flex, Ether, Security, MLB, USB, CAN, LIN</td>
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</tr>
<tr>
<td>MPC5746/5/4G</td>
<td>z4+z2, 160MHz, 1.5M to 3M Flash, Flex, Ether, Security, CAN, LIN</td>
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<tr>
<td>MPC5746/5/4B</td>
<td>z4, 160MHz, 1.5M to 3M Flash, Flex, Security, CAN, LIN</td>
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<tr>
<td>MPC5746/5/4C</td>
<td>z4+z2, 160MHz, 1.5M to 3M Flash, Flex, Ether, Security, CAN, LIN</td>
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</tbody>
</table>

**Fado/Bolero 90nm Products**

- MPC5604/3/2/B/C: z0, 64MHz, up to 512k Flash, 48k RAM CAN, LIN
- MPC5602/1D: z0, 48MHz, up to 256k Flash, 16k RAM CAN, LIN
- MPC5607/6/5/B: z0, 64MHz, up to 1.5M Flash, 96k RAM CAN, LIN
- MPC5646/5/4B: z4, 120MHz, up to 3M Flash, 192k RAM, Flex, Security, CAN, LIN
- MPC5668E: z6+z0, 116MHz, up to 2M Flash, 598k RAM Flex, Ether, MLB, CAN, LIN
- MPC5668G/E: z6+z0, 116MHz, up to 2M Flash, 598k RAM Flex, Ether, MLB, CAN, LIN

**Next Generation Products**

- MPC5748/7/6G: z4+z4+z2, 160MHz, 3M-6M Flash, Flex, Ether, Security, MLB, USB, CAN, LIN
- MPC5746/5/4G: z4+z2, 160MHz, 1.5M to 3M Flash, Flex, Ether, Security, CAN, LIN
- MPC5746/5/4B: z4, 160MHz, 1.5M to 3M Flash, Flex, Security, CAN, LIN
- MPC5746/5/4C: z4+z2, 160MHz, 1.5M to 3M Flash, Flex, Ether, Security, CAN, LIN

**Roadmap Details**

- **Integrated Gateways**
- **Mid-High BCM**
- **Entry BCM**

**Timeline**

- **Past**
- **2012**
- **2013**
- **2014**
- **2015**
- **2016**

**Products**

- **MPC5604/3/2/B/C**
- **MPC5602/1D**
- **MPC5607/6/5/B**
- **MPC5646/5/4B**
- **MPC5668E**
- **MPC5668G/E**
- **MPC5748/7/6G**
- **MPC5746/5/4G**
- **MPC5746/5/4B**
- **MPC5746/5/4C**

**Technology**

- Single Core
- Dual Core
- Triple Core

**Security**

- First Sample Date (left edge)
- Product Qualification (right edge)

**Freescale Semiconductor**
MPC5748C/G - High End Gateway/BCM Solution

Applications:
- High end Gateway and Body Modules

Key Characteristics:
- 2\(x\) e200z4 + 1\(x\) z2 cores, FPU on z4 cores
- 160 MHz max for z4s and 80 MHz on z2
- HSM Security Module option supports both SHE and EVITA low/medium standard
- Media Local Bus supports MOST communication
- 2 \(x\) USB 2.0 (1 OTG and 1 Host module) support interfacing to 3G modem and infotainment domain
- Ethernet 10/100 Mbps RMII, MII, +1588, AVB
- CAN module optionally supports CAN FD
- SDHC provides standard SDIO interface
- Low Power Unit provides reduced CAN, LIN, SPI, ADC functionality in low power mode
- Designed to ISO26262 process for use in ASIL B
- -40 to +125C (ambient)
- 3.0V to 5.5V

Packages:
- 176 LQFP, 256 BGA, 324 BGA
**S12 MagniV Roadmap**

**Motor Control**
- **S12VRxx (Tomar)**: 2 LS for relay based DC motor control
- **S12ZVMxx (Obidos)**: No PHY (PWM-control) + 6ch-MOSFET pre-driver
- **S12ZVML/Cxx (Carcassonne)**: 6ch-MOSFET pre-driver for BLDC/PMSM motor control
- **S12ZVHxx (Lumen 4W)**: LCD + Gauge

**Instrument Cluster**
- **S12ZVFP (Lumen HVAC)**: LCD
- **S12ZVH (Lumen 2W)**: LCD + Gauge

**Multi-PHY companion chip**
- **S12ZVAL (Teck)**: 3ch LED-drive Ambient Lighting

**Lighting**
- **S12ZVCxx (Hearst)**: 150°C
- **S12ZVL (Knox)**: 150°C

**General Purpose**
- **PSI5 - enabled**
- **CAN - enabled**
- **lin - enabled**

**Production**
- **First Sample Date (left edge)**
- **Product Qualification (right edge)**

**Other comms (eg. PWM-control)**
## What’s S12 MagniV?

<table>
<thead>
<tr>
<th>Semi-Discrete Solution (Multi-Chip)</th>
<th>Multi-die SiP</th>
<th>Monolithic SiP</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Standard MCU</td>
<td>• Single package</td>
<td>• MCU and Analog on the same die</td>
</tr>
<tr>
<td>• Application Specific Analog IC (ASIC)</td>
<td>• Die-to-die bonding</td>
<td></td>
</tr>
</tbody>
</table>

SiP = System in Package
## S12 MagniV Benefits

<table>
<thead>
<tr>
<th>Product Specific Benefits</th>
<th>Tomar</th>
<th>Carcassonne</th>
<th>Knox</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bill of Material Reduction</td>
<td>LIN phy VREG + Vsense 2xLS for relays 2xHS</td>
<td>LIN phy VREG + Vsense Gate Driver 2xOp-amps</td>
<td>LIN phy VREG + Vsense</td>
</tr>
<tr>
<td>PCB Space</td>
<td>2-3cm²</td>
<td>2-6cm²</td>
<td>1-2cm²</td>
</tr>
<tr>
<td>Manufacturing Cost</td>
<td>Fewer components to mount (pick &amp; place)</td>
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</tr>
<tr>
<td>General Benefits</td>
<td>Fewer solder joints → fewer points of failure</td>
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</tr>
<tr>
<td>Logistics</td>
<td>Fewer parts to qualify, source, store, track, etc…</td>
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</tr>
</tbody>
</table>
S12 CPU with an integrated Voltage regulator, LIN physical layer and HS/LS-drivers for Relay-driven Windowlift-motor
S12VRx – "High Voltage" Integration

LIN Physical Layer
LIN 2.1 compliant
+/- 8kV ESD capability

2 Low-Side Drivers
Protected LS Drivers to drive brushed DC Motor Relays

LIN Physical Interface
SCI 0
6ch. 10bit ADC + 8 int. Ch.

S12-core
48kB /64kB Flash

512Bytes EEPROM
2 kB RAM

2 HS Drivers

Vreg
5V VDDX1, 5V VDDX2

Vbat sense
Supply sense before and after protection diode

Up to 2 HS drivers
For LED and Switch supply

Voltage Regulator
No Ext regulator reqd
20mA to drive offchip components

Hall Supply
5V, 20mA,
Over curr. ctrl

Digital Components
5V Analogue Components

MCU Core and Memories
High-Voltage Components
16-bit MCU with 12/5V voltage regulator, LIN physical layer, and MOSFET pre-drivers for DC and BLDC motors
Carcassonne – S12ZVML128

- **Target applications:**
  - BLDC motor control
  - DC motor control

- **Key Features:**
  - S12Z CPU @ 50MHz bus speed
  - Embedded VREG
  - LIN phy, LIN2.1 compliant
  - Embedded GDU for 3ph BLDC
  - Embedded EE
  - 1x MSCAN controller
  - 2xSCI, 1xSPI
  - Dual 12bit ADC, synch with PWM
  - 20mA/5V EVDD sensor supply pin
  - 2x Op-amp for current sense (each needs 3 pins mux’d with ADC inputs)
  - 64LQFP-EP 10x10/0.5mm
General Purpose S12 MagniV 16-bit MCU with 12/5V voltage regulator, LIN-physical layer
**Key Features:**

- On chip 12V Vreg with Supply-capability:
  - 70mA total (170mA with ext. Ballast)
- LIN-PHY, LIN2.1 compliant
- On chip RC Oscillator; trimmed to +/- 1.3% tolerance over full temperature range
- Robust 12V inputs Vsup-sense & HVI (with ADC)
- 1x E-Vdd (20mA source capability)
- 1-3x N-GPIO (25 mA sink capability)
- 10Bit ADC
- EEPROM 4-Byte-erasable
- Ambient temperature-range: -40°C ... +125°C
- 5x5mm footprint 32QFN-package optional
- ASIL-A compliancy
Freescale Competitive Advantage
Freescale Competitive Advantage

- Calypso 6M highest end gateway device on the market
- Knowledge of networking and G/W requirements
- Ethernet based products in series production
  - First Ethernet Gateway
  - Ethernet camera application based on Salsa product
- Comprehensive Ethernet roadmap
  - 10/100/1000 Mbit/sec
  - Leader in automotive AVB applications
    - Steaming software
    - Specific AVB features in Ethernet IP to offload CPU
- Active member of CAN FD working groups
- Early to market with CAN FD
  - Supports interleaving CAN 2.0 and CAN FD frames
  - Flexible buffer management
Freescale Competitive Advantage

• MagniV Roadmap
  – Monolithic HV technology built upon proven high volume standard CMOS process
  – Integration of high voltage (e.g. CAN Phy, LIN Phy, Vregs)
  – Improved reliability
Conclusion

• Automotive networking market is evolving with the introduction of new protocols
• CAN FD, Ethernet AVB
• Freescale provide support for all protocols in Automotive
• LIN, SENT, CAN2.0, CAN FD, FlexRay, Ethernet and Ethernet AVB, MLB, USB
• Freescale devices developed specifically for gateway market
• Calypso family
• Bolero Family
• Freescale devices support high voltage and power (Magniv)
• LIN Phy, CAN Phy, Vregs
• Lower BOM, higher reliability