

Functional Safety and ISO26262 Compliance APF-AUT-T0503

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Agenda

- Introduction
 - Functional Safety Requirements
 - SafeAssure Program
- Role of the Semiconductor Supplier
 - System Challenges
 - Freescale System Solutions
- Safety Concepts of Freescale's Auto MCUs
 - Integrated Safety Architecture Example
- Safety Software
- Safety Support
 - Dynamic FMEDA
 - System level (beyond MCU)
- Summary









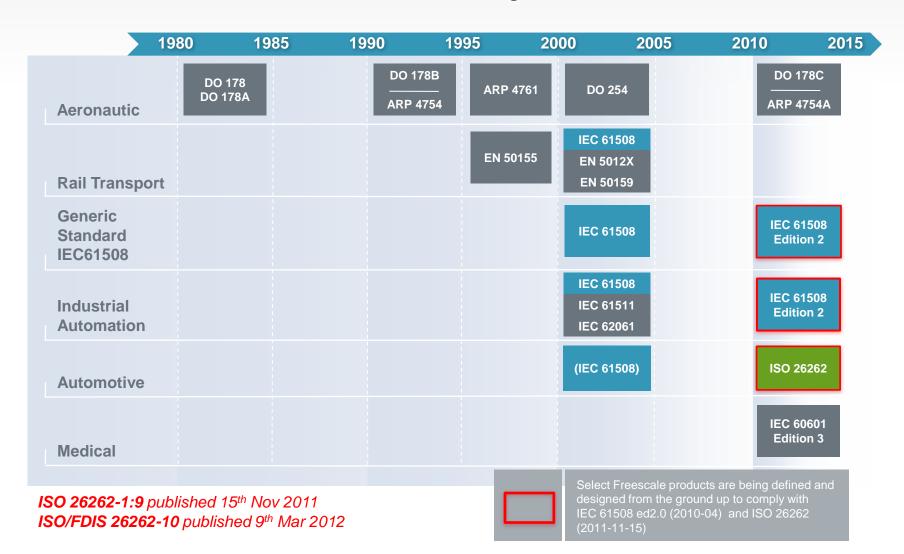
The problem







The World of Functional Safety Standards









ISO 26262 is changing the Automotive Market

- The market trends have one thing in common: If the underlying systems fail, humans can be put at risk
- Functional Safety means "absence of unreasonable risk due to hazards caused by malfunctioning behavior of E/E systems"
- ISO 26262 is the International Standard for Functional Safety. It is applicable to safety-related automotive systems that include one or more E/E systems and that are installed in series production passenger cars with a max gross weight up to 3.5t"
- ISO 26262 addresses
 - architectural & functional aspects
 - procedural aspects (incl. safety lifecycle)
 - to avoid systematic faults and to control random faults
- Safety management is needed from the start of the product development
- Functional Safety will become a standard requirement in future RFQ's, across most applications







ISO 26262 Outline

The ISO 26262 standard

- provides an automotive safety lifecycle which outlines handling of safety system development and operation from project initiation to system decommission
- provides an automotive specific risk-based approach for determining risk classes based on severity, exposure (probability) and controllability of the hazard
- uses four Automotive Safety Integrity Levels (ASIL) for specifying the item's safety requirements
 - ASIL A: the lowest ASIL level
 - ASIL B: at least 90% SPF and at least 60% latent fault (LF, a fault that isn't detected but doesn't lead directly to violation of a safety goal) being detected
 - ASIL C: at least 99% SPF and 90% LF detected
 - ASIL D: the highest ASIL level, at least 99.9% SPF and 99% LF detected
- provides requirements for validation and confirmation requirements to ensure the required safety level is achieved







Determining the ASIL of an Item

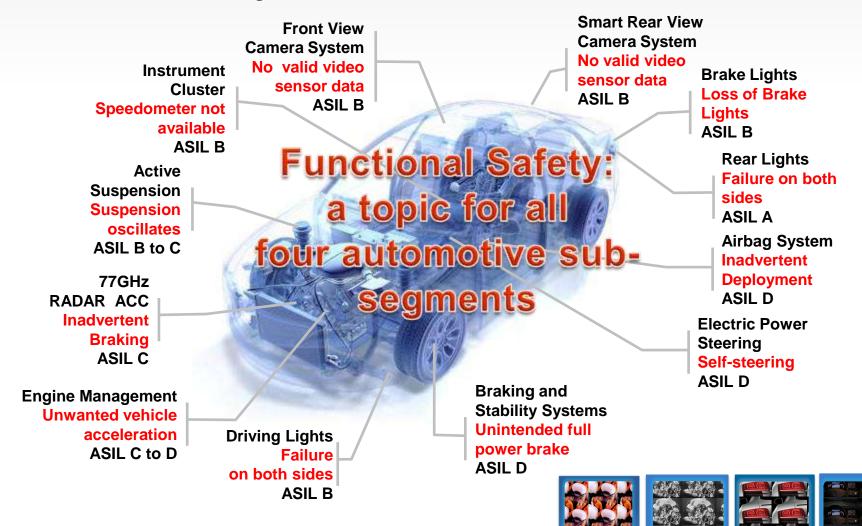
Class of severity	Class of probability of	Classes of controllability		
	exposure regarding operational situations	C1 (simple)	C2 (normal)	C3 (difficult, uncontrollable)
	E1 (very low)	QM	QM	QM
S1	E2 (low)	QM	QM	QM
(Light and moderate injuries)	E3 (medium)	QM	QM	А
	E4 (high)	QM	А	В
S2	E1 (very low)	QM	QM	QM QM
(Severe and life	E2 (low)	QM	QM	Α
threatening injuries [survival probable])	E3 (medium)	QM	А	В
	E4 (high)	А	В	С
S 3	E1 (very low)	QM	QM	А
(Life threatening	E2 (low)	QM	А	В
injuries,	E3 (medium) A B	В	С	
fatal injuries)	E4 (high)	В	С	D

(QM: "quality managed" → no requirements from standard applied explicitly)





Automotive System Trends for ASIL Levels



Source: Freescale: Expectations based on global customer feedback





Powertrain

DIS

IfeAssure Approach: The Four Key Elements

ISO 26262

Automotive Industry standard, adaptation of IEC 61508 for electrical/electronic systems within road vehicles

Integrity levels
ASIL A, ASILB, ASIL C, ASILD
Pub date: 2011

Microcontrollers

Lockstep Cores, ECC on Memories Redundant Functions, Internal Monitors, Built In Self Test, Fault Collection & Control

Analog and Power Management
Voltage Monitors, External Error
Monitor, Advanced Watchdog,

Sensors

Timing Checker, Digital Scan of Signal Chains, DSI3 or PSI5 Safety Data links

Organization

Safety is an integral part of the Freescale world wide organization

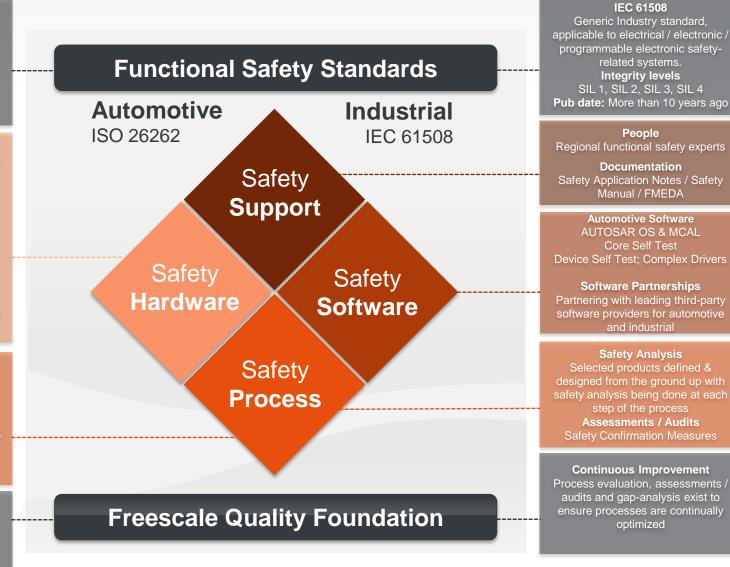
Project Management

Configuration & Change

Configuration & Change
Management, Quality Management,
Requirements Management,
Architecture & Design, Verification
& Validation

Quality Management

ISO TS 16949 Certified Quality Management System Hardware - Zero Defects Software - SPICE Level 3









Role of the Semiconductor Supplier







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Safety Architecture Challenge

- ISO 26262 safety lifecycle defined as top down approach
 - Next level requirements result from previous level
 - In practice also "push-back" due to availability of products with desired functionality and safety measures
- Safety architecture needs to be defined such that it is safe and can be realized in an efficient way
- Possible development options:
 - Commission custom ASICs with application specific safety measures
 - Use off-the shelf components with an integrated safety architecture
 - Many new components emerging in light of ISO 26262 adoption
 - Define major elements of safety architecture at system level
 - Use "standard" off-the shelf components → discrete (component) safety architecture
 - Traditional way of designing a functional safety system







No "best" Safety Architecture exists!

Every embedded application has its very specifics!

Microcontroller are successful due to the general purpose nature (can be adapted to the specifics of an application)

Therefore Freescale provides products with different Multi-Core safety architectures:

- Monolithic integration (safety system on chip)
- Multiple device system level integration (multiple chip ECU)
- Distributed system integration (multiple ECU system)
- À.,

Customer may select their most suitable architecture!





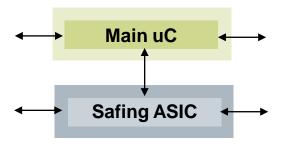


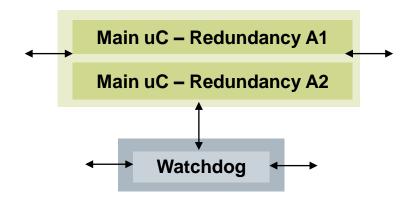
Discrete and Integrated HW Safety Architecture

- Discrete HW Safety Architecture
 - Redundancy resolved at system level by means of redundant components
 - Example: Traditional airbag system consisting of MCU and Safing ASIC
 - System designer performs dependent failure analysis

Integrated HW Safety Architecture

- Redundancy resolved at system level and at component level with redundant modules within a component
- Example: Electric power steering with dual-core lock-step uC
- Component designer performs dependent failure analysis for redundancy at module level









From Integrated to Discrete Safety Architecture

Integrated Safety Architecture		Discrete Safety Architecture
At system level and at component level	Safety Architecture	Resolved at system level
One or more devices contain dedicated safety measures based on an underlying safety concept	Device Level Safety Measures	No underlying safety concept at device level, typically, however, measures exploitable as safety measures available
Available for integrated safety measures	Device Level Safety Manual	None
FMEDA, FTA for dedicated safety measures	Device Level Safety Analysis	None, typically general supporting information sufficient
Safety case, with complete device level argument for ISO 26262 compliance at device level	Device Level Safety Argument	Qualification + optional evaluation of measures in development process against systematic faults







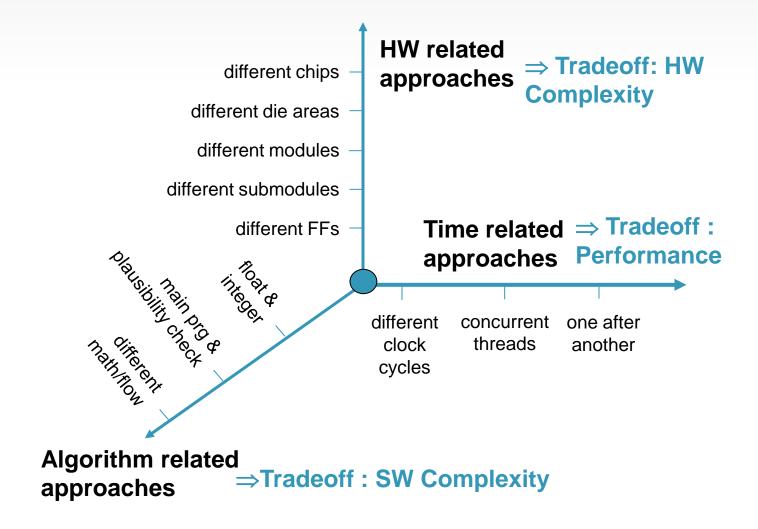
Quantitative ASIL Requirements for HW

	ASILA	ASIL B	ASIL C	ASIL D	
Discrete HW Safety Architecture	Feasible • Discrete safety architecture		 Feasible Discrete safety architecture using uC & separate watchdog or uC Functional and temporal alignment between uC & 2nd channel often challenging Fast recovery from transient faults potentially challenging 		
Integrated HW Safety Architecture	 Feasible However, redunction component level technical overkill Functional safety simplifies demondance 	is typically a enablement	 Feasible Integrated safety dual-core lockste Functional and to between two characters from the feasible 	ep uC emporal alignment nnels simplified	





Tradeoffs of Different Redundancy Approaches







From System Level to Component Level

- Functional safety is not just an issue on system level but also on component level
 - Integrated safety devices (customer has no "direct" access to details of safety functions)
- Functional safety standards explicitly address component level
 - ISO 26262: Safety Element out of Context (SEooC)
- Basic approach is to assume a system context (or several) of the component
 - Safety Application Guide (Safety Manual) specifies how the component is applied correctly in the assumed system context







How does the system context impact safety?

Customer asks for a "safe ladder"



The "safe ladder" in the field





History of Auto MCU Functional Safety Solutions

- Gen 1 Safety More than 10 years experience of safety development in the area of MCU & SBC
- Gen 2 Safety First general market MCU, MPC5643L ⇒ Certified ISO 26262!
- Gen 3 Safety From 2012, multiple MCUs in Body, Chassis and Powertrain are being designed and developed according to ISO 26262

Functional Safety Solutions

2012

Gen 3 Safety



MPC5744P/MPC5777K/etc 55nm

- 32-bit Dual/Quad-Core MCU
- Developed according to ISO 26262
- Target Applications Chassis & P/T for ASILD
- •Safe methodology, Architecture, SW and tools

PowerSBC Gen 2

- Voltage SupervisionFail-Safe State Machine
- T all-Sale State Maci
- Fail-Safe IO
- Advanced Watchdog

2008

Gen 2 Safety



MPC5643L - 90nm

- 32-bit Dual-Core MCU
- Developed according to ISO 26262
- Target Applications for Chassis ASILD



PowerSBC

- Voltage Supervision
- Fail-Safe State Machine
- Fail-Safe IO
- Advanced Watchdog

2000

Gen 1 Safety

Custom Safety Platform for Braking

- Started to ship in 2000 first safe MCU for braking applications
- IEC 61508 / ISO 26262 compliance achieved at system level (top down approach)
- MCU features are a key enabler for SIL3 / ASILD



Custom IC



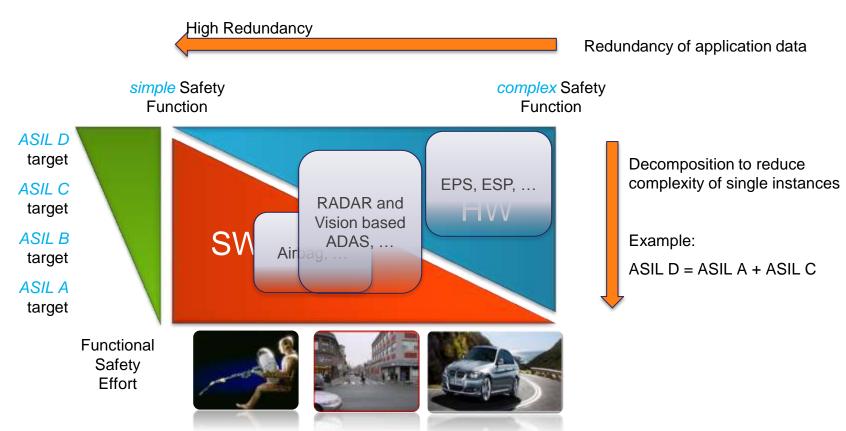




Our Vision in safety: know your context

Ideal partitioning between HW and SW measures dependant on ASIL target and complexity of safety function

Example Safety Applications ...



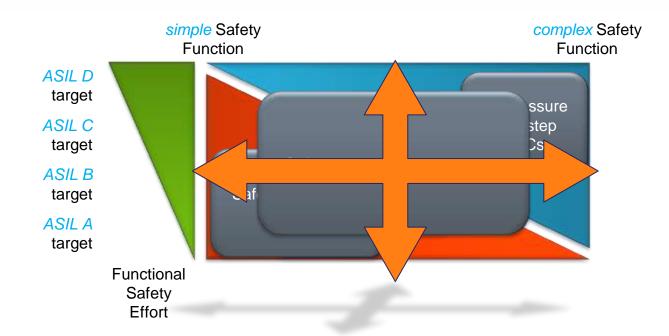






Our solution for safety: Balance and flexible

Offering products that scale to application specific safety requirements





Spanning the whole range efficiently ...







SafeAssure Products

Farget Warket	Product Type	Product	Target Applications	Safety Process	Safety Hardware	Safety Support
Automotive Analo, and Powe	Mcu	MPCS746M	Diesel Engine Management Directinjection Engines Electronically Controlled Transmissions Gasoline Engine Management	ISO 26262 ASIL D	Integrated Safety Architecture e.g.; Multi-core, delayed lockstep, e2eECC, replicated peripherals, LBIST & MBIST; FCCU	FMEDA Safety Manual
		MPC574×P	Electric Power Steering Braking and Stability Control Advanced Driver Assistance Systems (ADAS) Safety Domain Control	ISO 26262 ASIL D	Integrated Safety Architecture e.g.: Dual core, delayed lockstep, e2eECC, replicated peripherals, LBIST & MBIST, FCCU	FMEDA Safety Manual
		MPC567×K	77 GHz RADAR System	FSL QM	Integrated Safety Architecture e.g.: Dual core, lockstep or dual parallel processing, replicated peripherals, FCCU	FMEDA Safety Application Note
		MPC564×L	77 GHz RADAR System Electric Power Steering Braking and Stability Control	ISO 26262 ASIL D	Integrated Safety Architecture #.g.: Dual core, lockstep or dual parallel processing, replicated peripherals FCCU	PMEDA Safety Manual System Level Application Note
		MPC560×P	DSI Airbag System PSIS Airbag System Electric Power Steering	FSL QM	Single care, SEC/DED ECC, Clock Monitoring Unit, Low Voltage Detector, FCU	FMEDA Safety Application Note
	Analog and Power	MC33906	Safety Critical Motor Control Electric Power Steering	ISO 26262 ASIL D	Integrated Safety Architecture e.g.: Independant Voltage Monitoring and Fall Safe state Machine (ABIST, LBIST), PCCU Monitoring for Dual Core LockStep Mode, Several HW diagnostic to cover SPF, LT	Safety Manual, FMEDA System Level Application Note
		MC33907	Electrical Power Steering Safety critical motor control applications Vehicle dynamic and chazziz control	ISO 26262 ASIL D	Integrated Safety Architecture	Safety Manual, FMEDA System Level Application Note
		MC33908	integrated Chassis Domain Safety critical motor control applications	ISO 26252 ASIL D	Integrated Safety Architecture	Safety Manual, FMEDA System Level Application Note
		MC33789	PSIS Airbag System	FSL QM	4x PSIS Host, Safing Block	Safety FMEA
		MC33926	Valve control in Powertrain applications	FSL QM	Output state flag Thermal Shutdown	Safety FMEA
	Sensors	MMA16xx MMA26xx	DSI Airbag System	FSL QM	DSI2.5 safety bus, Triggered self test, Over-damped MEMS	PTA
		MMA51×× MMA52××	PSIS Air bag System	FSL QM	PSIS safety bus, Triggered self test. Over-damped MEMS	FTA
		MMAGS×× MMAGS××	PSIS Airbag System Electric Power Steering (EPS)	FSL QM	SPIW/ CRC, Triggered self test, Over-damped MEMS	FTA
		MMA69xx	Braking and Stability Control	FSL QM	SPIW/ CRC, Triggered self test, Over-damped MEMS	FTA
Industrial	меи	PK520	Aerospace Anesthesia Unit Monitor Input-Output Control (I/O Control) Process Control, Temperature Control Programmable Logic Control (PLC)	ISO 26262 ASIL D	Integrated Safety Architecture e.g.: Dual core, lockstep or dual parallel processing, replicated	FMEDA
			Motor Drivers Robotics Safety Shutdown Systems Ventilators and Respirators	FSL QM	peripherals, FCCU	Safety Application Note







Safety Concept of an MCU with Integrated Safety Architecture

Safety **Hardware**





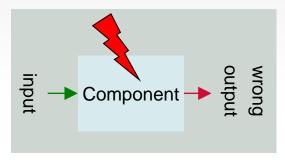


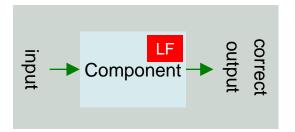
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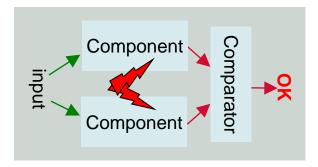


Random Failures and their Handling

- Single Point Failure (SPF)
 - Immediate potential to cause a hazard
 - Quick detection or mitigation
- Latent Failure (LF)
 - Can become dangerous in conjunction with a second fault
 - Can aggregate
 - Periodic detection
- Common Cause Failure (CCF)
 - Causes several component to fail
 - Can possibly annul redundancy-based measures
 - Mitigation or quick detection





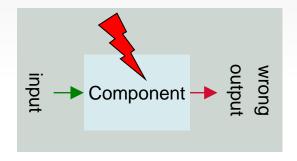


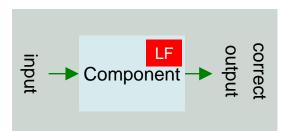


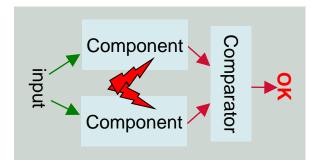


MCU Countermeasures for Failure Classes

- Single Point Failure (SPF)
 - Structural redundancy
 - Core, DMA
 - Information redundancy
 - E2E ECC, EDC on Cache
- Latent Failure (LF)
 - HW-Self test
 - Memory, logic
 - 90% stuck-at
- Common Cause Failure (CCF)
 - Delayed Checker Core
 - Supervision of clock, power and temperature
 - Independent safety clock
 - Independent failure signaling







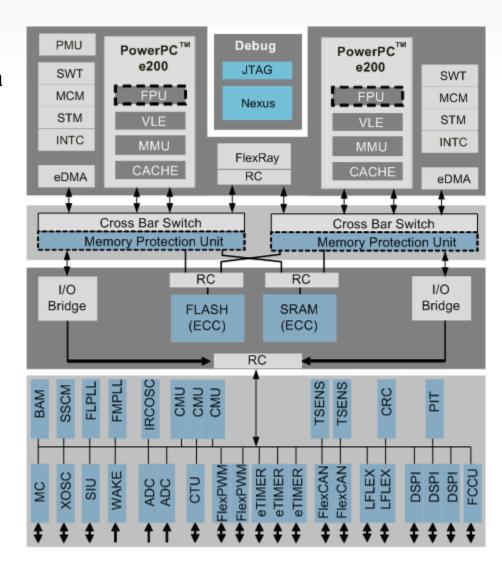






Safety Concept Example: MPC5643L (1)

- Target applications
 - Safety applications that require a high safety integrity level, such as:
 - Electric power steering
 - Electronic stability control
- Item must be in safe state for modes of (non)operation:
 - Completely unpowered
 - Reset
 - Operating correctly
 - Indicating an internal error
- Safety mechanism: technical solution to detect faults or control failures in order to achieve a safe state



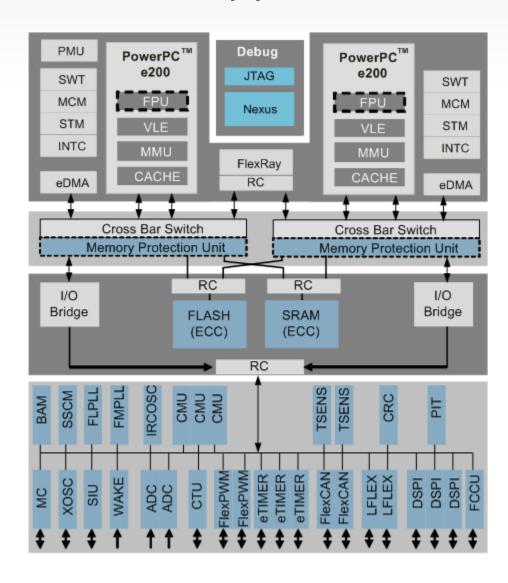






Safety Concept Example: MPC5643L (2)

- Safety mechanisms:
 - Built-in self tests (memory, logic, ADC)
 - Duplicate computational elements in lock-step
 - ECC for FLASH/SRAM
 - Temperature, clock and voltage monitors
 - Fault Collection and Control Unit (FCCU) with redundant fault notification path
 - Independent safety clock
 - eDMA and CRC
 - Access protection (MPU, register)









Safety Concept Example: MPC5643L (3)

- Elements having <u>low</u> application dependency
 - Safety architecture may not interfere with application
 - Hardware driven

Computational Shell
System Safety mechanisms

- Elements having <u>high</u> application dependency
 - Functional safety of the periphery is ensured by system-level measures
 - Flexible usage within application software

PMU PowerPC[™] Debug PowerPC[™] e200 e200 **JTAG** SWT SWT FPU MCM MCM Nexus STM STM INTC INTC MMU MMU FlexRay CACHE CACHE RC eDMA eDMA Cross Bar Switch Cross Bar Switch Memory Protection Unit Memory Protection Unit RC RC I/O I/O Bridge Bridae FLASH SRAM (ECC) (ECC) RC CMU DSPI

I/O & Communication Peripherals







First ISO 26262 Certified MCU- Qorivva MPC5643L

- Certified by exida an independent accredited assessor
- Certificate issued based on a successful assessment of the product design and applied development and production processes against all requirements and work product definitions of ISO 26262 identified as applicable to an MCU part
- MPC5643L MCU certified for use for all Automotive Safety Integrity Levels (ASIL), up to and including the most stringent level, ASIL D

Released on 6th September, 2012



Freescale 11/08-067-C R009 V1 R0 Results of the ISO 26262 Functional Safety

Validity:

This assessment is valid for Microcontroller MPC5643L

This assessment is valid until August 31, 2015.



Certificate / Certificat Zertifikat / 合格証

FREESCALE 1108067 P0026 C001

exida Certification S.A. hereby confirms that the:

MICROCONTROLLER MPC5643L

FREESCALE Halbleiter Deutschland **GmbH** Munich, Germany

Has been assessed per the relevant requirements regarding µC development and verification & validation of:

ISO 26262 : 2011 Parts 2, 4, 5, 7, 8, 9 and 10 (to the extent applicable)

and meets requirements providing:

Systematic Integrity: ASIL D

Safety related function:

The µC supports the execution of safety-related software by a dual-core lock-step architecture with memory protection and centralized fault collection and control unit.

Application restrictions:

The microcontroller shall be used per the Safety Application Guide requirements





Evaluating Assessor

Certifying Assessor

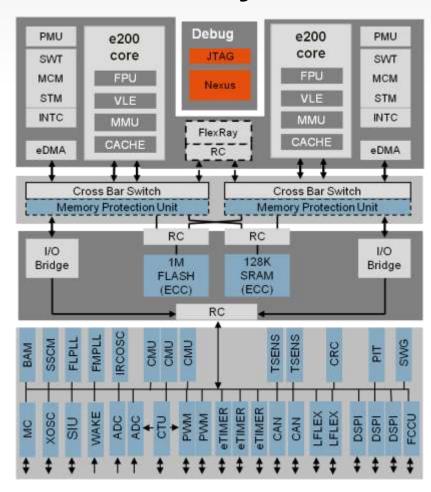






ISO 26262 Assessment and Audit Summary

- Assessment of the MPC5643L Safety Case
- Assessment and audit of Freescale's development processes used for the MPC5643L
- Assessment of the FMEDA (Failure Modes Effects and Diagnostic Analysis) of the MPC5643L to confirm it satisfies the SPFM, LFM and PMHF metrics required for ASIL D
- Assessment of the MPC5643L hardware design, implementation and verification activities
- Over 50 work products were provided to exida during the assessment and onsite audits



MPC5643L MCU



















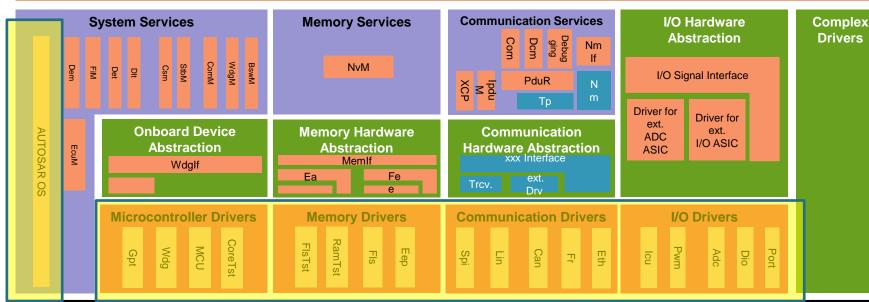
Freescale Automotive Software

 Freescale Automotive Software is mostly focused on AUTOSAR MCAL and OS

Not all modules are shown here

Application Layer

AUTOSAR Runtime Environment (RTE)



Microcontroller







Freescale Automotive Software

However, also about

- Instruction-based core self-test
- Libraries such as math library, motor control libraries, etc.
- Complex drivers such as Pulse Width Modulator (PWM) and Ethernet

ISO26262 imposes that all hardware and software elements are designed and developed to minimize the risk of causing hazardous events.

Freescale software for SafeAssure meets ISO26262

- supports hardware to meet ISO26262 requirements
 - detection of HW random faults
- supports efficient achievement of safety goals
 - detection of SW systematic faults
 - · assuring freedom from interference or preventing interference
 - following ISO26262 compliant FSL SW development process
 - reaction to faults



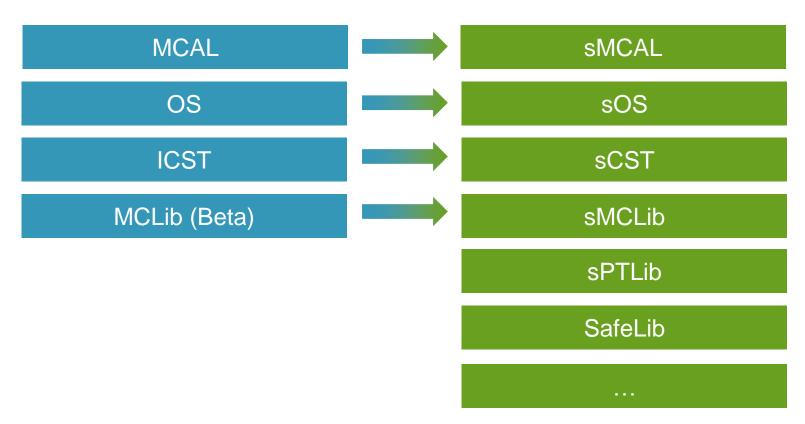




... Toward Functional Safety Software Portfolio

Ordinary Software Offering

SafeAssure Software Offering









Objectives of SafeAssure Software Portfolio

- Support efficient achievement of safety goals up to ASIL-D
 - Safety with minimized performance degradation
 - Safety simplified for integrators
 - Cross-platform consistent architecture
- Support achievement of hardware architectural metrics up to ASIL-D

All products in the Software SafeAssure portfolio are Safety Element out of Context (SEooC)

- safety-related requirements are assumed
- safety-related role is assumed
- deployment is envisioned





SafeAssure Solutions

Software components that facilitate and support safety-related applications.

Software components for detecting hardware faults to support compliance with ISO26262 hardware architectural metrics:

- SPFM
- LFM

Safety-Related Functional Layer

Safety Service Layer

HW Safety Layer

Freescale Microprocessor

Software functional components that may carry out safety-related functions

μPs with different set of safety measures and safety support functions







Classes of Freescale Software Components

Freescale Software Product Class	Products			
Safety-Related Functional Components	safety MCAL (sMCAL)safety Motor Control Lib (sMCLib)			
Safety Service Components	Safety Library (SafeLib) Microcontroller Error Management Software support for FCCU, MEMU, LBIST, MBIST Hardware error collection Safety Error Reporting and Reaction Collect both Hardware and Software faults Provides reaction mechanisms Resource Manager Manages peripheral control to enable run-time invocation of peripheral tests CRC driver Abstracts HW/SW implementation DMA protection Software Integrity Universal Checker Microcontroller Error Management BIST MBIST BIST MBIST			
HW Safety Components	safety Core Self Test (sCST)safety Peripheral Test Library (sPTLib)			

















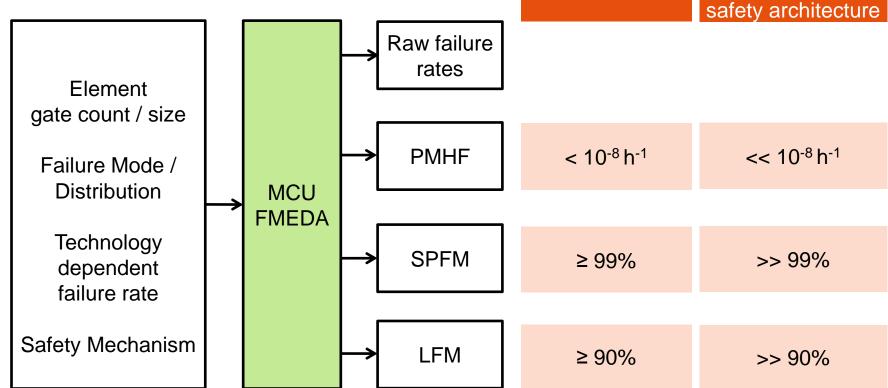


FMEDA: System-Level versus MCU

- Failure Mode, Effect and Diagnostic Analysis
- A systematic way to identify and evaluate failure modes, effects and diagnostic techniques, and to document the system.
- target values can be assigned to MCU
- FMEDA for MCU => for system-level FMEDA

ASIL D targets for whole item

Typical results for MCU with integr. safety architecture









SEooC safety assumption can be inflexible

Old SEooC assumption forces system vendors to implement unnecessary safety measures!

Example: First generation safety application guide for had 68 mandatory requirements





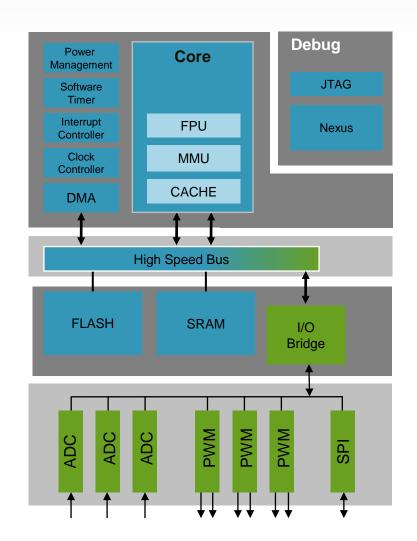


Example: Chassis Control Microcontroller

Without application context, an SEooC analysis requires safety measures for:

- PWM
- ADC
- SPI
- Core Subsystem

Consequence: over-engineering of architecture and suboptimal partitioning of software and hardware effort often









Tailoring SEooC safety assessment

A new approach shall complement the safety measures of a context, not duplicate what the context already provides!

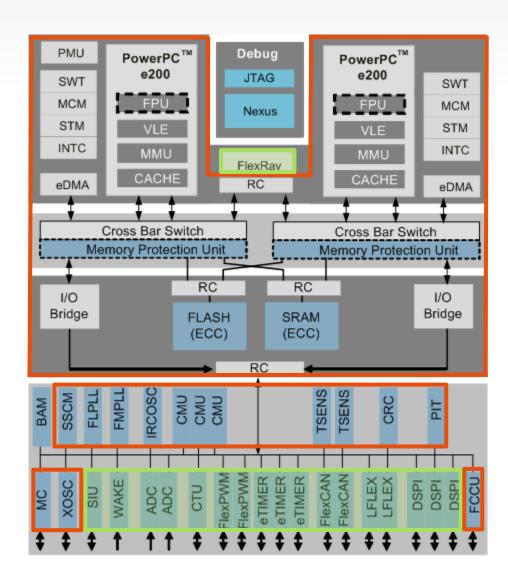






FMEDA Example: MPC5643L

- FMEDA for MPC5643L
 - Processing units (core, etc.)
 - Power supply
 - Clock
 - Non-volatile memory (FLASH)
 - Volatile memory (SRAM)
- Safety concept on system level not known
 - => Raw failure rates for
 - Digital I/O
 - Analogue I/O
 - External communication









Freescale introduces dynamic FMEDA approach:

- Customer communicates implemented safety measures and Freescale delivers respective tailored FMEDA (within e.g. 1 hour)
- E.g. MPC5675K has more than >1 million different FMEDAs in data base – so truly back to the world of general purpose!
- No longer applications have to fulfill FMEDA assumption but FMEDA tailors to application







Flexible FMEDA

Software Functional Self Test Routine for Core supported by Hardware periodically executed within Fault Tolerant Time Interval	Lockstep enabled sscM_status [LSM] = 1	Safety Relevant Core 2 Usage SSCM_STATUS(LSM) = 0	Temporal Core and DI Redundancy (recalculate on same cor doule move with same DI	implemented and e or detecting faillure within MA) Fault Tolerant Time Interval	MPU Enabled MPU_RGDx	MMU Enabled TLB0CFG,
TRUE	FALSE	TRUE	FALSE	TRUE	TRUE	TRUE
Diagnostic Coverage of Self Test Routine		Reciprocal comparison		Window Monitoring Watchdog configured		
30% diagnostic coverage		TRUE		TRUE)
Software Test within Fault Tolerant		Diagnostic Coverage of		Logical Monitoring		
Time Interval		Reciprocal comparison	1	Watchdog configured		
TRUE		100% diagnostic coverage Replicated Software use	e •	TRUE		
Software Test supported by hardware		different SRAM block		50% diagnostic coverage		
TRUE		FALSE		·	•	
50% diagnostic coverage		Reciprocal comparison within Fault Tolerant Time TRUE	e			•••
<u>Targe</u>	et Achiev	ement respe	ctive to ISO 2	6262 and IEC 61	1508 Ed. 2.0	
	Single-Poir	nt Fault Metric:	≥ 99,84%	ASIL D requires	a Single-Point fault Metric ≥ 9	99%
Latent Fault Metric:		≥ 99,94%	ASIL D requires a Latent Fault Metric ≥ 90%		%	
SFF: ≥ 99,84%		≥ 99,84%	SIL3 requires	a Single-Point fault Metric≥9	9%	
$\lambda_{SPF} + \lambda_{RF}$ (I	SO26262), 7	L _{DU} (IEC61508):	2,18E-10 h ⁻¹	ASIL D & SIL3 requires a single p	oint or dangerous undetected	d failure rate of ≤ 1E.5
		λ _{total_ISO26262} :	1,38E-07 h ⁻¹			
		λ _{total_IEC61508} :	1,38E-07 h ⁻¹			







Safety Support – FMEDA, Documentation & More

FSL QM Products - Typical Deliverables

- Safety Analysis of Architecture: Safety FMEA or FTA
- User Guide: Safety Application Note
- Development Process evidence: PPAP, Quality Plan (Mapping to ISO 26262 / IEC 61508 checklists)

ISO 26262 or IEC 61508 Products – Typical Deliverables

- Safety Analysis of Architecture: FMEDA, CCA or FTA
- User Guide: Safety Manual
- Development Process evidence: PPAP, Safety Plan, Certificates

Local Support

Functional Safety Field Experts

Learning

 Field Training / workshops – delivered by Local Functional Safety FAE Experts









Safety Support – Dynamic FMEDA

Objective

- Tailor FMEDA to match application configuration
- Enables customers, by supporting their system level architectural choices

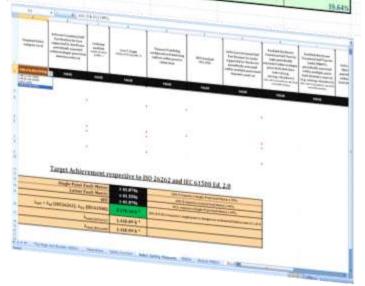
Content

- FMEDA methods aligned with functional safety standards
 - SPFM & LFM, PMFH ISO 26262
 - SFF & PFH- IEC 61508 ed-2.0
 - βic IEC 61508 ed-2.0 part 2, Annex E
- Dynamic FMEDA covers elements with low application dependency: Clock, Power Supply, Flash, STM, SRAM, Processing Unit...

Work flow and result

- Customer specifies the Safety Integrity Level required by their application, and then confirms the Safety Measures that will be used
- A tailored FMEDA is then supplied to customer's for their specific application

time	ration in hot crimate.	it "average" temperature		
Secure in h			CARL CIRIE	SEL
0 h	Tinggra 1010	Tennes in 'C	failure acceleration GATE	failure acceleration
400 h	-10 °C	-20 through -20 -20 through 0	4,01£-07 5,57£-06	1.84E-02
1000 h	50 %	0 through 40 40 through 60	1,47E-04	3,75E-02 5,126-02
3000 n	70 °C	60 through 80	2,125-05 9,675-05	1.886-01
1700 h	110 %	80 through 100 100 through 120	5,74E-02 1,25E-01	2.848-01 4.106-01
120 n	150 °C	140 through 14m	3,738-01	5,698-01 7,656-01
ECCO n	170 °C	140 through 160 160 through 180	1,006+00 2,456+00	1.008+00









Safety Support - Safety Manual

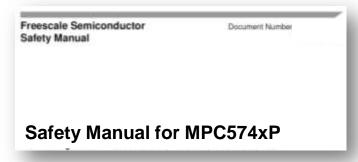
Objective

- Enables customers to extract the full value of Freescale's functional safety offering
- Simplify integration of Freescale's safety products into applications
- A comprehensible description of all information relating to FS in a single entity to ensure integrity of information and links with datasheet

Content

- SoC Safety Concept description
- System level assumptions of use (Safety specific usage considerations)
- Pseudo-code or C-Code to simplify adoption of safety application requirements
- FMEDA results
 - Latent Fault Matrix (LFM)
 - Single Point Fault Matrix (SPFM)
 - Probabilistic Metric for random Hardware Failures (PMHF)
- Provisions against Dependent Failures

Safety Manual for MCU Solution



Safety Manual for Analog Solution

Freescale Semiconductor
Safety Manual

Safety Manual for MC33906/7/8







Safety Support – System Level Application Notes

Design Guidelines for

- Integration of Microcontroller and Analog
 & Power Management device
- Explains main individual product Safety features
- Uses a typical Electrical Power steering application to explain product alignment
- Covers the ASIL D safety requirements that are satisfied by using both products:
 - MPC5643L requires external measures to support a system level ASIL D safety level
 - MC33907/08 provides those external measures:
 - External power supply and monitor
 - External watchdog timer
 - Error output monitor

Integrating the MPC5643L and MC33907/08 for ISO26262 ASIL-D Applications

This application note provides design guidelines for integrating the Freescale MPC5643L microcontroller unit (MCU) and Freescale MC33907/08 System Basis Chip in automotive electric/electronic systems that target the ISO 26262 functional safety standard. It provides an overview of the MPC5643L and the MC33907/08 feature set and covers the functional safety requirements that are satisfied in order to achieve ASU. Dievel of safety.

Integrating the IMPC5643L and IMC33907 /IMC33908 in a system provides many advantages for the customer. Presscale's ISO 26263 solutions, that form part of the Presscale Safe Assure program, help system manufacturers more easily achieve system compliance with functional safety standards by simplifying the system architecture.

I. MPC5643L Overview

This section describes the MPCS643L features that are of interest when integrating the device with the Aurasenz insi

A. Safety Concept

The MPC5643L is built around a dual e20024d core Sphere of Replication (SoR) safety platform with a safety concept targeting ISO 25552 ASIL D integrity level. In order to minimize additional software and module level features to reach this target, on-chipredundancy is offered for the critical components of the MOU (CPU core, DMA controller, interrupt controller, crossbar bus system, memory protection unit, flash memory and RAM controllers, peripheral bus bridge, system timers, and watchdog timer). A Redundancy control and checker unit (RCCU) is implemented at each output of this SoR. BCC is available for on-chip RAM and flash memories. The programmable Fault Collection and Control Unit (PCCU) monitors the integrity status of the device and provides flexible safe state control.

B. Power Supply Requirements

The on-chip voltage regulator module provides the following features: Single high supply requires nominal 3.3%. An external ballast transistor is used to reduce dissipation capacity at 1 high temperature but an embedded transistor can be used if power dissipation is maintained within package dissipation capacity (lower frequency of operation). All (I/Os are at same voltage









Functional Safety. Simplified.





Summary

- ISO 26262 has been widely adopted for Automotive functional safety
- Systems with safety goals according to ISO 26262 are no longer an exception
- Freescale support OEMs and Tier1s to achieve their ISO 26262 safety goals
 - Discrete and integrated safety architectures
 - System level chip set solutions beyond MCU
- Combined with a range of Safety HW products, Freescale supports customers by providing a set of differentiating collateral that enable our customers and can significantly reduce their development time
 - Dynamic FMEDA, Safety Manual, System Level Application Notes







