i.MX 6 Connectivity features
20th-August, 2013

FirstView Consultants
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PCB Design

Firmware & Driver Development

Multimedia Codecs

System Architecture

Rapid Prototyping

Mobile & Web Apps

Data Storage & Retrieval

Military-grade Encryption

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Core Services
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FirstView has 600+ people through exclusive partnerships with world class near-shore & off-shore firms.
Agenda

- Introduction to Freescale i.MX6 processors
- Connectivity in i.MX6 processors at a glance
- Memory and mass storage
- High speed interfaces
- General purpose interfaces
- Video, camera, multimedia and audio interfaces
- Automotive interfaces
- Boot up interfaces
- DDR interface
- Ethernet Interface
- Example reference designs
i.MX 6 Series Overview

Scalable series of five ARM Cortex A9-based SoC families

**i.MX 6SoloLite**
- 1x 1GHz
- x32 400MHz DDR3
- No HW video accel.
- 2D graphics (2 GPUs)
- LCD, EPD

**i.MX 6Solo**
- 1x 1GHz
- x32 400MHz DDR3
- **HD1080p video**
- 2D+3D (2 GPUs), 53Mtri/s
- LCD, EPD

**i.MX 6DualLite**
- 2x 1GHz
- x64 400MHz DDR3
- **HD1080p video**
- 2D+3D (2 GPUs), 53Mtri/s
- LCD, EPD

**i.MX 6Dual**
- 2x 1/1.2GHz
- x64 533MHz DDR3
- **Dual HD1080p video**
- 2D+3D (3 GPUs), **176 Mtri/s**
- LCD

**i.MX 6Quad**
- 4x 1/1.2GHz
- x64 533MHz DDR3
- **Dual HD1080p video**
- 2D+3D (3 GPUs), **176 Mtri/s**
- LCD

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Pin-to-pin Compatible

Software Compatible
**Application Processors: The Unbound User Experience**

*Display centric devices are the fastest growing segment of the market*

**Freescale Target Markets**

- Medical
- Smartphones, Smartbooks & Tablets
- Industrial
- Automotive
- Connected Displays
- eReaders

**Over 150 million processors shipped**

Top 3 AP silicon vendor

**Power & Performance Leadership**
- 1st Quad A9 + 64b memory, 1st Cortex CPU + integrated EPD
- Multi-core CPU, multi-core graphics, multi-stream video, console class 3D, rich interfaces

**Smooth Scalability**
- Quad, Dual and Single core CPU offerings
- Best in class flexibility/integration: Consumer, Auto, Industrial IO’s + qualifications + BGA/POP offerings
  - GbE, PCIe, SATA, MIPI, USB, HDMI, LVDS, EPD, CAN, MLB, etc
  - Full PMIC integration (lower complexity & BOM)
  - LP-DDR2 / DDR3 (cost versus power options)
- Single SW investment, multiple devices in market
- Pin compatibility

**Trusted Technology**
- Up to 15 year life cycle support
- Auto & Industrial grade quality design practices
- Fully featured, market targeted reference designs
- Android, Microsoft, QNX, Linux, Ubuntu optimizations
Markets and Applications

**Automotive**
- Infotainment
- Telematics
- Instrument Clusters
- Vision/Camera Systems

**eReaders**
- Monochrome eReader
- Color eReaders

**Smart Devices**
- Media Tablets
- IPTV/Streaming Media
- Smart Monitors
- Media Phones
- Printers
- Appliances
- Scanners

- Medical – Patient Monitoring
- Medical tablets
- Industrial tablets
- Smart Energy
- Factory Automation
- HMI
- Aerospace & Defense
- Digital Signage
**Specifications:**

- **CPU:**
  - i.MX6Quad: 4x Cortex-A9 @1.2GHz, 12000 DMIPS
  - i.MX6Dual: 2x Cortex-A9 @1.2GHz, 6000 DMIPS
- **Process:** 40nm
- **Core Voltage:** 1.25V (1.0 GHz)
- **Package:**
  - 21x21 0.8mm Flip-chip BGA
  - 12x12 PoP (LP-DDR2, NAND)
- **Temp Range (Tc):**
  - -20 to 85C
  - -40 to 85C

**Key Features and Advantages**

- Multi-core architecture for high performance, 1MB L2 cache
- 64-bit LP-DDR2, DDR3 and raw / managed NAND
- S-ATA 3Gbps interface (SSD / HDD)
- Delivers rich graphics and UI in HW
- OpenGL/ES 2.x 3D accelerator with OpenCL EP support, Direct3D 11 and OpenVG 1.1 acceleration
- Drives high resolution video in HW
- Multi-format HD1080 video decode and encode
- High quality video processing (resizing, de-interlacing, etc.)
- Flexible display support
- Four simultaneous: 2x Parallel, 2x LVDS, MIPI-DSI, or HDMI
- Dual display up to WUXGA (1920x1200) and HD1080
- MIPI-CSI2 and HSI
- Increased analog integration simplifies system design and reduces BOM
- DC-DC converters and linear regulators supply cores and all internal logic
- Temperature monitor for smart performance control
- Expansion port support via PCIe 2.0
- Car network: 2xCAN, MLB150 with DTCP, 1Gb Ethernet with IEEE1588 (Ethernet AVB)

**System Control**

- Secure JTAG
- PLL, Osc
- Clock & Reset
- Smart DMA
- IOMUX
- Timer x3
- PWM x4
- Watch Dog x2

**CPU Platform**

- Dual / Quad Cortex-A9
- 32KB I-cache Per core
- 32KB D-cache Per core
- NEON Per core
- PTM Per core
- 1MB L2-cache

**Multimedia**

- GPU 3D
- GPU VG
- GPU 2D Bit
- Video Codecs: 1080p30
- Audio: ASRC
- 2x Imaging Processing Unit
- Resizing & Blending
- Inversion / Rotation
- Image Enhancement
- LCD & Camera Interface
- HDMI & PHY
- MIPI CSI2, DSI
- 2x 24-bit RGB, 2x LVDS (x3-8)
- 2x 20-bit CSI

**Power Mgmt**

- Power Supplies
- Temp Monitor

**Security**

- RNG
- TrustZone
- Ciphers
- Security Ctrl
- Secure RTC
- eFuses

**Connectivity**

- MMC 4.4 / SD 3.0 x3
- MMC 4.4 / SDXC
- UART x5, 5Mbps
- I²C x3, SPI x5
- ESAI, I²S/SSI x3
- 3.3V GPIO
- Keypad
- S-ATA & PHY 3Gbps
- USB2 OTG & PHY
- USB2 Host & PHY
- USB2 HSIC & PHY x2
- MIPI HSI
- SPDIF Tx/Rx
- PCIe 2.0 (1-lane)
- FlexCAN x2
- MLB150 + DTCP
- 1Gb Ethernet, + IEEE1588
- NAND: BCH40 ECC
- NOR: 16-bit
- LP-DDR2, DDR3 / LV-DDR3
- 64-bit, 533 MHz

Updated from i.MX53
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**Connectivity - Memory and Mass Storage Interfaces**

**NAND**
- 8 bit bus
- Up to 40 bit ECC support – was 16bit in i.MX53
- 1.65 … 3.6V supply range
- Bootable

**EIM (SRAM, NOR, OneNAND)**
- 16/32 bit A/D multiplexed mode
- 16 bit A/D demuxed
- Address up to 27 bit
- Up to 6 EIM CS (were 4 in iMX53)
- 1.65 … 3.6V IO supply range
- Bootable

**SATA II (only on 6Q/6D)**
- SATA 2.5 specification compliant and AHCI 1.1 compliant  Serial ATA Bus Adapter and internal 1 x PHY, up to 3Gbps operations
- Bootable
NAND flash interface Overview

Raw NAND interface subsystem comprises of three components:

- **BCH** -- 40-bit error correction HW engine with AXI bus master and private connection to GPMI2.
- **GPMI2** -- NAND controller pin interface.
- **APBH_DMA** -- DMA engine to drive the GPMI2 module.
NAND Interface

- ONFI2.2 compliant - Timing modes 0-5 for both asynchronous and synchronous I/F. Synchronous clock rate of up to 100MHz with data rate of up to 200MB/s.
- Support for ganged ready/busy inputs. This allows for using a single package pin for all ready busy/busy input signals.
- Up to 4 NAND devices supported via 4 chip-selects and 1 ganged ready/busy.
- Legacy raw SLC, MLC type device – 8 and 16 bit width.
- BA-NAND (Micron).
- PBA-NAND and LBA-NAND (Toshiba).
- E2-NAND (Hynix).
- EF-NAND (Samsung).
- Samsung’s “Toggle-mode” NAND (clock rate of up to 66Mhz and 80Mhz, with data rate of up to 133MB/s and 160MB/s respectively).
- Configurable page size of 2KB, 4KB, 8KB.
- Configurable spare area per page of up to 512B.
- Highly configurable timing.
- Non-identical NAND devices are not supported simultaneously.
External Memory Interfaces - Details

Mass storage devices – concurrent/replacement:

<table>
<thead>
<tr>
<th></th>
<th>SD/eMMC 1&amp;2&amp;3</th>
<th>SD/eMMC 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NAND-Flash 8 bit</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>NAND-Flash 16 bit</td>
<td>Yes</td>
<td>No</td>
</tr>
</tbody>
</table>

- All mass storage interfaces use ultra high voltage IO – no need for external level shifters, no need to pre-configure pads voltage range before boot.
- External buffer still needed for some multi-die devices (load above 50 pF). Control signals for external buffer are provided.

► SATA II (i.MX 6Q/6D only):

Serial ATA interface comprises:
- Bus Adapter (Host controller) compliant with Serial ATA Specification 2.5, and AHCI Revision 1.1 specifications
- Internal PHY supporting SATA 2.5 devices - Gen1i, Gen1m, Gen2i, Gen2m, x1 configuration.

► SD / eMMC:
- Support DS/ HS/ SDR12/ SDR25/ SDR50 (52), SDR104 and DDR50 (52) speed grades
- Compatible with eMMC System **Specification version 4.4**
- Compatible with SD **Physical layer specification 3.0**
- Support for Standard Capacity, High Capacity and SDXC cards
- Support for low(1.8V nom), normal (3.3V nominal) and dual voltage operation. Automated setting of pads voltage range.
- Support for boot partition selection and “fast boot”
## Connectivity - SD / MMC Support

<table>
<thead>
<tr>
<th>SoC</th>
<th>MMC Ver/MHz/Vcc/Boot</th>
<th>SD Ver/MHz/Vcc/Boot</th>
<th>SDXC (1) Ver/MHz/Vcc/Boot</th>
</tr>
</thead>
<tbody>
<tr>
<td>i.MX51</td>
<td>v4.2 (v4.3 partially) 26/52 MHz 1.8V, 3.3V Bootable</td>
<td>SD Phy Layer spec 2.0 SDHC spec 2.0 12/25/50 MHz 1.8V, 3.3V Bootable</td>
<td>SDXC 12/25/50 MHz 1.8V, 3.3V Non-bootable</td>
</tr>
<tr>
<td>i.MX53</td>
<td>v4.4 26/52 MHz DDR 1.8V, 3.3V Bootable</td>
<td>SD spec 2.1 12/25/50 MHz 1.8V, 3.3V Bootable</td>
<td>SDXC 12/25/50 MHz DDR 1.8V, 3.3V Non-bootable</td>
</tr>
<tr>
<td>i.MX 6 series</td>
<td>v4.4 26/52 MHz DDR 1.8V, 3.3V Bootable</td>
<td>SD spec 3.0 12/25/50 MHz 1.8V, 3.3V Bootable</td>
<td>SDXC 12/25/50/100 MHz DDR 1.8V, 3.3V Bootable</td>
</tr>
</tbody>
</table>

(1) SDXC Software support - TBD
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Connectivity - USB, Ethernet, PCIe, SATA

USB:
- 4 link level USB 2.0 compliant ports:
  - OTG –
    - with internal HS/FS/LS PHY, External Vbus source.
    - No support for ULPI interface to external PHY.
    - No TLL and IC-USB options
  - Host1-
    - with HS/FS/LS PHY, External Vbus source.
    - No support for ULPI interface to external PHY.
    - No TLL and IC-USB options
  - Host 2 and Host 3 -
    - HS IC-USB (480 Mb/s) interface serving on-board connection to external devices.

Ethernet Controller (FEC) 10/100/1000:
- Support SNI, MII, RMII and RGMII interfaces to an external PHY.
- 1.65V … 3.6V voltage range and automated selection
- IEEE1588 v2 Precision Time Protocol (PTP) and Supports Ethernet AVB

PCIe 2.0
- 1 lane, 5 Gbps
- Root/Endpoint dual role complex w/integrated x1 PHY
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Connectivity - General Purpose

- **eCSPI/CSPI** – one CSPI and two eCSPI ports, same as in i.MX53
- **Keypad** – almost same as in i.MX53. 8x8 matrix supported. (all pads are shared with other interfaces).
- **One-wire** – same as in i.MX53 One wire EEPROM and battery connection. Dallas DS2205 compatible.
- **UART:**
  - High speed (up to 4MHz) – covers TIA/EIA-232-F Standard
  - 5 ports, one of them can operate as 8 pins full UART, DCE and DTE modes. Other are four-wire
  - IrDA 1.0
  - SIR protocol support (115.2kbps or lower)
  - 32 bytes FIFOs for transmitter and receiver, autobaud.
  - 9 bit mode supported
  - RS-485 (Multi-drop) mode supported
- **GPT**
  - One 32-bit up-counter
  - Two input capture channels
  - Three output compare channels
  - External/Internal clock selectable
  - External/Internal event interval capturing
  - Programmable output logic, external output signal, ARM interrupt.

- **PWM** - same as in i.MX53
  - Four pulse-width modulators (PWM): 16-bit resolution and a 4x16 data FIFO
- **SDMA** - same as in i.MX53. Two external SDMA events
- **I2C** –
  - Three I2C ports compatible with I2C specifications v2.1 (all up to 400Kb/s)
- **GPIO:**
  - All multifunctional digital pads have the GPIO functionality – Total number of GPIOs 224
  - The GPIO supports up to 32 interrupts:
    - Programmable as edge (rising/falling)
    - Programmable as level (high/low)
  - All of multifunctional (muxed) IOPADs are GPIO capable and could be programmed independently
  - Most of GPIO capable pads are of UHVIO type - 1.65 … 3.6 V operational range with automated voltage range selection
  - Default state for most of GPIO capable pads:
    - GPIO
    - Input
    - Weak PU or PD
    - That was done to avoid on-board contentions in default state after reset.
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Connectivity - Audio System

- **S/PDIF**
  - transmitter and receiver

- **SSI and AudioMUX** – same as in i.MX53
  - Three SSI ports, FIFO size increased x2 from i.MX35
  - 3 x 4 AudioMUX
  - Support I2S specification, Sony format, TDM and AC97. Supports 16x24 wide FIFO.

- **ESAI**
  - Enabling multi-channel digital audio transmission and receiving (7.1)

- **ASRC**
  - Enables on-the-fly sample rate conversion between various audio streams
Connectivity - MIPI HSI

The HSI is an interface primarily intended to connect an application processor to a cellular modem controller in cellular handsets. HSI provides a multi-processor/multi-context low-latency communication channels over an IC-to-IC link by dividing the physical link to logical channels at the hardware level.

- **The features of the HSI module:**
  - AHB slave interface support for PIO and configure.
  - Supports PIO and DMA access mode
  - Supports AHB Master interface to SOC interconnect
  - Compatible with the HSI specification version 1.0 and HSI Physical Layer v1.01.00 specification
  - Full-Duplex High Speed Serial interface
  - Supports 16 logical channels for both transmit and receive operations
  - Each channel is configurable and can be enabled and disabled
  - Bandwidth for each channel is programmable
  - Supports both stream mode and frame mode for data transmission and reception
  - Maximum bandwidth up to 200Mbs in both transmit and receive directions
  - Configurable transmit and receive FIFO
  - Programmable transmission bit rate
  - Support both round-robin and priority-based arbitration for transmission mode
  - Run-time configurability of channel ID bit
  - Data time out feature supported for receive operation
Camera Interface and Displays - Summary

Camera Interface:
- **Main**: legacy parallel, up to 20 bits, all muxed
- **MIPI CSI-2**: Two lanes, up to 1Gbit/s per lane, virtual channels supported

Displays:
- **Main display**
  - LVDS – optional one or two channels (LVDS i/f shared with the secondary display port, up to WSXGA+ resolution. Flexible synchronization timing and data mapping
  - Legacy parallel – up to 24 bits per pixel, up to ~150MHz maximal pixel rate. Flexible synchronization timing and data mapping
  - **MIPI DSI port**: Two lanes, up to 1Gbit/s per lane, w virtual channels and DCS2 supported

- **Secondary display**
  - LVDS – optional one or two channels (LVDS i/f shared with the main display port), up to WXGA resolution. Flexible synchronization timing and data mapping
  - Legacy parallel – up to 20 bits per pixel, up to ~150MHz maximal pixel rate. Flexible synchronization timing and data mapping
  - Serial legacy port for both Main and Secondary displays – actually is used as control interface in some applications
  - **HDMI 1.4 port**
  - **Display Content Integrity Checker**
Features of the MIPI DSI complex:

**Supported standard version:**

- MIPI DSI Compliant
- DSI Version 1.01
- DPI Version 2.0
- DBI Version 2.0
- DSC Version 1.02
- PPI for D-PHY
- MIPI D-PHY Version 1.0

**Configuration:** one clock lane, two data lanes

**Speed:** Up to 1Gb/s per lane (fast speed). Low speed/low power signaling supported

DSI can support both command and video modes and up to four virtual channels to accommodate multiple displays.

- Command and video mode support (type 1, 2, 3, and 4 display architecture)
- Mode switching: low power and ultra low power
- Burst mode: dual video channel
- Non-burst mode: single video channel
- Bus turnaround
- Fault error recovery scheme

Both DPI and DBI coexist in the system but only one of them could be active in a certain time moment.
Supports up to 4 D-PHY Rx Data Lanes;
- Dynamically configurable multi-lane merging;
- Long and Short packet decoding;
- Timing accurate signaling of Frame and Line synchronization packets;
- Support for several frame formats such as:
  - General Frame or Digital Interlaced Video with or without accurate sync timing
  - Data type (Packet or Frame level) and Virtual Channel interleaving
- 32-bit Image Data Interface delivering data formatted as recommended in CSI-2 Specification;
- Supports all primary and secondary data formats:
  - RGB, YUV and RAW color space definitions;
  - From 24-bit down to 6-bit per pixel;
  - Generic or user-defined byte-based data types
- Error detection and correction:
  - PHY level;
  - Packet level;
  - Line level;
  - Frame level;
LVDS Features

- **Features**
  - **Structure**
    - Two Channels, Each channel contains 4 data pairs + 1 clock pair
  - **Data**
    - 18 bpp pixels – using 3 LVDS data pairs
    - 24 bpp pixels – using 4 LVDS data pairs
  - **Control signals**: HSYNC, VSYNC, DE

- **Pixel clock rate**
  - Single Channel: up to 85 MHz; e.g. WXGA @ 60 fps or 720p60
  - Dual Channel: up to 170 MHz; e.g. UXGA @ 60 Hz or 1080p60

- **Relevant Standards**
  - **PHY Standard**: ANSI EIA-644A
  - **Display Protocol Standards**:
    - VESA PSWG – Panel Standardization Working Group – set of standards for panels using LVDS.
    - JEIDA/JEITA DISM Standard JEIDA-59-1999
    - OpenLDI (National) – Revision 0.95 13/May/1999. *Only* Unbalanced operating mode supported (aligned with vast majority of LCD vendors).
HDMI General Features

- **Description:** High-Definition Multimedia Interface (HDMI) Transmitter including both HDMI TX Controller and PHY
- **Standard Compliance:** HDMI 1.4a, DVI 1.0, HDCP 1.4 (with keys stored in embedded eFuses)
  - Supporting majority of primary 3D Video formats
- **TMDS Core Frequency:** From 25 MHz to 340 MHz
- **Consumer Electronic Control:** Supported
- **Monitor Detection:** Hot plug/unplug detection and link status monitor support
- **Testing Capabilities:** Integrated test module
- **Maximal Power Consumption:** 70mW
Six ports
- Two parallel - driven directly by the IPU
- Two LVDS channels - driven by the LVDS bridge
- One HDMI – driven by the HDMI transmitter
- One MIPI-DSI – driven by the MIPI-DSI transmitter

Four simultaneous outputs
- Each IPU has two display ports (DI0 and DI1)
- Therefore, up to four external ports can be active at any given time.
- Additional asynchronous data flows can be sent through the parallel ports and the MIPI-DSI port

Display Content Integrity Check (DCIC)
- For parallel interfaces: probes the I/O loopback (essentially equivalent to probing the external wires)
- For other integrated interfaces (e.g. LVDS): probes the IPU output (essentially equivalent to the inputs to the serializers)
Video Input Ports In i.MX 6Dual/Quad

- **Three ports; up to six input channels**
  - Two parallel – connected directly to the IPUs; independent clock and format setting
  - One MIPI/CSI-2 – can transfer up to four concurrent channels
  - Each port: up to 150Mpxl/s @200MHz, e.g. 10Mpxl @ 15fps

- **Four concurrent channels**
  - Each IPU has two input ports (CSI0 and CSI1), each can process an input channel from one of the external ports.
  - The MIPI/CSI-2 bridge sends all its channels to all the IPU input ports and each port can select for processing a different channel, identified by its DI (Data Identifier).
  - Additional channels can be transferred through a CSI transparently – as generic data, directly to the system memory.

- **Formats supported:**
  - BT.656, BT.1120. BT 1358 (not validated)
  - YUV422, RGB888, YUV444 = over an 8 bit bus
  - RAW format up to 16bpp which will be translated to 8 bit using companding
  - Generic data up to 20bit
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Connectivity - Controller Area Network (CAN)

- The FlexCAN module is a full implementation of the CAN protocol specification, Version 2.0 B, which supports both standard and extended message frames.
- 64 Message buffers are supported per module. The Message Buffers are stored in an embedded RAM dedicated to the FlexCAN module.
Flexible Controller Area Network (FLEXCAN)

• Implements CAN 2.0B protocol specification.
• FlexCAN is similar to CAN except for the following improvements:
  − Deterministic Behavior
  − Increased reliability
• Is a full implementation of the CAN protocol specification:
  − Supports both standard and extended message frames.
  − 64 Message Buffers
  − 64 Flexible Mailboxes of eight bytes data length
  − Listen only mode capability
  − Programmable loop-back mode supporting self-test operation
  − Powerful Rx FIFO ID filtering, capable of matching incoming IDs against either 128 extended, 256 standard or 512 partial (8 bits) IDs, with up to 32 individual masking capabilities.
Media Local Bus (MLB)

• Functionality is implemented as either a 3-pin interface (single-ended) or 6-pin interface (differential), however, only one interface can be active at a time.

• Interfaces are capable of exchanging data at speeds up to 1024xFs in 3-pin mode or 6144xFs in 6-pin mode.

• A set of physical channels (4 bytes in length, or a quadlet) for exchanging data over the MediaLB bus is supported.

• These physical channels can be grouped into logical channels, where each logical channel is referenced using a ChannelAddress.

• The 6-pin interface provides support for up to 860 bytes of data per frame. The logical channels, configured by system software, can be any combination of channel types (synchronous, asynchronous, isochronous, or control) and direction (transmit or receive).
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Connectivity - Boot Modes and Boot Sources

- **Flash Devices**
  - NOR flash (using WEIM)
  - OneNand (using WEIM)
  - NAND flash (using NFC)

- **Serial ATA (using SATA)**
  - Only for 6Quad / 6Dual

- **Expansion Devices**
  - SD/eSD/SDXC/MMC/eMMC (using USDHC1 / USDHC2 / USDHC3 / USDHC4)
  - I2C (using I2C1 / I2C2 / I2C3)
  - SPI (using eCSPI1 / eCSPI2 / eCSPI3/eCSPI4/eCSPI5)

- **Serial Downloader**
  - USB (using USB OTG)

- **Plug-in mode**
  - For custom / user-defined boot

- **Boot modes are set via eFuses**

- **For development purposes, there is an option to set boot modes via external pins**
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### Multi-Mode DDR Controller

<table>
<thead>
<tr>
<th>Parameter</th>
<th>i.MX 6Dual/6Quad</th>
<th>i.MX 6DL/6Solo</th>
</tr>
</thead>
<tbody>
<tr>
<td>LPDDR2 support</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>DDR2 support</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>DDR3/LVDDR3 support</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Bus width</td>
<td>1x32/64 DDR3; 2x32 (Dual channel) LPDDR2</td>
<td>1x16/32 DDR3; 1x16/32 (Single Channel) LPDDR2</td>
</tr>
<tr>
<td>Max memory size</td>
<td>~4GB</td>
<td>~4GB</td>
</tr>
<tr>
<td>Address</td>
<td>15 Row, 10 Column, 3 Bank (DDR3) CA DDR bus (LPDDR2)</td>
<td>15 Row, 10 Column, 3 Bank (DDR3) CA DDR bus (LPDDR2)</td>
</tr>
<tr>
<td># of CS</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Max freqeuncy</td>
<td>533MHz (1066Mb/s)</td>
<td>400MHz (800Mb/s)</td>
</tr>
<tr>
<td>ODT</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Calibration</td>
<td>Yes</td>
<td>Yes</td>
</tr>
</tbody>
</table>

- Support of Dynamic Frequency Scaling
- Self Refresh and Power Down support
- Support Real-Time priority via QoS, e.g. for screen refresh
- Access Latency hiding
- Bank interleaving, Channel interleaving
- Consecutive read/write access optimizations
- Enabling access priority to open memory pages
- Deep queues for read and write requests

**MMDC: 64-bit, 2GB LV-DDR3 / DDR3**

**MMDC: 2xCh 32-bit, 1GB LPDDR2**
Multi-Mode DDR Ctrl: Low Power

► Support of Dynamic Frequency Scaling
  ▪ Software transparent, ensuring data integrity

► Refresh schema: configurable, flexible
  ▪ How often to issue refresh command, how much in a raw, etc.

► Self Refresh and Power Down support
  ▪ Self Refresh - most power saving (longest latency)
  ▪ Partial self-refresh (per JEDEC)
  ▪ Enter per software control or Activity Timer event
  ▪ Exit per master access
Agenda

- Introduction to Freescale i.MX6 processors
- Connectivity in i.MX6 processors at a glance
- Memory and mass storage
- High speed interfaces
- General purpose interfaces
- Video, camera, multi media and audio interfaces
- Automotive interfaces
- Boot up interfaces
- DDR interface
- Ethernet Interface
- Example reference designs
Wireless connectivity to i.MX Platform

- Bluetooth
  - Support profiles:
    - A2DP/AVRCP/OPP/RFCOMM
  - Support USB BT dongle BU-2073-J
  - Support Atheros Wifi/BT combo mini PCI-E dongle DS_UHMC-AGNB-AR-01

- WIFI
  - Support two WIFI modules (with Atheros SDK3.0 release):
    - Atheros 6002 (802.11a/b/g)
    - Atheros 6003 (802.11n)
Gigabit Ethernet Features

- The Ethernet MAC is single channel and without L2 switch
- Fully compliant to 802.3 specification with preamble/SFD generation, frame padding generation, CRC generation and checking, dynamically configurable to support 10/100 Mbps and Gigabit operation
- Supports 10/100/1000 Mbps full duplex and 10/100 Mbps configurable half duplex operation
- Supports AMD magic packet detection with interrupt for node remote power management
- Seamless interface to commercial Ethernet PHY device via:
  - a 4-bit Medium Independent Interface (MII) operating at 2.5MHz/25 MHz for 10/100M respectively, or
  - a 2-bit Reduced MII (RMII) operating at 50 MHz, or
  - a (double data rate) 4-bit Reduced GMII (RGMII) operating at 125 MHz. Though the RGMII is associated with 1G operations ENET also supports RGMII 10/100 at 2.5/25 MHz (internally generated clock)
- Simple 64-Bit FIFO interface to user application
- CRC-32 checking at full speed with optional forwarding of the frame check sequence (FCS) field to the client
- CRC-32 generation and append on transmit or forwarding of user application provided FCS selectable on a per-frame basis
- Support for all IEEE 1588 frames
Media Independent Interface

- **MII:** Media Independent Interface
  - IEEE 802.3 standard
  - 16 pins (+2 MDIO)
  - 4 data bits @ 2.5/25 MHz operation for 10/100 Ethernet respectively

- **RMII:** Reduced Media Independent Interface
  - Industry Standard (RMII Consortium)
  - 8 pins (+2 MDIO)
  - 2 data bits @ 50 MHz operation

- **RGMII:** Reduced Gigabit Media Independent Interface
  - Industry Standard 12 pins (+2 MDIO)
  - 4 data bits @ 125 MHz (DDR mode, 1G operations) Also 2.5/25 MHz with internally generated clocks for 10/100 Ethernet operations
Agenda

- Introduction to Freescale i.MX6 processors
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- Ethernet Interface
- Example reference designs
3G Modem and Telephony (Data)

- Protocol Stack on Communication CPU (MT)
  - Interface layer with Application processor
  - Protocol Stack (L3/L2/L1)
  - RTOS

- SW stack (Android) on Application CPU (TA)
  - Interface layer (MT-TA)
  - Inter-CPU physical interface (USB, SLIMbus, etc)

- 3G modem and telephony
  - Support Huawei EM750M/E180/E220/E770M (HSPA/WCDMA/GPRS), verified in China Mobile network, with MO Voice Call, MO SMS, and PS call.
  - Support on-board Infineon mini PCI-E 3G Amazone module.

- Multi-touch
  - Support ILITEK multi touch panel
  - Enable the multi touch function in Android framework to let applications like gallery and Web browser work.

- Support Huawei EM750M/E180/E220/E770M (HSPA/WCDMA/GPRS), verified in China Mobile network, with MO Voice Call, MO SMS, and PS call.
Car Infotainment Reference BD (Ethernet, IEEE1394)

Total: = 422
Example: Car Infotainment (Ethernet, MOST150)
Q & A
About the Presenter

Doug Schwanke
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Senior Technical Staff

Over 30 years working with embedded systems
6 years as Project Manager for Engineering Services group
Developed CAN bus system for long haul trucks
About the Presenter

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Software Architect

• Over 20 years experience working with embedded systems, concentrating on low-level connectivity firmware, drivers and software systems.

• Bachelor’s Degree in Computer Engineering from Rochester Institute of Technology

• Co-inventor of patented embedded USB design and contributor to USB Mass Storage Compliance Test specification