Optimally Configuring DDR for Custom Boards

AMF-NET-T1021

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Agenda

• Introduction and Industry Trends
• Memory Organization and Operation
• Features and Capabilities

• Demo
  - DDR configuration using QorIQ Configuration Suite
  - DDR validation using DDRv plug-in to QCS
DDR SDRAM Memories

Introduction and Industry Trends
Introduction

• Many customers are deploying and expect DDR3 support on their new product offerings, especially since the price crossover point occurred in Q1 of 2010.

• Since 2008, almost all Freescale networking devices offer DDR3 support.

• Many of the QorIQ devices offer DDR3L support.

• Freescale devices with DDR3/DDR3L support provide customers with higher performance memories at lower power consumptions levels.

• The first QorIQ device with DDR4 is expected by end of 2013 (T1040).
DDR – Major Vendors

- Supported by all major memory vendors
DRAM Migration Roadmap

<table>
<thead>
<tr>
<th></th>
<th>2010</th>
<th>2011</th>
<th>2012</th>
<th>2013</th>
<th>2014</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR</td>
<td>9%</td>
<td>7%</td>
<td>5%</td>
<td>2%</td>
<td>1%</td>
</tr>
<tr>
<td>DDR2</td>
<td>37%</td>
<td>23%</td>
<td>18%</td>
<td>13%</td>
<td>9%</td>
</tr>
<tr>
<td>DDR3</td>
<td>54%</td>
<td>70%</td>
<td>75%</td>
<td>75%</td>
<td>70%</td>
</tr>
<tr>
<td>DDR4</td>
<td>0%</td>
<td>0%</td>
<td>2%</td>
<td>10%</td>
<td>20%</td>
</tr>
</tbody>
</table>
## DDR SDRAM Highlights and Comparison

<table>
<thead>
<tr>
<th>Feature/Category</th>
<th>DDR1</th>
<th>DDR2</th>
<th>DDR3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package</td>
<td>TSOP</td>
<td>BGA only</td>
<td>BGA only</td>
</tr>
<tr>
<td>Densities</td>
<td>128Mb - 1Gb</td>
<td>256Mb - 4Gb</td>
<td>512Mb - 8Gb</td>
</tr>
<tr>
<td>Voltage</td>
<td>2.5V Core 2.5V I/O</td>
<td>1.8V Core 1.8V I/O</td>
<td>1.5V Core 1.5V I/O</td>
</tr>
<tr>
<td>I/O Signaling</td>
<td>SSTL_2</td>
<td>SSTL_18</td>
<td>SSTL_15</td>
</tr>
<tr>
<td>Internal Memory Banks</td>
<td>4</td>
<td>4 to 8</td>
<td>8</td>
</tr>
<tr>
<td>Data Rate</td>
<td>200-400 Mbps</td>
<td>400–800 Mbps</td>
<td>800–1600 Mbps</td>
</tr>
<tr>
<td>Termination</td>
<td>Motherboard termination to $V_{TT}$ for all signals</td>
<td>On-die termination for data group. $V_{TT}$</td>
<td>On-die termination for data group. $V_{TT}$</td>
</tr>
<tr>
<td>Data Strobes</td>
<td>Single Ended</td>
<td>Differential or single</td>
<td>Differential</td>
</tr>
<tr>
<td>Feature/Category</td>
<td>DDR1</td>
<td>DDR2</td>
<td>DDR3</td>
</tr>
<tr>
<td>--------------------------</td>
<td>-------------------------------------</td>
<td>-------------------------------------</td>
<td>-------------------------------------</td>
</tr>
<tr>
<td>Burst Length</td>
<td>BL= 2, 4, 8 (2-bit prefetch)</td>
<td>BL= 4, 8 (4-bit prefetch)</td>
<td>BL= 8 (Burst chop 4) (8-bit prefetch)</td>
</tr>
<tr>
<td>CL/tRCD/tRP</td>
<td>15 ns each</td>
<td>15 ns each</td>
<td>12 ns each</td>
</tr>
<tr>
<td>Master Reset</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>ODT (On-die termination)</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Driver Calibration</td>
<td>No</td>
<td>Off-Chip (OCD)</td>
<td>On-Chip with ZQ pin (ZQ cal)</td>
</tr>
<tr>
<td>Write Leveling</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
</tbody>
</table>
## DDR SDRAM Highlights and Comparison

<table>
<thead>
<tr>
<th>Feature/Category</th>
<th>DDR3</th>
<th>DDR4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package</td>
<td>BGA only</td>
<td>BGA only</td>
</tr>
<tr>
<td>Densities</td>
<td>512Mb -8Gb</td>
<td>2Gb -16Gb</td>
</tr>
<tr>
<td>Voltage</td>
<td>1.5V Core 1.5V I/O</td>
<td>1.2V Core 1.2V I/O</td>
</tr>
<tr>
<td>Data I/O CMD, ADDR I/O</td>
<td>Center Tab Termination (CTT)</td>
<td>Pseudo Open Drain (POD) Center Tab Termination (CTT)</td>
</tr>
<tr>
<td>Internal Memory Banks</td>
<td>8</td>
<td>16 for x4/x8 8 for x16</td>
</tr>
<tr>
<td>Data Rate</td>
<td>800–2133 Mbps</td>
<td>1600–3200 Mbps</td>
</tr>
<tr>
<td>VREF</td>
<td>VREFCA &amp; VREFDQ external</td>
<td>VREFCA external VREFDQ internal , per DRAM</td>
</tr>
<tr>
<td>Data Strobes/Prefetch/Burst Length/Burst Type</td>
<td>Differential/8-bits/BC4, BL8/ Fixed, OTF</td>
<td>Same as DDR3</td>
</tr>
<tr>
<td>Additive/read/write Latency</td>
<td>0, CL-1, CL-2/ AL+CL/ AL +CWL</td>
<td>Same as DDR3</td>
</tr>
</tbody>
</table>
### DDR SDRAM Highlights and Comparison (continued)

<table>
<thead>
<tr>
<th>Feature/Category</th>
<th>DDR3</th>
<th>DDR4</th>
</tr>
</thead>
<tbody>
<tr>
<td>CRC Data Bus</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Boundary Scan/Connectivity test (TEN pin)</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Bank Grouping</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Data Bus Inversion (DBI_n pin)</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Write Leveling / ZQ</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>ACT_n new pin &amp; command</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Low power Auto self-refresh</td>
<td>No</td>
<td>Yes</td>
</tr>
</tbody>
</table>
DDR3/DDR3L/DDR4 Power Saving

- DDR3 DRAM provides 25% power savings over DDR2
- DDR3L DRAM provides 15% power saving over DDR3
- DDR4 DRAM provides 37% power saving over DDR3L
Basic DDR SDRAM Structure
Memory Organization and Operation
Single Transistor Memory Cell

Access Transistor

Row (word) line

Column (bit) line

S
D
G

“1” => Vcc
“0” => Gnd

“precharged” to Vcc/2

Vcc/2

Cbit

Ccol

Storage Capacitor

Parasitic Line Capacitance

Access Transistor

Row (word) line

Column (bit) line

S
D
G

“1” => Vcc
“0” => Gnd

“precharged” to Vcc/2

Vcc/2

Cbit

Ccol

Storage Capacitor

Parasitic Line Capacitance
Memory Arrays

ROW ADDRESS DECODER

W0

W1

W2

B0 B1 B2 B3 B4 B5 B6 B7

SENSE AMPS & WRITE DRIVERS

COLUMN ADDRESS DECODER
Internal Memory Banks

- Multiple arrays organized into banks
- Multiple banks per memory device
  - DDR1 – 4 banks, 2 bank address (BA) bits
  - DDR2 & DDR3 – 4 or 8 banks, 2 or 3 bank address (BA) bits
  - DDR4 - 16 banks, with 4 banks in each of 4 bank groups
- Can have one active row in each bank at any given time

- Concurrency
  - Can be opening or precharging a row in one bank while accessing another bank

- May be referred to as “internal”, “logical” or “sub-” banks
Memory Access

- A requested row is **ACTIVATED** and made accessible through the bank’s row buffer
- **READ** and/or **WRITE** are issued to the active row
- The row is **PRECHARGED** and is no longer accessible through the bank’s row buffer
QorIQ Family
DDR Controllers
Features and Capabilities
DDR1/DDR2/DDR3/DDR3L Controller Features

- Supports most JEDEC standard x8, x16, x32 DDR1 & 2 & 3 devices
- Memory device densities from 64Mb – through 4Gb
- Data rates up to: 333 Mb/s for DDR1, 800 Mb/s for DDR2 and 1600 Mb/s DDR3
- Devices with 12-16 row address bits, 8-11 column address bits, 2-3 logical bank address bits
- Data mask signals for sub-doubleword writes
- Up to four physical banks (ranks / chip selects)
- Physical bank (rank) sizes up to 4GB, total memory up to 16GB per controller
- Physical bank interleaving between 2 or 4 chip selects
- Memory controller interleaving when more than 2 controllers are available
- Un-buffered or registered DIMMs
DDR1/DDR2/DDR3/DDR3L Controller Features (continued)

- Up to 32 open pages
  - Open row table
  - Amount of time rows stay open is programmable
- Auto-precharge, globally or by chip select
- Self-refresh
- Up to 8 posted refreshes
- Automatic or software-controlled memory device initialization
- ECC: 1-bit error correction, 2-bit error detection, detection of all errors within a nibble
- ECC error injection
- Read-modify-write for sub-doubleword writes when using ECC
- Automatic data initialization for ECC
- Dynamic power management
Partial array self refresh
Address and command parity for Registered DIMM
Independent driver impedance setting for data, address/command, and clock
Synchronous and Asynchronous clock-in option
Write-leveling for DDR3
Automatic CPO (operational)
Asynchronous RESET for DDR3
Automatic ZQ calibration for DDR3
Fixed or On-the-Fly burst chop mode for DDR3
Mirrored DIMM supported
Many QorIQ devices offer full DDR3L support
Fly-By Routing Topology

• Introduction of “fly-by” architecture
  - Address, command, control & clocks
  - Improved signal integrity…enabling higher speeds
  - On module termination
Fly-By Routing Improved SI

DDDR2 Matched Tree Routing

DDDR3 Fly By Routing
What Is Write Leveling

- During a write cycle, the skew between the clock and strobes is increased due to the fly-by topology. The write leveling will delay the strobe (and the corresponding data lanes) for each byte lane to reduce/compensate for this delay.
Read Adjustment

- Instead of JEDEC’s MPR method, Freescale controllers use a proprietary method of read adjust method. Auto CPO will provide the expected arrival time of preamble for each strobe line of each byte lane during the read cycle to adjust for the delays caused by the fly-by topology.

- Automatic CAS to preamble calibration
- Data strobe to data skew adjustment
Write Adjustment

• Write leveling sequence during the initialization process will determine the appropriate delays to each strobe/data byte lane and add this delay for every write cycle

• Write leveling used to add delay to each strobe/data line.
DDR3L support

- DDR3L (1.35V) is a low voltage version of the DDR3 (1.5V)
- DDR3L meets the exact same functional and timing specifications of DDR3
- VIH/VIL differences are compensated by corresponding derating values to Vref resulting in no change in AC timing, and timing budget calculation
- The main considerations for using DDR3L are:
  - Memory controller needs to support DDR3L
    - P1023, P1017, P1010, P1014, P2040, P3041, P5020
  - The supply voltage needs to be at 1.35V
  - Using DDR3L SDRAM
Register Configuration

• Two general type of registers to be configured in the memory controller
• First register type is set to the DRAM related parameter values that are provided via SPD or DRAM datasheet
• Second register type is the non-SPD values that are set based on the specific application. For example:
  - On-die-termination (ODT) settings for DRAM and controller
  - Driver impedance setting for DRAM and controller
  - Clock adjust, write data delay, Cast to preamble override (CPO)
  - 2T or 3T timing
  - Burst type selection (fixed or on-the-fly burst chop mode)
  - Write-leveling start value (WRLVL_START)
• Freescale’s Processor Expert QorIQ Configuration Suite includes a DDR configuration tool for many devices. For other devices, Freescale support resources can help generate or analyze DDR settings.
DDR3 SDRAM

Summary
Summary

- DDR3/DDR3L is mainstream now
- DDR4 is expected to start entering the market by 2013
- All QorIQ devices support DDR3
- All features of DDR3, such as write leveling, ZQ calibration, ODT, Mirrored DIMM, … are supported by the memory controller in QorIQ devices
- Follow JEDEC recommended topologies for discrete parts
- Configuration and initialization of memory controller is easily achieved
Useful References

• Books:
• Freescale AppNotes:
  - AN2582 Hardware and Layout Design Considerations for DDR Memory Interfaces
  - AN2910 Hardware and Layout Design Considerations for DDR2 Memory Interfaces
  - AN2583 Programming the PowerQUICCIII / PowerQUICCII Pro DDR SDRAM Controller
  - AN3369 PowerQUICC DDR2 SDRAM Controller Register Setting Considerations
  - AN3939 PQ & QorIQ Interleaving
  - AN3940 Layout Design Considerations for DDR3 Memory Interface
  - AN4039 PowerQUICC DDR3 SDRAM Controller Register Setting Considerations
• Micron AppNotes:
  - TN-46-05 General DDR SDRAM Functionality
  - TN-47-02 DDR2 Offers New Features and Functionality
  - TN-47-01 DDR2 Design Guide
  - TN-41-07 DDR3 Power-Up, Initialization, and Reset
  - TN-41-08 DDR3 Design Guide
• JEDEC Specs:
  - JESD79E Double Data Rate (DDR) SDRAM Specification
  - JESD79-2F DDR2 SDRAM Specification
  - JESD79-3D DDR3 SDRAM Specification
DDR Configuration and Validation Tools
QorIQ Configuration Suite – Now Available!

• **QorIQ Configuration Suite v2.3 is NOW AVAILABLE!!!**
  - Supports all QorIQ and Qorivva devices
  - Works with Eclipse 3.5, Eclipse 3.6, Eclipse 3.7 development tools
    ▪ Pure Java solution for maximum choice of host system support
    ▪ Add-in to CodeWarrior Development Studio for PA, v10.1 or later
  - Available from [www.freescale.com/QCS](http://www.freescale.com/QCS) – FREE DOWNLOAD*

• **Includes the following four configuration tools all designed to collaborate on consistent configuration:**
  - PBL tool to define the Reset Control Word bit values and PBI data for the pre-boot
  - BOOTROM generator for those QorIQ without RCW functionality
  - DDR configuration supports setting the controller to a working state for any DDR
  - Data path graphical view helps to define data path configuration for the DPAA.
  - Hardware Device Tree editor supports references, synchronous GUI and XML editing, node validation based on specification bindings
  - Packaged as a separate product with installer and wizard functionality

* Must be a QorIQ customer or under QorIQ NDA for download permission

Installing Processor Expert for QorIQ

• You need CodeWarrior for PA 10.1 or later

OR, you download an Eclipse version for free

OR, you use an existing Eclipse workbench you have installed (Wind River, QNX, GNU, etc.)

• Processor Expert for QorIQ Configuration Suite installs using the Eclipse updater’s “Add new software...” capability

• The Configuration Suite is 100% pure Java so it should run on any Eclipse 3.6.1 or later host environment (Windows, Linux, Solaris, Mac OS, 32-bit/64-bit, ...)

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DDR Configuration
Lab: Creating New DDR Configuration
Create New QCS project

Create a QoriQ Configuration Project
Choose the location for the new project

Project name: P2020_DDRv

Location: C:/Workspace/DDRv/eclipse/workspace/P2020_DDRv

< Back | Next > | Finish | Cancel

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Select device and DDR component

1. Select the SoC you would like to use:
   - P2010
   - P2020
   - P2040
   - P2041

2. Components to be selected:
   - DDR Memory Controller Configuration
   - Device Tree Editor

The DDR Memory Controller configuration tool supports the specific settings for a custom DDR based on the manufacturer's data sheet and includes optional clock, bus, and DMA settings.
Get DRAM information – P2020RDB-PCA

From back of RDB box

CPU: P2020NSE2MHC 1200MHz

From DRAM datasheet

MT41J128M16HA-15ED 1333MHz

DDR3 SDRAM

MT41J512M4 – 64 Meg x 4 x 8 Banks

MT41J256M8 – 32 Meg x 8 x 8 Banks

MT41J128M16 – 16 Meg x 16 x 8 Banks
How about rest of the timing parameters?

- Tool automatically computes tRCD, tRP, and CL!
- User can change these values if required.
From memory data sheet:
- Maximum speed rating
- Capacity
QCS project explorer
Review DDR registers values
Review DDR registers values – contd.

<table>
<thead>
<tr>
<th>Reg. name</th>
<th>Init. value</th>
<th>After reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR1_CS0_BNDS</td>
<td>0000003F</td>
<td>00000000</td>
</tr>
<tr>
<td>DDR1_CS1_BNDS</td>
<td>00000000</td>
<td>00000000</td>
</tr>
<tr>
<td>DDR1_CS2_BNDS</td>
<td>00000000</td>
<td>00000000</td>
</tr>
<tr>
<td>DDR1_CS3_BNDS</td>
<td>00000000</td>
<td>00000000</td>
</tr>
<tr>
<td>DDR1_CS0_CONFIG</td>
<td>80014202</td>
<td>00000000</td>
</tr>
<tr>
<td>DDR1_CS1_CONFIG</td>
<td>00000000</td>
<td>00000000</td>
</tr>
<tr>
<td>DDR1_CS2_CONFIG</td>
<td>00000000</td>
<td>00000000</td>
</tr>
<tr>
<td>DDR1_CS3_CONFIG</td>
<td>00000000</td>
<td>00000000</td>
</tr>
<tr>
<td>DDR1_TIMING_CFG_3</td>
<td>00030000</td>
<td>00000000</td>
</tr>
<tr>
<td>DDR1_TIMING_CFG_0</td>
<td>00330104</td>
<td>00111015</td>
</tr>
<tr>
<td>DDR1_TIMING_CFG_1</td>
<td>6668846</td>
<td>00000000</td>
</tr>
<tr>
<td>DDR1_TIMING_CFG_2</td>
<td>0FA8D000</td>
<td>00000000</td>
</tr>
<tr>
<td>DDR1_SDRAM_CFG</td>
<td>47000008</td>
<td>03000000</td>
</tr>
<tr>
<td>DDR1_SDRAM_CFG</td>
<td>24401050</td>
<td>00000000</td>
</tr>
<tr>
<td>DDR1_SDRAM_MODE</td>
<td>00061421</td>
<td>00000000</td>
</tr>
<tr>
<td>DDR1_SDRAM_MODE_2</td>
<td>00000000</td>
<td>00000000</td>
</tr>
</tbody>
</table>
Generate DDR configuration
# DDR Controller 1 Registers

# DDR_SDRAM_CFG
mem [0xFF702110] = 0x47000000

# CS0_BNDS
mem [0xFF702000] = 0x3F

# CS0_CONFIG
mem [0xFF702080] = 0x80014202

# CS0_CONFIG_2
mem [0xFF7020C0] = 0x00

# TIMING_CFG_3
mem [0xFF702100] = 0x00030000

# TIMING_CFG_0
mem [0xFF702104] = 0x00300104

# TIMING_CFG_1
mem [0xFF702108] = 0x6E6B8846

# TIMING_CFG_2
mem [0xFF70210C] = 0x0FA8D0CC

# DDR_SDRAM_CFG_2
mem [0xFF702114] = 0x24401050

# DDR_SDRAM_MODE
mem [0xFF702118] = 0x00061421

#define DDR_1_INIT_EXT_ADDR_ADDR 0xFF70214C
#define DDR_1_SDRAM_RW_ADDR 0xFF702180
#define DDR_1_SDRAM_RW2_ADDR 0xFF7021C4
#define DDR_1_DATA_INIT_ADDR 0xFFF702188
#define DDR_1_SDRAM_MD_CNTL_ADDR 0xFFF7021D0
#define DDR_1_DDRCDR_1_ADDR 0xFFF702B28
#define DDR_1_DDRCDR_2_ADDR 0xFFF702B2C
#define SDRAM_CFG_MEM_EN_MASK 0x80000000
#define SDRAM_CFG2_D_INIT_MASK 0x00000010

/* DDR Controller configured registers' values */
#define DDR_1_CS0_BNDS_VAL 0x3F
#define DDR_1_CS1_BNDS_VAL 0x00
#define DDR_1_CS2_BNDS_VAL 0x00
#define DDR_1_CS3_BNDS_VAL 0x00
#define DDR_1_CS0_CONFIG_VAL 0x80014202
#define DDR_1_CS1_CONFIG_VAL 0x00

#define PEX_CONFIG_DDR1_INIT_EXT_ADDR 0x00000000
#define PEX_CONFIG_DDR1_TIMING_4 0x00220001
#define PEX_CONFIG_DDR1_TIMING_5 0x02401400
#define PEX_CONFIG_DDR1_2Q_CNTL 0x59000000
#define PEX_CONFIG_DDR1_WRLVL_CNTL 0x5653F014
#define PEX_CONFIG_DDR1_RW_CNTL 0x00000000
#define PEX_CONFIG_DDR1_RW_CNTL_2 0x00000000

/* DDR Controller 1 configuration global structures */
s1_ddr_cfg_regs_t ddr_cfg_regs_0 = {
  .cs[0].bnds = PEX_CONFIG_DDR1_CS0_BNDS,
  .cs[1].bnds = PEX_CONFIG_DDR1_CS1_BNDS,
  .cs[2].bnds = PEX_CONFIG_DDR1_CS2_BNDS,
  .cs[3].bnds = PEX_CONFIG_DDR1_CS3_BNDS,
  .cs[0].config = PEX_CONFIG_DDR1_CS0_CONFIG,
  .cs[1].config = PEX_CONFIG_DDR1_CS1_CONFIG,
  .cs[2].config = PEX_CONFIG_DDR1_CS2_CONFIG,
Steps to adapt DDR configuration file in CodeWarrior

• Open the CW config file you want to adapt

D:\Program Files\Freescale\CW PA v10.1\PA\PA_Support\Initialization_Files\QorIQ_P4\P4080DS_init_core0.cfg

• Replace DDR1 config section with the one from

D:\Profiles\b08844\workspace\p4080\Generated_Code\ddrCtrl_1.cfg

• Use this new config file with your stationary project
DDR Validation Tool
License file:
<QCS Install directory>/eclipse/Optimization/license.dat
DDRv Connection Setup
• Run basic test to confirm target connection
Configure DDR scenarios and tests

1. Select the test to run, e.g., Centering the clock.
2. Choose the run times for each test.
3. Start validation.

Choose validation mode:
- In depth

Connection settings:
- System: P2020; USBTAP id: 
- Hardware configurations
Centering of the clock results

- Click “cell” to choose Write level start and CLK_ADJ values.
Click “cell” to choose optimized ODT value.
• Click “cell” to choose optimized ODT value.
Centering of the clock - after ODT optimization

- Centering of clock scenario was re-run after finding the right ODT values

<table>
<thead>
<tr>
<th>CLK_ADJ</th>
<th>0 clocks</th>
<th>1/8 clocks</th>
<th>1/4 clocks</th>
<th>3/8 clocks</th>
<th>1/2 clocks</th>
<th>5/8 clocks</th>
<th>3/4 clocks</th>
<th>7/8 clocks</th>
<th>1 clocks</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 clock delay</td>
<td>0/3</td>
<td>3/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
</tr>
<tr>
<td>1/8 clock delay</td>
<td>0/3</td>
<td>3/3</td>
<td>3/3</td>
<td>3/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
</tr>
<tr>
<td>1/4 clock delay</td>
<td>0/3</td>
<td>3/3</td>
<td>3/3</td>
<td>3/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
</tr>
<tr>
<td>3/8 clock delay</td>
<td>0/3</td>
<td>3/3</td>
<td>3/3</td>
<td>3/3</td>
<td>3/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
</tr>
<tr>
<td>1/2 clock delay</td>
<td>0/3</td>
<td>3/3</td>
<td>3/3</td>
<td>3/3</td>
<td>3/3</td>
<td>3/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
</tr>
<tr>
<td>5/8 clock delay</td>
<td>0/3</td>
<td>3/3</td>
<td>3/3</td>
<td>3/3</td>
<td>3/3</td>
<td>3/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
</tr>
<tr>
<td>3/4 clock delay</td>
<td>0/3</td>
<td>0/3</td>
<td>3/3</td>
<td>3/3</td>
<td>3/3</td>
<td>3/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
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<tr>
<td>7/8 clock delay</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>3/3</td>
<td>3/3</td>
<td>3/3</td>
<td>2/3</td>
<td>3/3</td>
<td>0/3</td>
</tr>
<tr>
<td>1 clock delay</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>3/3</td>
<td>3/3</td>
<td>3/3</td>
<td>3/3</td>
<td>0/3</td>
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<tr>
<td>9/8 clock delay</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>3/3</td>
<td>3/3</td>
<td>3/3</td>
<td>3/3</td>
<td>0/3</td>
</tr>
<tr>
<td>5/4 clock delay</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>3/3</td>
<td>2/3</td>
<td>3/3</td>
<td>0/3</td>
</tr>
<tr>
<td>11/8 clock delay</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>3/3</td>
<td>0/3</td>
<td>0/3</td>
</tr>
<tr>
<td>3/2 clock delay</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
</tr>
<tr>
<td>13/8 clock delay</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
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<tr>
<td>7/4 clock delay</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
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<tr>
<td>15/8 clock delay</td>
<td>0/3</td>
<td>3/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
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<tr>
<td>2 clock delay</td>
<td>0/3</td>
<td>3/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
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</tr>
<tr>
<td>17/8 clock delay</td>
<td>0/3</td>
<td>3/3</td>
<td>3/3</td>
<td>3/3</td>
<td>0/3</td>
<td>0/3</td>
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<tr>
<td>9/4 clock delay</td>
<td>0/3</td>
<td>3/3</td>
<td>3/3</td>
<td>3/3</td>
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<tr>
<td>19/8 clock delay</td>
<td>0/3</td>
<td>3/3</td>
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<td>0/3</td>
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<td>5/2 clock delay</td>
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</tr>
</tbody>
</table>
Generate optimized DDR configuration

Pricing $995
License file:
<QCS Install directory>/eclipse/Optimization/license.dat
F2020RDB-PCA: Import DDR configuration from existing system running uboot

- At uboot prompt
  - => md ffe02000
    - ffe02000: 00000000 00000000 00000000 00000000 ...
    - ffe02080: 80014202 00000000 00000000 00000000 .B....
    - ffe02100: 00030000 00110104 6f6b8846 0fa8c8cc ....Ok.F....
    - ffe02110: c7000008 24401040 00441421 00000000 ...$@.@.D!
    - ffe02120: 00000000 0c300100 deadbeef 00000000 ....O........
    - ffe02130: 03000000 00000000 00000000 00000000 ...........
    - ffe02160: 02200001 02401400 00000000 00000000 ...
    - ffe02170: 89080600 86756b8 00000000 00000000 ....U....
  - => md ffe02b00
    - ffe02b00: 00000000 00000000 00000000 00000000 ...........
    - ffe02b10: 00000000 00000000 00000000 00000000 ...........
    - ffe02b20: 5dc07777 77000000 00000000 00000000 ].

- Save content to a file.
Processor Expert for QorIQ … For More Info

• Freescale’s Processor Expert landing page
  - http://www.processorexpert.com/

• QorIQ Configuration Suite

• QorIQ Optimization Suite

• Freescale Component Store – purchasing embedded software
  - http://www.freescale.com/webapp/sps/site/homepage.jsp?code=BEAN_STORE_MAIN&tid=SWnT
Pricing & Availability

• Part numbers: CWA-QIQ-OPTP-FL (floating license) & CWA-QIQ-OPTP-NL (node locked)
• Price: $999 Annual Subscription
• License Duration: 1 year
• Support & Maintenance: Included
• Availability
  - Scenarios Tool – Now
  - DDRv – Now