Optimally Configuring DDR for Custom Boards

AMF-NET-T1021

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Agenda

- Introduction and Industry Trends
- Memory Organization and Operation
- Features and Capabilities

- Demo
  - DDR configuration using QorIQ Configuration Suite
  - DDR validation using DDRv plug-in to QCS

DDR SDRAM Memories

Introduction and Industry Trends

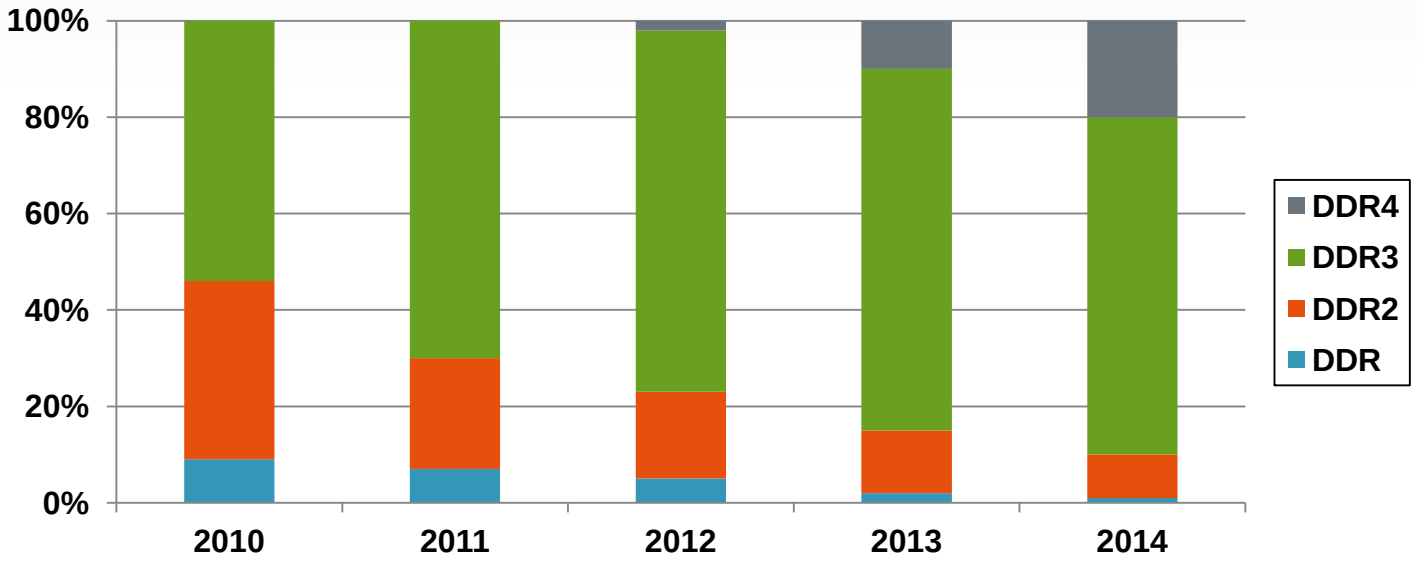
Introduction

- Many customers are deploying and expect DDR3 support on their new product offerings, especially since the price cross-over point occurred in Q1 of 2010
- Since 2008, almost all Freescale networking devices offer DDR3 support
- Many of the QorIQ devices offer DDR3L support
- Freescale devices with DDR3/DDR3L support provide customers with higher performance memories at lower power-consumptions levels
- The first QorIQ device with DDR4 is expected by end of 2013 (T1040).

DDR – Major Vendors

- Supported by all major memory vendors

DRAM Migration Roadmap



	2010	2011	2012	2013	2014
DDR	9%	7%	5%	2%	1%
DDR2	37%	23%	18%	13%	9%
DDR3	54%	70%	75%	75%	70%
DDR4	0%	0%	2%	10%	20%

DDR SDRAM Highlights and Comparison

Feature/Category	DDR1	DDR2	DDR3
Package	TSOP	BGA only	BGA only
Densities	128Mb -1Gb	256Mb - 4Gb	512Mb -8Gb
Voltage	2.5V Core 2.5V I/O	1.8V Core 1.8V I/O	1.5V Core 1.5V I/O
I/O Signaling	SSTL_2	SSTL_18	SSTL_15
Internal Memory Banks	4	4 to 8	8
Data Rate	200-400 Mbps	400–800 Mbps	800–1600 Mbps
Termination	Motherboard termination to V_{TT} for all signals	On-die termination for data group. V_{TT} termination for address, command, and control	On-die termination for data group. V_{TT} termination for address, command, and control
Data Strobes	Single Ended	Differential or single	Differential

DDR SDRAM Highlights and Comparison (continued)

Feature/Category	DDR1	DDR2	DDR3
Burst Length	BL= 2, 4, 8 (2-bit prefetch)	BL= 4, 8 (4-bit prefetch)	BL= 8 (Burst chop 4) (8-bit prefetch)
CL/tRCD/tRP	15 ns each	15 ns each	12 ns each
Master Reset	No	No	Yes
ODT (On-die termination)	No	Yes	Yes
Driver Calibration	No	Off-Chip (OCD)	On-Chip with ZQ pin (ZQ cal)
Write Leveling	No	No	Yes

DDR SDRAM Highlights and Comparison

Feature/Category	DDR3	DDR4
Package	BGA only	BGA only
Densities	512Mb -8Gb	2Gb -16Gb
Voltage	1.5V Core 1.5V I/O	1.2V Core 1.2V I/O
Data I/O CMD, ADDR I/O	Center Tab Termination (CTT) CTT	Pseudo Open Drain (POD) CTT
Internal Memory Banks	8	16 for x4/x8 8 for x16
Data Rate	800–2133 Mbps	1600–3200 Mbps
VREF	VREFCA & VREFDQ external	VREFCA external VREFDQ internal , per DRAM
Data Strobes/Prefetch/Burst Length/Burst Type	Differential/8-bits/BC4, BL8/ Fixed, OTF	Same as DDR3
Additive/read/write Latency	0, CL-1, CL-2/ AL+CL/ AL +CWL	Same as DDR3

DDR SDRAM Highlights and Comparison (continued)

Feature/Category	DDR3	DDR4
CRC Data Bus	No	Yes
Boundary Scan/Connectivity test (TEN pin)	No	Yes
Bank Grouping	No	Yes
Data Bus Inversion (DBI_n pin)	No	Yes
Write Leveling / ZQ	Yes	Yes
ACT_n new pin & command	No	Yes
Low power Auto self-refresh	No	Yes

DDR3/DDR3L/DDR4 Power Saving

- DDR3 DRAM provides 25% power savings over DDR2
- DDR3L DRAM provides 15% power saving over DDR3
- DDR4 DRAM provides 37% power saving over DDR3L

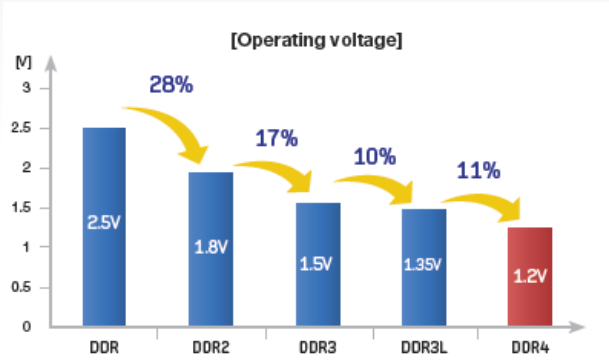


Figure 4. Reduced operating voltage requirements of DDR4 compared to DDR3L

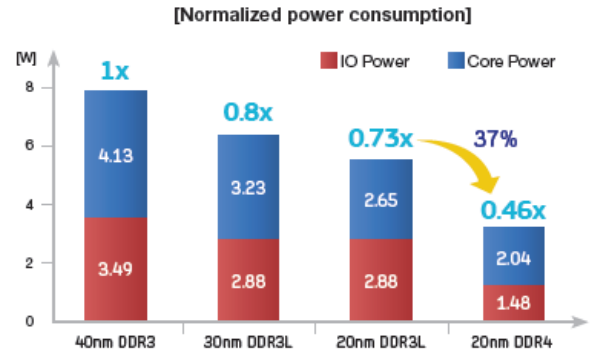


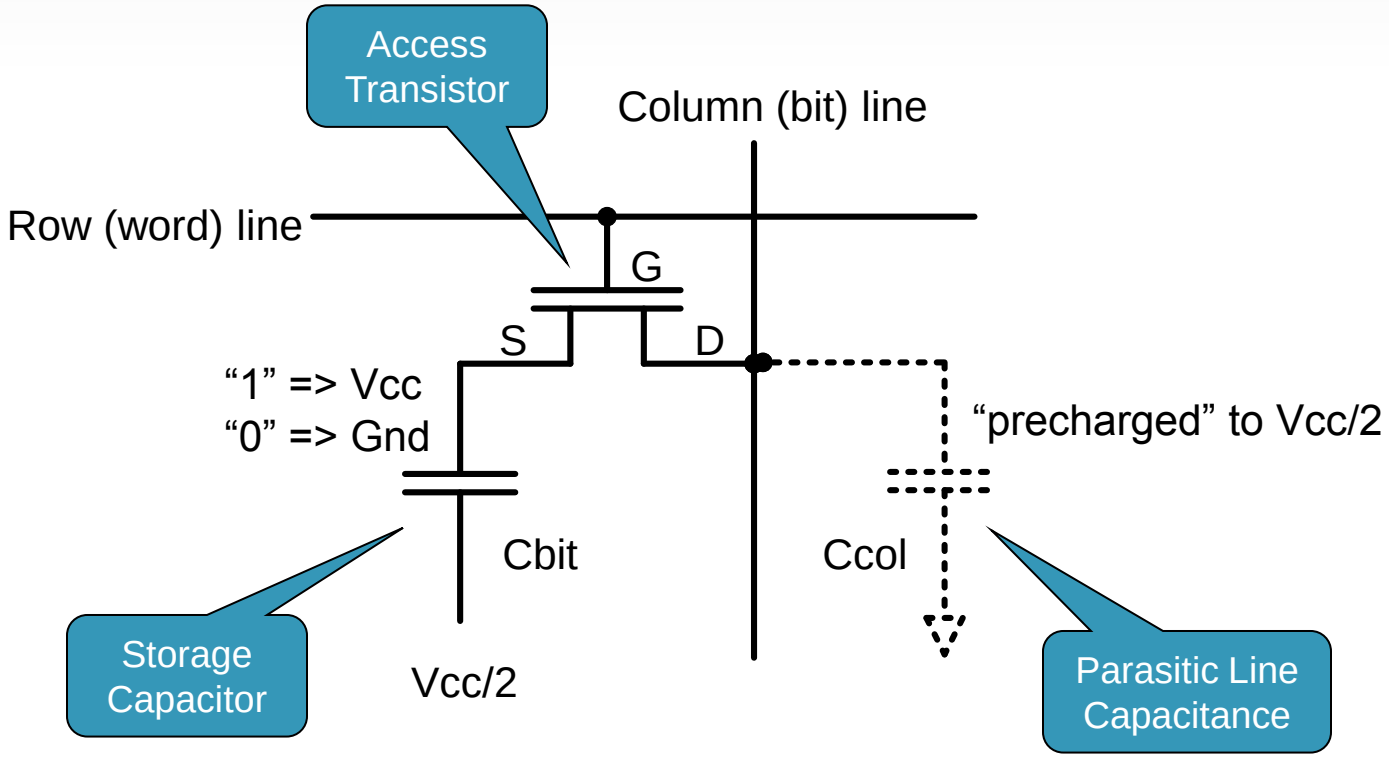
Figure 5. Reduced normalized power consumption requirements of DDR4 compared to DDR3L

SAMSUNG

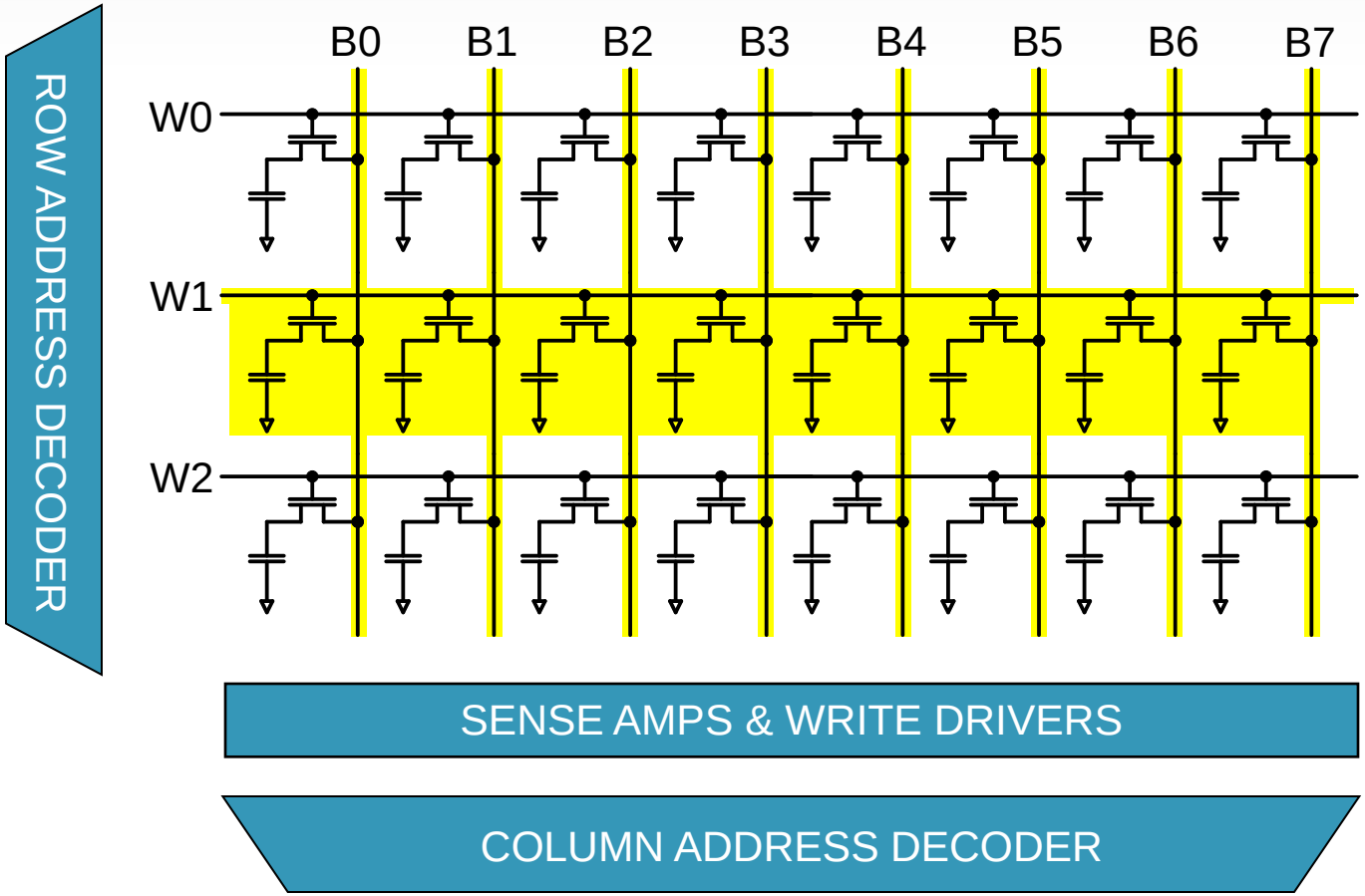
Basic DDR SDRAM Structure

Memory Organization and Operation

Single Transistor Memory Cell

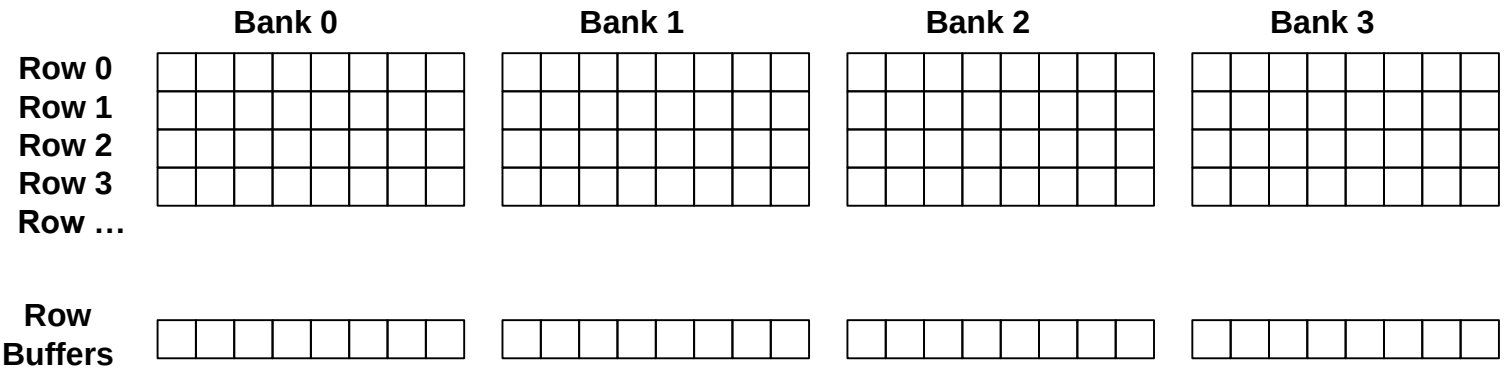


Memory Arrays



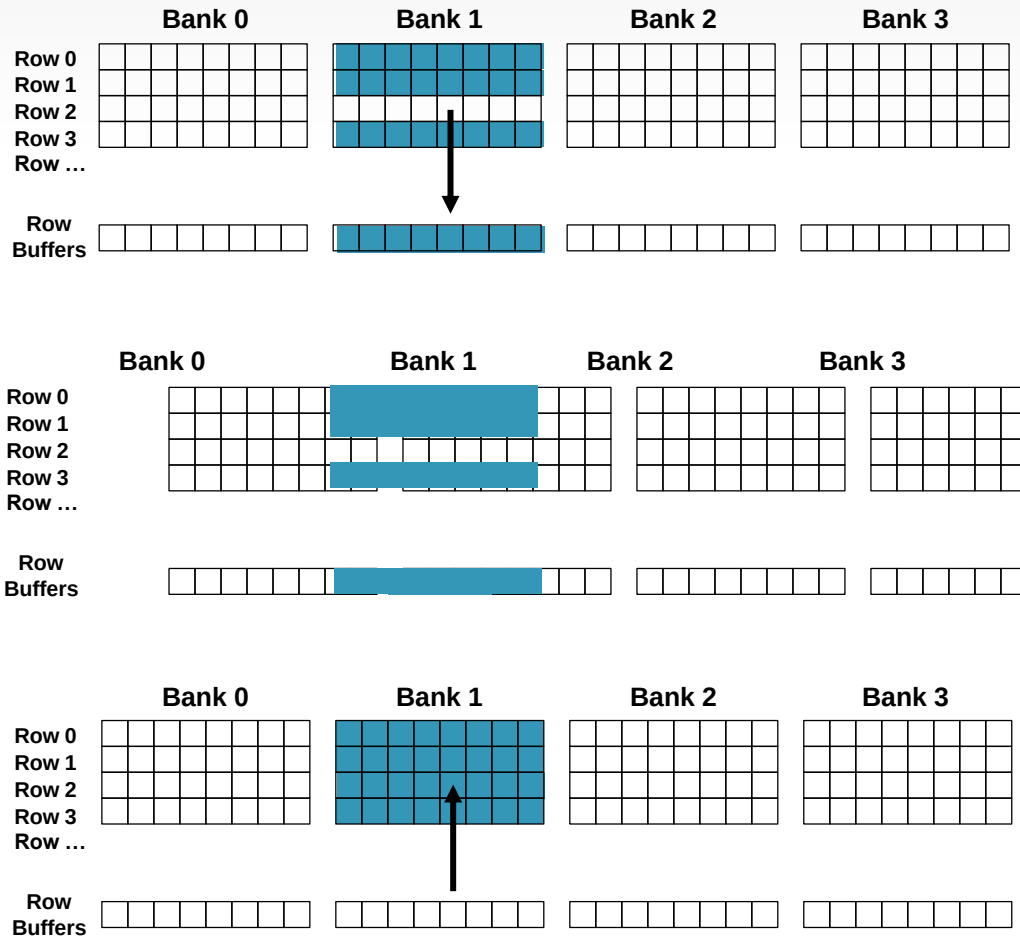
Internal Memory Banks

- Multiple arrays organized into banks
- Multiple banks per memory device
  - DDR1 – 4 banks, 2 bank address (BA) bits
  - DDR2 & DDR3 – 4 or 8 banks, 2 or 3 bank address (BA) bits
  - DDR4 -16 banks , with 4 banks in each of 4 bank groups
  - Can have one active row in each bank at any given time
- Concurrency
  - Can be opening or precharging a row in one bank while accessing another bank
- May be referred to as “internal”, “logical” or “sub-” banks



Memory Access

- A requested row is **ACTIVATED** and made accessible through the bank's row buffer
- **READ** and/or **WRITE** are issued to the active row
- The row is **PRECHARGED** and is no longer accessible through the bank's row buffer



QorIQ Family DDR Controllers

Features and Capabilities

DDR1/DDR2/DDR3/DDR3L Controller Features

- Supports most JEDEC standard x8, x16, x32 DDR1 & 2 & 3 devices
- Memory device densities from 64Mb – through 4Gb
- Data rates up to: 333 Mb/s for DDR1, 800 Mb/s for DDR2 and 1600 Mb/s DDR3
- Devices with 12-16 row address bits, 8-11 column address bits, 2-3 logical bank address bits
- Data mask signals for sub-doubleword writes
- Up to four physical banks (ranks / chip selects)
- Physical bank (rank) sizes up to 4GB, total memory up to 16GB per controller
- Physical bank interleaving between 2 or 4 chip selects
- Memory controller interleaving when more than 2 controllers are available
- Un-buffered or registered DIMMs

DDR1/DDR2/DDR3/DDR3L Controller Features (continued)

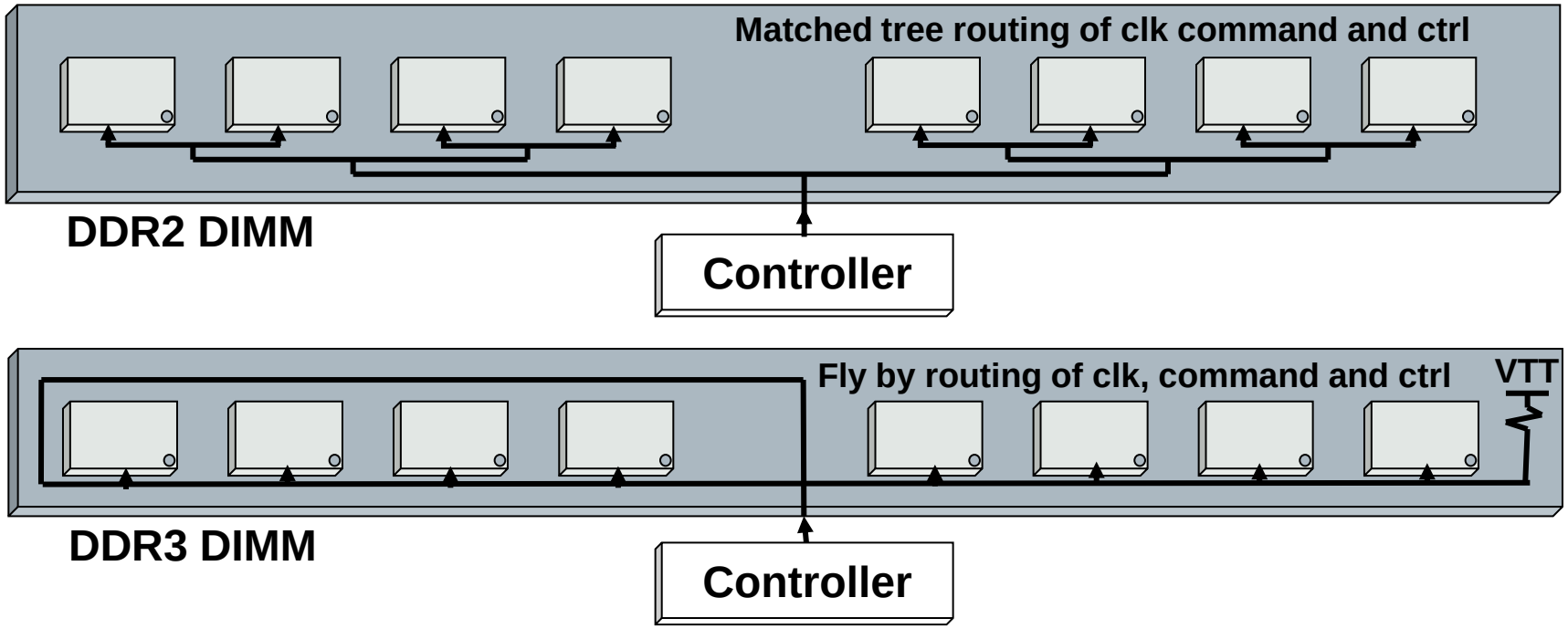
- Up to 32 open pages
  - Open row table
  - Amount of time rows stay open is programmable
- Auto-precharge, globally or by chip select
- Self-refresh
- Up to 8 posted refreshes
- Automatic or software-controlled memory device initialization
- ECC: 1-bit error correction, 2-bit error detection, detection of all errors within a nibble
- ECC error injection
- Read-modify-write for sub-doubleword writes when using ECC
- Automatic data initialization for ECC
- Dynamic power management

DDR2/DDR3/DDR3L Controller Additional Features

- Partial array self refresh
- Address and command parity for Registered DIMM
- Independent driver impedance setting for data, address/command, and clock
- Synchronous and Asynchronous clock-in option
- Write-leveling for DDR3
- Automatic CPO (operational)
- Asynchronous RESET for DDR3
- Automatic ZQ calibration for DDR3
- Fixed or On-the-Fly burst chop mode for DDR3
- Mirrored DIMM supported
- Many QorIQ devices offer full DDR3L support

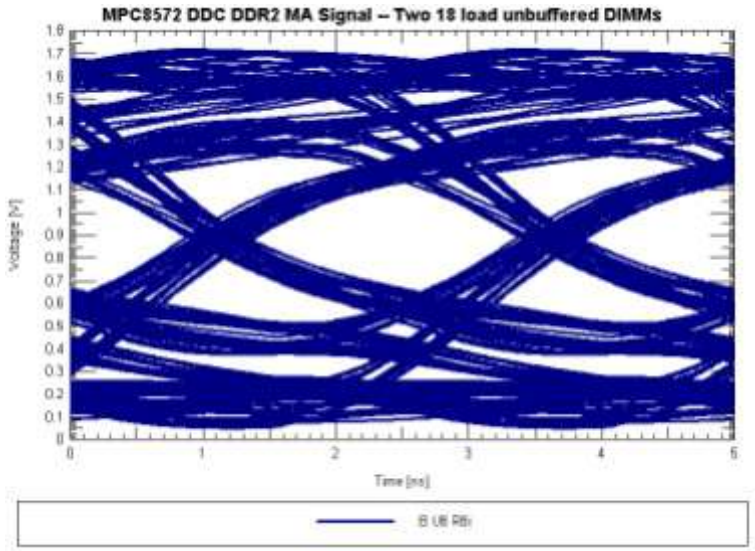
Fly-By Routing Topology

- Introduction of “fly-by” architecture
  - Address, command, control & clocks
  - Improved signal integrity…enabling higher speeds
  - On module termination

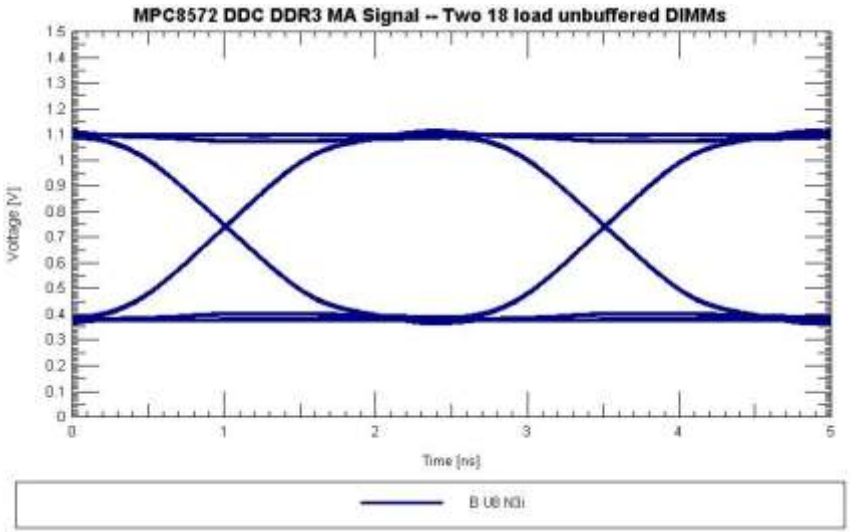


Fly-By Routing Improved SI

DDR2 Matched Tree Routing

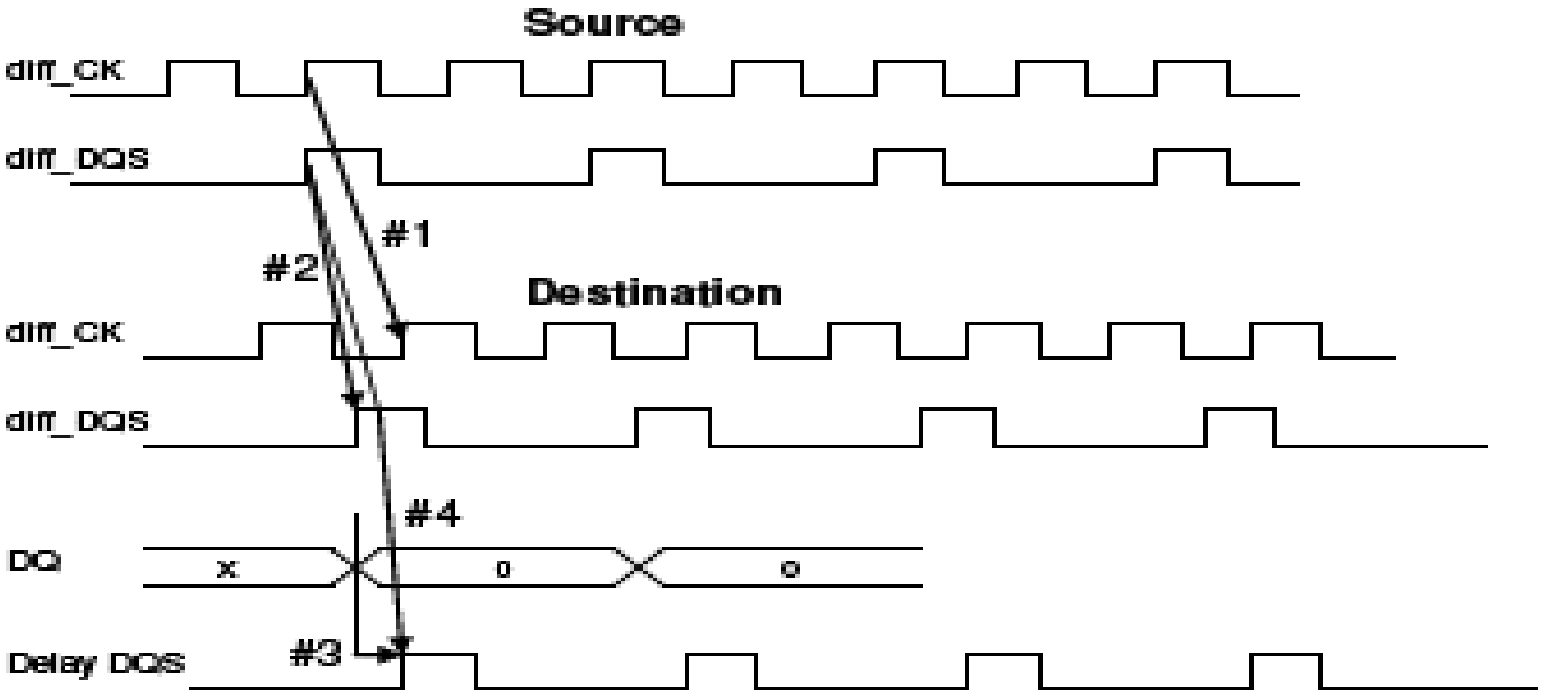


DDR3 Fly By Routing



What Is Write Leveling

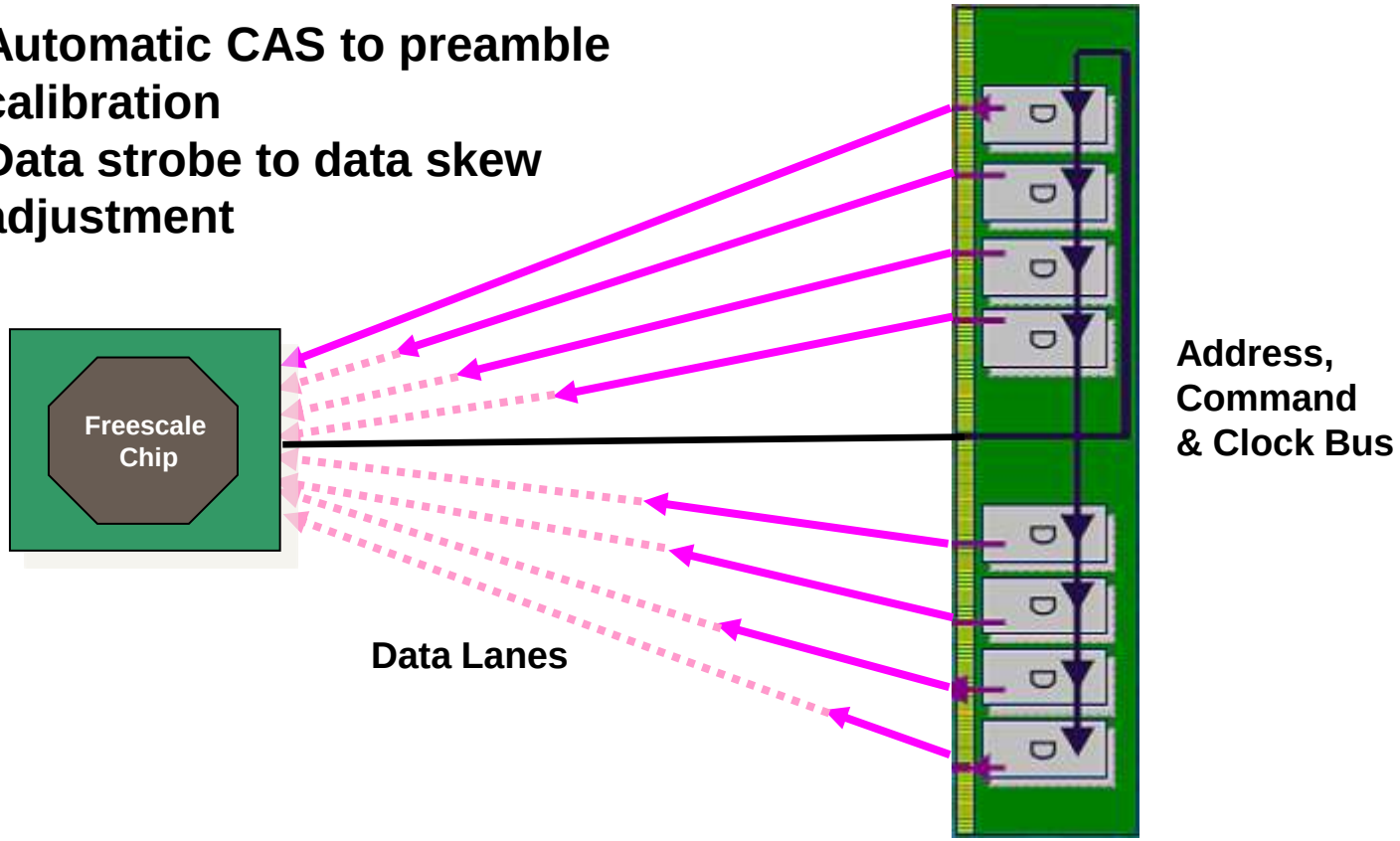
- During a write cycle, the skew between the clock and strobes is increased due to the fly-by topology. The write leveling will delay the strobe (and the corresponding data lanes) for each byte lane to reduce/compensate for this delay



Read Adjustment

- Instead of JEDEC's MPR method, Freescale controllers use a proprietary method of read adjust method. Auto CPO will provide the expected arrival time of preamble for each strobe line of each byte lane during the read cycle to adjust for the delays cased by the fly-by topology

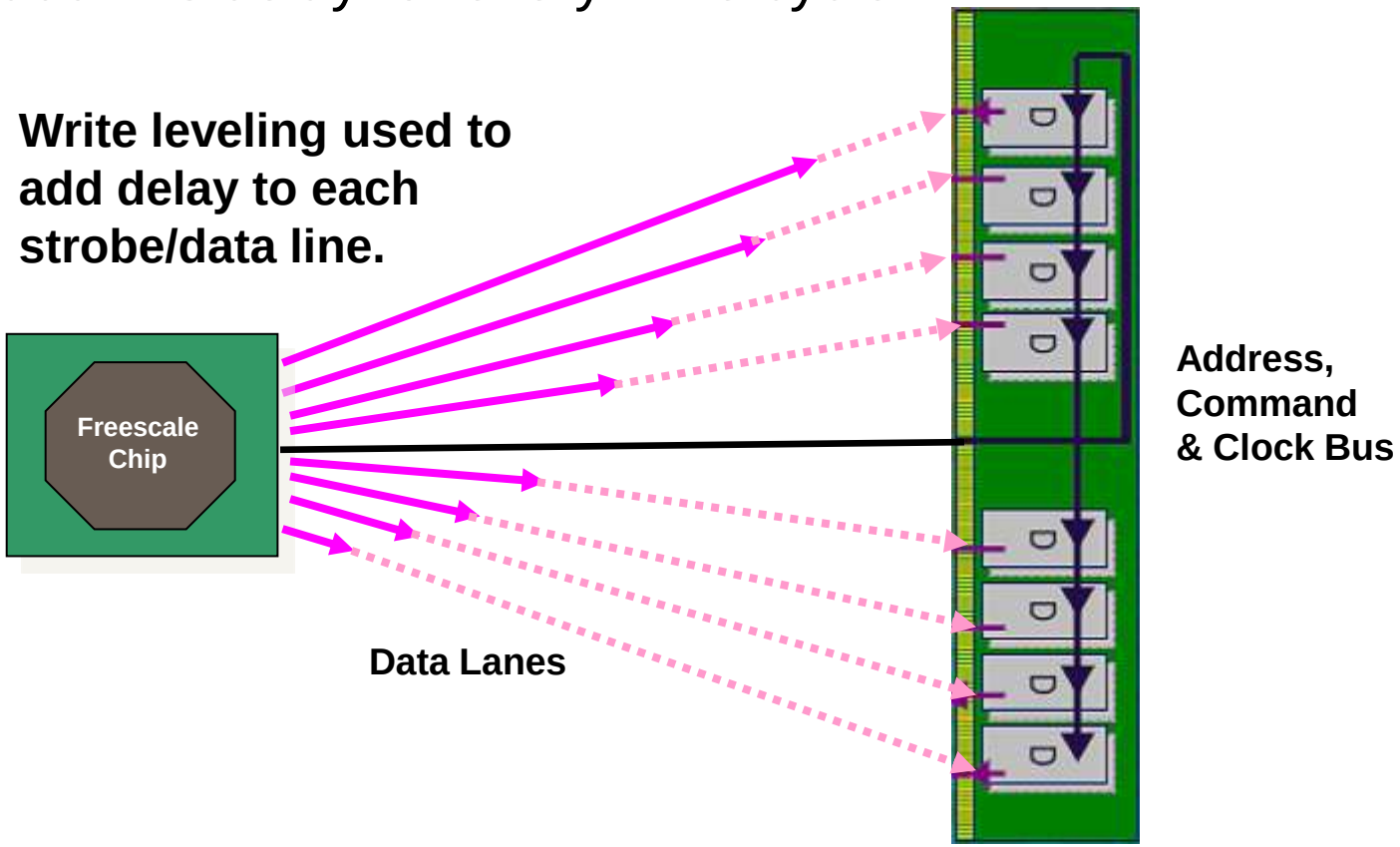
  - **Automatic CAS to preamble calibration**
  - **Data strobe to data skew adjustment**



Write Adjustment

- Write leveling sequence during the initialization process will determine the appropriate delays to each strobe/data byte lane and add this delay for every write cycle

  - **Write leveling used to add delay to each strobe/data line.**



DDR3L support

- DDR3L (1.35V) is a low voltage version of the DDR3 (1.5V)
- DDR3L meets the exact same functional and timing specifications of DDR3
- VIH/VIL differences are compensated by corresponding derating values to Vref resulting in no change in AC timing, and timing budget calculation
- The main considerations for using DDR3L are:
  - Memory controller needs to support DDR3L
    - P1023, P1017, P1010, P1014, P2040, P3041, P5020
  - The supply voltage needs to be at 1.35V
  - Using DDR3L SDRAM

Register Configuration

- Two general type of registers to be configured in the memory controller
- First register type is set to the DRAM related parameter values that are provided via SPD or DRAM datasheet
- Second register type is the non-SPD values that are set based on the specific application. For example:
  - On-die-termination (ODT) settings for DRAM and controller
  - Driver impedance setting for DRAM and controller
  - Clock adjust, write data delay, Cast to preamble override (CPO)
  - 2T or 3T timing
  - Burst type selection (fixed or on-the-fly burst chop mode)
  - Write-leveling start value (WRLVL_START)
- Freescale's Processor Expert QorIQ Configuration Suite includes a DDR configuration tool for many devices. For other devices, Freescale support resources can help generate or analyze DDR settings.

DDR3 SDRAM

Summary

Summary

- DDR3/DDR3L is mainstream now
- DDR4 is expected to start entering the market by 2013
- All QorIQ devices support DDR3
- All features of DDR3, such as write leveling, ZQ calibration, ODT, Mirrored DIMM, … are supported by the memory controller in QorIQ devices
- Follow JEDEC recommended topologies for discrete parts
- Configuration and initialization of memory controller is easily achieved

Useful References

- Books:
  - DRAM Circuit Design: A Tutorial, Brent Keeth and R. Jacob Baker, IEEE Press, 2001
- Freescale AppNotes:
  - AN2582 Hardware and Layout Design Considerations for DDR Memory Interfaces
  - AN2910 Hardware and Layout Design Considerations for DDR2 Memory Interfaces
  - AN2583 Programming the PowerQUICCIII / PowerQUICCII Pro DDR SDRAM Controller
  - AN3369 PowerQUICC DDR2 SDRAM Controller Register Setting Considerations
  - AN3939 PQ & QorIQ Interleaving
  - AN3940 Layout Design Considerations for DDR3 Memory Interface
  - AN4039 PowerQUICC DDR3 SDRAM Controller Register Setting Considerations
- Micron AppNotes:
  - TN-46-05 General DDR SDRAM Functionality
  - TN-47-02 DDR2 Offers New Features and Functionality
  - TN-47-01 DDR2 Design Guide
  - TN-41-07 DDR3 Power-Up, Initialization, and Reset
  - TN-41-08 DDR3 Design Guide
- JEDEC Specs:
  - JESD79E Double Data Rate (DDR) SDRAM Specification
  - JESD79-2F DDR2 SDRAM Specification
  - JESD79-3D DDR3 SDRAM Specification

DDR Configuration and Validation Tools

QorIQ Configuration Suite – Now Available!

- **QorIQ Configuration Suite v2.3 is NOW AVAILABLE!!!**
  - Supports all QorIQ and Qorivva devices
  - Works with Eclipse 3.5, Eclipse 3.6, Eclipse 3.7 development tools
    - Pure Java solution for maximum choice of host system support
    - Add-in to CodeWarrior Development Studio for PA, v10.1 or later
  - Available from www.freescale.com/QCS – FREE DOWNLOAD*
- **Includes the following four configuration tools all designed to collaborate on consistent configuration:**
  - PBL tool to define the Reset Control Word bit values and PBI data for the pre-boot
  - BOOTROM generator for those QorIQ without RCW functionality
  - DDR configuration supports setting the controller to a working state for any DDR
  - Data path graphical view helps to define data path configuration for the DPAA.
  - Hardware Device Tree editor supports references, synchronous GUI and XML editing, node validation based on specification bindings
  - Packaged as a separate product with installer and wizard functionality

* Must be a QorIQ customer or under QorIQ NDA for download permission

Actual URL is http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=PE_QORIQ_SUITE&tid=PEH

Installing Processor Expert for QorIQ

- You need CodeWarrior for PA 10.1 or later

  OR, you download an Eclipse version for free

  OR, you use an existing Eclipse workbench you have installed (Wind River, QNX, GNU, etc.)

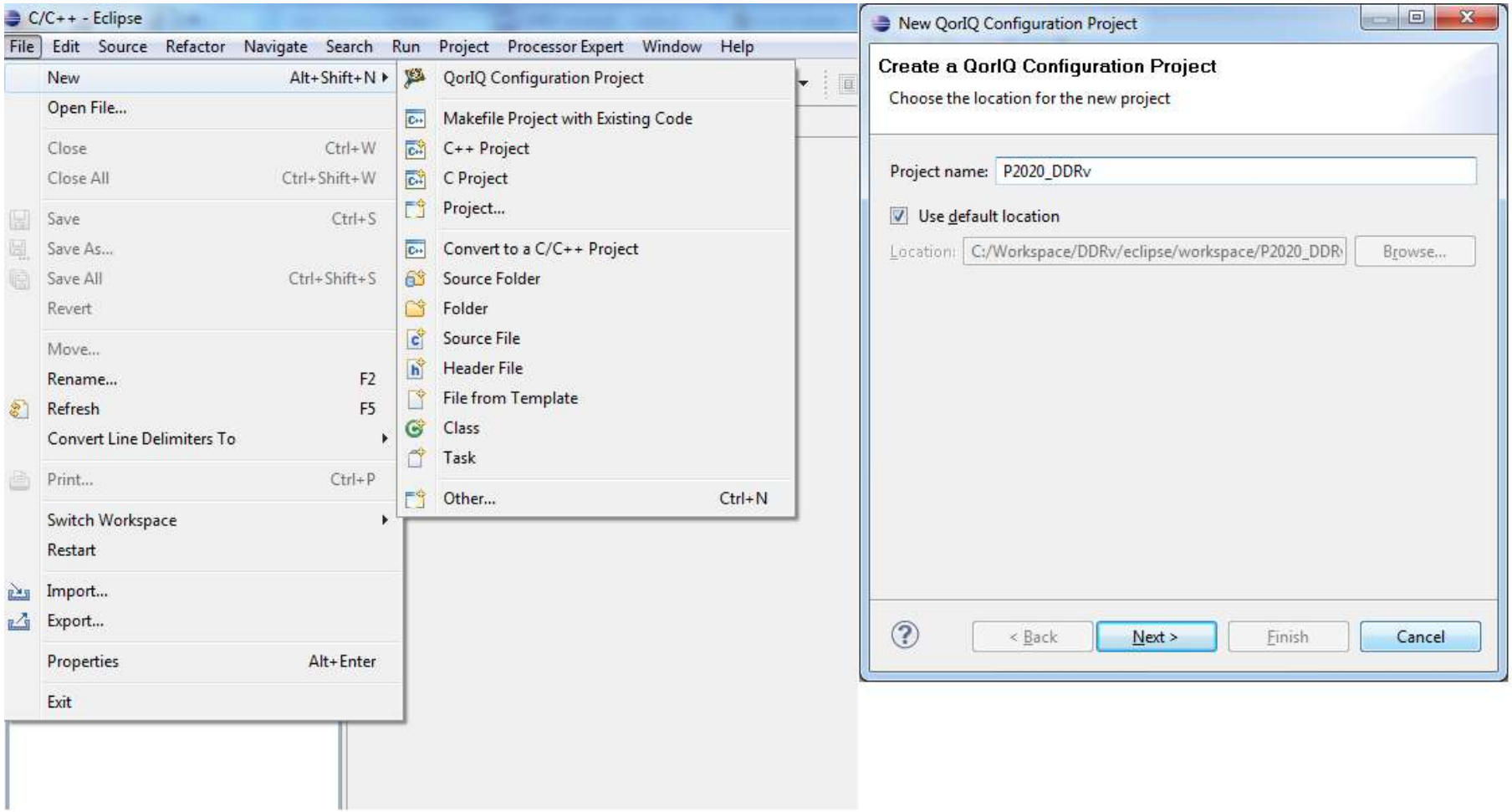
- Processor Expert for QorIQ Configuration Suite installs using the Eclipse updater's "Add new software…" capability

- The Configuration Suite is 100% pure Java so it should run on any Eclipse 3.6.1 or later host environment (Windows, Linux, Solaris, Mac OS, 32-bit/64-bit, …)

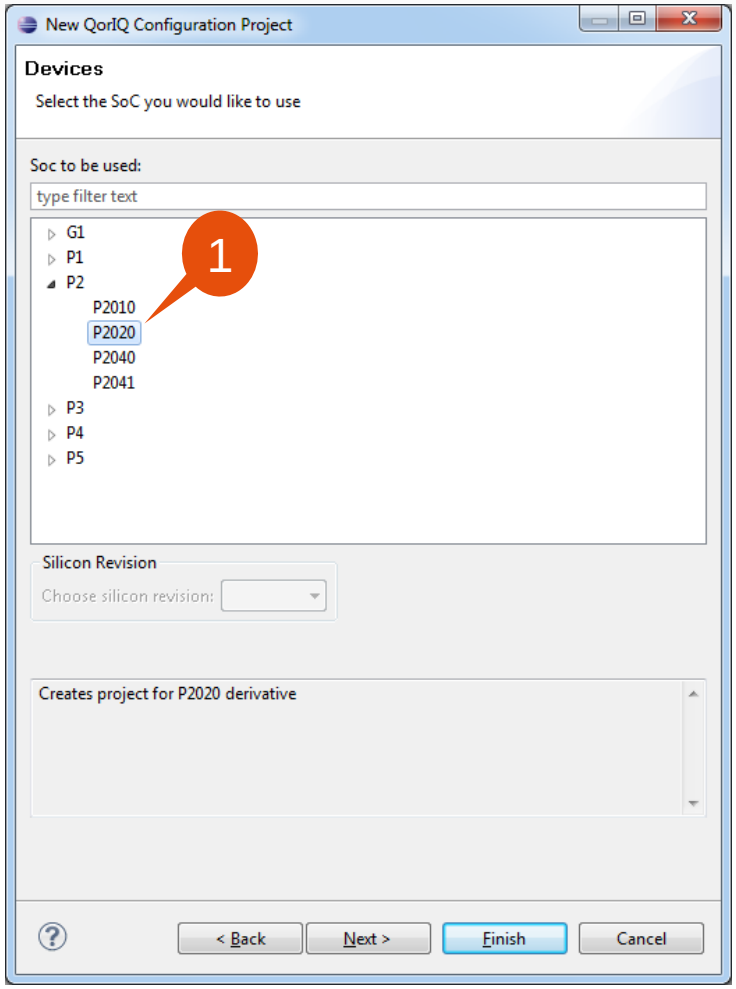
DDR Configuration

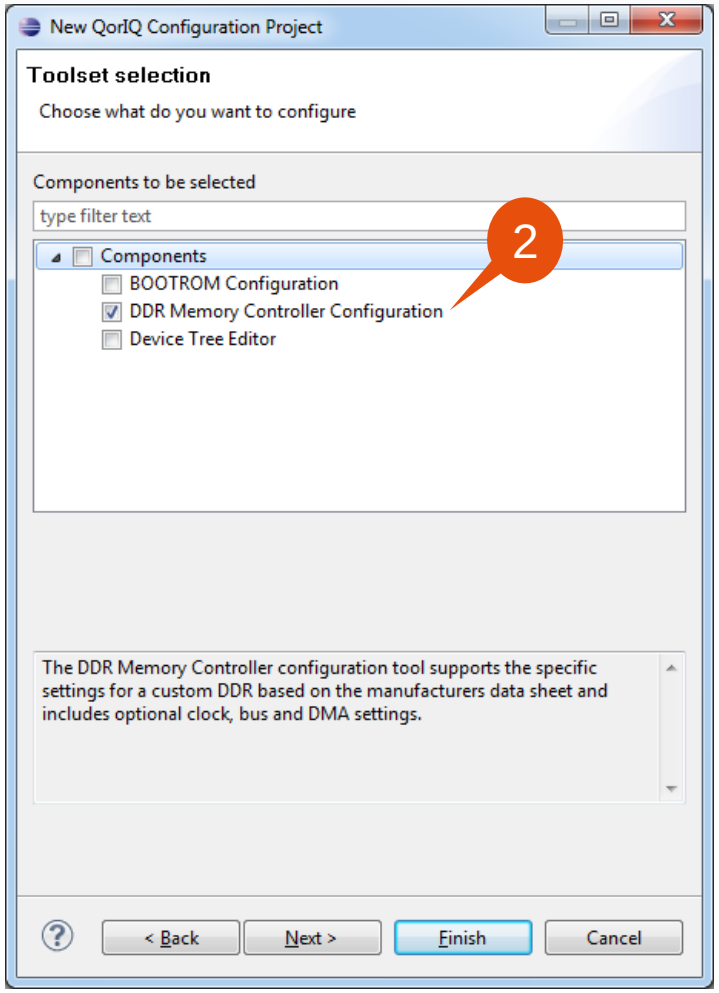
Lab: Creating New DDR Configuration

Create New QCS project

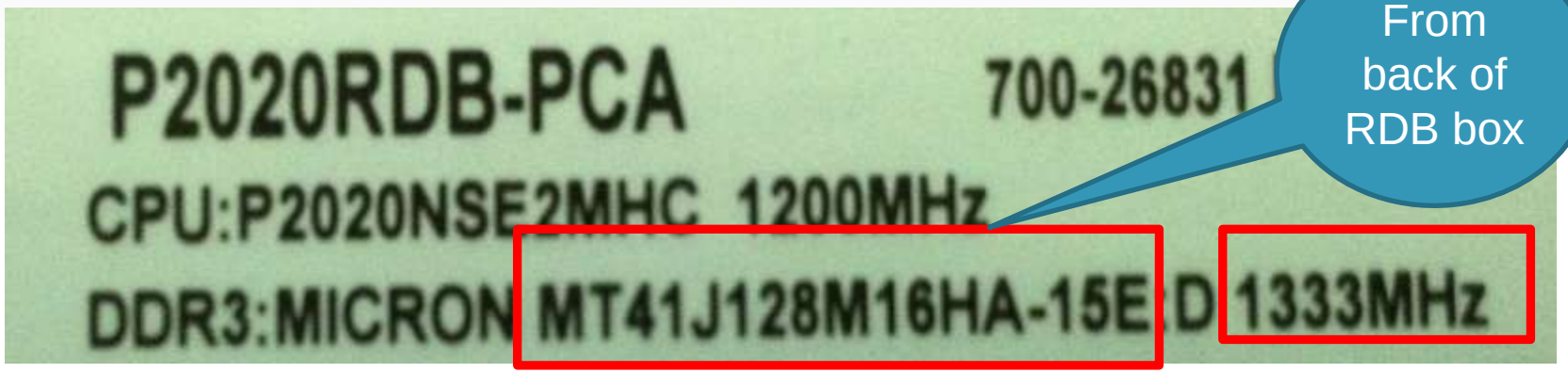


Select device and DDR component





Get DRAM information – P2020RDB-PCA



Micron

DDR3 SDRAM

MT41J512M4 – 64 Meg x 4 x 8 Banks

MT41J256M8 – 32 Meg x 8 x 8 Banks

MT41J128M16 – 16 Meg x 16 x 8 Banks

From DRAM datasheet

How about rest of the timing parameters?

Table 1: Key Timing Parameters

Speed Grade	Data Rate (MT/s)	Target tRCD-tRP-CL	tRCD (ns)	tRP (ns)	CL (ns)
-093[1, 2, 3, 4]	2133	14-14-14	13.09	13.09	13.09
-107[1, 2, 3]	1866	13-13-13	13.91	13.91	13.91
-125[1, 2]	1600	11-11-11	13.75	13.75	13.75
-15E[1]	1333	9-9-9	13.5	13.5	13.5
-187E	1066	7-7-7	13.1	13.1	13.1

Features

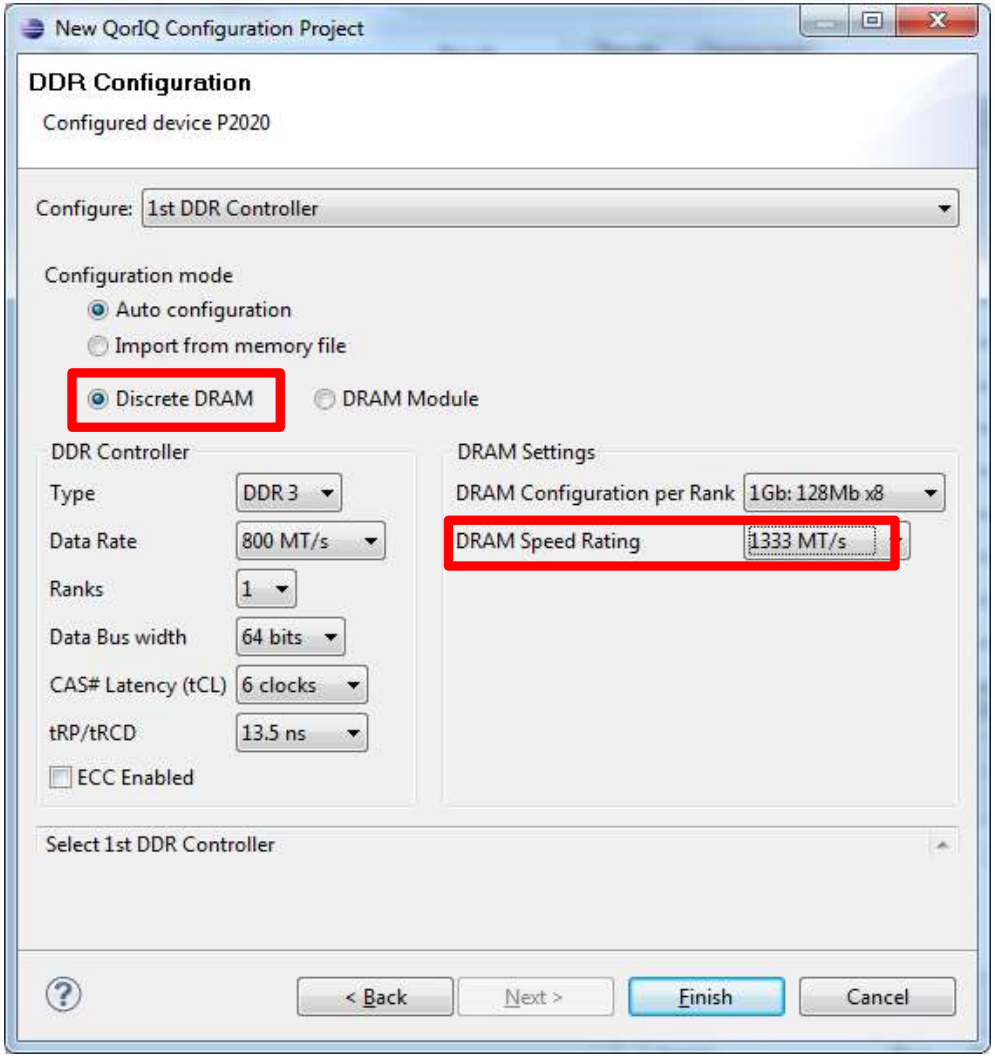
- $V_{DD} = V_{DDQ}$ = 1.5V ±0.075V
- 1.5V center-terminated push/pull I/O
- Differential bidirectional data strobe
- 8*n*-bit prefetch architecture
- Differential clock inputs (CK, CK#)
- 8 internal banks
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Programmable CAS READ latency (CL)
- Posted CAS additive latency (AL)
- Programmable CAS WRITE latency (CWL) based on tCK
- Fixed burst length (BL) of 8 and burst chop (BC) of 4 (via the mode register set [MRS])
- Selectable BC4 or BL8 on-the-fly (OTF)
- Self refresh mode
- T_C of 0°C to 95°C
  - 64ms, 8192 cycle refresh at 0°C to 85°C
  - 32ms, 8192 cycle refresh at 85°C to 95°C
- Self refresh temperature (SRT)
- Write leveling
- Multipurpose register
- Output driver calibration

Options[1]	Marking
• Configuration	
– 512 Meg x 4	512M4
– 256 Meg x 8	256M8
– 128 Meg x 16	128M16
• FBGA package (Pb-free) – x4, x8	
– 78-ball (8mm x 10.5mm) Rev. H,M,J,K	DA
– 78-ball (9mm x 11.5mm) Rev. D	HX
• FBGA package (Pb-free) – x16	
– 96-ball (9mm x 14mm) Rev. D	HA
– 96-ball (8mm x 14mm) Rev. K	JT
• Timing – cycle time	
– 938ps @ CL = 14 (DDR3-2133)	-093
– 1.071ns @ CL = 13 (DDR3-1866)	-107
– 1.25ns @ CL = 11 (DDR3-1600)	-125
– 1.5ns @ CL = 9 (DDR3-1333)	-15E
– 1.87ns @ CL = 7 (DDR3-1066)	-187E
• Operating temperature	
– Commercial (0°C ≤ T_C ≤ +95°C)	None
– Industrial (–40°C ≤ T_C ≤ +95°C)	IT
• Revision	:D/:H/:J/:K/:M

Note: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on http://www.micron.com for available offerings.

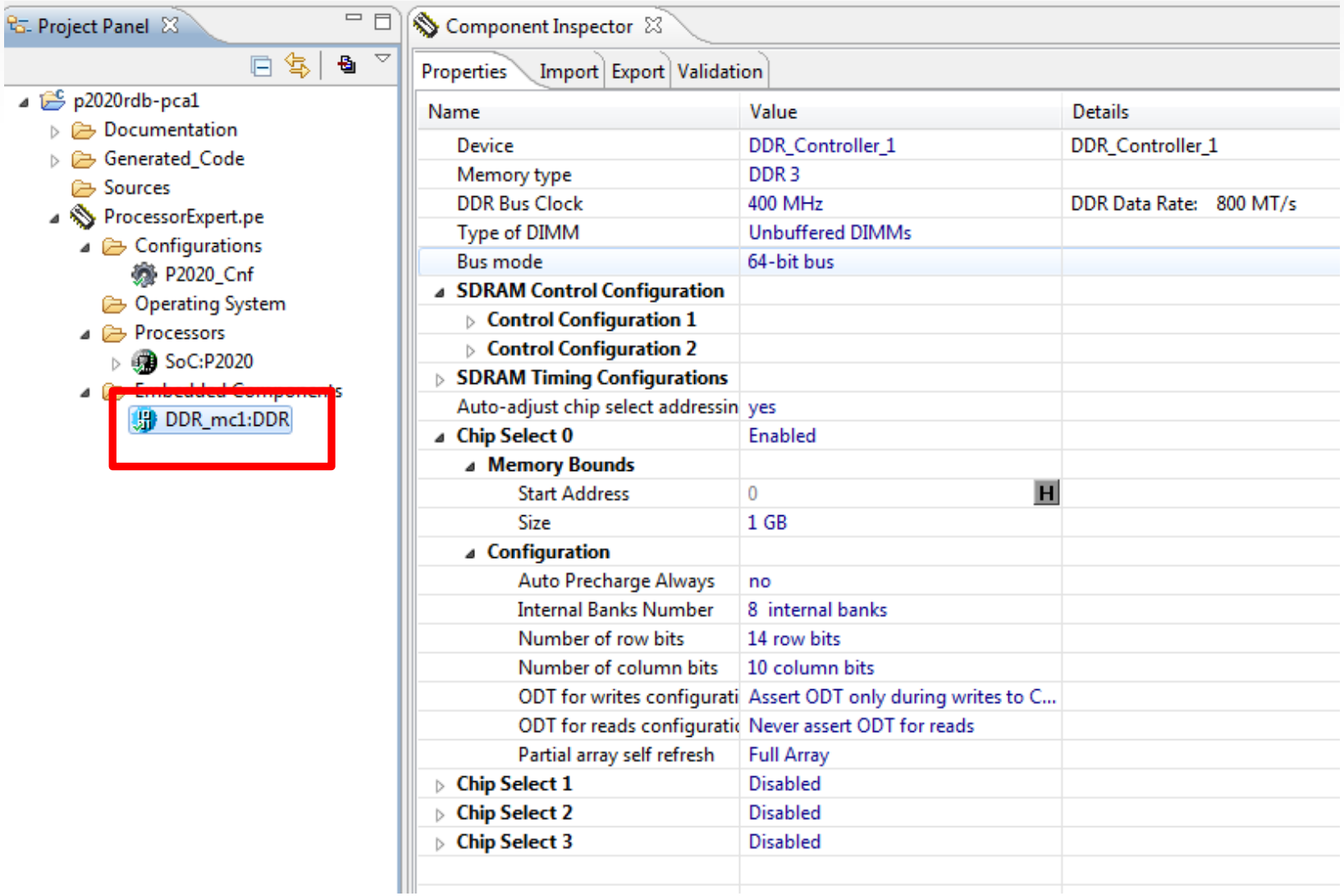
- Tool automatically computes tRCD, tRP, and CL!
  - User can change these values if required.

DDR New Project Wizard

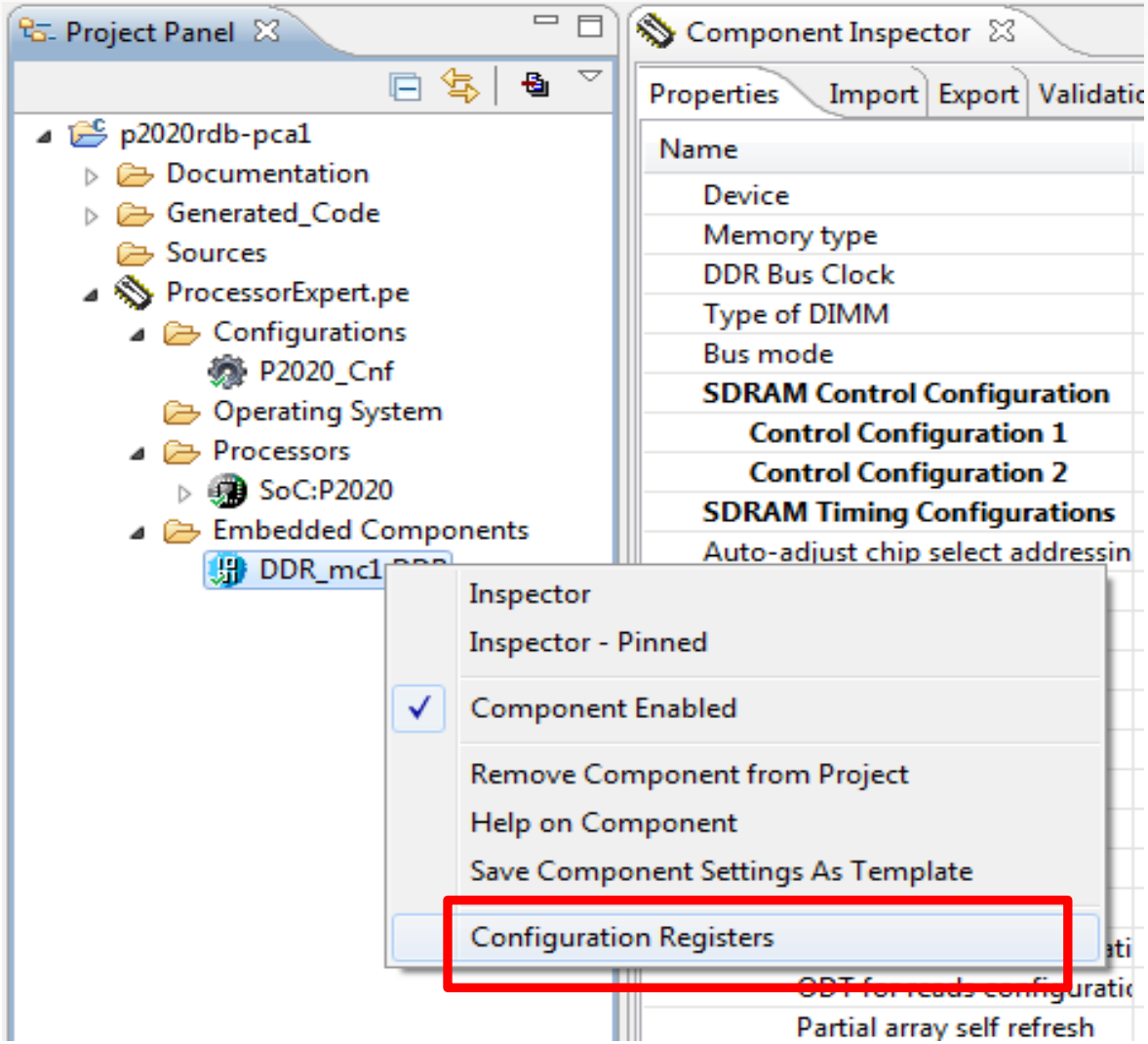


- From memory data sheet:
  - Maximum speed rating
  - Capacity

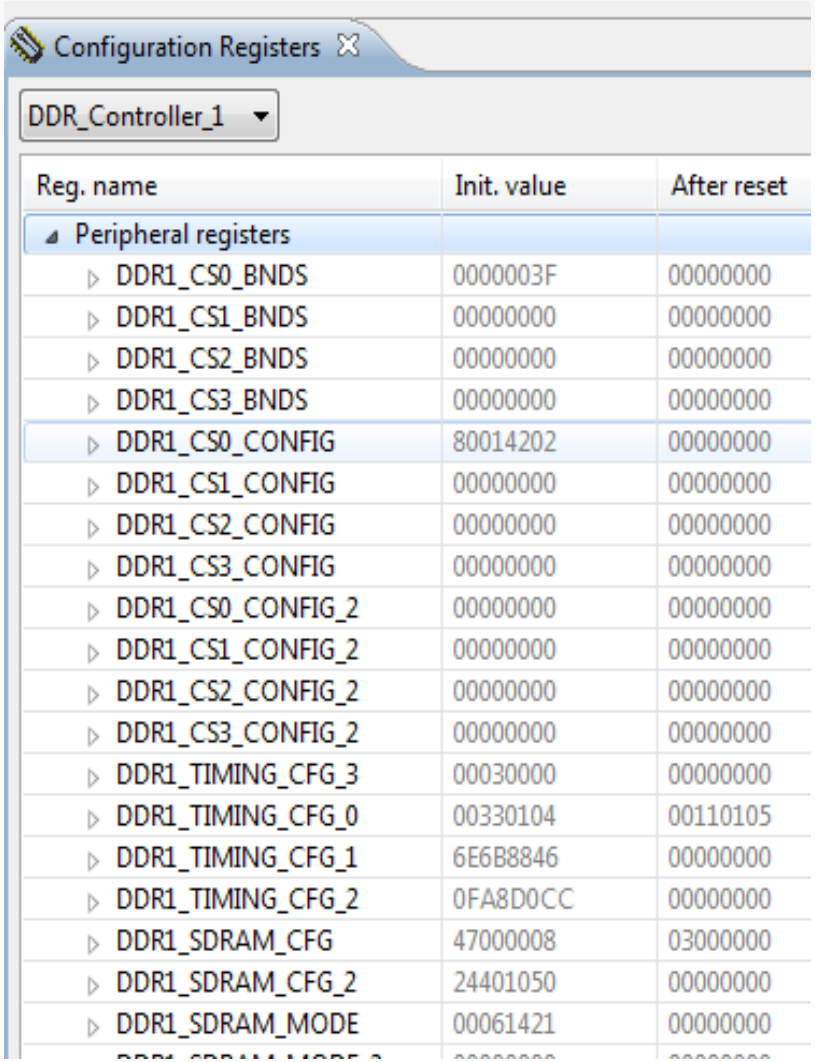
QCS project explorer



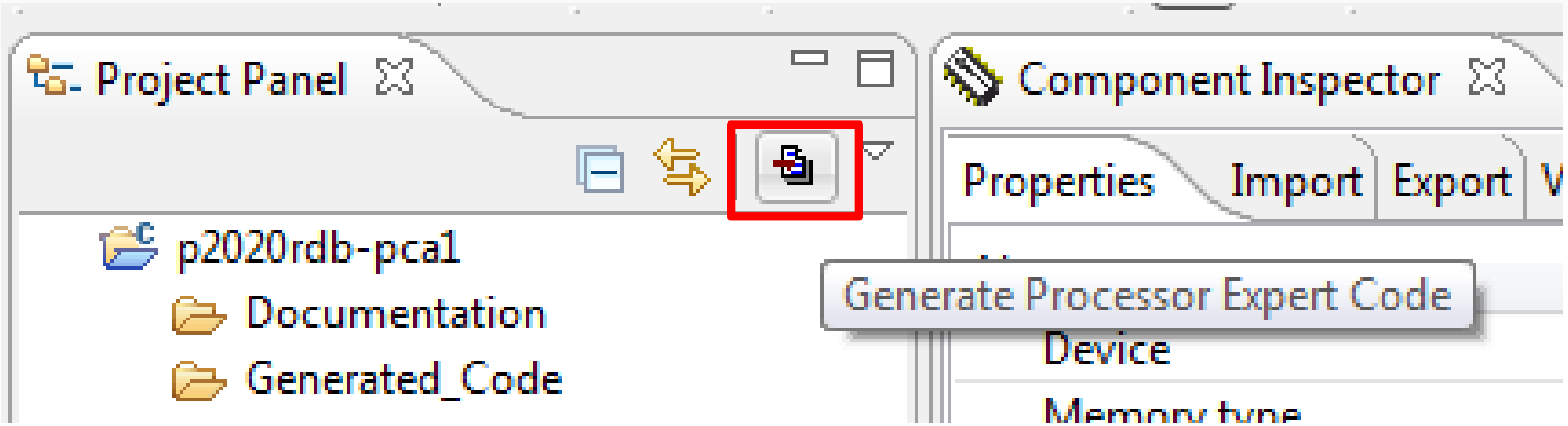
Review DDR registers values

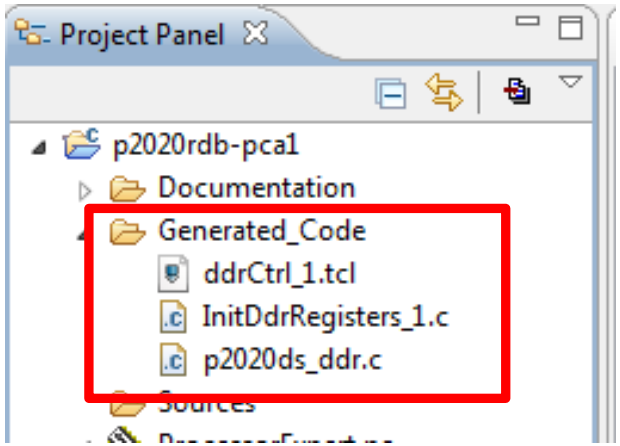


Review DDR registers values – contd.



Generate DDR configuration





Generated files – CW, uboot, ddrinit.c

```
# DDR Controller 1 Registers

  # DDR_SDRAM_CFG
  mem [0xFF702110] = 0x47000008

  # CS0_BNDS
  mem [0xFF702000] = 0x3F

  # CS0_CONFIG
  mem [0xFF702080] = 0x80014202

  # CS0_CONFIG_2
  mem [0xFF7020C0] = 0x00

  # TIMING_CFG_3
  mem [0xFF702100] = 0x00030000

  # TIMING_CFG_0
  mem [0xFF702104] = 0x00330104

  # TIMING_CFG_1
  mem [0xFF702108] = 0x6E6B8846

  # TIMING_CFG_2
  mem [0xFF70210C] = 0x0FA8D0CC

  # DDR_SDRAM_CFG_2
  mem [0xFF702114] = 0x24401050

  # DDR_SDRAM_MODE
  mem [0xFF702118] = 0x00061421
```

```
#define DDR_1_INIT_EXT_ADDR_ADDR     0xFF70214C
#define DDR_1_SDRAM_RCW_1_ADDR       0xFF702180
#define DDR_1_SDRAM_RCW_2_ADDR       0xFF702184
#define DDR_1_DATA_INIT_ADDR         0xFF702128
#define DDR_1_SDRAM_MD_CNTL_ADDR     0xFF702120
#define DDR_1_DDRCDR_1_ADDR          0xFF702B28
#define DDR_1_DDRCDR_2_ADDR          0xFF702B2C

#define SDRAM_CFG_MEM_EN_MASK        0x80000000
#define SDRAM_CFG2_D_INIT_MASK       0x00000010

/* DDR Controller configured registers' values */
#define DDR_1_CS0_BNDS_VAL           0x3F
#define DDR_1_CS1_BNDS_VAL           0x00
#define DDR_1_CS2_BNDS_VAL           0x00
#define DDR_1_CS3_BNDS_VAL           0x00
#define DDR_1_CS0_CONFIG_VAL         0x80014202
#define DDR_1_CS1_CONFIG_VAL         0x00
```

```
#define PEX_CONFIG_DDR1_INIT_EXT_ADDR     0x00000000
#define PEX_CONFIG_DDR1_TIMING_4          0x00220001
#define PEX_CONFIG_DDR1_TIMING_5          0x02401400
#define PEX_CONFIG_DDR1_ZQ_CNTL           0x89080600
#define PEX_CONFIG_DDR1_WRLVL_CNTL        0x8655F614
#define PEX_CONFIG_DDR1_RCW_1             0x00000000
#define PEX_CONFIG_DDR1_RCW_2             0x00000000


/* DDR Controller 1 configuration global structures */
fsl_ddr_cfg_regs_t ddr_cfg_regs_0 = {
  .cs[0].bnds = PEX_CONFIG_DDR1_CS0_BNDS,
  .cs[1].bnds = PEX_CONFIG_DDR1_CS1_BNDS,
  .cs[2].bnds = PEX_CONFIG_DDR1_CS2_BNDS,
  .cs[3].bnds = PEX_CONFIG_DDR1_CS3_BNDS,
  .cs[0].config = PEX_CONFIG_DDR1_CS0_CONFIG,
  .cs[1].config = PEX_CONFIG_DDR1_CS1_CONFIG,
  .cs[2].config = PEX_CONFIG_DDR1_CS2_CONFIG,
```

Steps to adapt DDR configuration file in CodeWarrior

- Open the CW config file you want to adapt

  D:\Program Files\Freescale\CW PA v10.1\PA\PA_Support\Initialization_Files\QorIQ_P4\P4080DS_init_core0.cfg

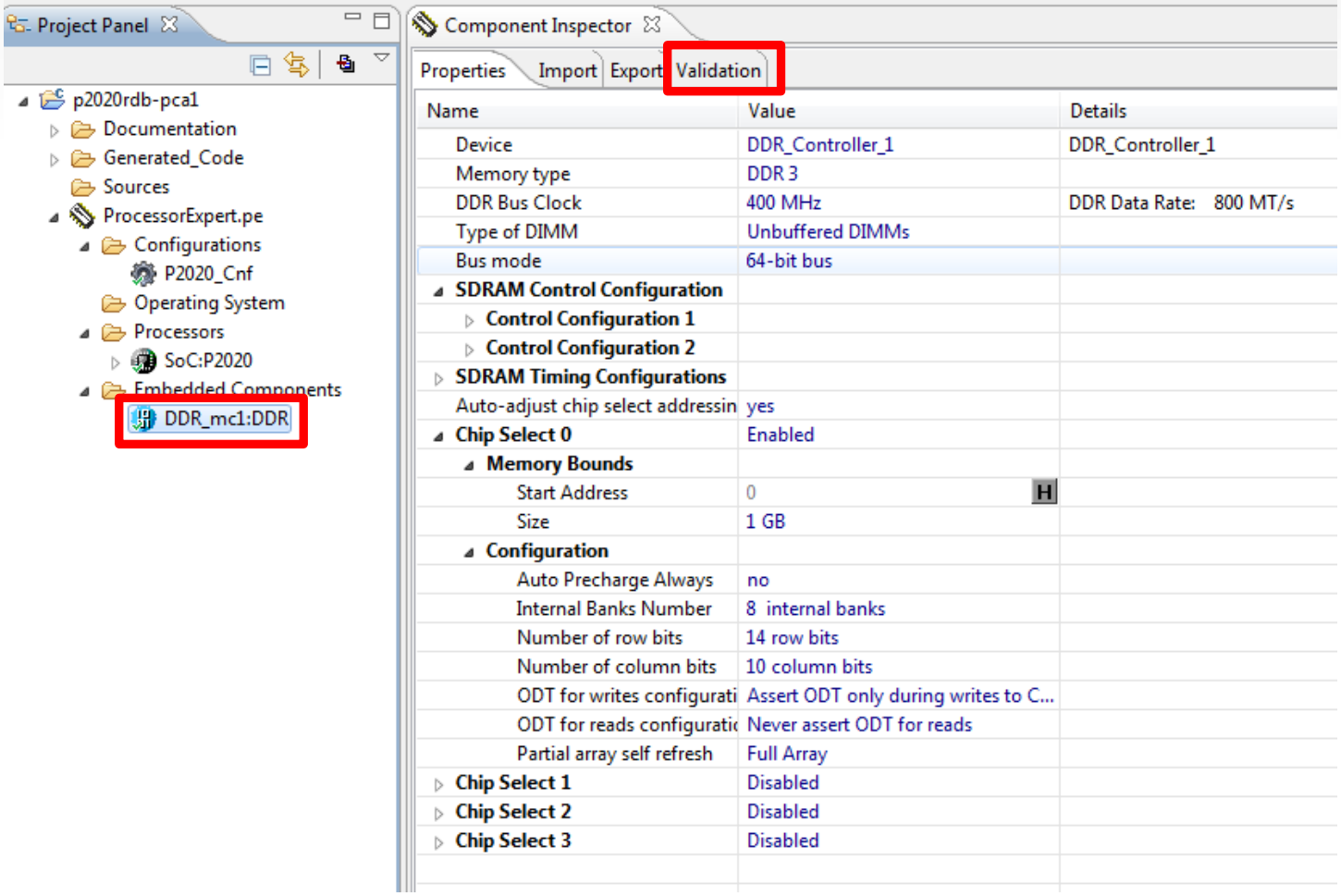
- Replace DDR1 config section with the one from

  D:\Profiles\b08844\workspace\p4080\Generated_Code\ddrCtrl_1.cfg

- Use this new config file with your stationary project

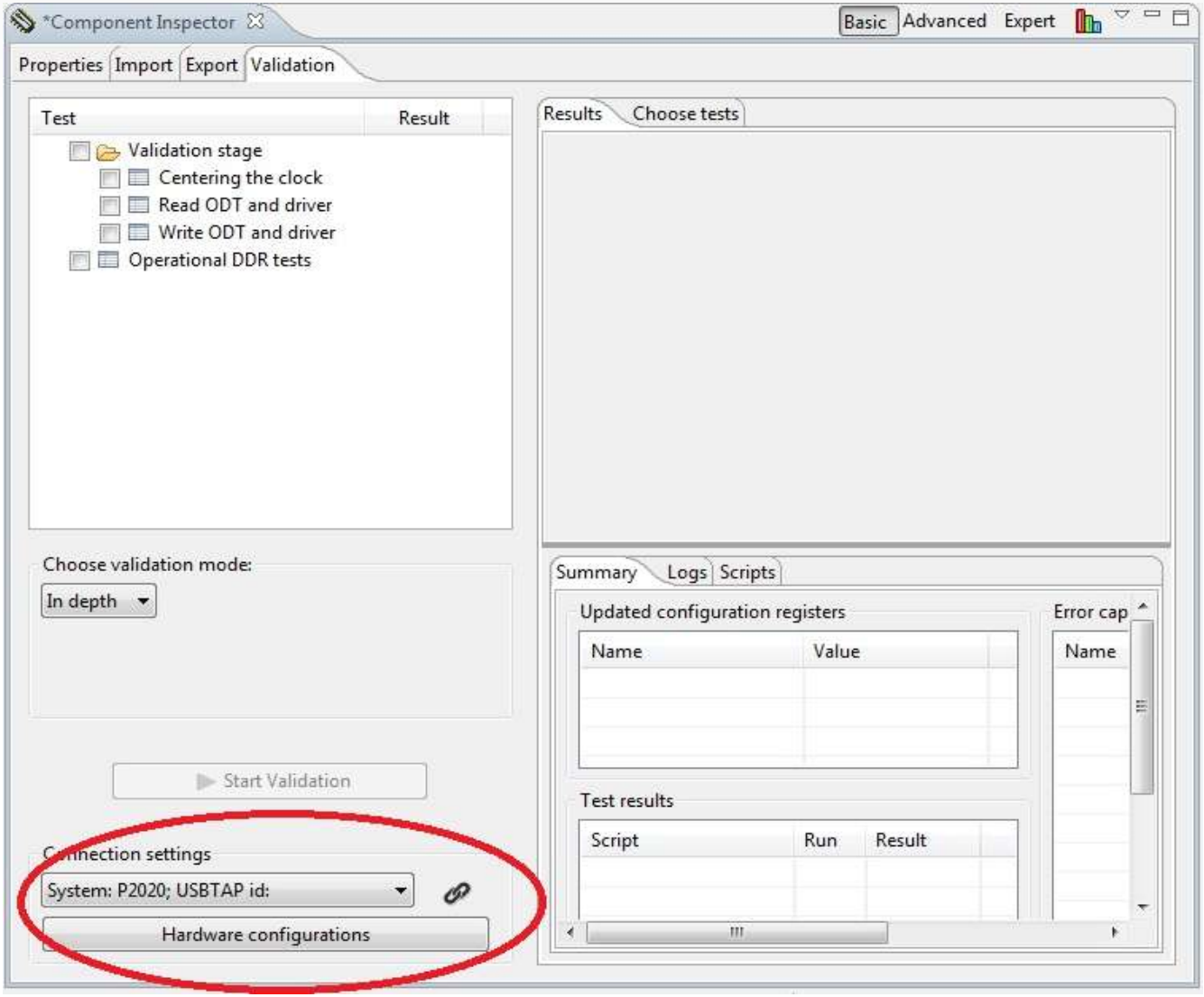
DDR Validation Tool

DDR Validation Tool - Activate

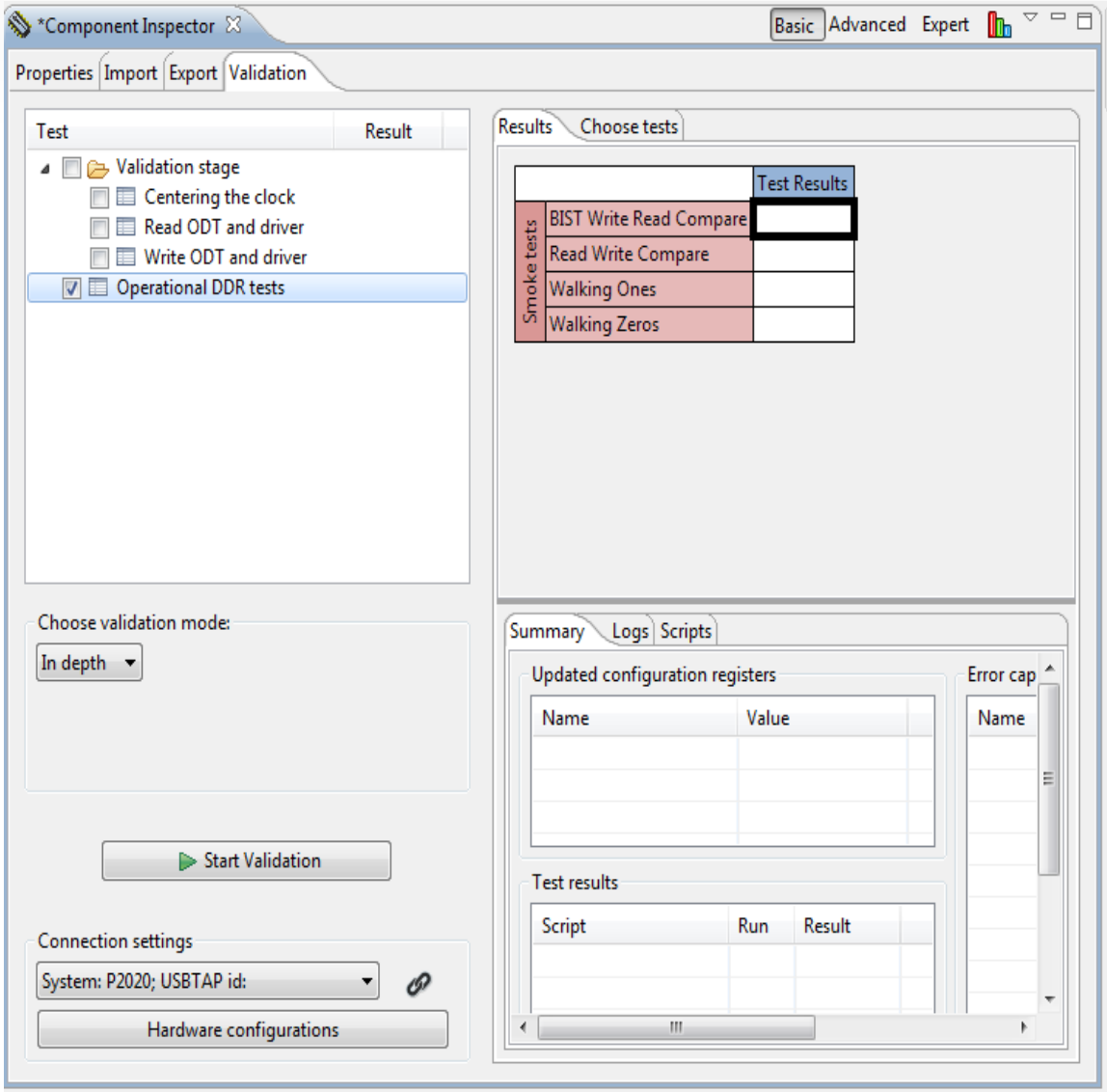


License file:
<QCS Install directory>/eclipse/Optimization/license.dat

DDRv Connection Setup

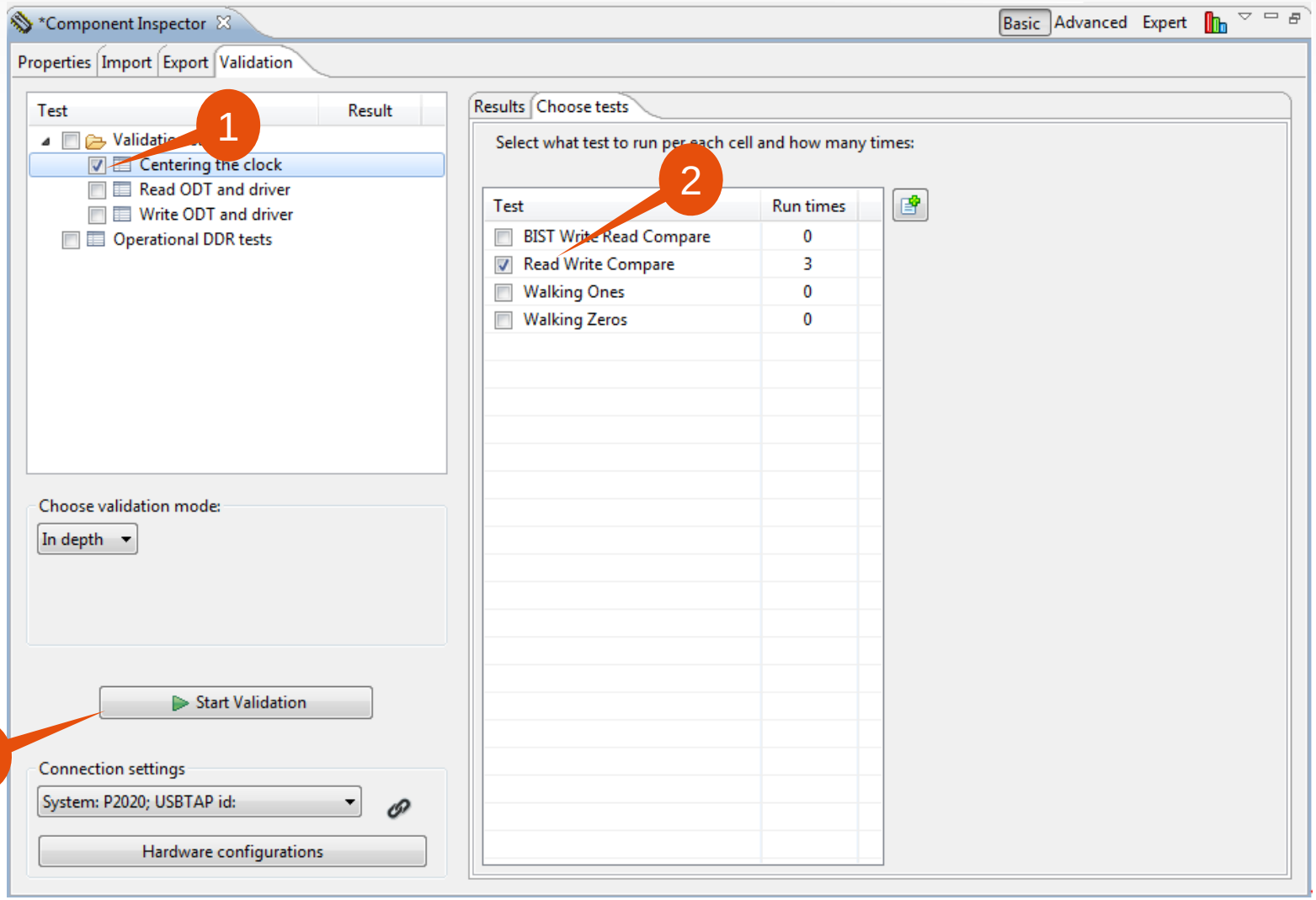


DDRv Basic Connection Test

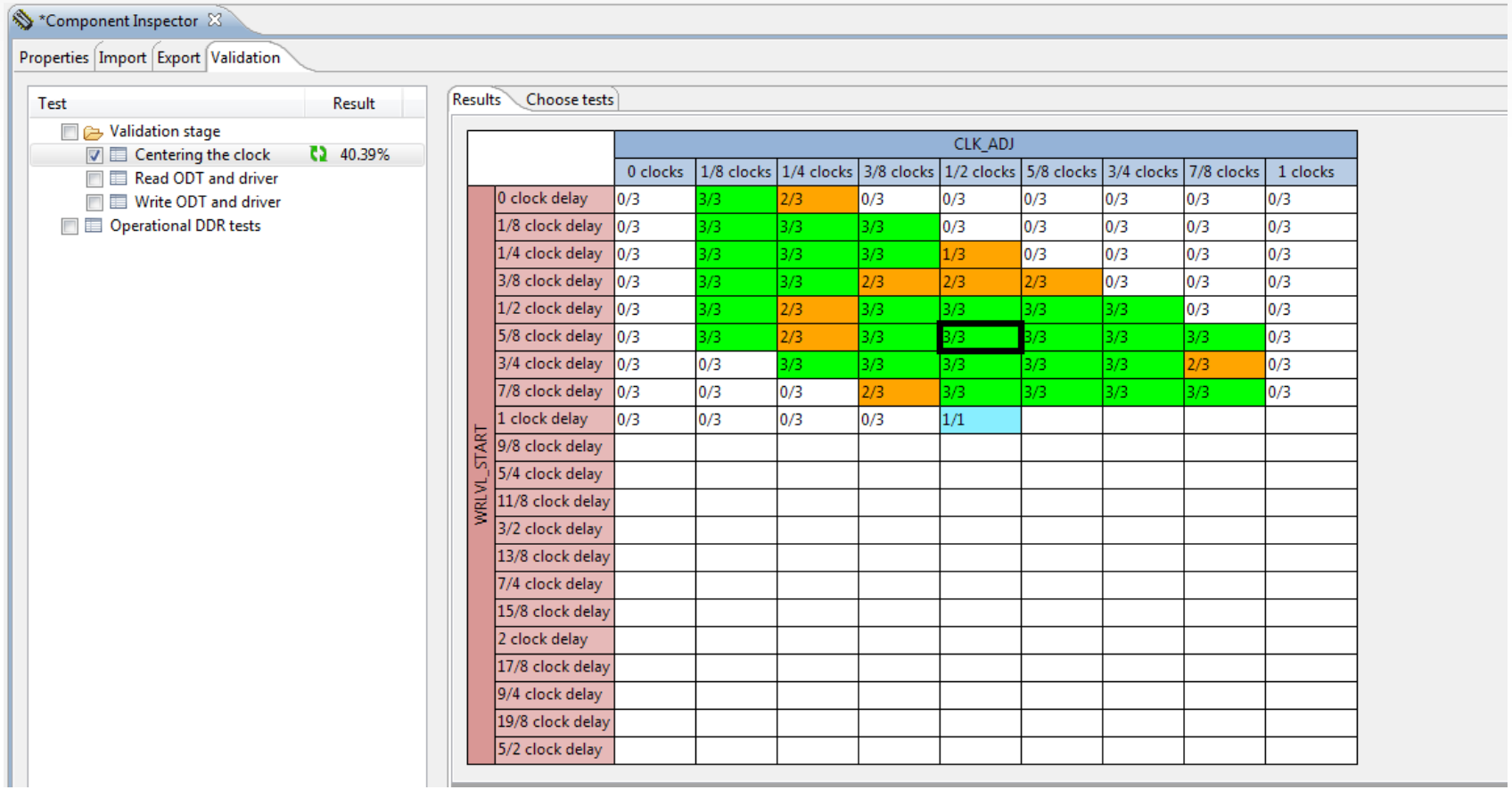


- Run basic test to confirm target connection

Configure DDR scenarios and tests

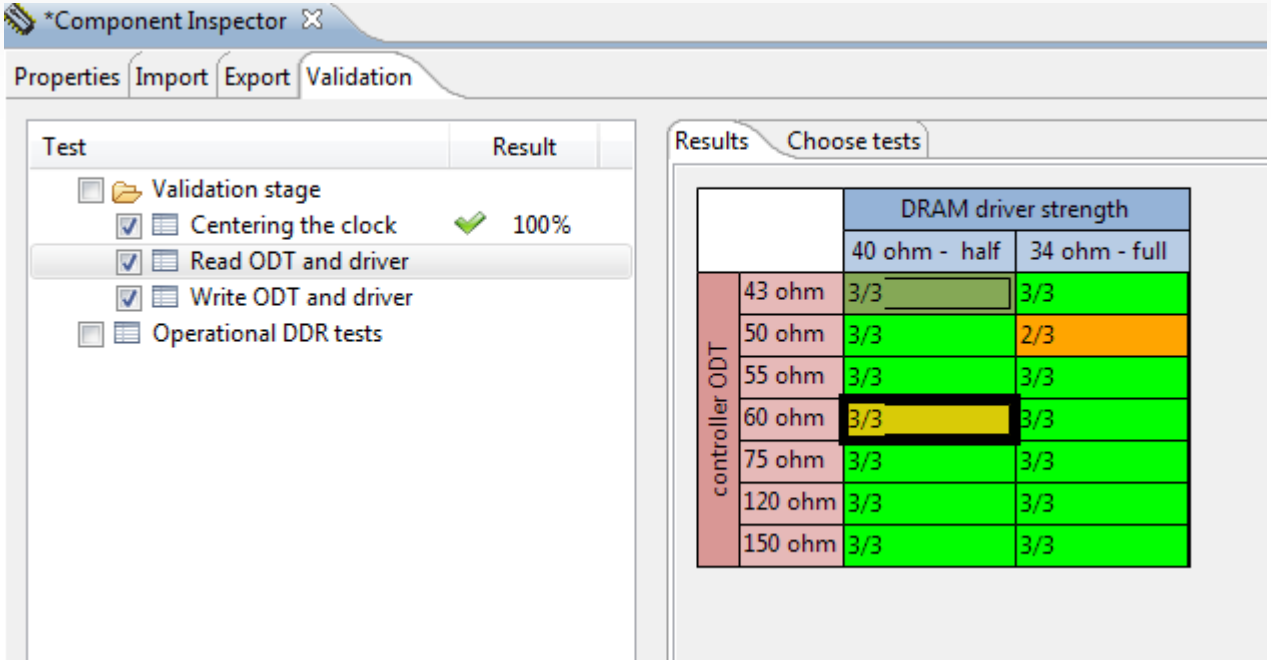


Centering of the clock results



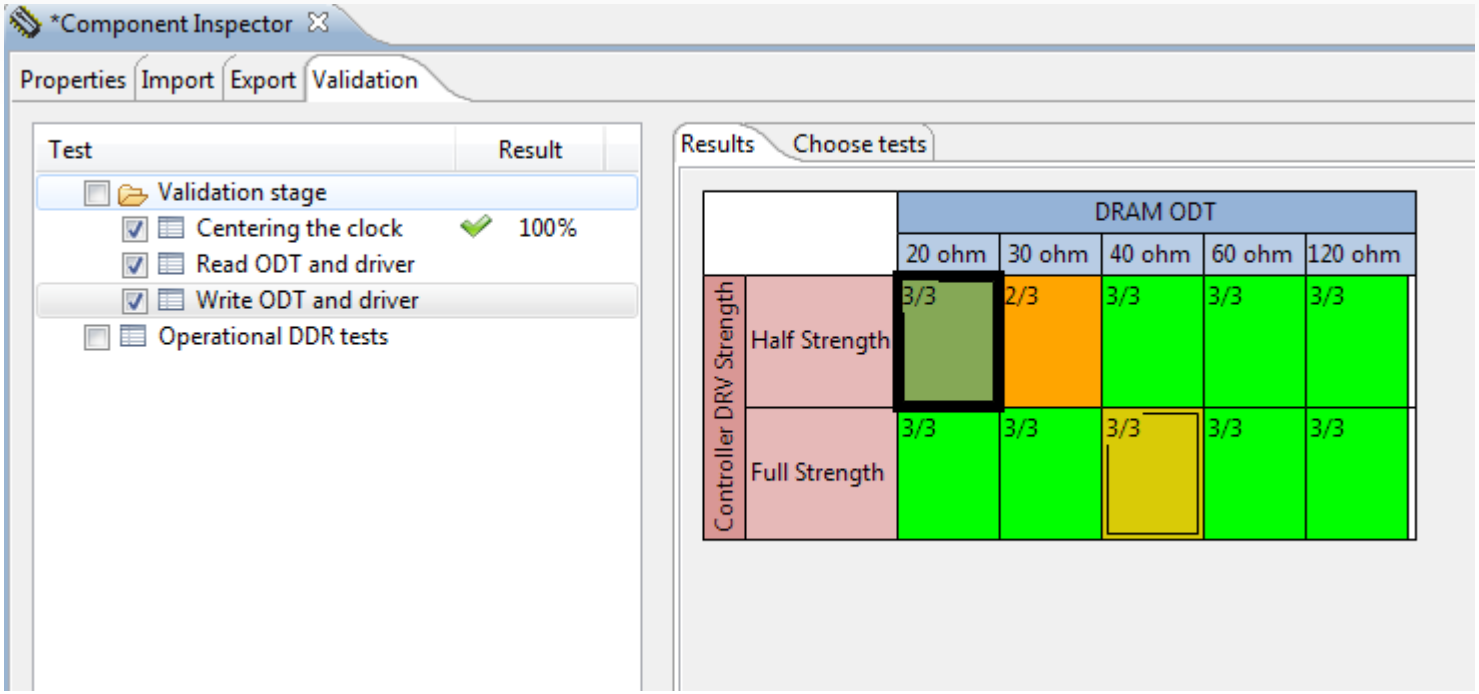
- Click “cell” to choose Write level start and CLK_ADJ values.

DDR read ODT and driver strength – test results



- Click “cell” to choose optimized ODT value.

DDR write ODT and drive strength – test results



- Click “cell” to choose optimized ODT value.

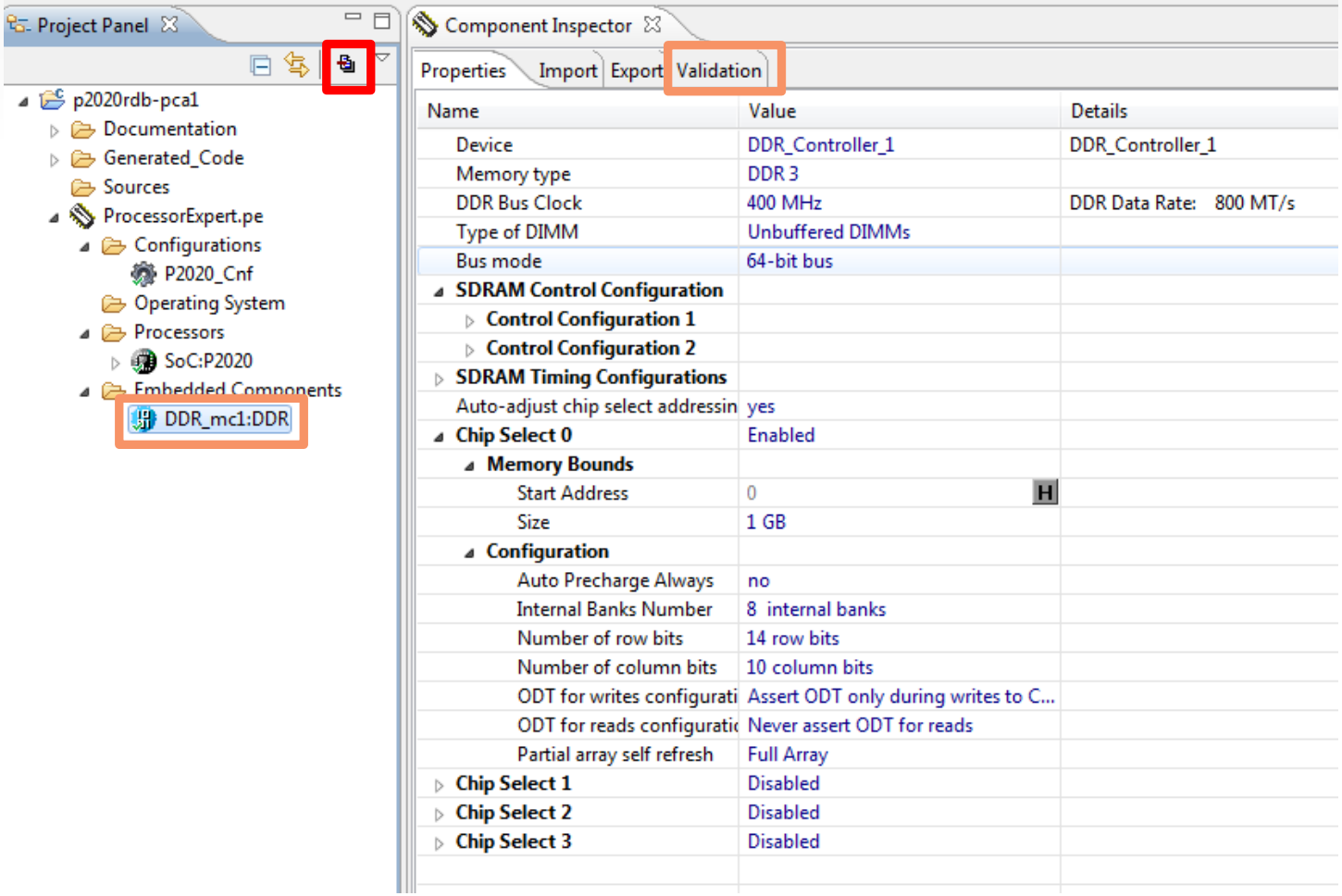
Centering of the clock - after ODT optimization

Results | Choose tests

WRLVL_START	CLK_ADJ								
	0 clocks	1/8 clocks	1/4 clocks	3/8 clocks	1/2 clocks	5/8 clocks	3/4 clocks	7/8 clocks	1 clocks
0 clock delay	0/3	3/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3
1/8 clock delay	0/3	3/3	3/3	3/3	0/3	0/3	0/3	0/3	0/3
1/4 clock delay	0/3	3/3	3/3	3/3	0/3	0/3	0/3	0/3	0/3
3/8 clock delay	0/3	3/3	3/3	3/3	3/3	3/3	0/3	0/3	0/3
1/2 clock delay	0/3	3/3	3/3	3/3	3/3	3/3	0/3	0/3	0/3
5/8 clock delay	0/3	3/3	3/3	3/3	3/3	3/3	3/3	3/3	0/3
3/4 clock delay	0/3	0/3	3/3	3/3	3/3	3/3	3/3	3/3	0/3
7/8 clock delay	0/3	0/3	0/3	3/3	3/3	3/3	2/3	3/3	0/3
1 clock delay	0/3	0/3	0/3	0/3	3/3	3/3	3/3	3/3	0/3
9/8 clock delay	0/3	0/3	0/3	0/3	0/3	3/3	3/3	3/3	0/3
5/4 clock delay	0/3	0/3	0/3	0/3	0/3	0/3	2/3	3/3	0/3
11/8 clock delay	0/3	0/3	0/3	0/3	0/3	0/3	0/3	3/3	0/3
3/2 clock delay	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3
13/8 clock delay	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3
7/4 clock delay	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3
15/8 clock delay	0/3	3/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3
2 clock delay	0/3	3/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3
17/8 clock delay	0/3	3/3	3/3	3/3	0/3	0/3	0/3	0/3	0/3
9/4 clock delay	0/3	3/3	3/3	3/3	0/3	0/3	0/3	0/3	0/3
19/8 clock delay	0/3	3/3	3/3	3/3	3/3	3/3	0/3	0/3	0/3
5/2 clock delay	0/3	3/3	3/3	3/3	3/3	3/3	0/3	0/3	0/3

- Centering of clock scenario was re-run after finding the right ODT values

Generate optimized DDR configuration



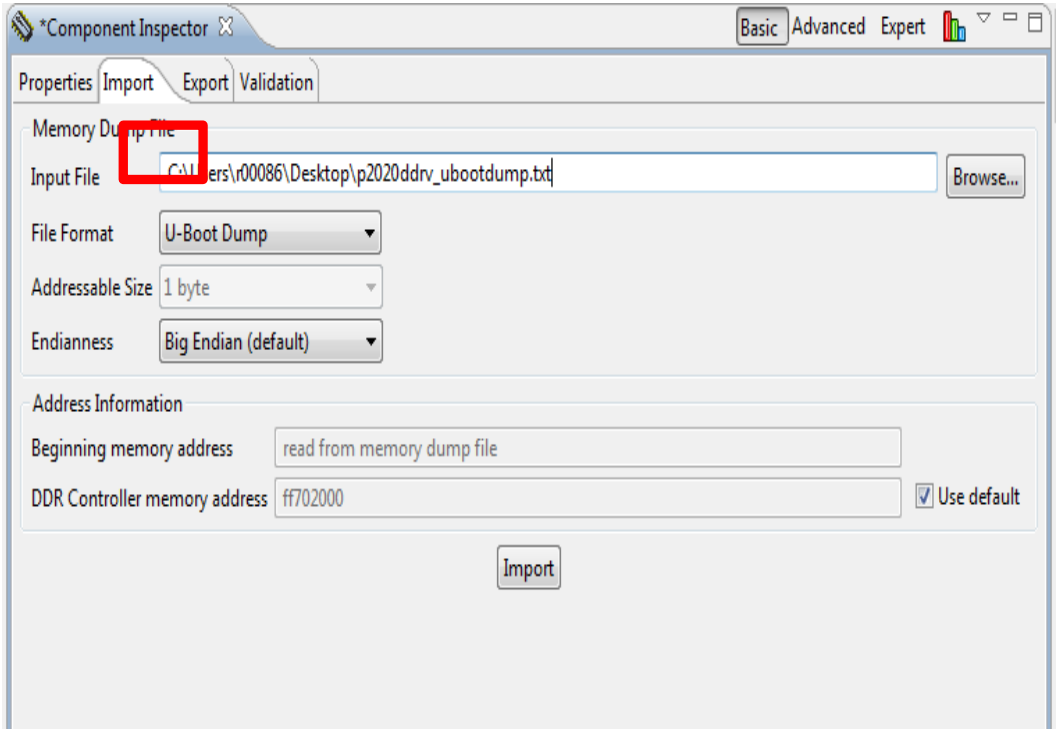
Pricing $995

License file:

<QCS Install directory>/eclipse/Optimization/license.dat

P2020RDB-PCA: Import DDR configuration from existing system running uboot

- At uboot prompt
- => md ffe02000
  - ffe02000: 0000003f 00000000 00000000 00000000 ...?.....
  - ffe02080: 80014202 00000000 00000000 00000000 ..B.....
  - ffe02100: 00030000 00110104 6f6b8846 0fa8c8cc .....ok.F....
  - ffe02110: c7000008 24401040 00441421 00000000 ....$@.@.D.!....
  - ffe02120: 00000000 0c300100 deadbeef 00000000 .....0.....
  - ffe02130: 03000000 00000000 00000000 00000000 .....
  - ffe02160: 00220001 02401400 00000000 00000000 ."...@.....
  - ffe02170: 89080600 8675f608 00000000 00000000 .....u.....
- => md ffe02b00
  - ffe02b00: 00000000 00000000 00000000 00000000 .....
  - ffe02b10: 00000000 00000000 00000000 00000000 .....
  - ffe02b20: 5dc07777 77000000 00000000 00000000].www.....
- Save content to a file.



Processor Expert for QorIQ … For More Info

- Freescale's Processor Expert landing page
  - http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=PROCESSOR-EXPERT&tid=PEH
  - http://www.processorexpert.com/
- QorIQ Configuration Suite
  - http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=PE_QORIQ_SUITE&tid=PEH
- QorIQ Optimization Suite
  - http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=PE_QORIQ_OPTI_SUITE&tid=PEH
- Freescale Component Store – purchasing embedded software
  - http://www.freescale.com/webapp/sps/site/homepage.jsp?code=BEAN_STORE_MAIN&tid=SWnT

Pricing & Availability

- Part numbers : CWA-QIQ-OPTP-FL (floating license) & CWA-QIQ-OPTP-NL (node locked)
- Price : $999 Annual Subscription
- License Duration : 1 year
- Support & Maintenance : Included
- Availability
  - Scenarios Tool – Now
  - DDRv – Now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