Optimally Configuring DDR for Custom Boards

AMF-NET-T1021

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Session Outline

AMF-NET-T1021

Optimally Configuring DDR for Custom Boards

- An overview of QorIQ processor's memory controller capabilities, configuration and testing for your board. Learn how to use QCS Configuration and DDRv tools to generate a customized configuration, run memory tests, and validate functionality on your board in a matter of hours. Will include a demo of these tools running memory tests on a QorIQ processor board.

Agenda

- Introduction and Industry Trends
- Memory Organization and Operation
- Features and Capabilities

- Overview and Demo of DDR Tools
  - DDR configuration using QorIQ Configuration Suite (QCS)
  - DDR validation using QorIQ Optimization Suite (QOS) DDRv plug-in to QCS

DDR SDRAM Memories

Introduction and Industry Trends

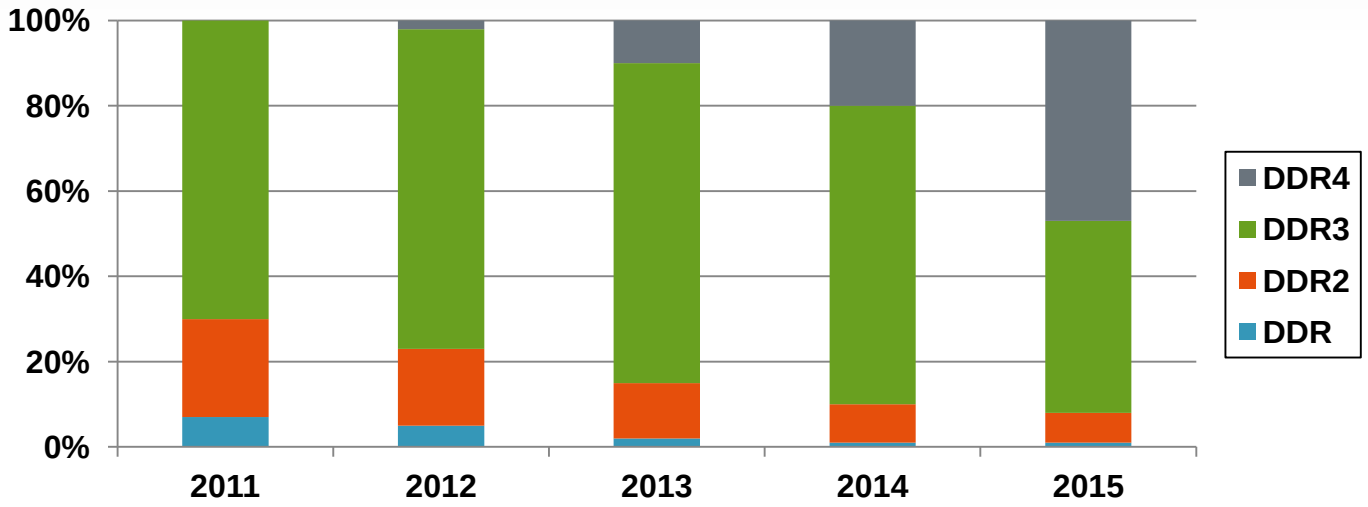
Introduction

- The current industry mainstream DRAM product is DDR3/3L. It is expected for this trend to continue till 2015 when the pricing cross-over is expected to occur.
- Almost all Freescale networking devices offer and support DDR3/3L.
- DDR4 has been introduced and DRAM vendors are expected to ramp production in 2014.
- The first Freescale device with DDR3L/DDR4 support is expected by end of 2013 (QorIQ T1040 family) followed by LS102x family products shortly after in Q1 2014.

DDR3 and DDR4 – Major Vendors

- Supported by all major memory vendors

DRAM Migration Roadmap



	2011	2012	2013	2014	2015
DDR	7%	5%	2%	1%	1%
DDR2	23%	18%	13%	9%	7%
DDR3	70%	75%	75%	70%	45%
DDR4	0%	2%	10%	20%	47%

DDR3L vs DDR4

DRAM differences

DDR SDRAM Highlights and Comparison

Feature/Category	DDR3L	DDR4
Package	BGA only	BGA only
Densities	512Mb -8Gb	2Gb -16Gb
Voltage	1.35V Core 1.35V I/O	1.2V Core 1.2V I/O
Data I/O CMD, ADDR I/O	Center Tab Termination (CTT) CTT	Pseudo Open Drain (POD) CTT
Internal Memory Banks	8	16 for x4/x8 8 for x16
Data Rate	800–1866 Mbps	1600–3200 Mbps
VREF	VREFCA & VREFDQ external	VREFCA external VREFDQ internal
Data Strobes/Prefetch/Burst Length/Burst Type	Differential/8-bits/BC4, BL8/ Fixed, OTF	Same as DDR3L
Additive/read/write Latency	0, CL-1, CL-2/ AL+CL/ AL +CWL	Same as DDR3L

DDR SDRAM Highlights and Comparison (continued)

Feature/Category	DDR3L	DDR4
CRC Data Bus	No	Yes
Boundary Scan/Connectivity test (TEN pin)	No	Yes
Bank Grouping	No	Yes
Data Bus Inversion (DBI_n pin)	No	Yes
Write Leveling / ZQ	Yes	Yes
ACT_n new pin & command	No	Yes
Low power Auto self-refresh	No	Yes

DDR3/DDR3L/DDR4 Power Saving

- DDR3 DRAM provides 25% power savings over DDR2
- DDR3L DRAM provides 20% to 27% power saving over DDR3
- DDR4 DRAM provides 37% power saving over DDR3L

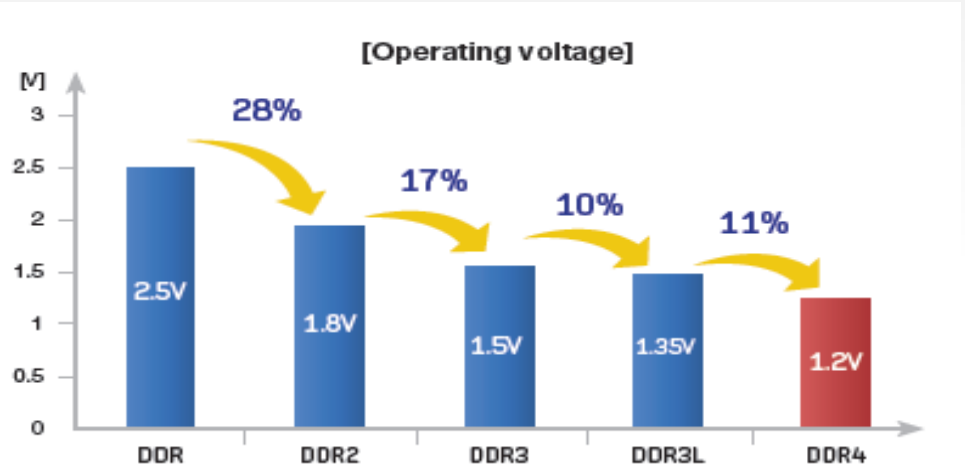


Figure 4. Reduced operating voltage requirements of DDR4 compared to DDR3L

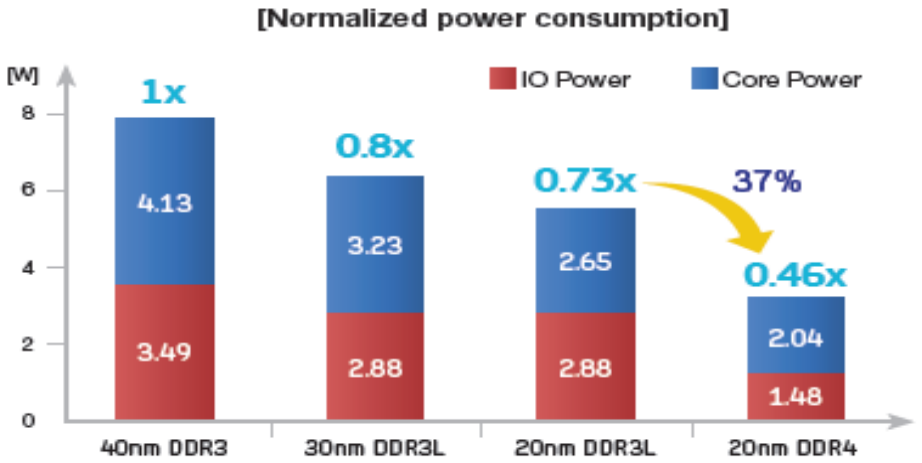


Figure 5. Reduced normalized power consumption requirements of DDR4 compared to DDR3L

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DDR3L vs. DDR4 DRAM pinouts

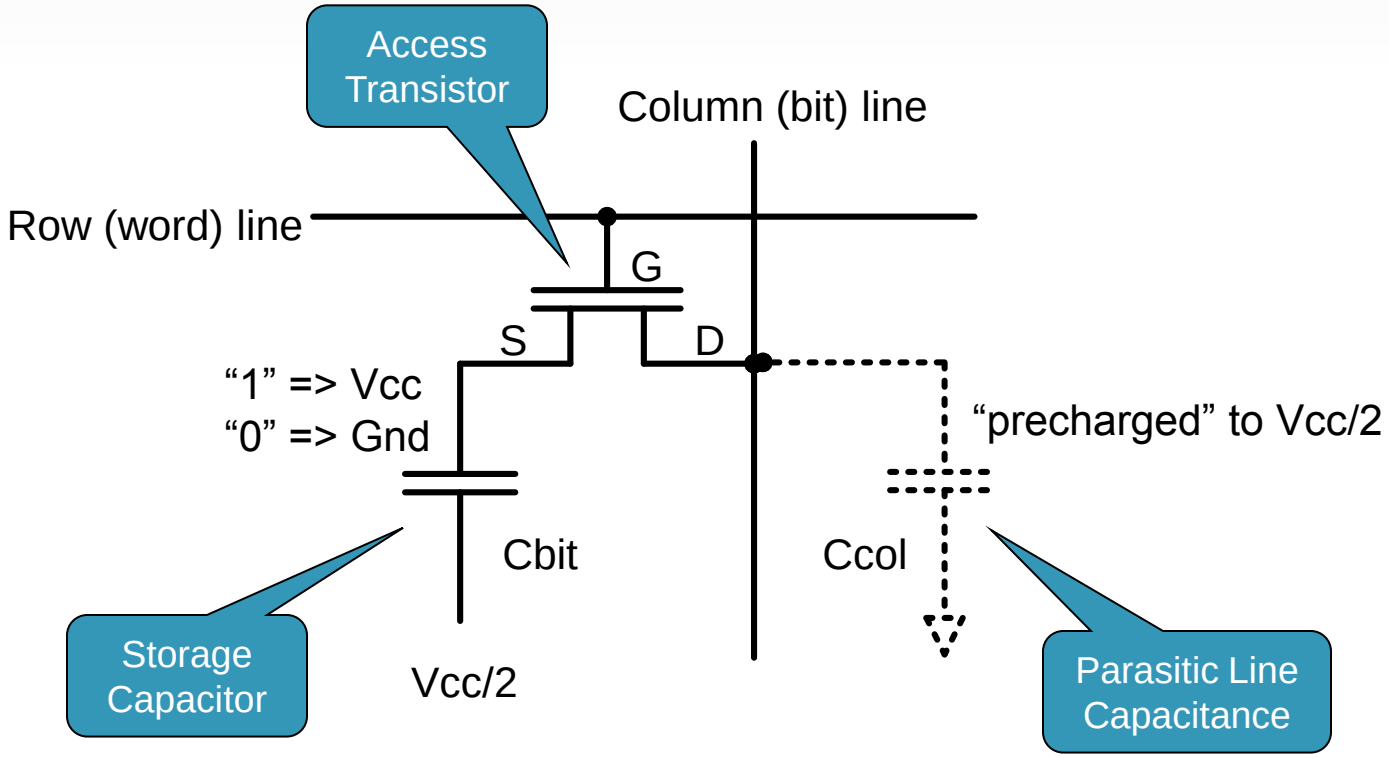
- DDR4 Pins added
  - VDDQ (2) : 1.2V pins to DRAM
  - VPP : 2.5V external voltage source for DRAM internal word line driver
  - Bank Group (2): pins to identify the bank groups
  - DBI_n: Data Bus Inversion
  - ACT_n: Active command
  - PAR: Parity error signal for address bus
  - Alert_n: Both, Parity error on C\A and CRC error on data bus
  - TEN: Connectivity test mode

- DDR3 Pins eliminated
  - VREFDQ
  - Bank Address (1): one less BA pin
  - VDD (1), VSS (3), VSSQ (1)

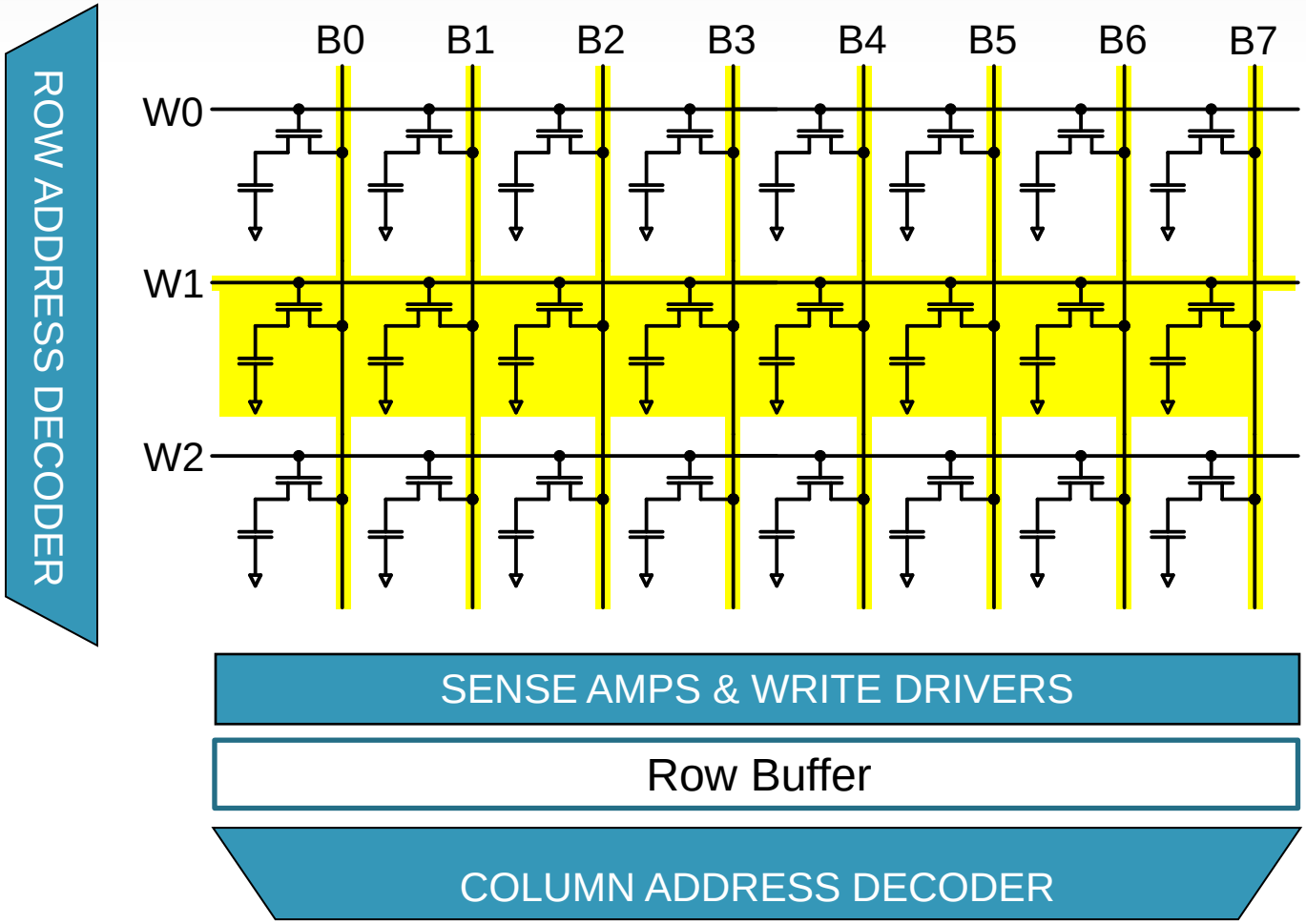
Basic DDR SDRAM Structure

Memory Organization and Operation

Single Transistor Memory Cell

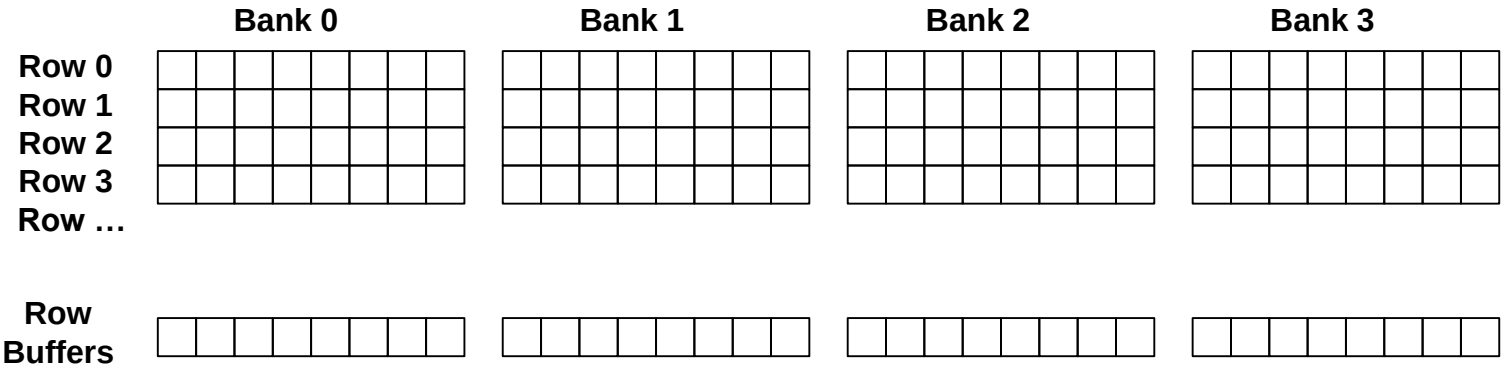


Memory Arrays



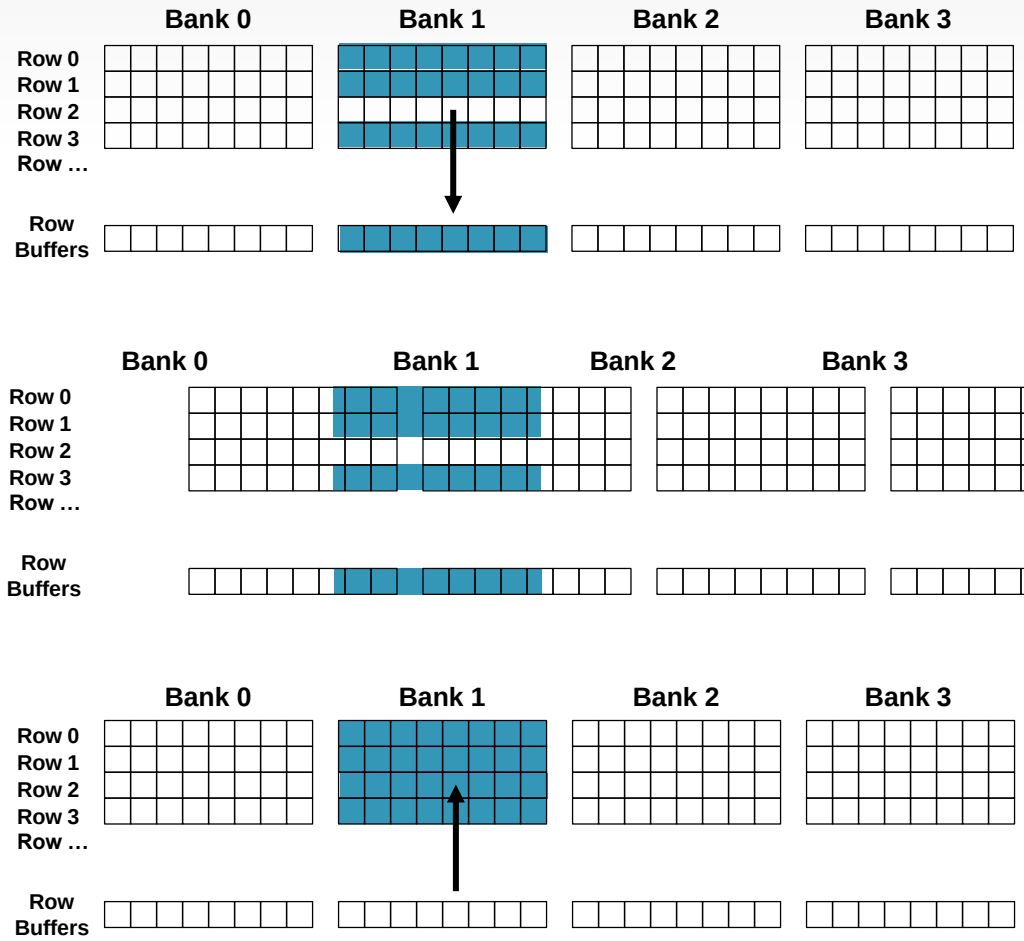
Internal Memory Banks

- Multiple arrays organized into banks
- Multiple banks per memory device
  - DDR3 – 8 banks, and 3 bank address (BA) bits
  - DDR4 -16 banks with 4 banks in each of 4 sub bank groups
  - Can have one active row in each bank at any given time
- Concurrency
  - Can be opening or closing a row in one bank while accessing another bank

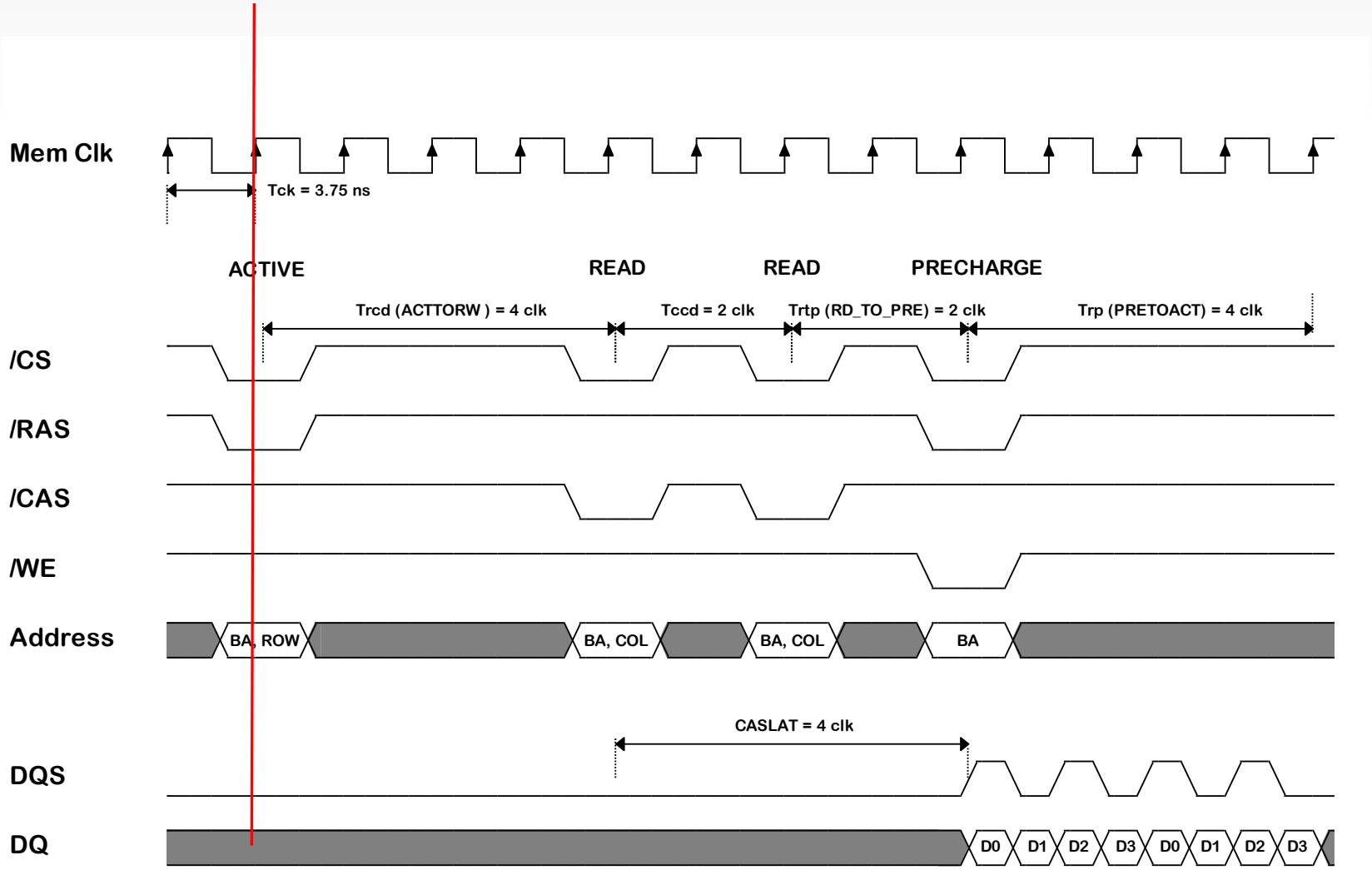


Memory Access

- A requested row is **ACTIVATED** and made accessible through the bank's row buffer
- **READ** and/or **WRITE** are issued to the active row
- The row is **PRECHARGED** and is no longer accessible through the bank's row buffer

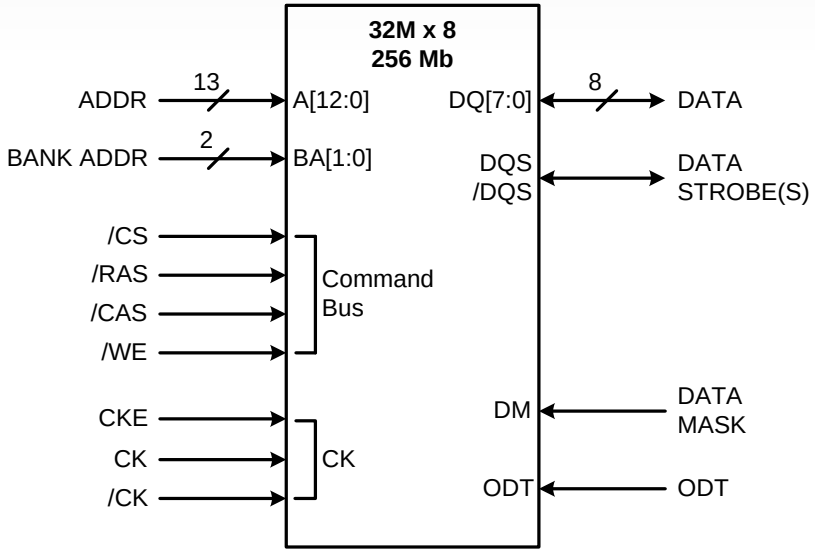


DDR2-533 Read Timing Example



Example – DDR2/3 SDRAM

- Micron MT47H32M8
- 32M x 8 (8M x 8 x 4 banks)
- 256 Mb total
- 13-bit row address
  - 8K rows
- 10-bit column address
  - 1K bits/row (8K total when you take into account the x8 width)
- 2-bit bank address
- Data bus: DQ, DQS, /DQS, DM
- ADD bus: A, BA, /CS, /RAS, /CAS, /WE, ODT, CKE, CK, /CK

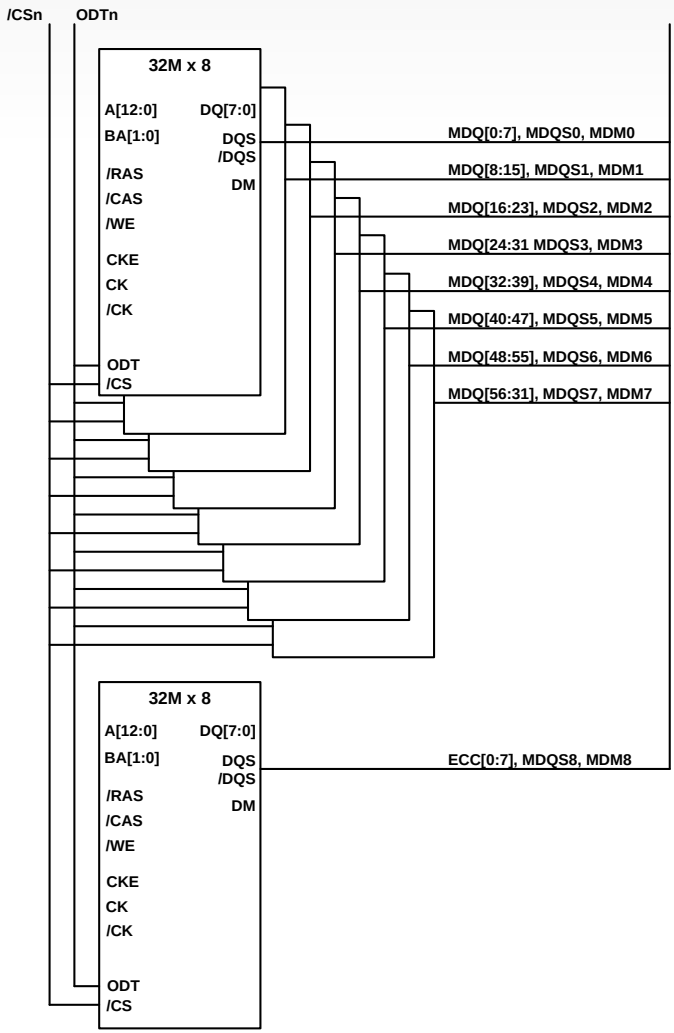


Example – DDR2/3 DIMM

- Micron MT9HTF3272A
- 9 each 32M x 8 memory devices
- 32M x 72 overall
- 256 MB total, single “rank”
- 9 “byte lanes”

Two Signal Bus

- 1- Address, command, control, and clock signals are shared among all 9 DRAM devices
- 2- Data, strobe, data mask not shared



DRAM Module Type

UDIMM: Unbuffered Desktop standard

SODIMM: Notebook standard

MiniDIMM:
Computing and Networking

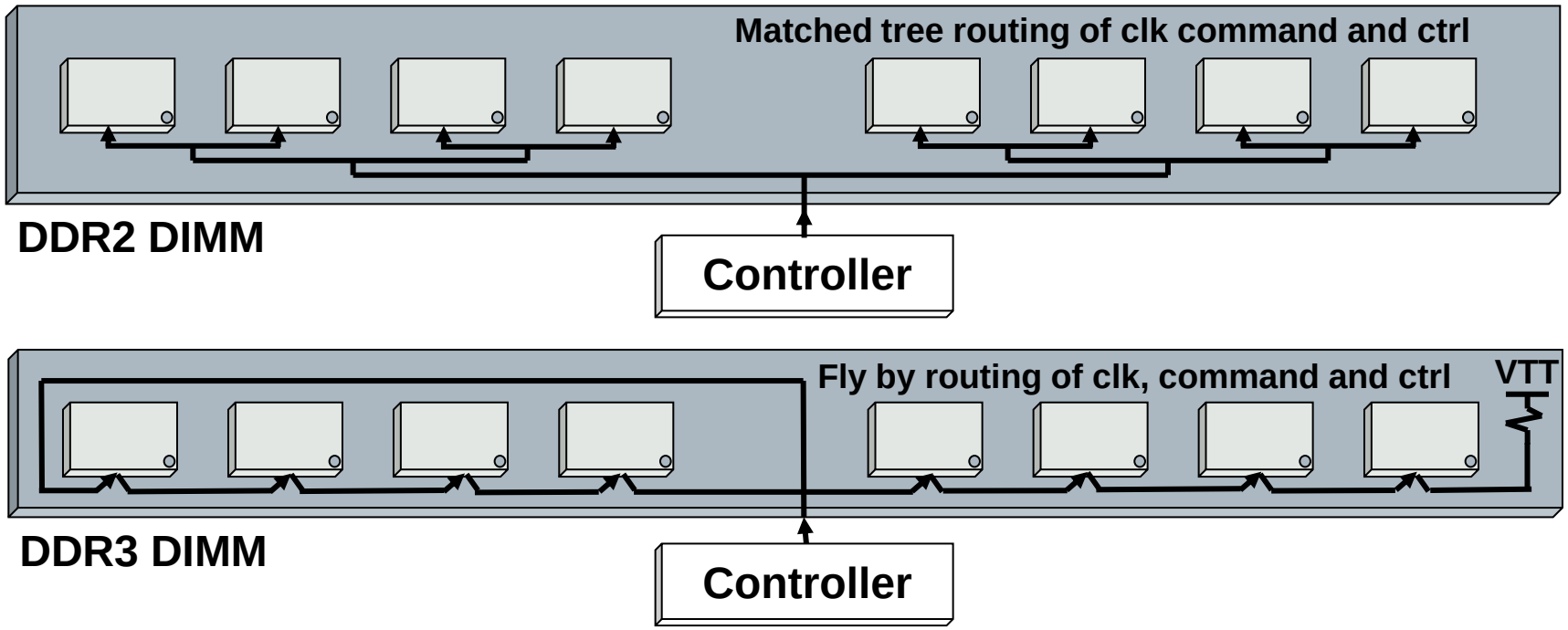
VLP MiniDIMM:
Computing and Networking

RDIMM: Registered Server standard

VLP RDIMM: Very Low Profile
Computing and Networking

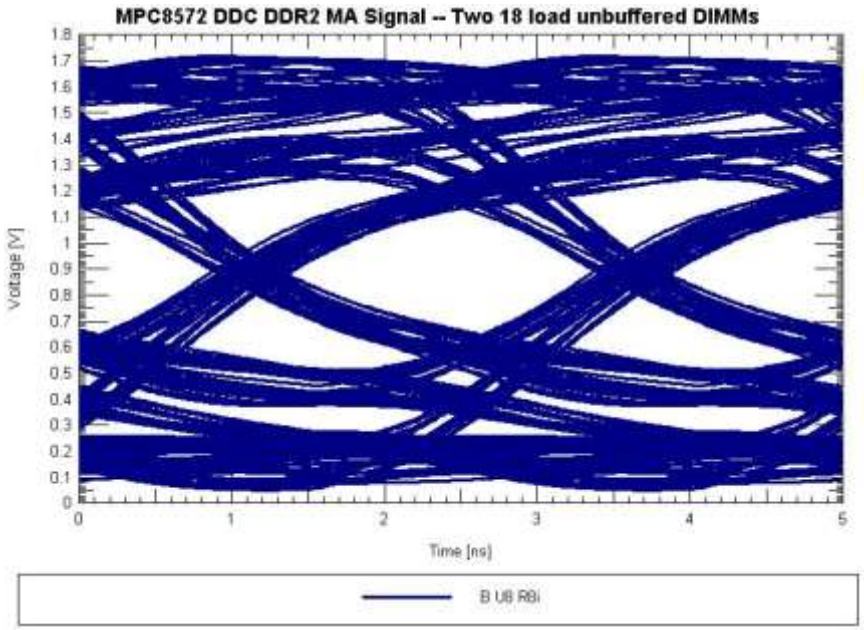
Fly-By Routing Topology

- **Introduction of "fly-by" architecture**
  - Address, command, control & clocks
  - Data bus (not illustrated below) remains unchanged, ie, direct 1-to-1 connection between the Controller bus lanes and the individual DDR devices.
  - Improved signal integrity…enabling higher speeds
  - On module termination

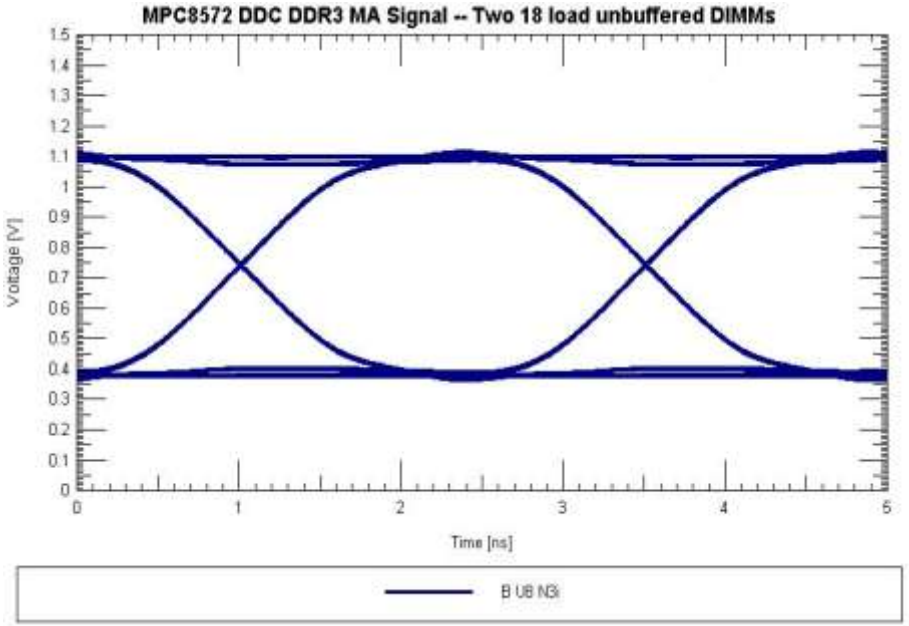


Fly-By Routing Improved SI

DDR2 Matched Tree Routing

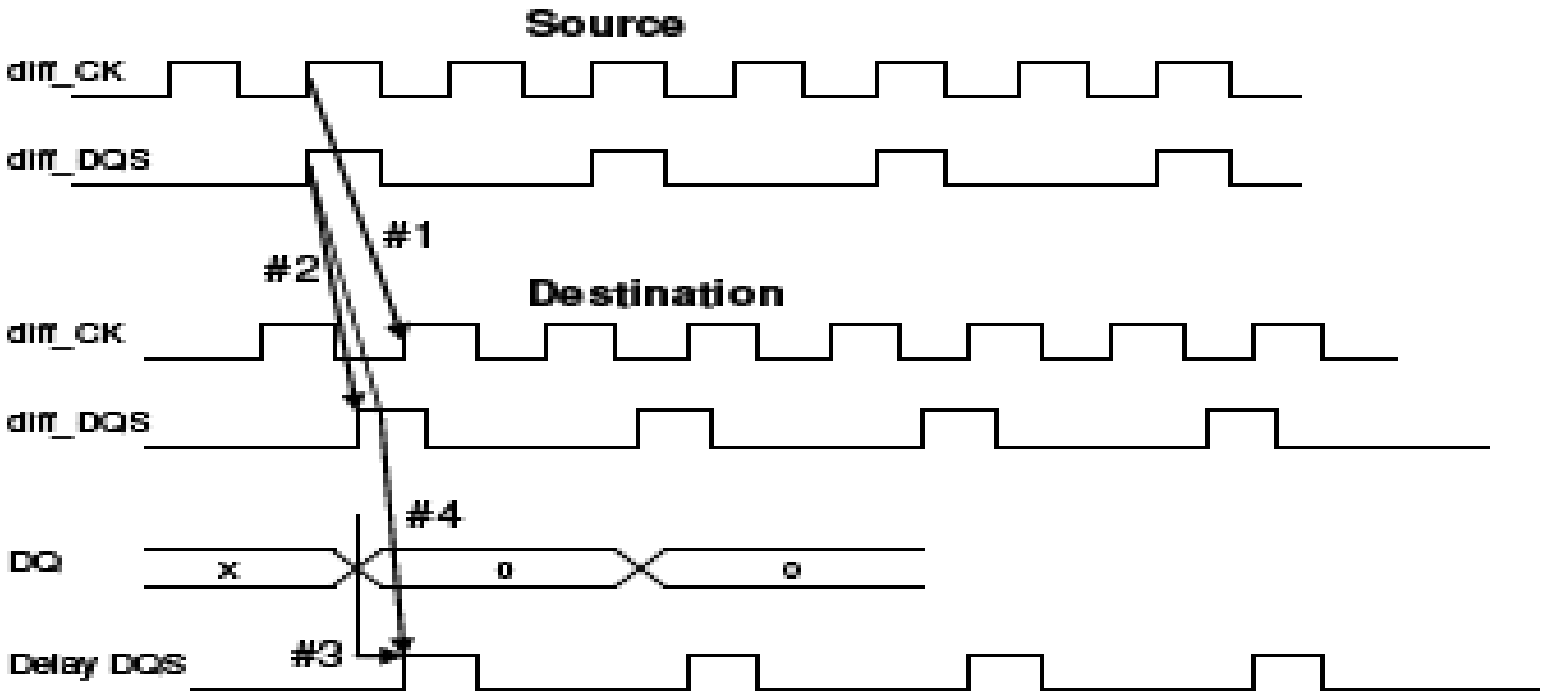


DDR3 Fly By Routing

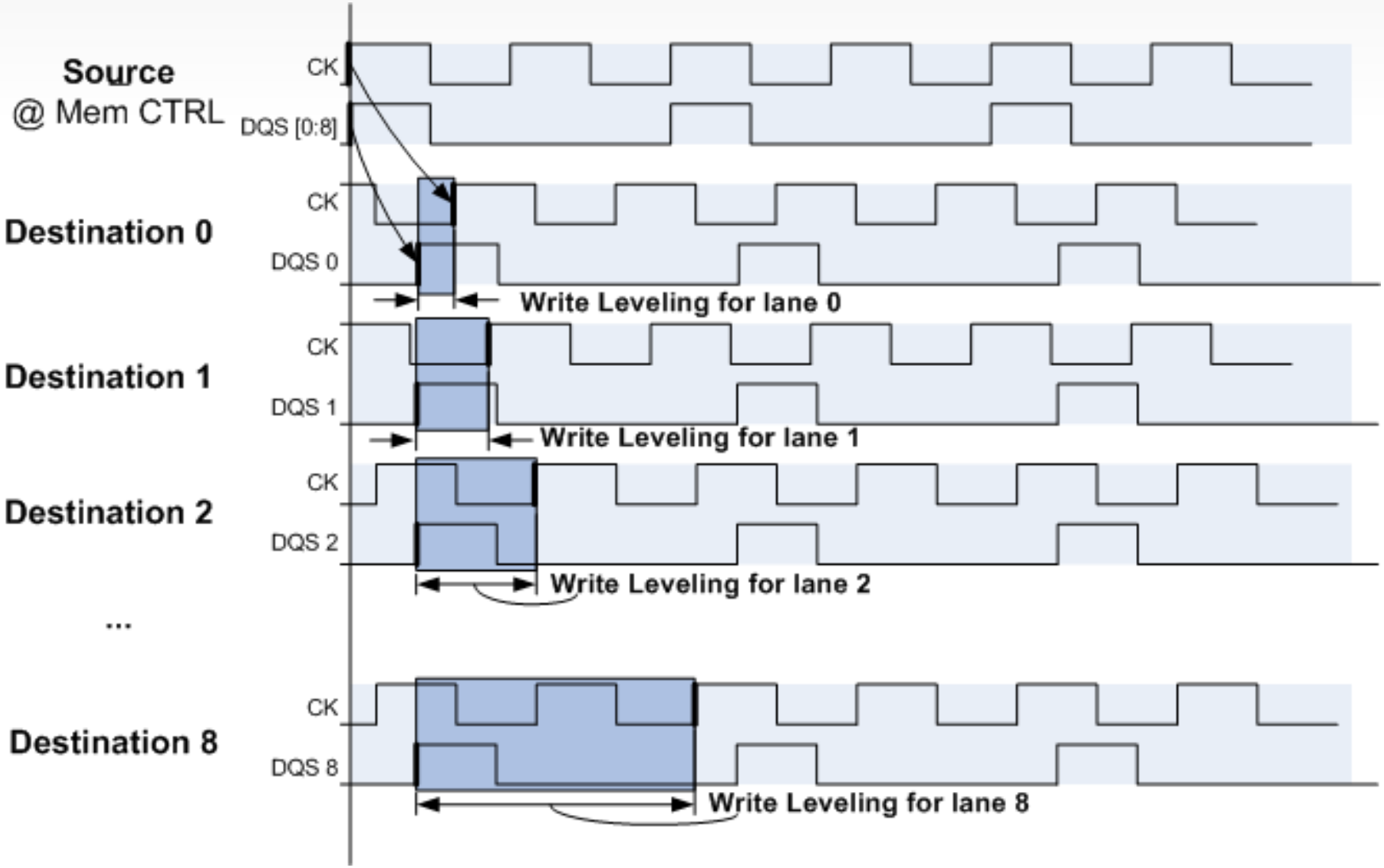


What Is Write Leveling?

- During a write cycle, the skew between the clock and strobes is increased due to the fly-by topology. The write leveling will delay the strobe (and the corresponding data lanes) for each byte lane to reduce/compensate for this delay



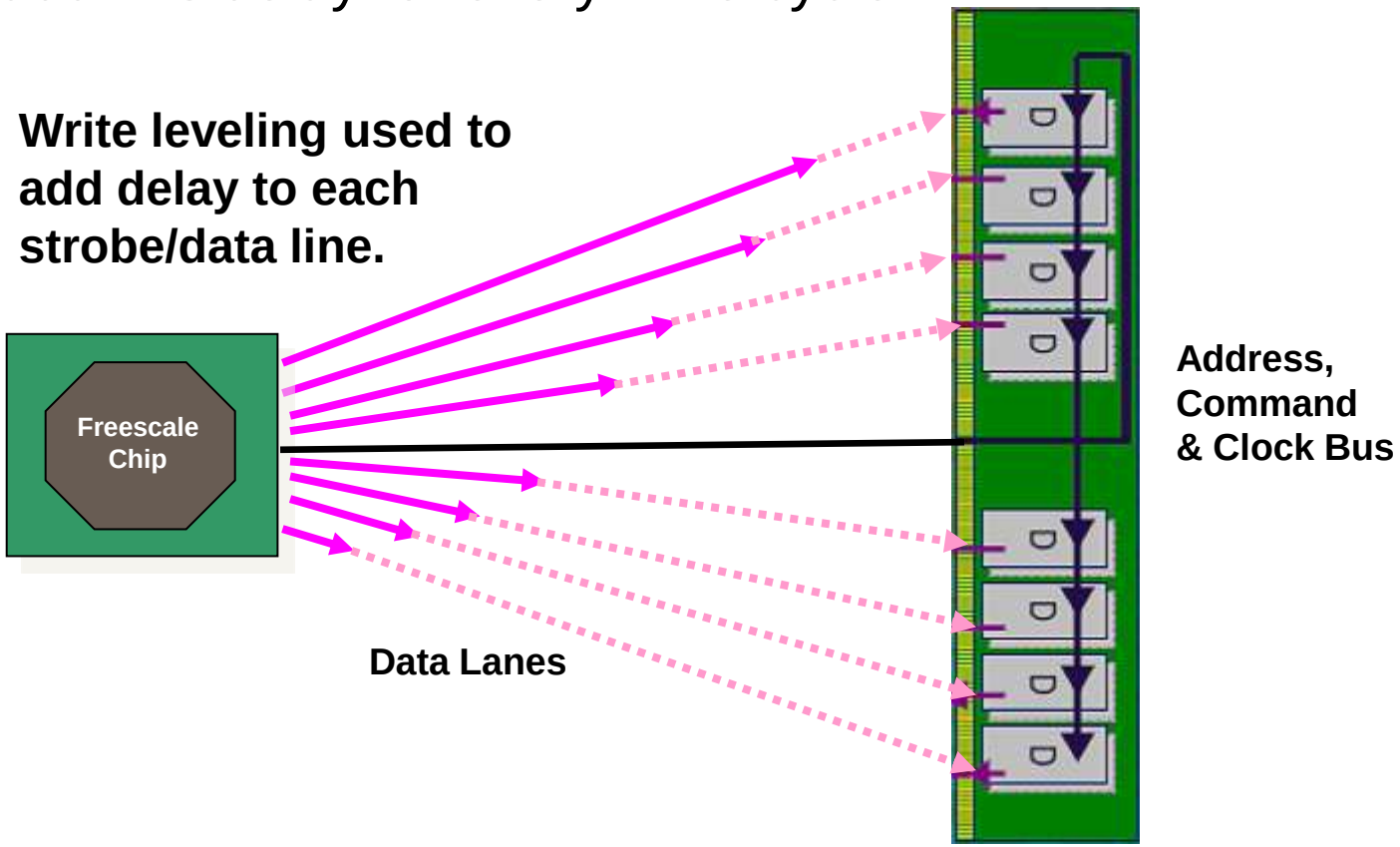
What Is Write Leveling?



Write Adjustment

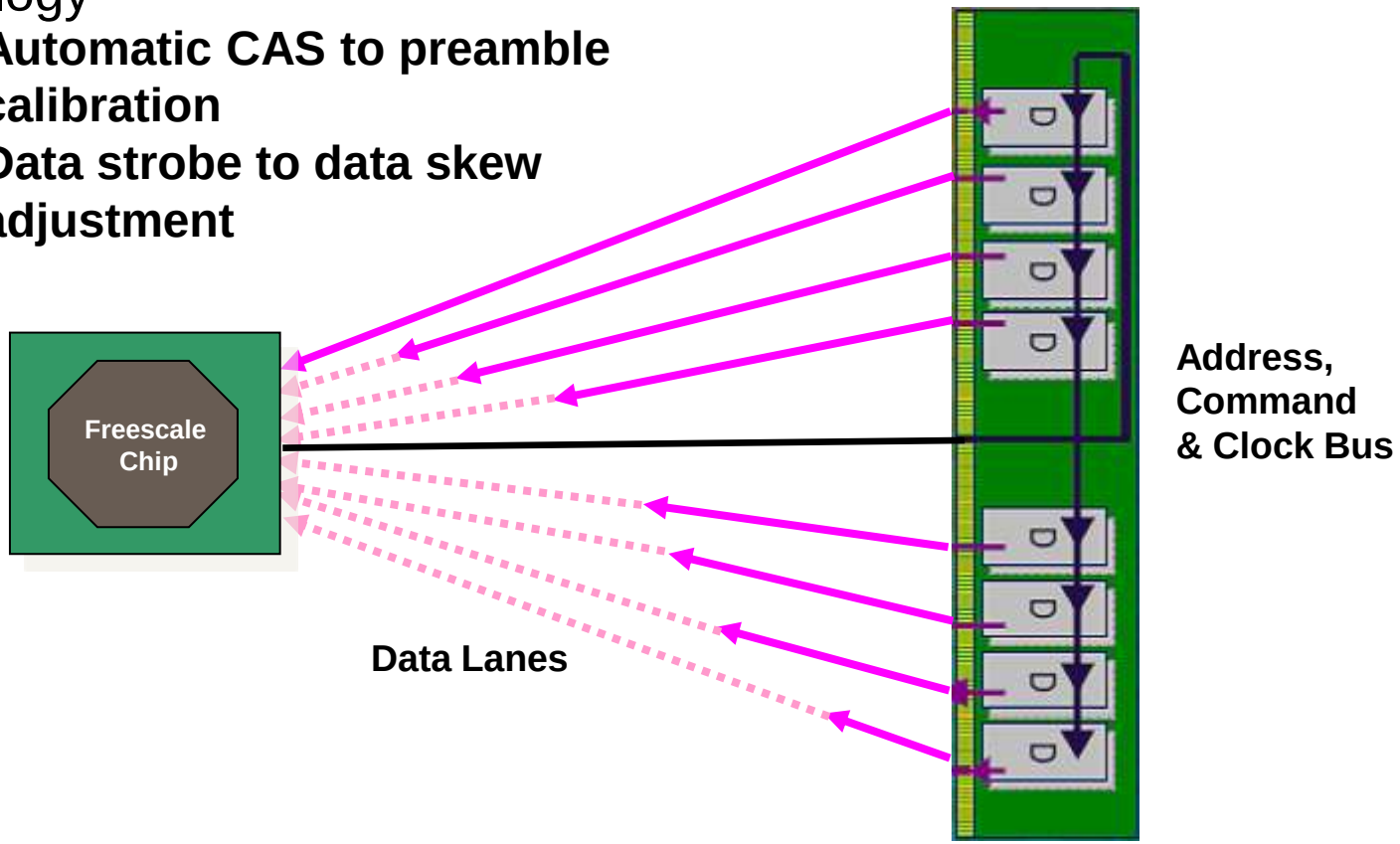
- Write leveling sequence during the initialization process will determine the appropriate delays to each strobe/data byte lane and add this delay for every write cycle

  - **Write leveling used to add delay to each strobe/data line.**



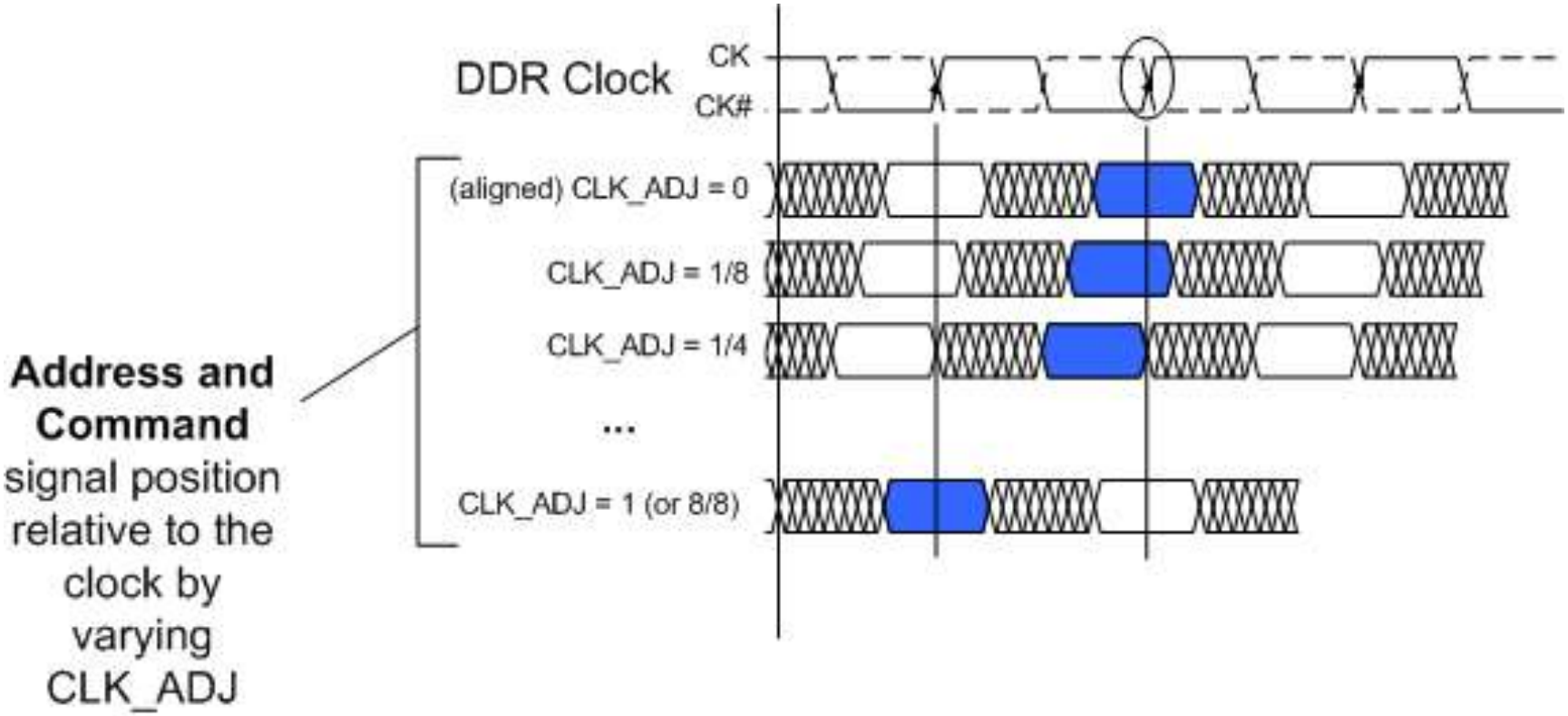
Read Adjustment

- Instead of JEDEC's MPR method, Freescale controllers use a proprietary method of read adjust method. Auto CPO will provide the expected arrival time of preamble for each strobe line of each byte lane during the read cycle to adjust for the delays cased by the fly-by topology
  - **Automatic CAS to preamble calibration**
  - **Data strobe to data skew adjustment**

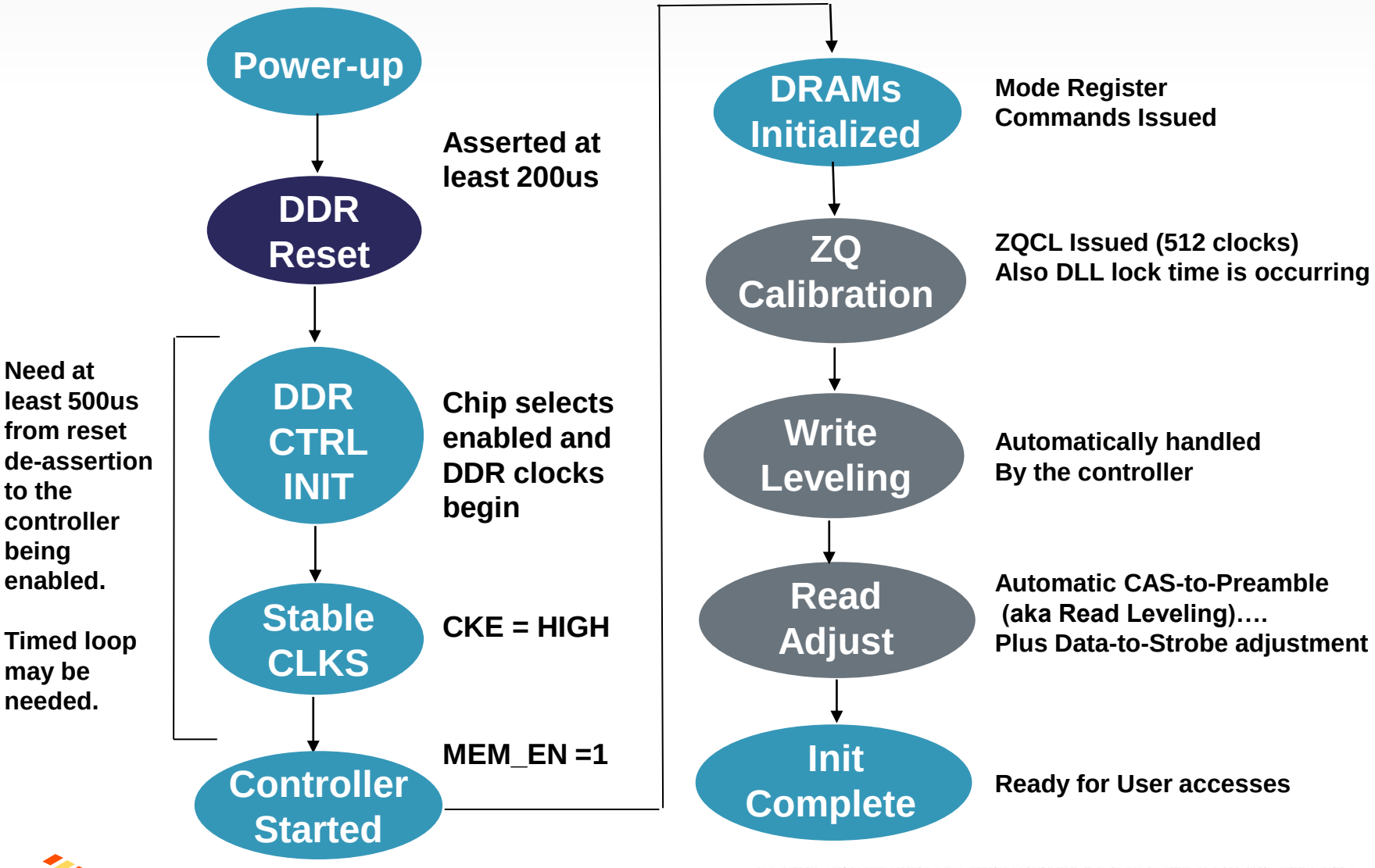


CLK_ADJ - Clock Adjust

- CLK_ADJ defines the timing of the address and command signals relative to the DDR clock.



DDR3 Initialization Flow



Register Configuration

- **Two general type of registers to be configured in the memory controller**
- **First register type is set to the DRAM related parameter values that are provided via SPD or DRAM datasheet**
- **Second register type is the non-SPD values that are set based on customer's application. For example:**
  - On-die-termination (ODT) settings for DRAM and controller
  - Driver impedance setting for DRAM and controller
  - Clock adjust, write data delay, Cast to preamble override (CPO)
  - 2T or 3T timing
  - Burst type selection (fixed or on-the-fly burst chop mode)
  - Write-leveling start value (WRLVL_START)
- **Freescale's Processor Expert QorIQ Configuration Suite includes a DDR configuration tool for many devices. For other devices, Freescale support resources can help generate or analyze DDR settings.**

QorIQ Layerscape Family DDR Controllers

Features and Capabilities DDR3L and DDR4

Common DDR3L & DDR4 Controller Features

- Supports most JEDEC standard x8, x16 DDR3L & DDR4 devices
- Memory device densities from 1Gb – through 8Gb
- Data rates up to: 1600 MT/s DDR3L and DDR4
- Devices with 12-16 row address bits, 8-11 column address bits, 2-3 logical bank address bits
- Data mask signals for sub-doubleword writes
- Up to four physical banks (ranks / chip selects)
- Physical bank (rank) sizes up to 8GB, total memory up to 32GB per controller
- Physical bank interleaving between 2 or 4 chip selects
- Memory controller interleaving when more than 2 controllers are available
- Un-buffered or registered DIMMs

Common DDR3L /4 Controller Features (continued)

- Up to 32 open pages (DDR3L only), 64 open pages for DDR4
  - Open row table
  - Amount of time rows stay open is programmable
- Auto-precharge, globally or by chip select
- Self-refresh
- Up to 8 posted refreshes
- Automatic or software-controlled memory device initialization
- ECC: 1-bit error correction, 2-bit error detection, detection of all errors within a nibble
- ECC error injection
- Read-modify-write for sub-doubleword writes when using ECC
- Automatic data initialization for ECC
- Dynamic power management

Common DDR3L /4 Controller Features (continued)

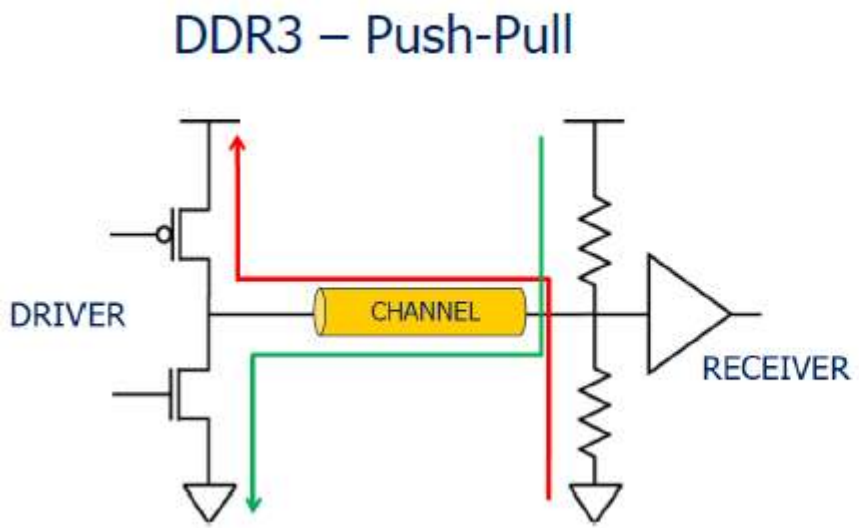
- Partial array self refresh
- Address and command parity for Registered DIMM (DDR3 only)
- Independent driver impedance setting for data, address/command, and clock
- Synchronous and Asynchronous clock-in option
- Write-leveling
- Automatic CPO
- Asynchronous RESET
- Automatic ZQ calibration
- Mirrored DIMM supported

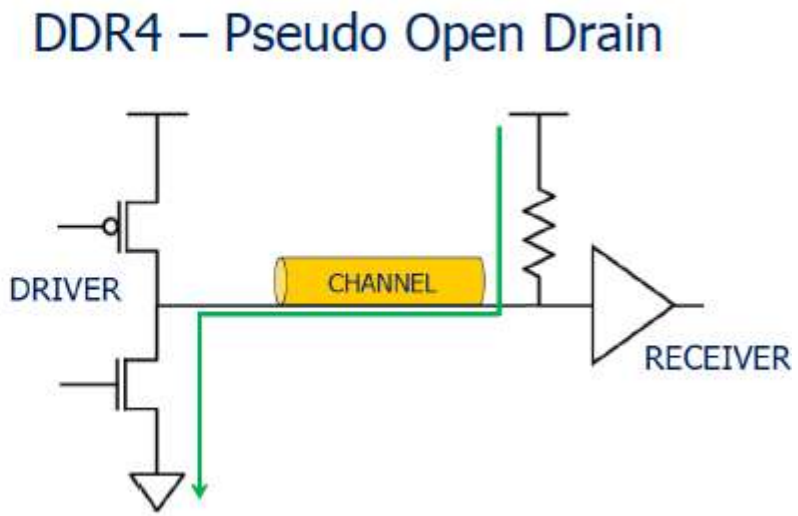
DDR4 only Controller Features

- Internal DQa Vref supply & calibration, both controller & DRAM
- Data write CRC (not available in LS1)
- Data Inversion bus
- Address bus parity error
- 16 banks for more concurrency
- Connectivity test mode
- ODT park and buffer disable
- DRAM mode register readout capability
- Low power auto self refresh
- Pseudo open drain (POD) driver and termination
- Command Address latency (CAL)

DDR4 Output Driver / Termination

- Center tap termination is used in DDR3 receiver
- POD termination or pull up is used in DDR4 receiver
- Push-Pull driver in DDR3 and POD driver in DDR4
- Less power is consumed using POD driver & termination.





Pin Muxing in Layerscape LS102x memory controller

- DDR4 support up to 16Gb vs. 8Gb in DDR3
- DDR4 uses A0-A13 for column accesses (i.e. MA[14] & MA[15] not used for column access)
- DDR4 has 4 banks within each group (i.e. MBA[2] not used)

DDR3	DDR4
MRAS	MRAS/ MA[16]
MCAS	MCAS/ MA[15]
MWE	MWE/ MA[14]
MA[15]	ACT_n
MA[14]	BG1
MBA[2]	BG0
MDM[0-8]	MDM / DBI
MAPAR_ERR	Alert_n
MAPAR_OUT	PAR

New pin: ACT_n

- ACT_n is a single pin for Active command input

- When ACT_n is low:
  - ACT Command is asserted
  - WE/CAS/RAS pins will be treated as address pins (A14:A16)

- When ACT_n is high
  - WE/CAS/RAS pins will be treated as command pins

New pin: DBI_n

- Active low input/output for data bus inversion mode
- As an input to DRAM, a low on DBI_n indicates that the DRAM inverts write data received on the DQ inputs
- As an output from the DRAM, a low on DBI_n indicates that the DRAM has inverted the data on its DQ outputs.
- Maximum of half of the bits driven low including DBI_n pin
- Available only on x8 and x 16 DRAM
- Fewer bits driven low means less noise, better data eye and lower power consumption.

Data Bus Inversion - DBI

- If more than 4-bits of a byte lane are low, invert the data and drive the DBI_n pin low
- If 4 or less bits of a byte lane are low, do not invert the data and drive the DBI_n pin high

	Controller				Data Bus				Memory			
DQ0	0	1	0	0	1	1	0	1	0	1	0	0
DQ1	1	1	0	0	0	1	0	1	1	1	0	0
DQ2	0	0	0	0	1	0	0	1	0	0	0	0
DQ3	0	1	1	0	1	1	1	1	0	1	1	0
DQ4	0	1	0	0	1	1	0	1	0	1	0	0
DQ5	1	0	1	0	0	0	1	1	1	0	1	0
DQ6	1	1	1	0	0	1	1	1	1	1	1	0
DQ7	0	0	1	0	1	0	1	1	0	0	1	0
DBI_n					0	1	1	0				
# low bits	5	3	4	8	4	3	4	1				

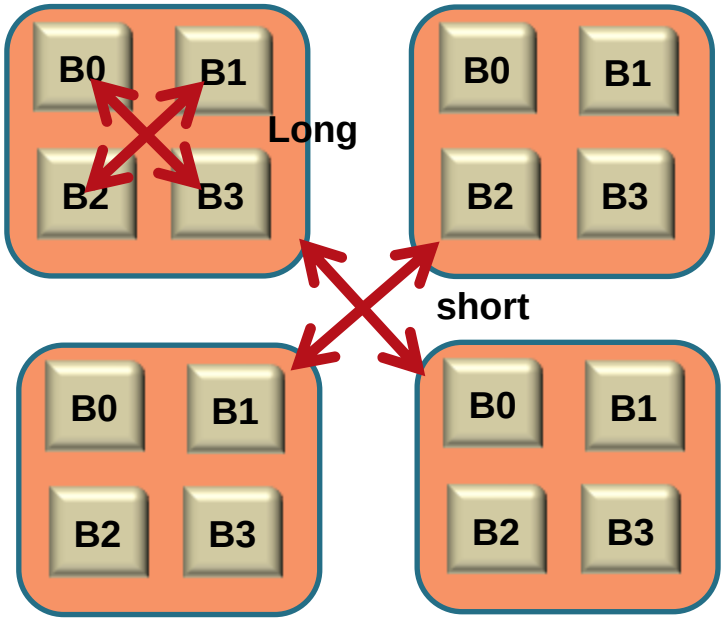
New pin: BGn Bank Group Address

- Different timing within a group and between groups
  - Active to active
  - Write to read
  - CAS to CAS
- Controller to maintain

Timing requirements for both

Within a group (Long) and

Between groups (short)



New pin: Parity

- C/A Parity signal (PAR) covers ACT_n, RAS_n, CAS_n, WE_n and the address bus. Control signals CKE, ODT, CS_n are not included.
- Even parity, i.e. valid parity is defined as an even number of ones across the inputs used for parity computation combined with the parity signal. The parity bit is chosen so that the total number of ‘1’s in the transmitted signal, including the parity bit is even.
- Commands must be qualified by CS_n.
- Alert_n used to flag error to memory controller.

Data Write CRC

- Example data mapping with CRC for 8-bit, 4-bit and 16-bit devices
- Note: not the same as ECC

The following figure shows detailed bit mapping for a x8 device.

	0	1	2	3	4	5	6	7	8	9
DQ0	d0	d1	d2	d3	d4	d5	d6	d7	CRC0	1
DQ1	d8	d9	d10	d11	d12	d13	d14	d15	CRC1	1
DQ2	d16	d17	d18	d19	d20	d21	d22	d23	CRC2	1
DQ3	d24	d25	d26	d27	d28	d29	d30	d31	CRC3	1
DQ4	d32	d33	d34	d35	d36	d37	d38	d39	CRC4	1
DQ5	d40	d41	d42	d43	d44	d45	d46	d47	CRC5	1
DQ6	d48	d49	d50	d51	d52	d53	d54	d55	CRC6	1
DQ7	d56	d57	d58	d59	d60	d61	d62	d63	CRC7	1
DBI_n	d64	d65	d66	d67	d68	d69	d70	d71	1	1

The following figure shows detailed bit mapping for a x4 device.

	0	1	2	3	4	5	6	7	8	9
DQ0	d0	d1	d2	d3	d4	d5	d6	d7	CRC0	CRC4
DQ1	d8	d9	d10	d11	d12	d13	d14	d15	CRC1	CRC5
DQ2	d16	d17	d18	d19	d20	d21	d22	d23	CRC2	CRC6
DQ3	d24	d25	d26	d27	d28	d29	d30	d31	CRC3	CRC7

Data Write CRC (continued)

A x16 device is treated as two x8 devices. x16 device will have two identical CRC trees implemented. CRC(0-7) covers data bits d(0-71). CRC(8-15) covers data bits d(72-143).

	0	1	2	3	4	5	6	7	8	9
DQ0	d0	d1	d2	d3	d4	d5	d6	d7	CRC0	1
DQ1	d8	d9	d10	d11	d12	d13	d14	d15	CRC1	1
DQ2	d16	d17	d18	d19	d20	d21	d22	d23	CRC2	1
DQ3	d24	d25	d26	d27	d28	d29	d30	d31	CRC3	1
DQ4	d32	d33	d34	d35	d36	d37	d38	d39	CRC4	1
DQ5	d40	d41	d42	d43	d44	d45	d46	d47	CRC5	1
DQ6	d48	d49	d50	d51	d52	d53	d54	d55	CRC6	1
DQ7	d56	d57	d58	d59	d60	d61	d62	d63	CRC7	1
DBIL_n	d64	d65	d66	d67	d68	d69	d70	d71	1	1
DQ8	d72	d73	d74	d75	d76	d77	d78	d79	CRC8	1
DQ9	d80	d81	d82	d83	d84	d85	d86	d87	CRC9	1
DQ10	d88	d89	d90	d91	d92	d93	d94	d95	CRC10	1
DQ11	d96	d97	d98	d99	d100	d101	d102	d103	CRC11	1
DQ12	d104	d105	d106	d107	d108	d109	d110	d111	CRC12	1
DQ13	d112	d113	d114	d115	d116	d117	d118	d119	CRC13	1
DQ14	d120	d121	d122	d123	d124	d125	d126	d127	CRC14	1
DQ15	d128	d129	d130	d131	d132	d133	d134	d135	CRC15	1
DBIU_n	d136	d137	d138	d139	d140	d141	d142	d143	1	1

New pin Alert_n

- Alert_n – Active low output signal that indicates an error event for both the C/A Parity Mode and the CRC Data Mode
- CRC Data mode. Not ECC. The DRAM device generates a checksum per byte lane for both READ and WRITE data and returns the checksum to the controller. Based on the checksum, the controller can decide if the data or the returned CRC was transmitted in error and take appropriate measures, details TBD.

Low power auto self-refresh

- While DRAM is in self-refresh mode, four refresh mode options available:
  - Manual mode, normal temperature (0 – 85C)
  - Manual mode, extended temperature (0 – 95C)
  - Manual mode, reduced temperature (0 – 45C)
  - Automatic mode: automatically switches between modes based on temperature sensor measurements

- Power savings by reducing refresh rate when possible

Command Address Latency (CAL)

- DDR4 supports Command Address Latency, CAL, function as a power savings feature. CAL is the delay in clock cycles between CS_n and CMD/ADDR. CAL gives the DRAM time to enable the CMD/ADDR receivers before a command is issued. Once the command and the address are latched the receivers can be disabled.

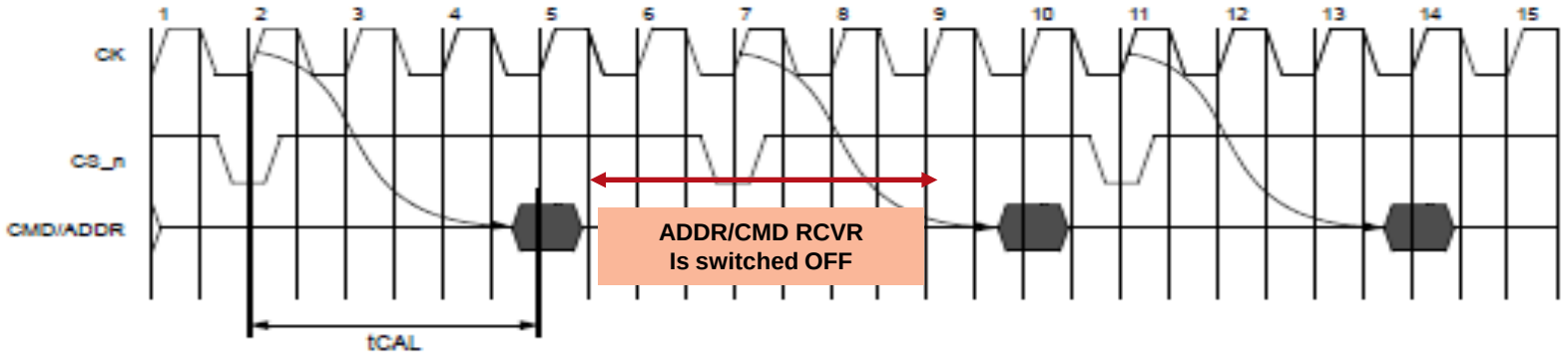
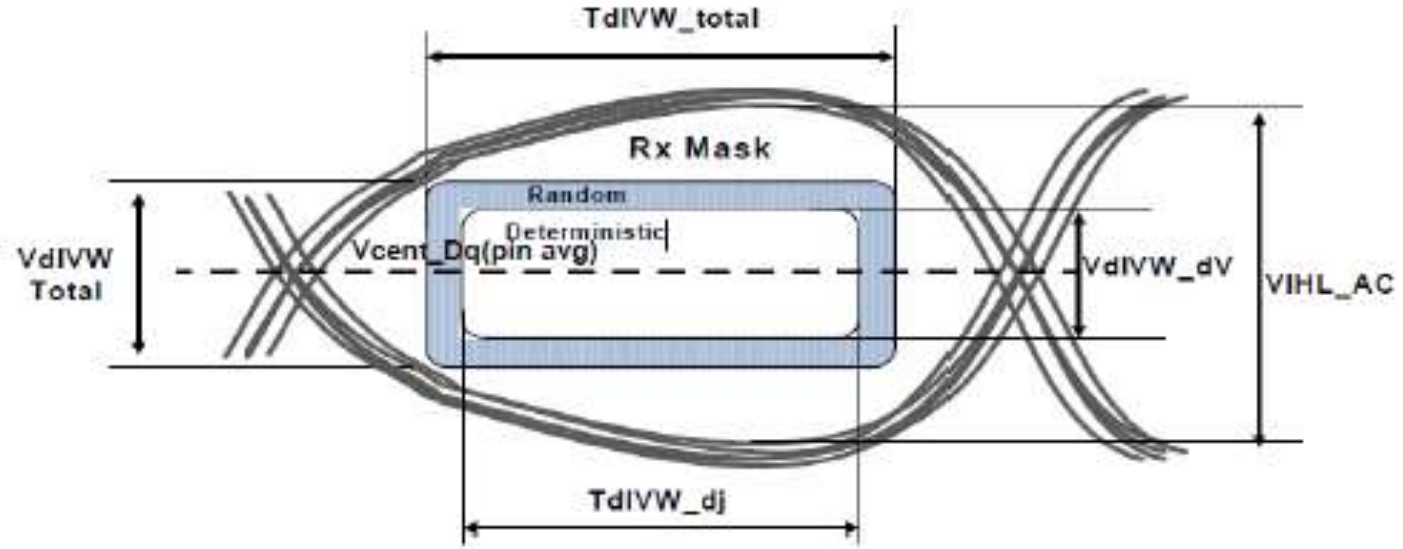


Figure 34 — Definition of CAL

DRAM Receiver data eye mask and BER

- Bit error rate (similar to serdes) is defined for DRAM receiver measurement
- DRAM receiver data mask is defined for random and deterministic Jitter as data rates approaching 3GT/s.
- For LS1 (i.e. data rates of 1600MT/s or less) we will continue with the conventional setup and hold time measurements.



Summary

- DDR3/3L is mainstream now
- DDR4 is expected to start gaining market share by 2014
- Next generation QorIQ Layerscape and QorIQ T Series devices families support DDR3L & DDR4
- DDR4 low power consumption is suitable for next generation devices
- Follow JEDEC recommended topologies for discrete parts
- Using QCS and DDRv tool, configuration and initialization of memory controller can be easily achieved

Useful References

- Books:
  - DRAM Circuit Design: A Tutorial, Brent Keeth and R. Jacob Baker, IEEE Press, 2001
- Freescale Application Notes:
  - AN2582 Hardware and Layout Design Considerations for DDR Memory Interfaces
  - AN2910 Hardware and Layout Design Considerations for DDR2 Memory Interfaces
  - AN2583 Programming the PowerQUICCIII / PowerQUICCII Pro DDR SDRAM Controller
  - AN3369 PowerQUICC DDR2 SDRAM Controller Register Setting Considerations
  - AN3939 PQ & QorIQ Interleaving
  - AN3940 Layout Design Considerations for DDR3 Memory Interface
  - AN4039 PowerQUICC DDR3 SDRAM Controller Register Setting Considerations
- Micron Application Notes:
  - TN-46-05 General DDR SDRAM Functionality
  - TN-47-02 DDR2 Offers New Features and Functionality
  - TN-47-01 DDR2 Design Guide
  - TN-41-07 DDR3 Power-Up, Initialization, and Reset
  - TN-41-08 DDR3 Design Guide
- JEDEC Specifications:
  - JESD79E Double Data Rate (DDR) SDRAM Specification
  - JESD79-2F DDR2 SDRAM Specification
  - JESD79-3D DDR3 SDRAM Specification
- Tools
  - QorIQ Configuration Suite
  - QorIQ Optimization Suite

DDR Configuration and Validation Tools

QorIQ Configuration Suite – Now Available!

- **QorIQ Configuration Suite v3.0 is NOW AVAILABLE!!!**
  - Supports all QorIQ and Qorivva devices
  - Works with Eclipse 3.5, Eclipse 3.6, Eclipse 3.7 development tools
    - Pure Java solution for maximum choice of host system support
    - Add-in to CodeWarrior Development Studio for PA, v10.1 or later
  - Available from www.freescale.com/QCS – FREE DOWNLOAD*
- **Includes the following configuration tools all designed to collaborate on consistent configuration:**
  - PBL tool to define the Reset Control Word bit values and PBI data for the pre-boot
  - BOOTROM generator for those QorIQ without RCW functionality
  - DDR configuration supports setting the controller to a working state for any DDR
  - Data path graphical view helps to define data path configuration for the DPAA.
  - Hardware Device Tree editor supports references, synchronous GUI and XML editing, node validation based on specification bindings
  - Packaged as a separate product with installer and wizard functionality

* Must be a QorIQ customer or under QorIQ NDA for download permission

Actual URL is http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=PE_QORIQ_SUITE&tid=PEH

Installing Processor Expert for QorIQ

- You need CodeWarrior for PA 10.1 or later

  OR, you download an Eclipse version for free

  OR, you use an existing Eclipse workbench you have installed (Wind River, QNX, GNU, etc.)

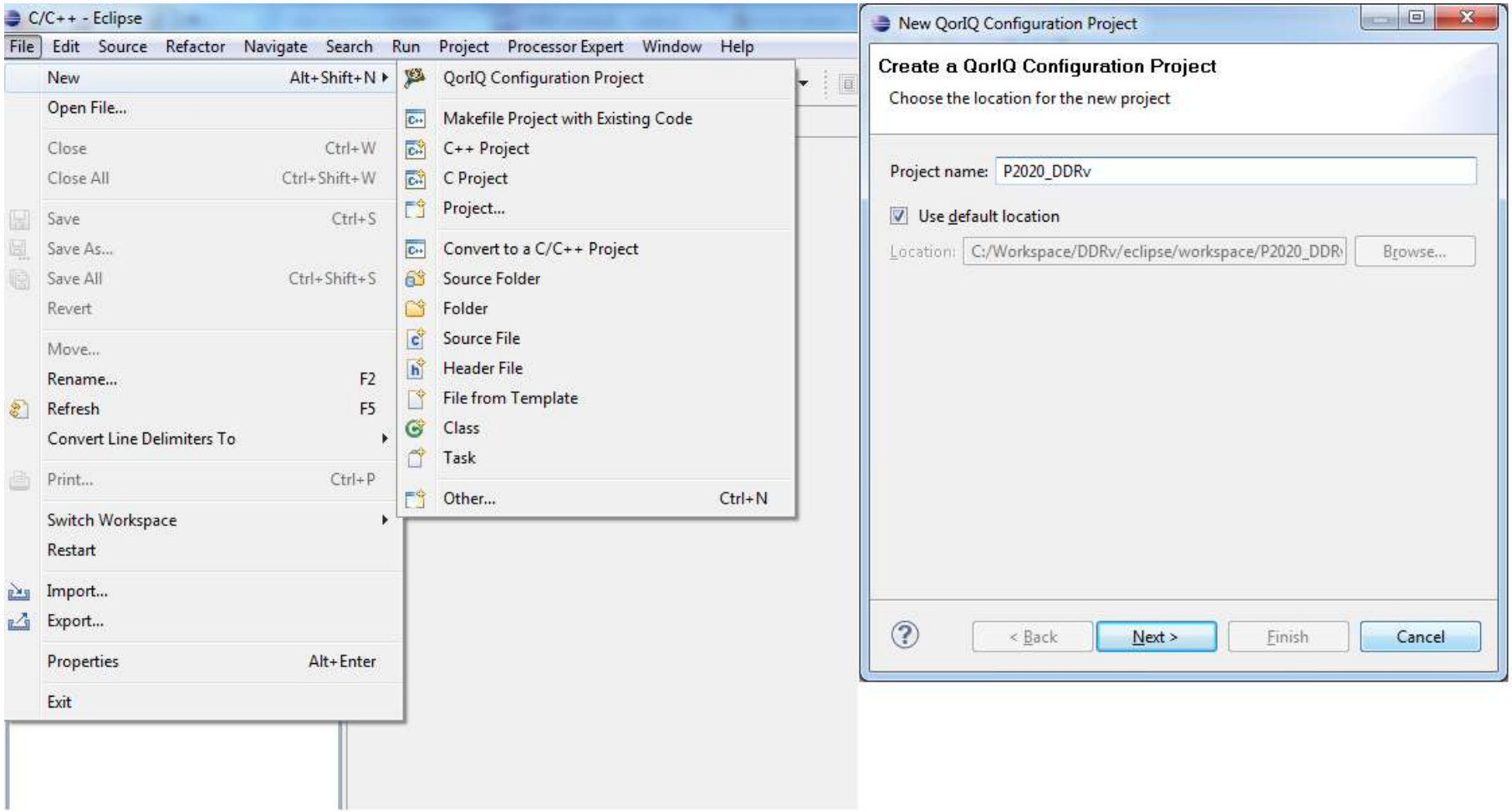
- Processor Expert for QorIQ Configuration Suite installs using the Eclipse updater's "Add new software…" capability

- The Configuration Suite is 100% pure Java so it should run on any Eclipse 3.6.1 or later host environment (Windows, Linux, Solaris, Mac OS, 32-bit/64-bit, …)

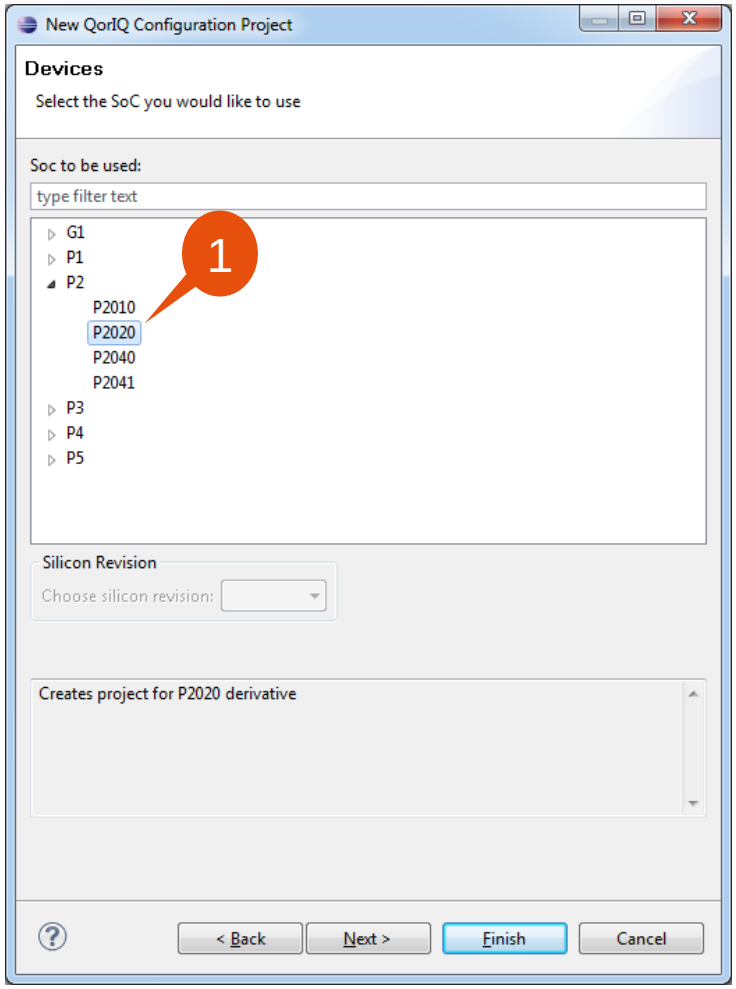
DDR Configuration

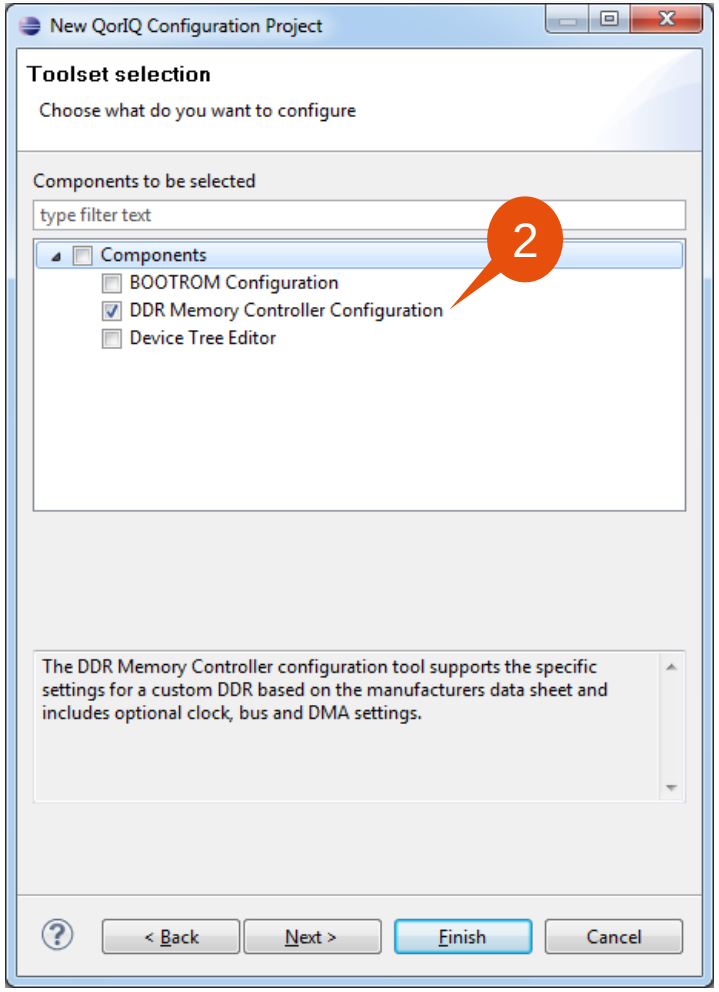
Creating New DDR Configuration

Create New QCS project

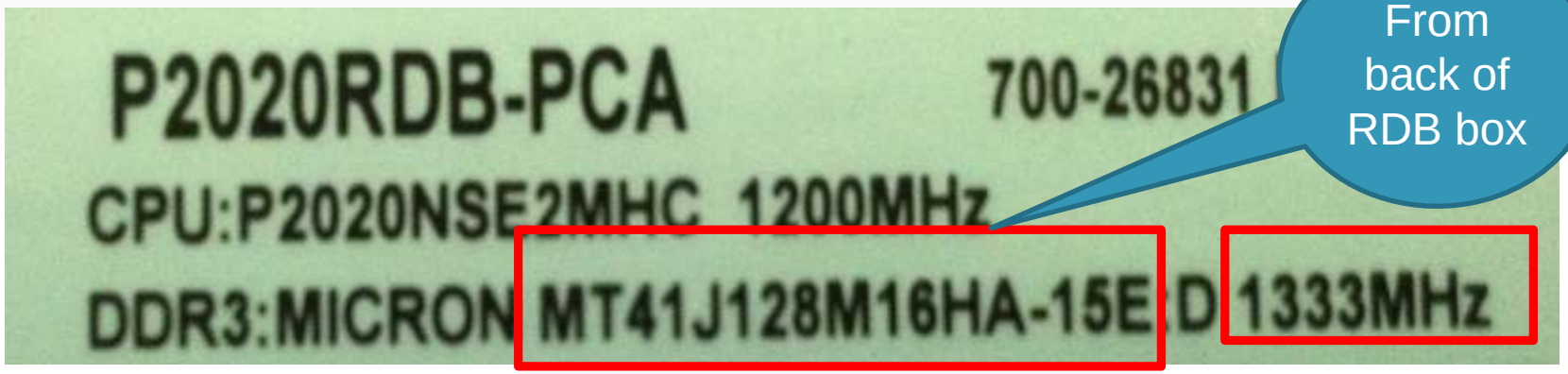


Select device and DDR component





Get DRAM information – P2020RDB-PCA



Micron

DDR3 SDRAM

MT41J512M4 – 64 Meg x 4 x 8 Banks

MT41J256M8 – 32 Meg x 8 x 8 Banks

MT41J128M16 – 16 Meg x 16 x 8 Banks

From DRAM datasheet

How about rest of the timing parameters?

Table 1: Key Timing Parameters

Speed Grade	Data Rate (MT/s)	Target ^{t}RCD-^{t}RP-CL	^{t}RCD (ns)	^{t}RP (ns)	CL (ns)
-093[1, 2, 3, 4]	2133	14-14-14	13.09	13.09	13.09
-107[1, 2, 3]	1866	13-13-13	13.91	13.91	13.91
-125[1, 2,]	1600	11-11-11	13.75	13.75	13.75
-15E[1,]	1333	9-9-9	13.5	13.5	13.5
-187E	1066	7-7-7	13.1	13.1	13.1

Features

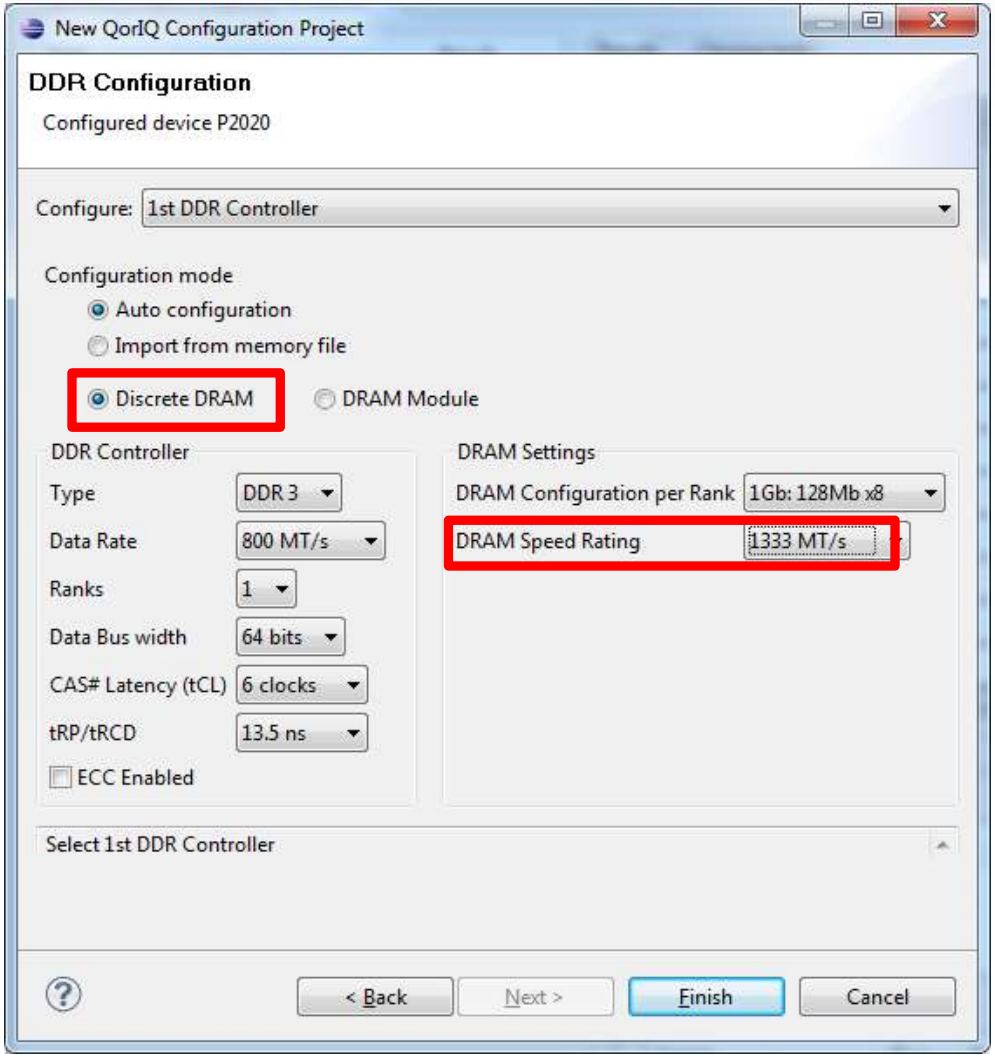
- $V_{DD} = V_{DDQ}$ = 1.5V ±0.075V
- 1.5V center-terminated push/pull I/O
- Differential bidirectional data strobe
- 8*n*-bit prefetch architecture
- Differential clock inputs (CK, CK#)
- 8 internal banks
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Programmable CAS READ latency (CL)
- Posted CAS additive latency (AL)
- Programmable CAS WRITE latency (CWL) based on ^{t}CK
- Fixed burst length (BL) of 8 and burst chop (BC) of 4 (via the mode register set [MRS])
- Selectable BC4 or BL8 on-the-fly (OTF)
- Self refresh mode
- T_C of 0°C to 95°C
  - 64ms, 8192 cycle refresh at 0°C to 85°C
  - 32ms, 8192 cycle refresh at 85°C to 95°C
- Self refresh temperature (SRT)
- Write leveling
- Multipurpose register
- Output driver calibration

Options[1]	Marking
• Configuration	
– 512 Meg x 4	512M4
– 256 Meg x 8	256M8
– 128 Meg x 16	128M16
• FBGA package (Pb-free) – x4, x8	
– 78-ball (8mm x 10.5mm) Rev. H,M,J,K	DA
– 78-ball (9mm x 11.5mm) Rev. D	HX
• FBGA package (Pb-free) – x16	
– 96-ball (9mm x 14mm) Rev. D	HA
– 96-ball (8mm x 14mm) Rev. K	JT
• Timing – cycle time	
– 938ps @ CL = 14 (DDR3-2133)	-093
– 1.071ns @ CL = 13 (DDR3-1866)	-107
– 1.25ns @ CL = 11 (DDR3-1600)	-125
– 1.5ns @ CL = 9 (DDR3-1333)	-15E
– 1.87ns @ CL = 7 (DDR3-1066)	-187E
• Operating temperature	
– Commercial (0°C ≤ T_C ≤ +95°C)	None
– Industrial (–40°C ≤ T_C ≤ +95°C)	IT
• Revision	:D/:H/:J/:K/ :M

Note: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on http://www.micron.com for available offerings.

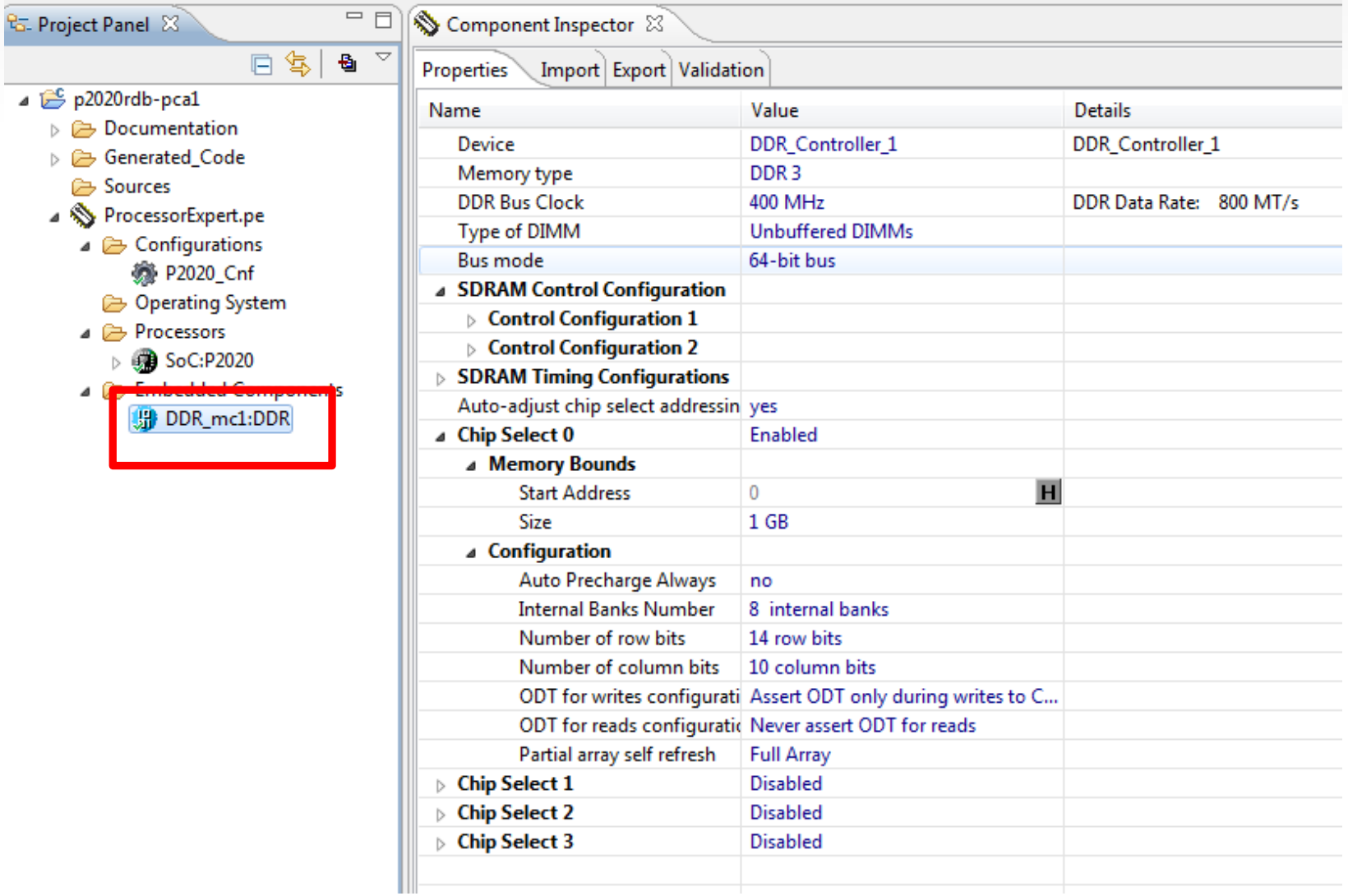
- Tool automatically computes tRCD, tRP, and CL!
  - User can change these values if required.

DDR New Project Wizard

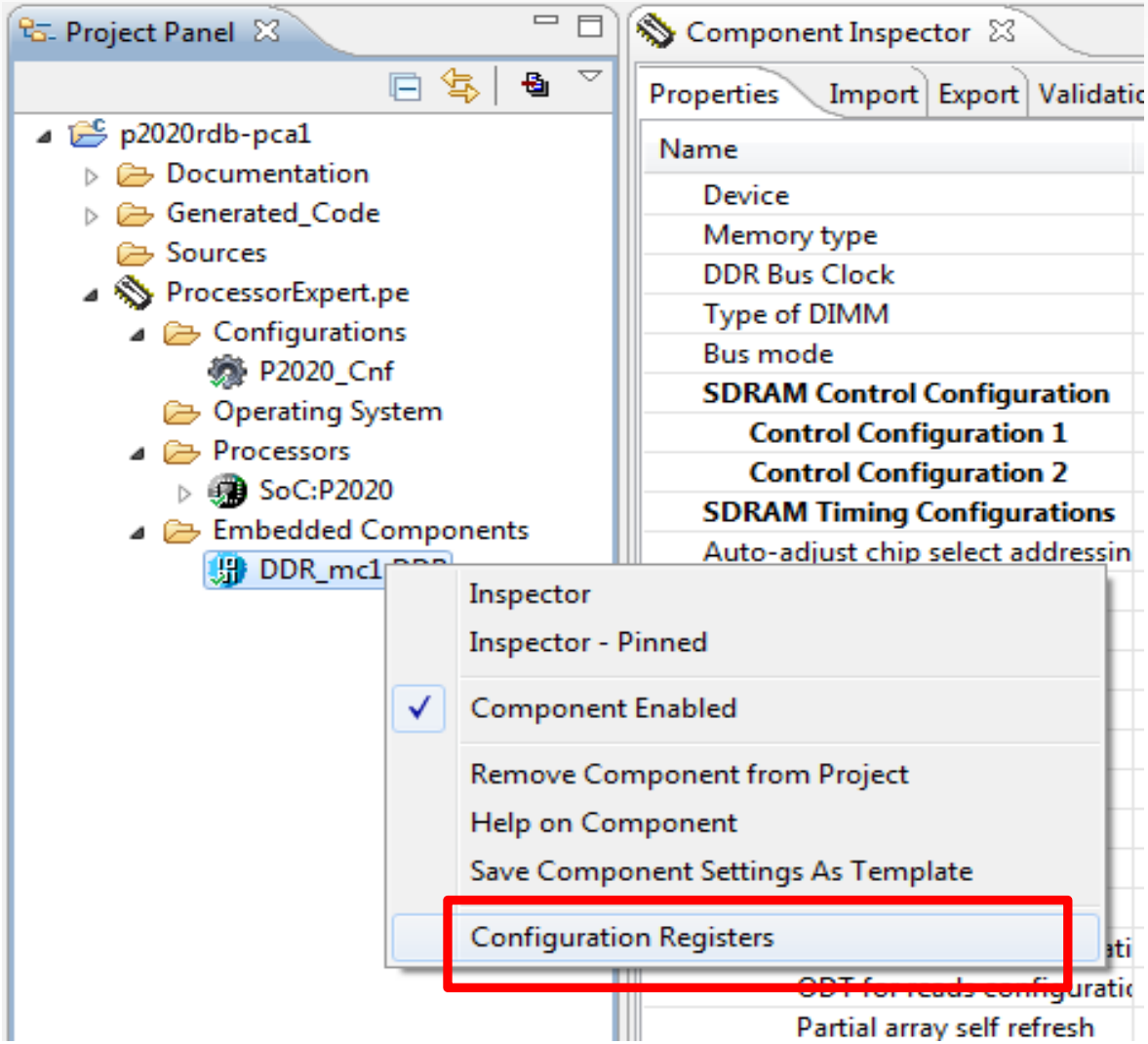


- From memory data sheet:
  - Maximum speed rating
  - Capacity

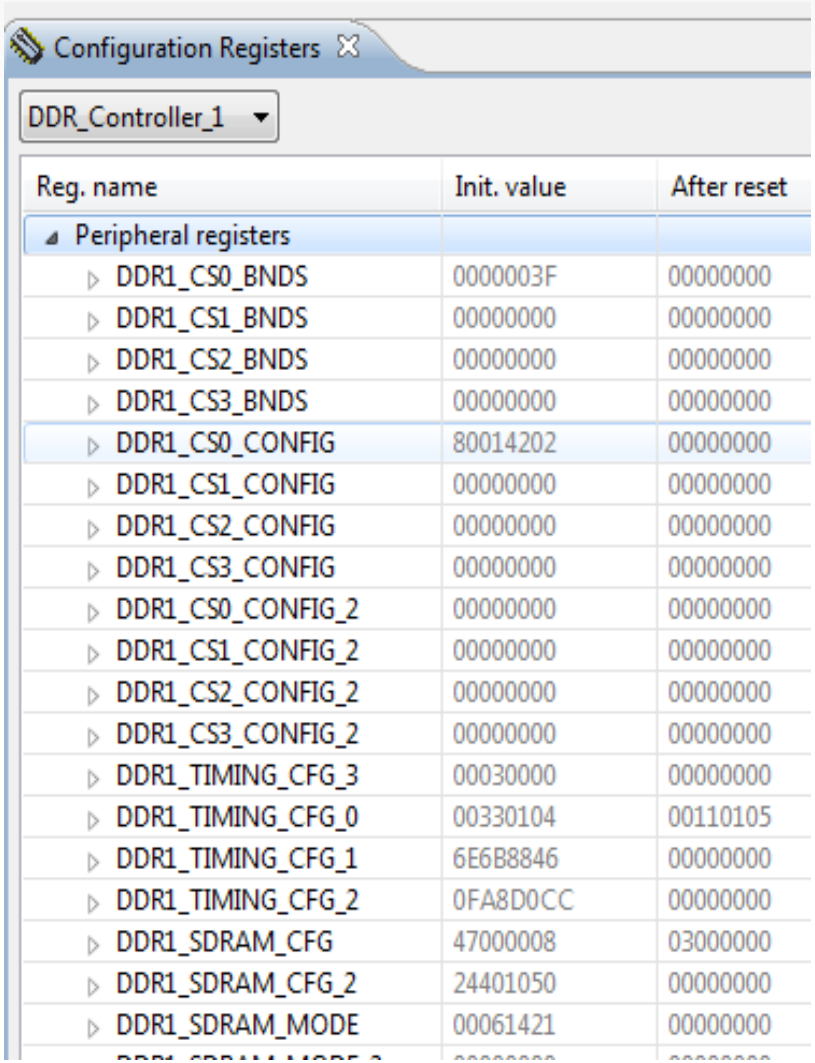
QCS project explorer



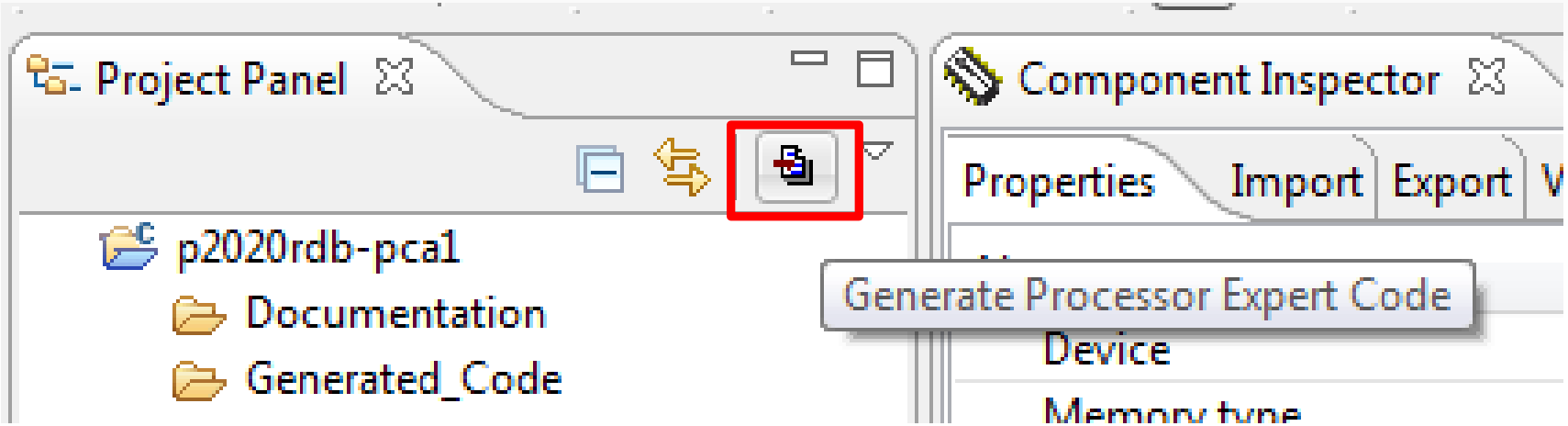
Review DDR registers values

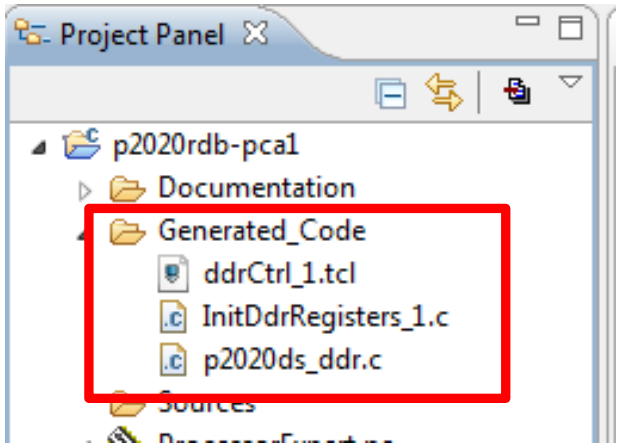


Review DDR registers values – contd.



Generate DDR configuration





Generated files – CW, uboot, ddrinit.c

```
# DDR Controller 1 Registers

  # DDR_SDRAM_CFG
  mem [0xFF702110] = 0x47000008

  # CS0_BNDS
  mem [0xFF702000] = 0x3F

  # CS0_CONFIG
  mem [0xFF702080] = 0x80014202

  # CS0_CONFIG_2
  mem [0xFF7020C0] = 0x00

  # TIMING_CFG_3
  mem [0xFF702100] = 0x00030000

  # TIMING_CFG_0
  mem [0xFF702104] = 0x00330104

  # TIMING_CFG_1
  mem [0xFF702108] = 0x6E6B8846

  # TIMING_CFG_2
  mem [0xFF70210C] = 0x0FA8D0CC

  # DDR_SDRAM_CFG_2
  mem [0xFF702114] = 0x24401050

  # DDR_SDRAM_MODE
  mem [0xFF702118] = 0x00061421
```

```
#define DDR_1_INIT_EXT_ADDR_ADDR     0xFF70214C
#define DDR_1_SDRAM_RCW_1_ADDR       0xFF702180
#define DDR_1_SDRAM_RCW_2_ADDR       0xFF702184
#define DDR_1_DATA_INIT_ADDR         0xFF702128
#define DDR_1_SDRAM_MD_CNTL_ADDR     0xFF702120
#define DDR_1_DDRCDR_1_ADDR          0xFF702B28
#define DDR_1_DDRCDR_2_ADDR          0xFF702B2C

#define SDRAM_CFG_MEM_EN_MASK        0x80000000
#define SDRAM_CFG2_D_INIT_MASK       0x00000010

/* DDR Controller configured registers' values */
#define DDR_1_CS0_BNDS_VAL           0x3F
#define DDR_1_CS1_BNDS_VAL           0x00
#define DDR_1_CS2_BNDS_VAL           0x00
#define DDR_1_CS3_BNDS_VAL           0x00
#define DDR_1_CS0_CONFIG_VAL         0x80014202
#define DDR_1_CS1_CONFIG_VAL         0x00
```

```
#define PEX_CONFIG_DDR1_INIT_EXT_ADDR     0x00000000
#define PEX_CONFIG_DDR1_TIMING_4          0x00220001
#define PEX_CONFIG_DDR1_TIMING_5          0x02401400
#define PEX_CONFIG_DDR1_ZQ_CNTL           0x89080600
#define PEX_CONFIG_DDR1_WRLVL_CNTL        0x8655F614
#define PEX_CONFIG_DDR1_RCW_1             0x00000000
#define PEX_CONFIG_DDR1_RCW_2             0x00000000


/* DDR Controller 1 configuration global structures */
fsl_ddr_cfg_regs_t ddr_cfg_regs_0 = {
  .cs[0].bnds = PEX_CONFIG_DDR1_CS0_BNDS,
  .cs[1].bnds = PEX_CONFIG_DDR1_CS1_BNDS,
  .cs[2].bnds = PEX_CONFIG_DDR1_CS2_BNDS,
  .cs[3].bnds = PEX_CONFIG_DDR1_CS3_BNDS,
  .cs[0].config = PEX_CONFIG_DDR1_CS0_CONFIG,
  .cs[1].config = PEX_CONFIG_DDR1_CS1_CONFIG,
  .cs[2].config = PEX_CONFIG_DDR1_CS2_CONFIG,
```

Steps to adapt DDR configuration file in CodeWarrior

- Open the CW config file you want to adapt

  D:\Program Files\Freescale\CW PA v10.1\PA\PA_Support\Initialization_Files\QorIQ_P4\P4080DS_init_core0.cfg

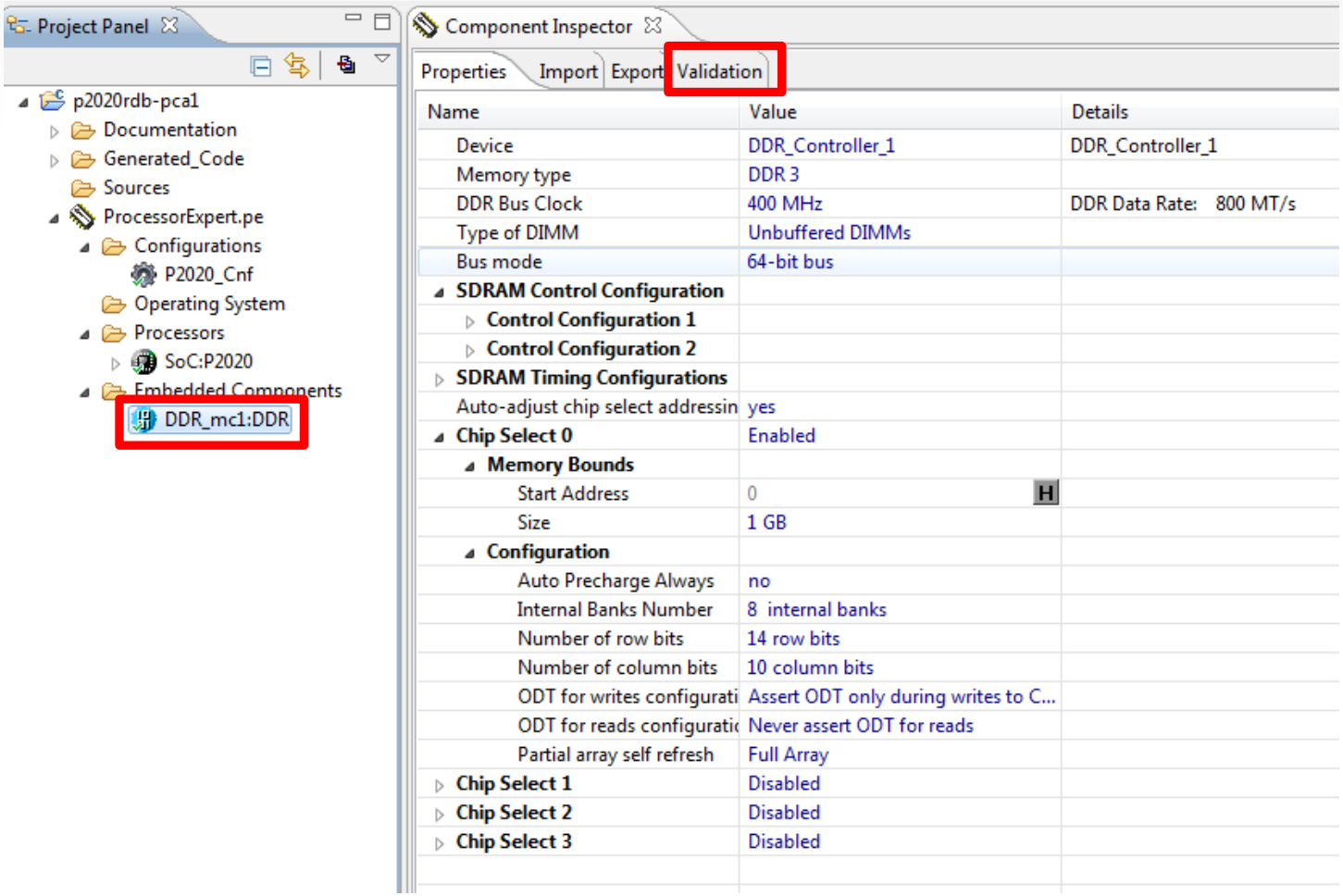
- Replace DDR1 config section with the one from

  D:\Profiles\b08844\workspace\p4080\Generated_Code\ddrCtrl_1.cfg

- Use this new config file with your stationary project

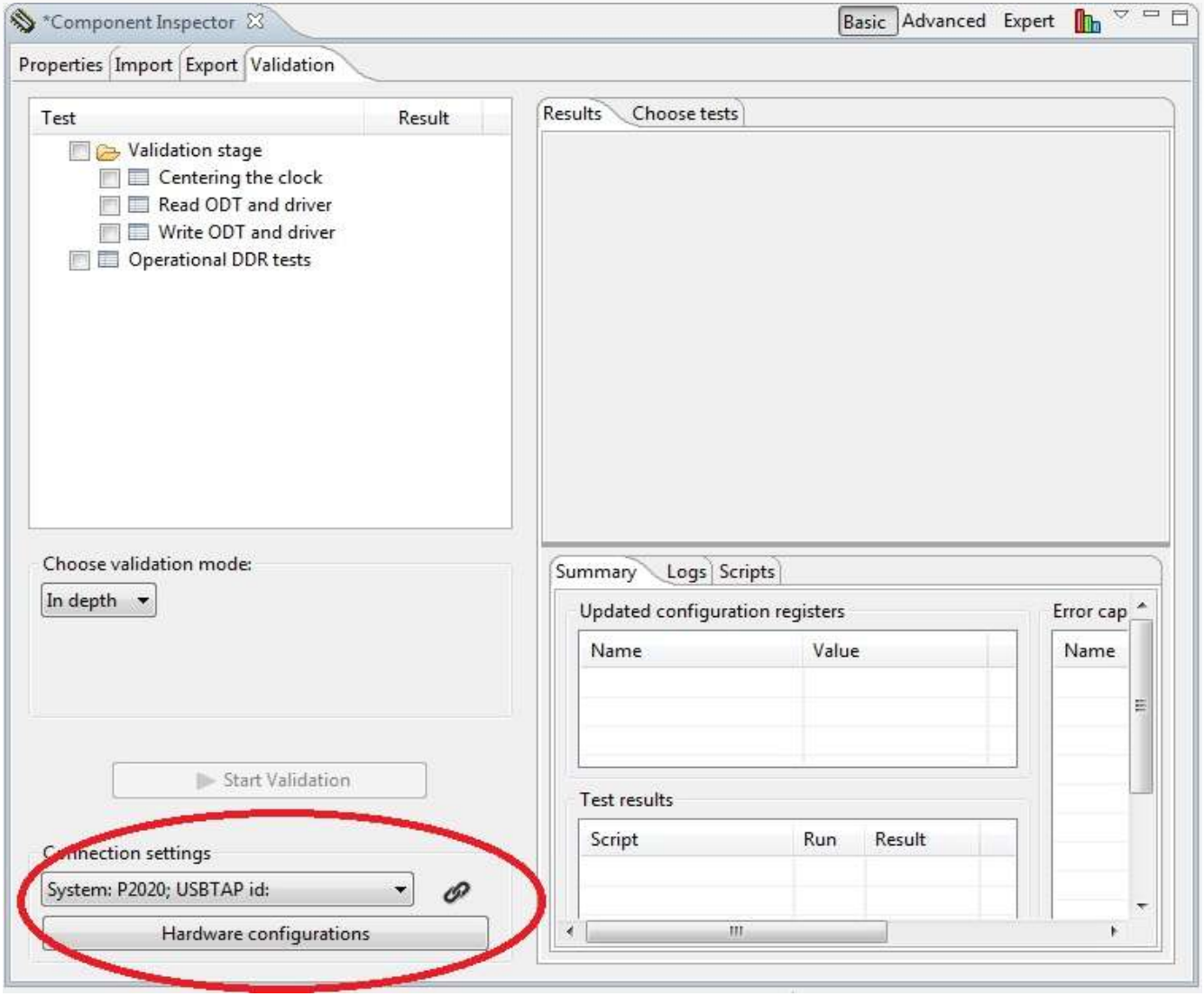
DDR Validation Tool

DDR Validation Tool - Activate

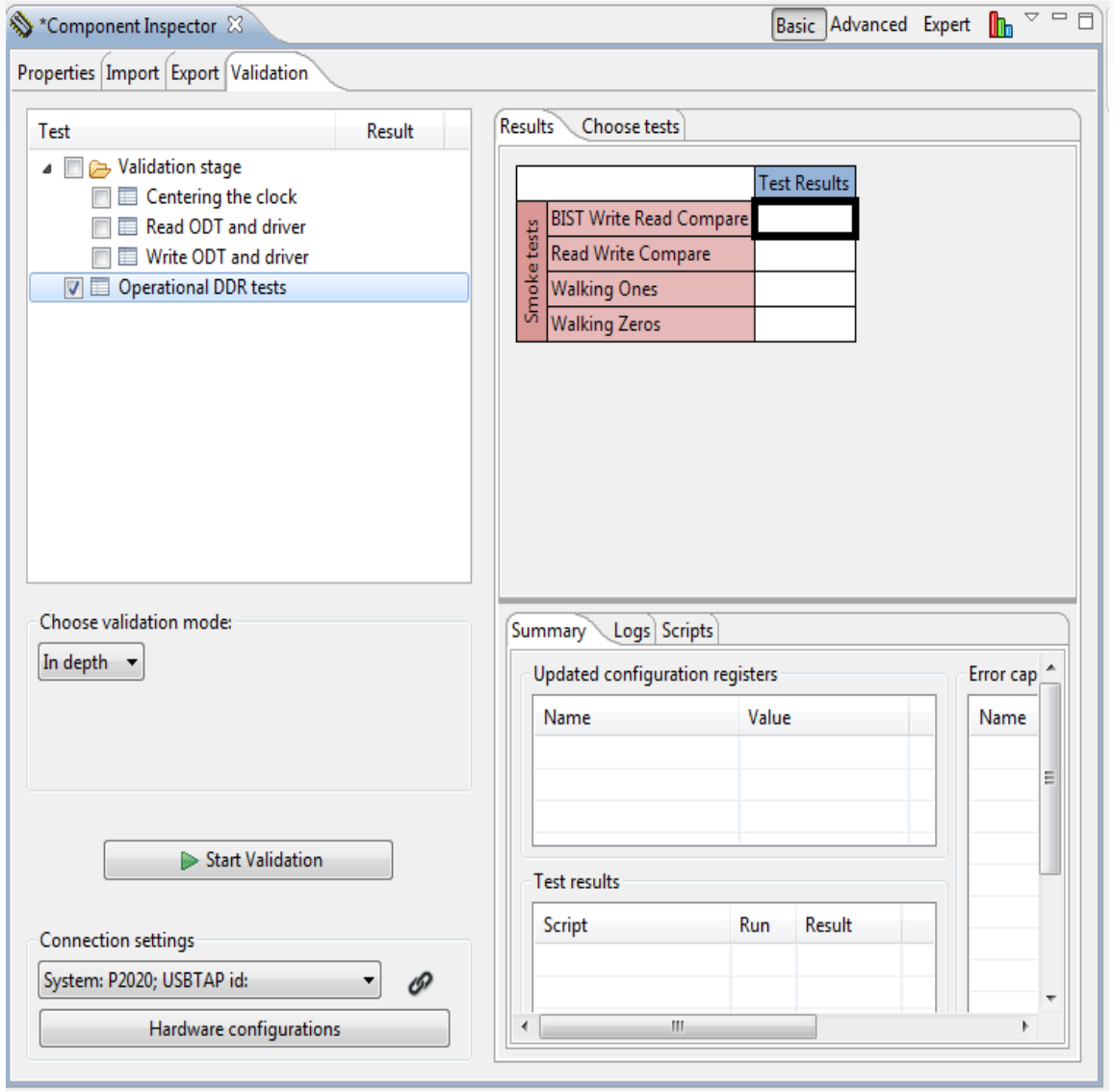


License file:
<QCS Install directory>/eclipse/Optimization/license.dat

DDRv Connection Setup

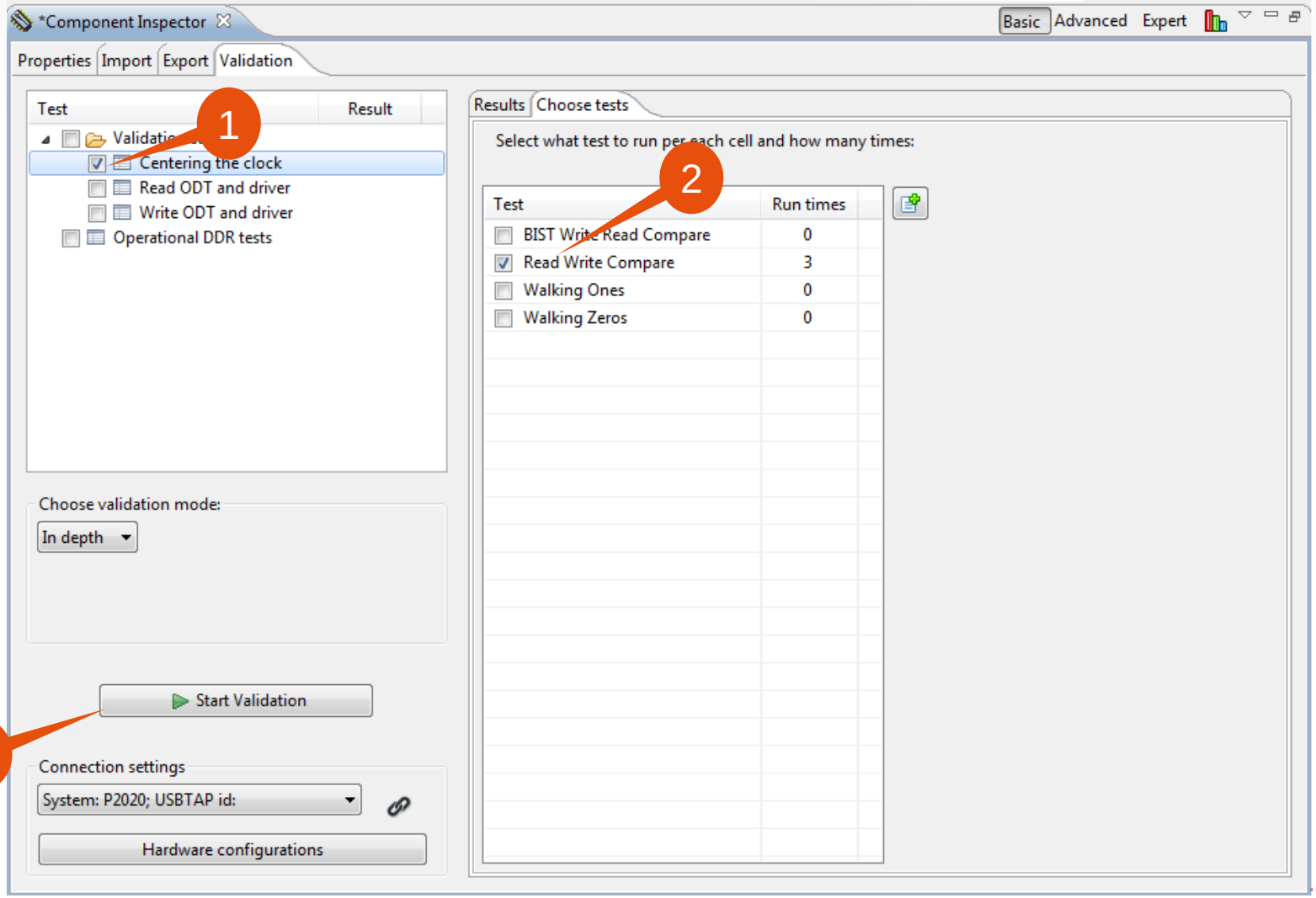


DDRv Basic Connection Test

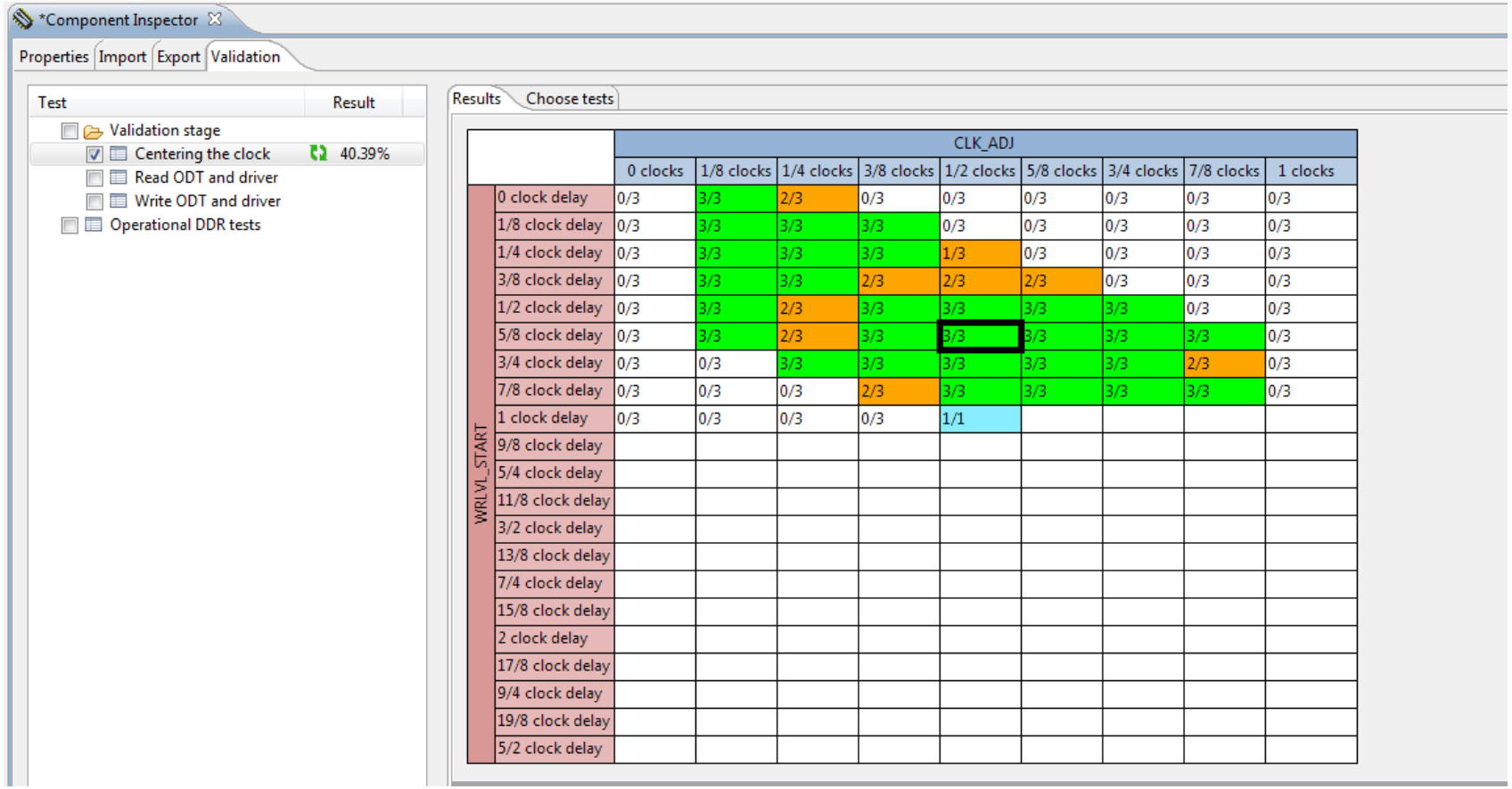


- Run basic test to confirm target connection

Configure DDR scenarios and tests

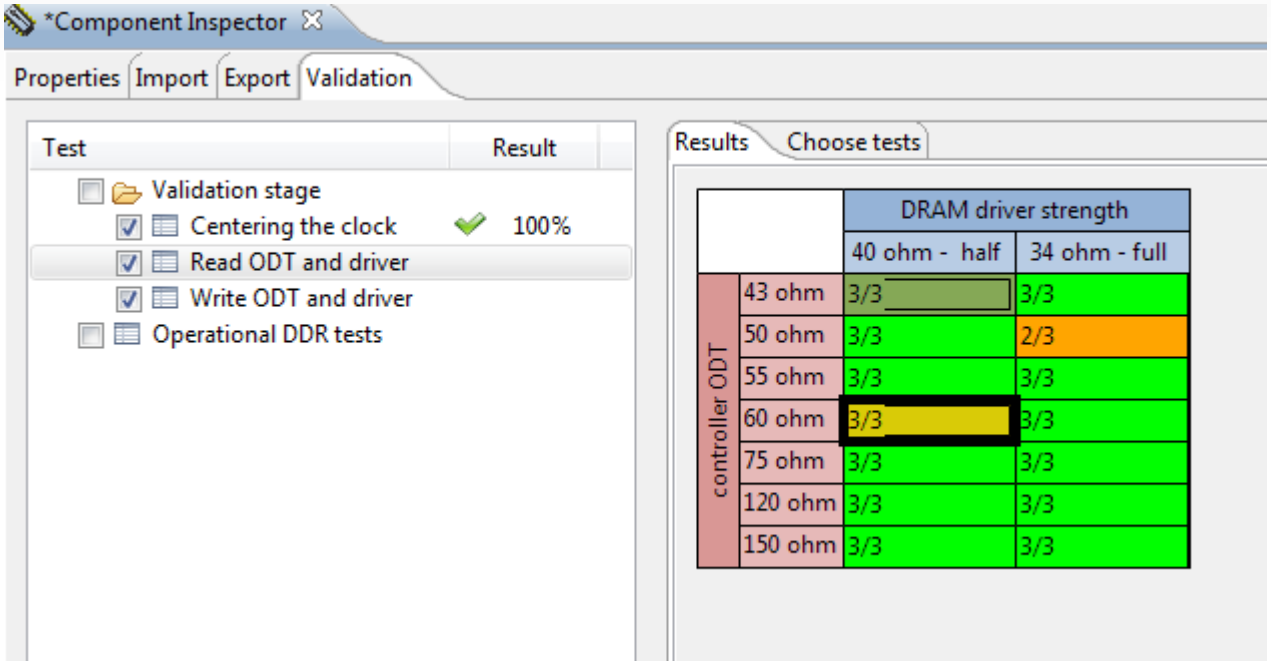


Centering of the clock results



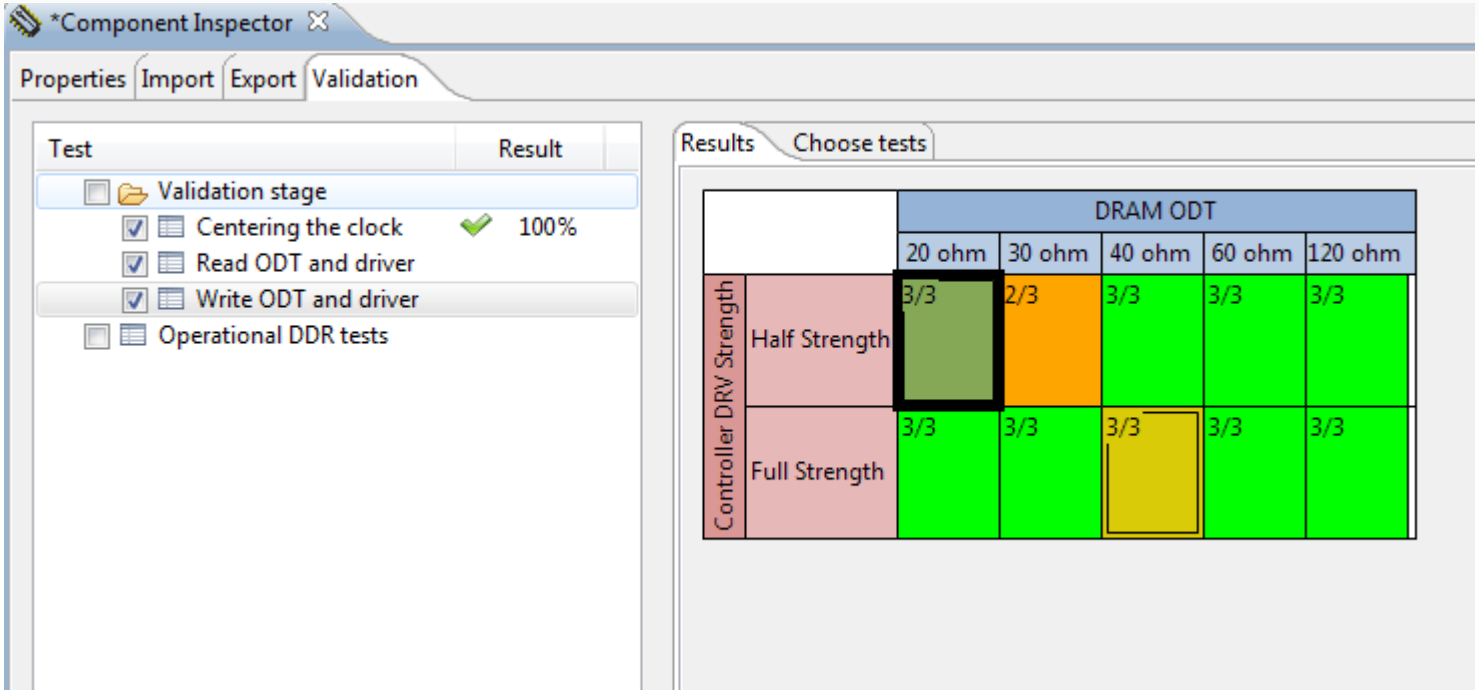
- Click “cell” to choose Write level start and CLK_ADJ values.

DDR read ODT and driver strength – test results



- Click “cell” to choose optimized ODT value.

DDR write ODT and drive strength – test results



- Click “cell” to choose optimized ODT value.

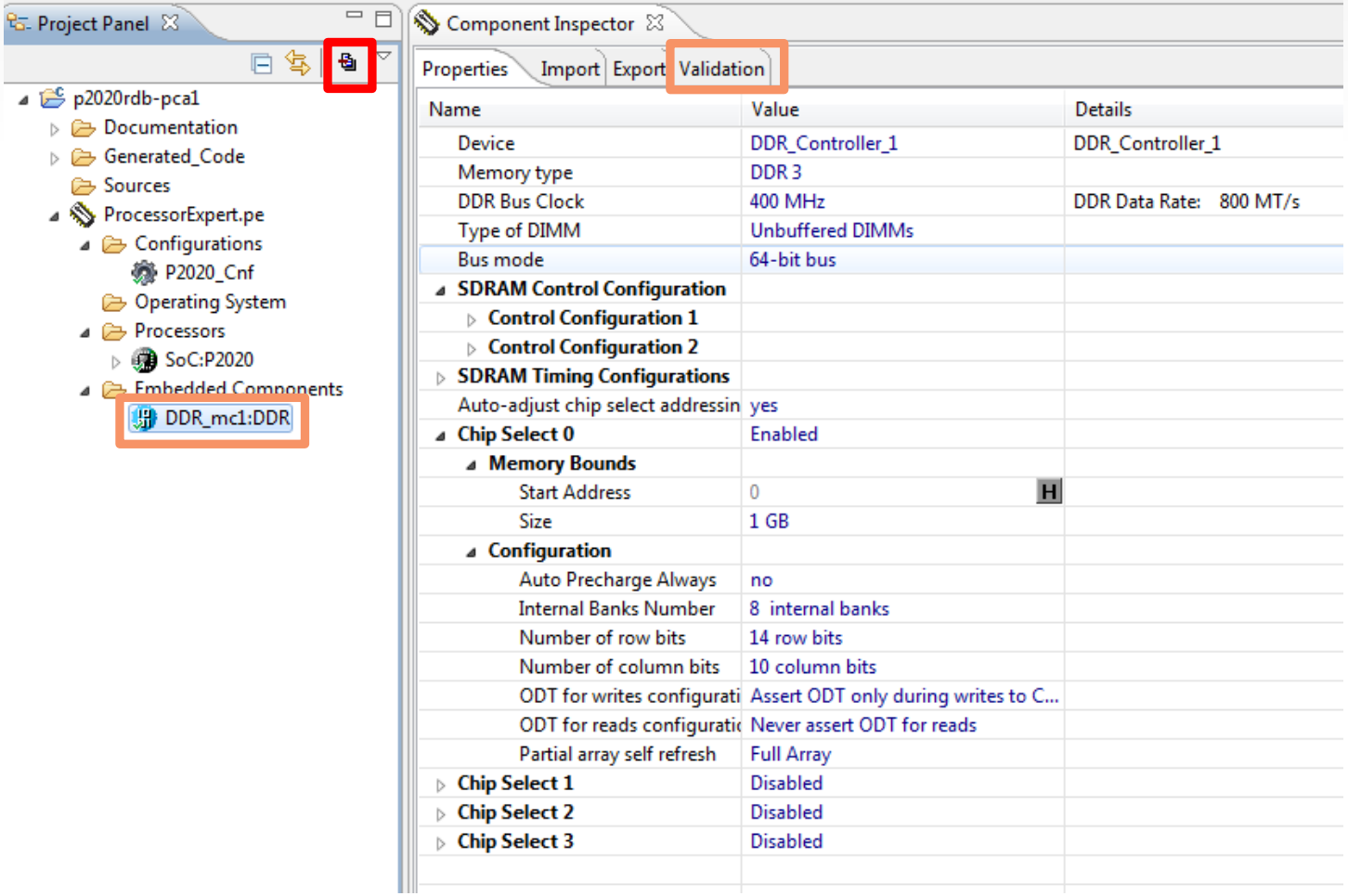
Centering of the clock - after ODT optimization

Results | Choose tests

WRLVL_START	CLK_ADJ								
	0 clocks	1/8 clocks	1/4 clocks	3/8 clocks	1/2 clocks	5/8 clocks	3/4 clocks	7/8 clocks	1 clocks
0 clock delay	0/3	3/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3
1/8 clock delay	0/3	3/3	3/3	3/3	0/3	0/3	0/3	0/3	0/3
1/4 clock delay	0/3	3/3	3/3	3/3	0/3	0/3	0/3	0/3	0/3
3/8 clock delay	0/3	3/3	3/3	3/3	3/3	3/3	0/3	0/3	0/3
1/2 clock delay	0/3	3/3	3/3	3/3	3/3	3/3	0/3	0/3	0/3
5/8 clock delay	0/3	3/3	3/3	3/3	3/3	3/3	3/3	3/3	0/3
3/4 clock delay	0/3	0/3	3/3	3/3	3/3	3/3	3/3	3/3	0/3
7/8 clock delay	0/3	0/3	0/3	3/3	3/3	3/3	2/3	3/3	0/3
1 clock delay	0/3	0/3	0/3	0/3	3/3	3/3	3/3	3/3	0/3
9/8 clock delay	0/3	0/3	0/3	0/3	0/3	3/3	3/3	3/3	0/3
5/4 clock delay	0/3	0/3	0/3	0/3	0/3	0/3	2/3	3/3	0/3
11/8 clock delay	0/3	0/3	0/3	0/3	0/3	0/3	0/3	3/3	0/3
3/2 clock delay	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3
13/8 clock delay	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3
7/4 clock delay	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3
15/8 clock delay	0/3	3/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3
2 clock delay	0/3	3/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3
17/8 clock delay	0/3	3/3	3/3	3/3	0/3	0/3	0/3	0/3	0/3
9/4 clock delay	0/3	3/3	3/3	3/3	0/3	0/3	0/3	0/3	0/3
19/8 clock delay	0/3	3/3	3/3	3/3	3/3	3/3	0/3	0/3	0/3
5/2 clock delay	0/3	3/3	3/3	3/3	3/3	3/3	0/3	0/3	0/3

- Centering of clock scenario was re-run after finding the right ODT values

Generate optimized DDR configuration

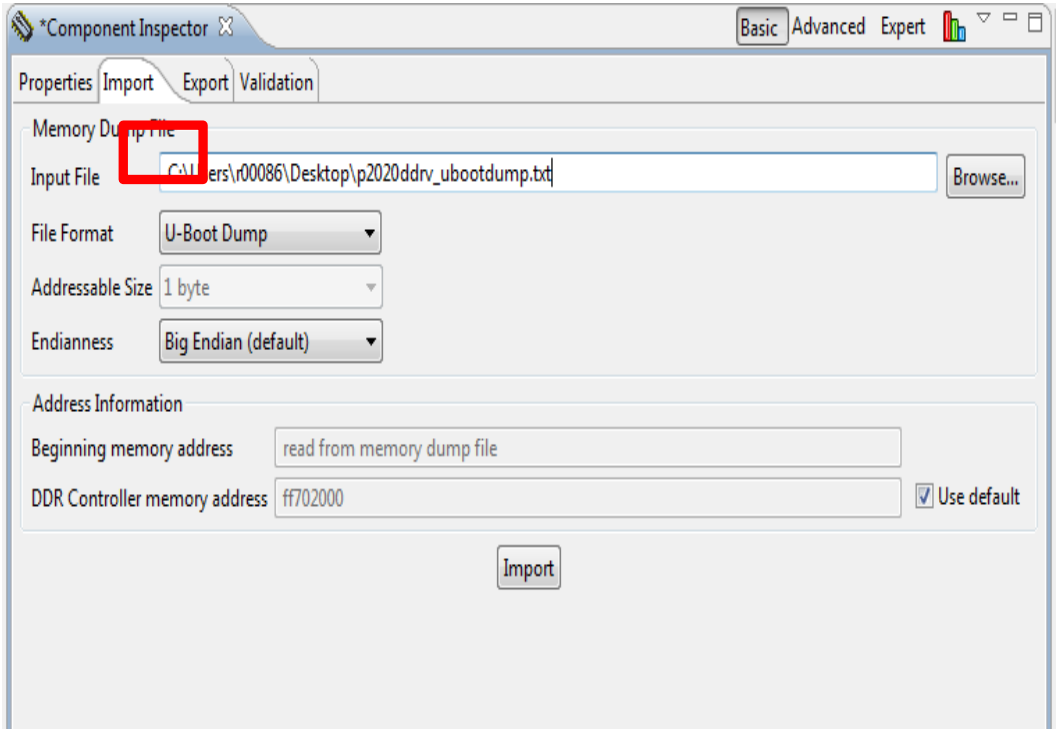


Pricing $995

License file:
<QCS Install directory>/eclipse/Optimization/license.dat

P2020RDB-PCA: Import DDR configuration from existing system running uboot

- At uboot prompt
- => md ffe02000
  - ffe02000: 0000003f 00000000 00000000 00000000 ...?.....
  - ffe02080: 80014202 00000000 00000000 00000000 ..B.....
  - ffe02100: 00030000 00110104 6f6b8846 0fa8c8cc .....ok.F....
  - ffe02110: c7000008 24401040 00441421 00000000 ....$@.@.D.!....
  - ffe02120: 00000000 0c300100 deadbeef 00000000 .....0.....
  - ffe02130: 03000000 00000000 00000000 00000000 .....
  - ffe02160: 00220001 02401400 00000000 00000000 ."...@.....
  - ffe02170: 89080600 8675f608 00000000 00000000 .....u.....
- => md ffe02b00
  - ffe02b00: 00000000 00000000 00000000 00000000 .....
  - ffe02b10: 00000000 00000000 00000000 00000000 .....
  - ffe02b20: 5dc07777 77000000 00000000 00000000].www.....
- Save content to a file.



Processor Expert for QorIQ … For More Info

- Freescale's Processor Expert landing page
  - http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=PROCESSOR-EXPERT&tid=PEH
  - http://www.freescale.com/**ProcessorExpert**
- QorIQ Configuration Suite
  - http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=PE_QORIQ_SUITE&tid=PEH
  - http://www.freescale.com/**QCS**
- QorIQ Optimization Suite
  - http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=PE_QORIQ_OPTI_SUITE&tid=PEH
  - http://www.freescale.com/**QOS**
- Freescale Component Store – purchasing embedded software
  - http://www.freescale.com/webapp/sps/site/homepage.jsp?code=BEAN_STORE_MAIN&tid=SWnT

Pricing & Availability

- Part numbers : CWA-QIQ-OPTP-FL (floating license) & CWA-QIQ-OPTP-NL (node locked)
- Price : $999 Annual Subscription
- License Duration : 1 year
- Support & Maintenance : Included
- Availability
  - Scenarios Tool – Now
  - DDRv – Now

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