Designing in the QorIQ T Series Product Family: Hardware Considerations

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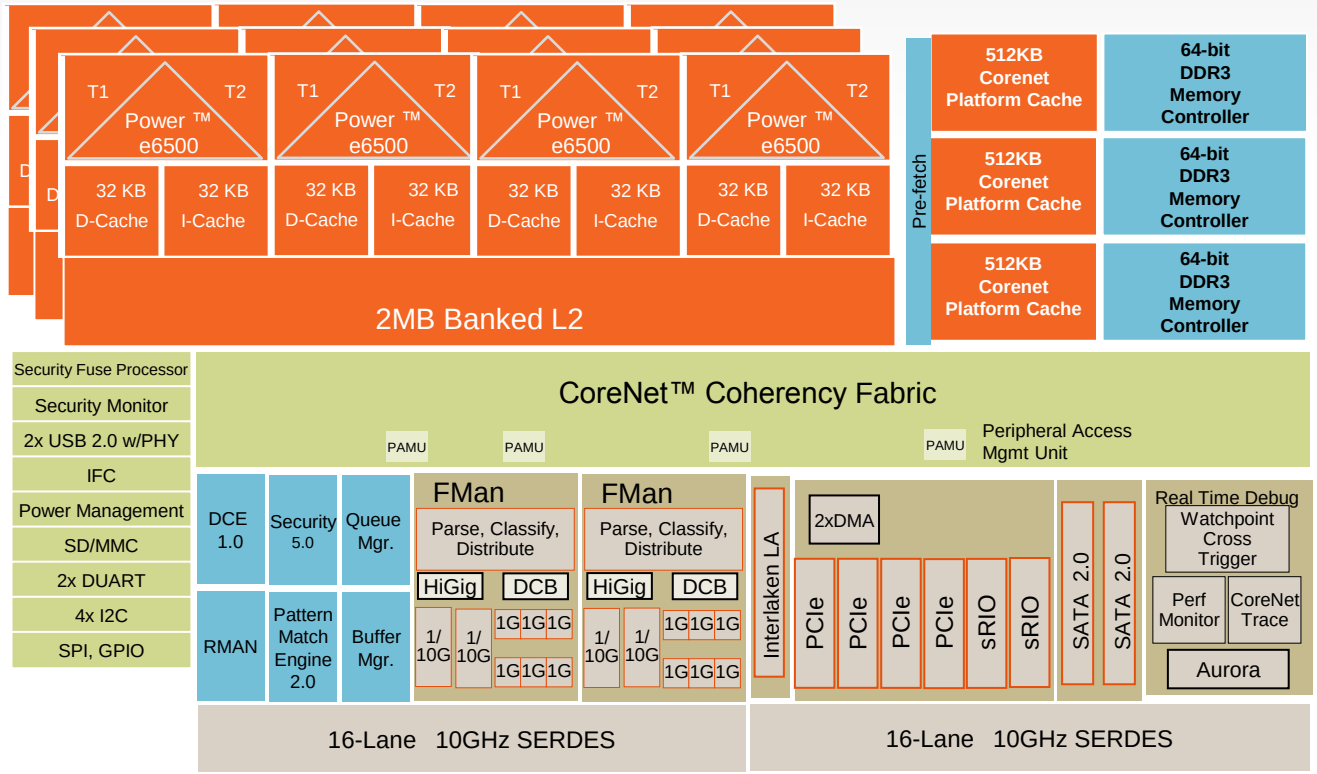
Opening

- This session will demonstrate some of the practical design aid tools from Freescale.
  - How to use the T4240 QorIQ Integrated Processor Design Checklist (AN4559)
  - How to setup and configure the T series device using the QorIQ Configuration suite
  - Initial board Power On/Validation steps

Design Checklist

- Power Design recommendation
- Power-on reset recommendations
- DDR controller recommendations
- IFC recommendations
- High-speed serial interfaces (HSSI) recommendations
- JTAG and Aurora configuration signals
- Thermal recommendations

T4240



Network IO

- 2 Frame Managers, each with:
  - Up to 25Gbps parse/classify/distribute
  - 2x10GE, 6x1GE
  - HiGig, Data Center Bridging Support
  - SGMII, QSGMII, XAUI, XFI

Processor

- 12x e6500, 64b, up to 1.8GHz
- Dual threaded, with128b AltiVec
- Arranged as 3 clusters of 4 CPUs, with 2MB L2 per cluster; 256KB per thread

Memory SubSystem

- 1.5MB CoreNet Platform Cache w/ECC
- 3x DDR3 Controllers up to 2.1GHz
- Each with up to 1TB addressability (40 bit physical addressing)
- HW Data Prefetching

CoreNet Switch Fabric

High Speed Serial IO

- 4x PCIe Controllers, Gen1.1/2.0/3.0
  - SR-IOV support
- 2x sRIO Controllers
  - Type 9 and 11 messaging
  - Interworking to DPAA via Rman
- 1 Interlaken Look-Aside at up to10GHz
- 2 SATA 2.0 3Gb/s
- 2 USB 2.0 with PHY
- **SEC**- crypto acceleration
- **PME-** Reg-ex Pattern Matcher
- **DCE-** Data Compression

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Defining the Problem

Requirements

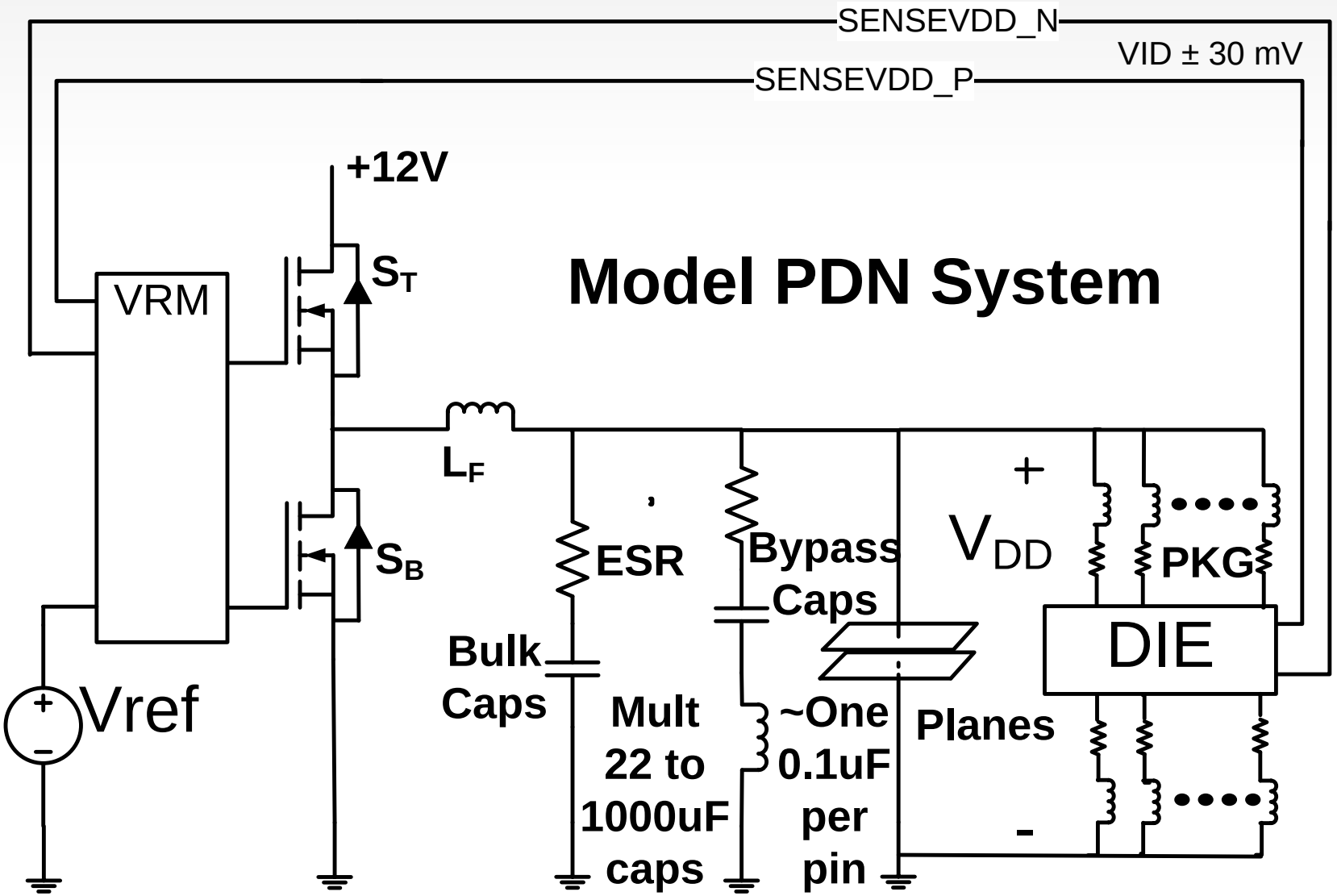
- Power Supply must supply a stable voltage reference
- Power Supply must distribute adequate current

Observations:

- Switching power supplies actually supply a digitally varying voltage (~500 KHz)
- Microprocessor's current demand may vary as fast as core frequency (~2GHz)
- Power Distribution Network (PDN) has resistance, capacitance, inductance, mutual capacitance, and mutual inductance through PCB, socket, vias, and capacitors.
- Changes in current at a particular frequency causes voltage changes at that frequency across these impedances.

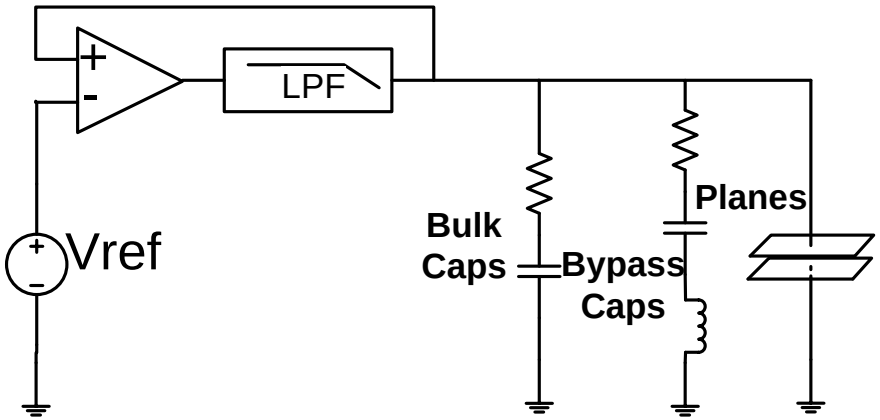
Problem:

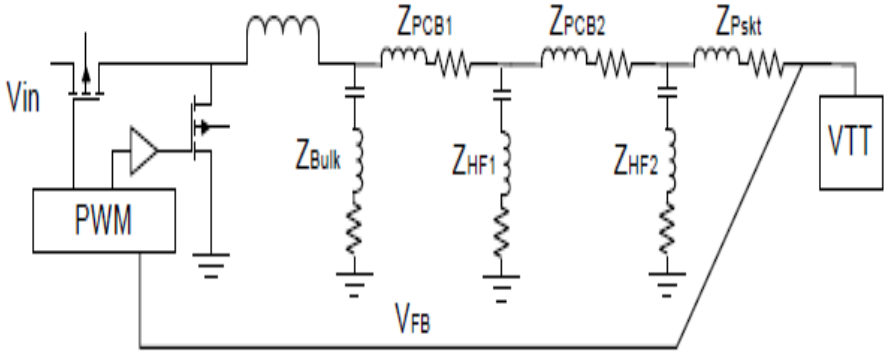
- **Silicon vendors are tightening the voltage specifications while the current continues to increase.**



Power Distribution System Theory – VRMs

- Voltage Regulator Modules (VRMs) use feedback to hold a constant supply voltage (up to the frequency of the inherent low pass filter).
- QorIQ parts allow feedback from the die voltage plane – SENSEVDD
- T4240QDS VRM (typical of most VRMs) advertises ±0.5% Closed-loop System Accuracy Over Load, Line and Temperature [for transients < 1/3 of switching frequency – 350kHz].

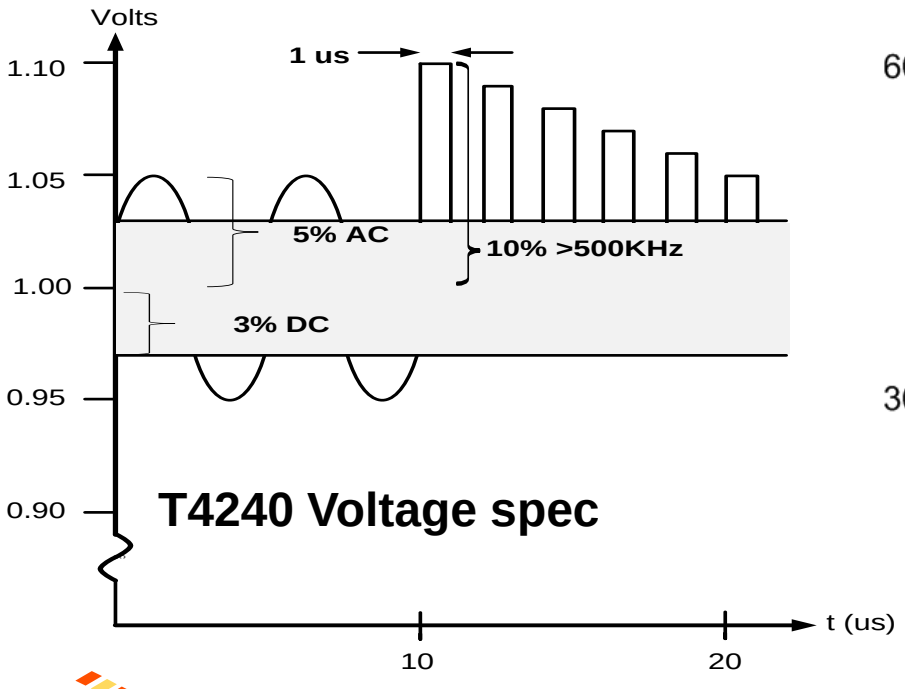




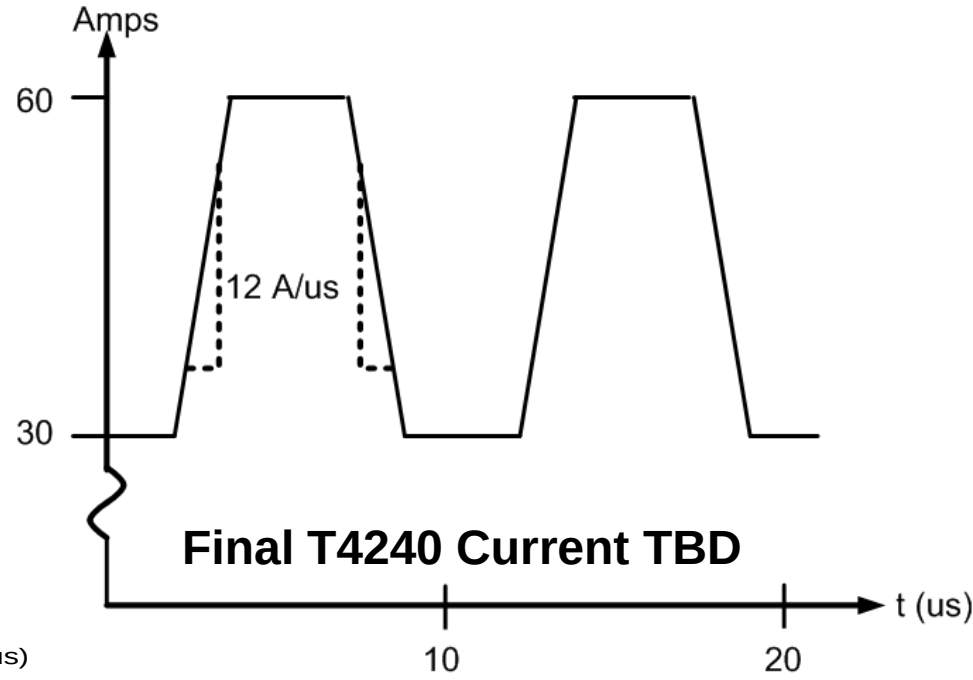
From Intel VRM 11.1

Original T4240 Voltage Specifications

- Core and Platform Supply Voltage – **VID** (or 1.05V boot up) **± 30 mV**
- Supply voltage measured at the voltage sense pins
- Combined DC and AC variance from nominal not to exceed ±50 mV except for an overshoot of less than +100 mV for less than 1 uS during transients. Transient voltages may result from current steps of up to 30A with slew rates of 12 A/us max.



T4240 Voltage spec



Final T4240 Current TBD

what is Voltage ID (VID) for 28nm Products?

- A specific method of selecting the optimum voltage-level to guarantee performance and power targets.
  - QorIQ device contains fuse block registers defining required voltage level. This EFUSE definition is accessed through the Fuse Status Register (DCFG_FUSESR).
  - Customer system must use the VID to change the voltage regulators in the system in a reliable and safe methodology.
- the general EFUSE definition.
  - A set of Fuses that determine the speed bin and voltage requirements for the device domains.
  - The range and steps are much more flexible than actually needed by manufacturing; only the fuses necessary to provide the required voltages will be implemented.

“Better” T4240 Voltage Specifications

- Core and Platform Supply Voltage – **VID** (or 1.05V bootup) **± 30 mV**
- Supply voltage measured at the voltage sense pins
- Combined DC and AC variance from nominal not to exceed ±30 mV except for an overshoot of less than +50 mV during transients. Transient voltages may result from current steps of up to 20A with slew rates of 12 A/us max.

WHAT THIS MEANS:

- Voltage regulator will boot up to 1.05V and then software should adjust VR to VID to comply with power specification.
- Voltage regulator is assumed to hold the DC Set Point – as measured at SENSE_VDD pins – to very small error (VID ±10 mV?)
- Switching voltage regulator ripple is suppressed to within a very small range (VID ±20 mV?)
- Load step transients are suppressed by capacitance to VID +50mV and VID -30mV. Overshoot is judged to be harder to suppress than undershoot. Overshoot is also less of a concern to the processor.
- Load step varies with program activity on the processor.

How to Check for Spec Compliance?

- Check VRMS value between SENSEVDD and SENSEGND with a True-RMS DMM.
- Check ripple and load step transients between SENSEVDD and SENSEGND with a differential probe and the oscilloscope set for 20MHz bandwidth offset and zoomed into a 20mV/DIV range…
- …while running your worst case application software.
- Measuring power-up current-step induced transients is not necessary because they are not likely to create program failure. Internal delays in enabling logic during power-up reduces the likelihood of that happening.

Power system-level recommendations

General Recommendation

- Ensure that VDD nominal voltage supply is set for 1.0 V with voltage tolerance of +/- 30 mV from the nominal VDD value.
- Ensure that all other power supplies have a voltage tolerance no greater than 5% from the nominal value
- Ensure the power supply is selected based on MAXIMUM power dissipation
- Ensure the thermal design is based on THERMAL power dissipation
- Ensure the power-up sequence is within 75 ms
- Ensure the PLL filter circuit is applied to AVDD_CGAn, AVDD_CGBn, AVDD_PLAT, AVDD_Dn.
- If SerDes is enabled, ensure the PLL filter circuit is applied to the respective AVDD_SDn_PLLn Otherwise, a filter is not required. Even if an entire SerDes module is not used, the power is still needed to the AVDD pins. However, instead of using a filter, it needs to be connected to the XVDD rail through a zero Ω resistor.
- Ensure the PLL filter circuits are placed as close to the respective AVDD_*SDn_PLLn* pins as possible.

Power system-level recommendations, continued

Power supply decoupling

- Provide sufficiently-sized power planes for the respective power rail.
- Use separate planes if possible; split (shared) planes if necessary. If split planes are used, ensure that signals on adjacent layers do not cross splits. Avoid splitting ground planes at all costs.
- Place at least one decoupling capacitor at each VDD, DVDD, OVDD, *GnVDD, LVDD, SnVDD*, and *XnVDD* pin of this chip.
- decoupling capacitors best if receive their power from separate VDD, DVDD, OVDD, *GnVDD, LVDD, SnVDD, XnVDD, and GND vias in the PCB, utilizing short traces to minimize inductance.*
- Ensure the board has at least one 0.1 µF SMT ceramic chip capacitor as close as possible to each supply ball of the chip (VDD, DVDD, OVDD, *GnVDD, LVDD*)
- Only use ceramic surface-mount technology (SMT) capacitors to minimize lead inductance, preferably 0402 or 0603.
- Distribute several bulk storage capacitors around the PCB, feeding (the VDD and other planes (for example, DVDD, OVDD, *GnVDD, LVDD, SnVDD, and XnVDD planes to enable quick recharging of the smaller chip capacitors.*
- Ensure the bulk capacitors have a low equivalent series-resistance (ESR) rating to ensure the quick response time necessary.
- Ensure the bulk capacitors are connected to the power and ground planes through two vias to minimize inductance.
- Ensure you work directly with your power regulator vendor for best values and types of bulk capacitors. The capacitors need to be selected to work well with the power supply to be able to handle the chip's power requirements.2 Most regulators perform best with a mix of ceramic and very low ESR Tantalum type capacitors.

Power system-level recommendations, continued

SerDes Power Supply Decoupling

- Use only SMT capacitors to minimize inductance.
- Connections from all capacitors to power and ground must be done with multiple vias to further reduce inductance.
- Ensure the board has at least one 0.1 µF SMT ceramic chip-capacitor as close as possible to each supply ball of the chip (*SnVDD, XnVDD*)
- Where the board has blind vias, ensure these capacitors are placed directly below the chip supply and ground connections.
- Where the board does not have blind vias, ensure these capacitors are placed in a ring around the chip as close to the supply and ground connections as possible.
- **For all SerDes supplies: Ensure there is a 1-µF ceramic chip capacitor on each side of the chip.**
- **For all SerDes supplies: Ensure there is a 10-nF, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100-µF, low ESR SMT tantalum chip capacitor between the device and any SerDes voltage regulator.**

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- JTAG and AURORA recommendations.
- Thermal recommendations

Introduction

- Various chip functions are initialized by sampling certain signals during the assertion of PORESET_B.
- These power-on reset (POR) inputs are pulled either high or low during this period.
- While these pins are generally output pins during normal operation, they are treated as inputs while PORESET_B is asserted.

Table 7. T4240 reset configuration signals

Reset configuration name	Functional interface	Functional Signal Name	Default
cfg_rcw_src[0:7]	IFC	IFC_AD[8:15]	1111 1111 [1]
cfg_rcw_src[8]	IFC	IFC_CLE	1 [1]
cfg_ifc_te	IFC	IFC_TE	1
cfg_dram_type	IFC	IFC_AD[21]	1
cfg_gpinput[0:7]	IFC	IFC_AD[0:7]	1111 1111
cfg_xvdd_sel	Power management	ASLEEP	1

Introduction – Cont'd

- What does PBL (Pre-boot Loader) do?
  - Device Configuration
  - Initialization before the core fetches instructions

- History

  Before PBL, how did we do these?

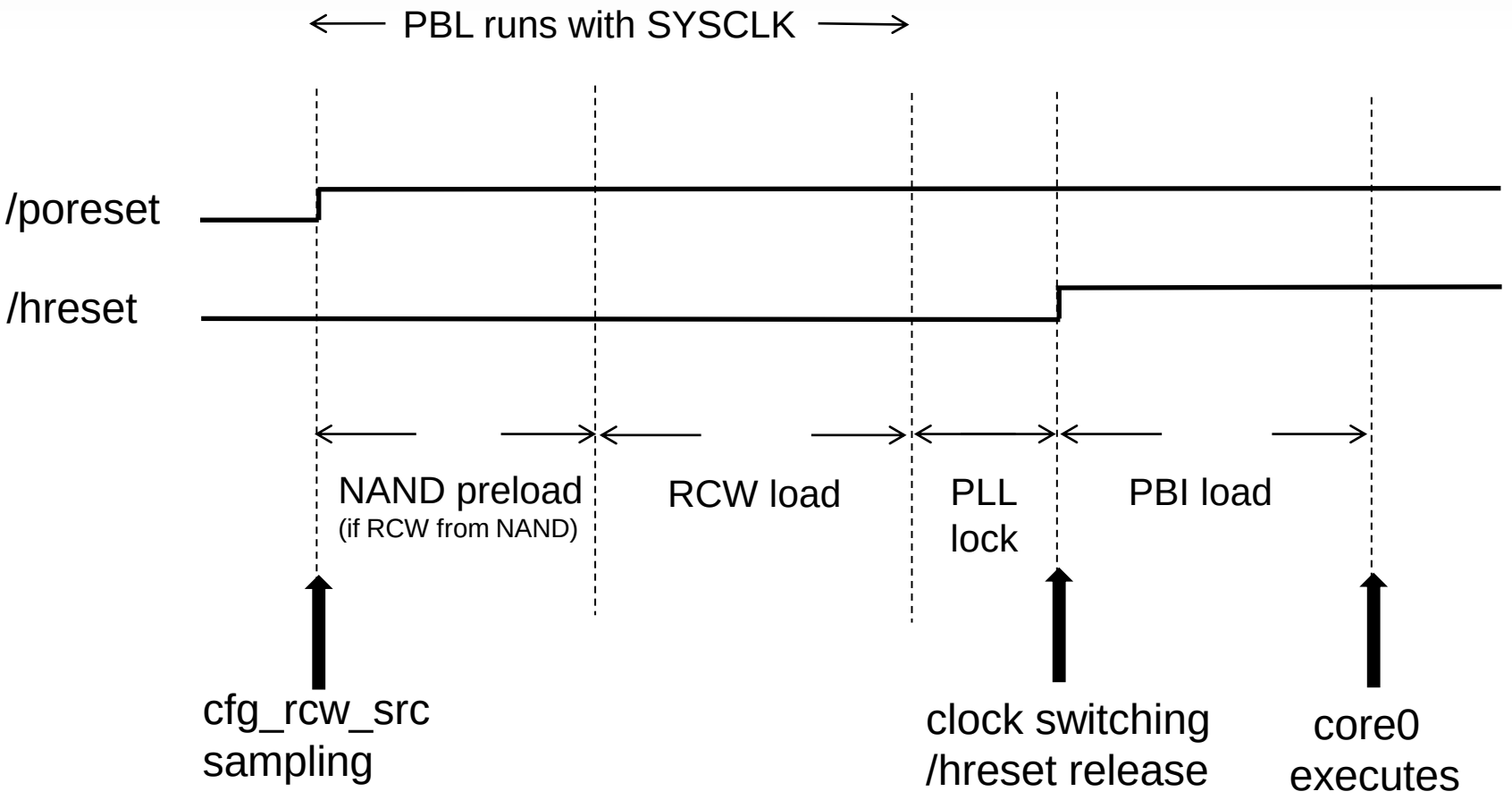
  MPC85xx etc
  - Device configuration

    Pins strapping
  - Initialization

    I2C Boot sequencer

- Improvements
  - Greatly reduce the number of pin strapping
  - Expand the sources of boot sequencer from I2C only to I2C, eSPI, eSDHC, NAND flash, NOR flash

PBL in the Power up sequence



Description of PBL functionality

- PBL PBI phase
  - PBL switches to platform clock.
  - PBL checks RCW[PBI_SRC].

    if PBI is disabled, then PBL is done.

    if PBI is enabled, proceed to fetch PBI data from the source.
  - PBL finishes the PBI, release the core0 to fetch instruction if RCW[BOOT_HO] is 0.

    The boot code location is specified in RCW[BOOT_LOC] for PowerPC device.

  - Error reports to DCFG_RSTRQPBLSR
  - For both RCW and PBI phase, if there is any error, the boot stops and /RESET_REQ is asserted

CFG_RCW_SRC(Device with eLBC)

It is pin strapping

RCW Source Location

Functional Signals	Reset Configuration Name	Value (Binary)	RCW Source
LGPL0/LFCLE, LGPL1/ LFALE, LGPL2/LOE/ LFRE, LGPL3/LFWP, LGPL5 Default (1_1111)	cfg_rcw_src[0:4]	0_0000	I^2C1 normal addressing (supports ROMs up to 256 bytes)
		0_0001	I^2C1 extended addressing
		0_0010	Reserved
		0_0011	Reserved
		0_0100	SPI 16-bit addressing
		0_0101	SPI 24-bit addressing
		0_0110	eSDHC
		0_0111	Reserved
		0_1000	eLBC FCM (NAND flash, 8-bit small page)
		0_1001	eLBC FCM (NAND flash, 8-bit large page)
		0_1010	Reserved
		0_1011	Reserved
		0_1100	eLBC GPCM (NOR flash, 8-bit)
		0_1101	eLBC GPCM (NOR flash, 16-bit)
		0_1110	Reserved
		0_1111	Reserved
		1_0000 - 1_1011	Hard-coded RCW options (See Hard Coded RCW Options, for more information.)
		1_1100 - 1_1111	Reserved

RCW (device with eLBC)

- 512-bits(64-bytes)

  Bits related to PBL or booting

  RCW[192:195] -- PBI_SRC

0000 I^2C1 normal addressing (up to 256 byte ROMs)

0001 I^2C1 extended addressing

0100 SPI 16-bit addressing

0101 SPI 24-bit addressing

0110 SD/MMC

1000 eLBC FCM 8-bit small page NAND Flash

1001 eLBC FCM 8-bit large page NAND Flash

1100 eLBC GPCM 8-bit

1101 eLBC GPCM 16-bit

1111 disabled

RCW (device with eLBC)

- RCW[196:200] -- BOOT_LOC

0_0000 PCIe1

0_0001 PCIe2

0_0010 PCIe3

0_1000 sRIO1

0_1001 sRIO2

1_0000 Memory complex 1

1_0001 Memory complex 2

1_0100 Interleaved memory complexes

1_1000 eLBC FCM 8-bit small page NAND Flash

1_1001 eLBC FCM 8-bit large page NAND Flash

1_1100 eLBC GPCM 8-tb

1_1101 eLBC GPCM 16-bit

Devices with IFC

- CFG_RCW_SRC[0:8] (based on T4240)

  it needs more bits to specify the IFC NOR/NAND options

  NOR: port size/address shift/AVD

  NAND: port size/page/block/BBI/ECC

  This is due to the difference between IFC and eLBC.

- If RCW/PBI is not from IFC, but BOOT_LOC is from IFC, then RCW[IFC_MODE] determines the IFC configuration

Restriction on CFG_RCW_SRC, PBI_SRC, BOOT_LOC

- RCW and pre-boot initialization data must be loaded from the same non-volatile memory device

  In the design, PBI_SRC is ignored. PBI is always loaded from CFG_RCW_SRC.

- At most, only one given IFC option can be used for CFG_RCW_SRC, PBI_SRC, and BOOT_LOC.

CFG_RCW_SRC	PBI_SRC	BOOT_LOC	
I2C	I2C	NAND or NOR	OK
eSPI	eSPI	NAND or NOR	OK
eSDHC	eSDHC	NAND or NOR	OK
NAND	NAND	NOR	No
I2C	eSPI	NAND or NOR	eSPI is ignored No error

PBL data format: RCW format

Required Format of Data Structure Consumed by PBL

	0	1	2	3	4	5	6	7
Preamble (required)	1	0	1	0	1	0	1	0
	0	1	0	1	0	1	0	1
	1	0	1	0	1	0	1	0
	0	1	0	1	0	1	0	1
RCW Data	ACS=0	BYTE_CNT = 000000 (64 bytes)						CONT=1
	SYS_ADDR[23-16][1]							
	SYS_ADDR[15-8][1]							
	SYS_ADDR[7-0][1]							
	BYTE0							
	BYTE1							
	BYTE2							
	.....							
	BYTE63							

A
5
A
5

R
C
W

PBL data format: PBI format

Address/Data pair, write(exception: PBL command)

	0	1	2	3	4	5	6	7
First Pre-Boot Initialization Command (optional)	ACS	BYTE_CNT						CONT=1
	SYS_ADDR[23-16]							
	SYS_ADDR[15-8]							
	SYS_ADDR[7-0]							
	BYTE0							
	BYTE1							
	BYTE2							
	.....							
	BYTE N-1 (up to 63)							
Second Pre-Boot Initialization Command (optional)	ACS	BYTE_CNT						CONT=1
	SYS_ADDR[23-16]							
	SYS_ADDR[15-8]							
	SYS_ADDR[7-0]							
	BYTE0							
	BYTE1							
	BYTE2							
	.....							
	BYTE N-1 (up to 63)							
.....								
.....								

End of PBL data structure

	0	1	2	3	4	5	6	7
End Command (required, special CRC Check command with CONT=0)	ACS=0	BYTE_CNT = 00100 (4 bytes)						CONT=0
	SYS_ADDR[23:16] = 0x13[2]							
	SYS_ADDR[15:8] = 0x80[2]							
	SYS_ADDR[7:0] = 0x40[2]							
	CRC0							
	CRC1							
	CRC2							
	CRC3							

- CONT=0, end command
- PBL reports 0x79(Invalid End command error) if it detects the followings:
    1. BYTE_CNT != 4
    2. ACS==1.
    3. For PowerPC based device, SYS_ADDR!=0x138040.

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DDR Controller Features

- The three fully programmable DDR SDRAM controllers support most JEDEC standard x4, x8, x16, or x32 DDR3/3L memories available.
- Support for DDR3/3L SDRAM
- Unbuffered and registered DIMMs are supported. However, mixing different memory types or unbuffered and registered DIMMs in the same system is not supported.
- Built-in error checking and correction (ECC) ensures very low bit-error rates for reliable high-frequency operation.
- 64-/72-bit SDRAM data bus, 32-/40-bit SDRAM for DDR3/3L
- As many as four physical banks (chip selects), each bank independently addressable
- 64-Mbit to 8-Gbit devices depending on internal device configuration with x4/x8/ x16/x32 data ports

DDR Controller Block Diagram

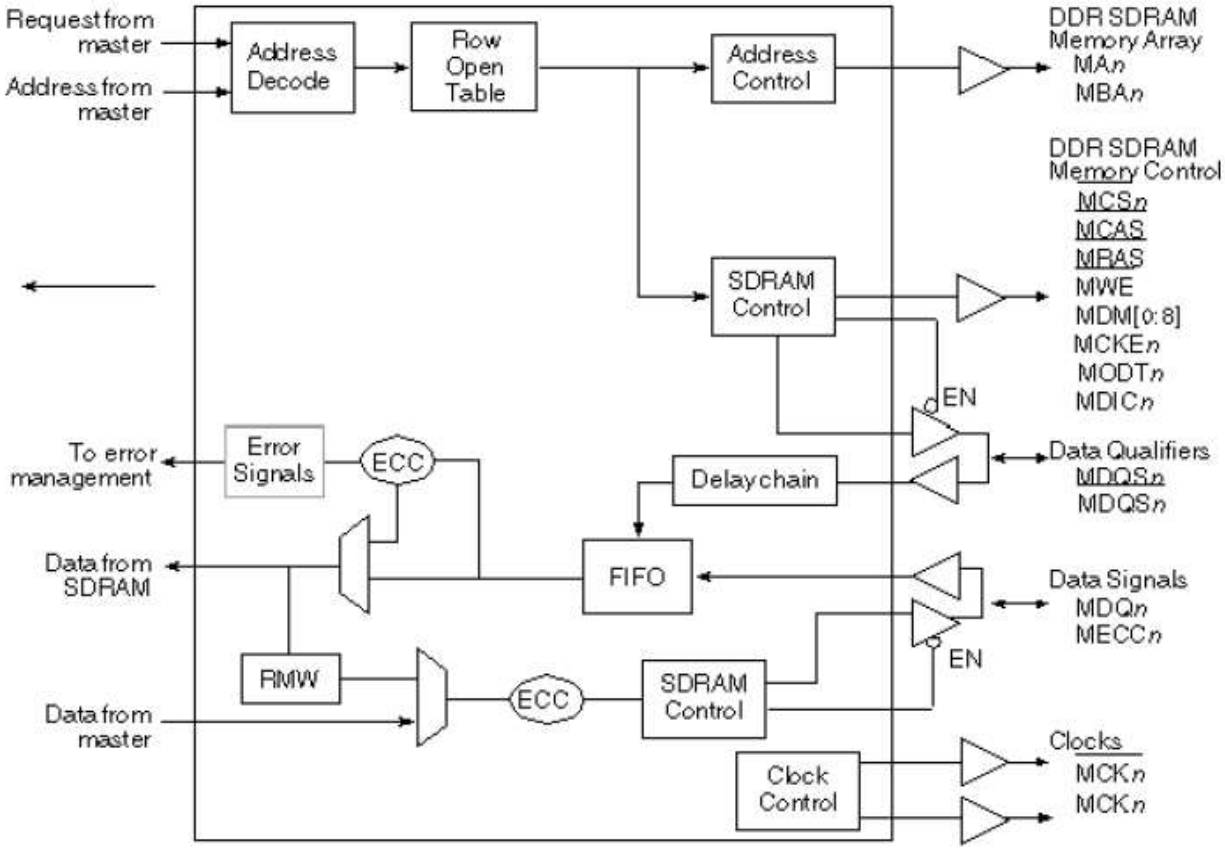
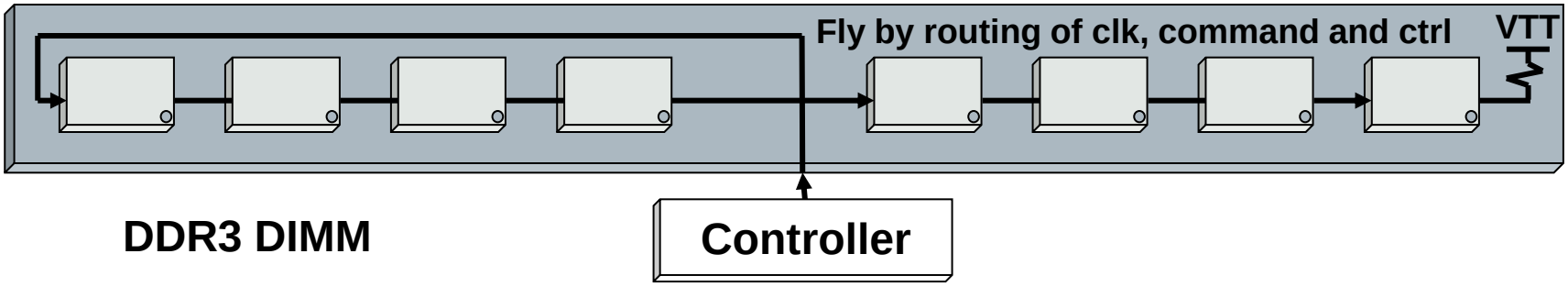


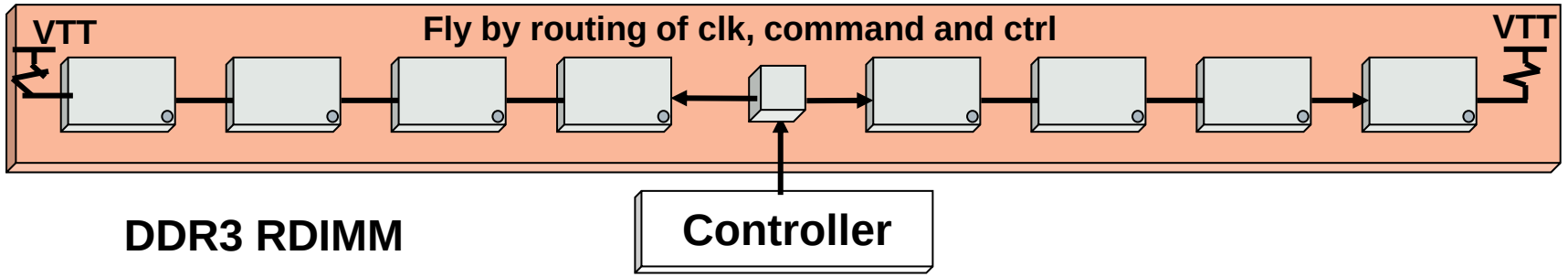
Figure 12-1. DDR Memory Controller Simplified Block Diagram

DDR2/DDR3/DDR3L Controller additional Features

- Partial array self refresh
- Address & command parity for Registered DIMM
- Independent driver impedance setting for data, address/command, and clock
- Synchronous & Asynchronous clock-in option
- Write-leveling for DDR3
- Automatic CPO
- Asynchronous RESET for DDR3
- Dynamic calibration
- Automatic ZQ calibration for DDR3
- Fixed or On-the-fly Burst chop mode for DDR3
- Mirrored DIMM supported

DDR3/3L RDIMM, unbuffered DIMM





HW Pitfalls

- Pitfall 1Noisy Vref: Care must be taken to isolate Vref
- Pitfall 2 No ECC. Without ECC it is very difficult to detect errors
- Pitfall 3 Ref Plane: ensure excellent reference plane for all DDR signals
- Pitfall 4 Proper Termination: Discrete implementations require term on address/command/control/clock.
- Pitfall 5 POR Config: Insure correct DDR type is selected
- Pitfall 6 Expandability: Hook up unused address lines
- Pitfall 7 Incorrect Topology: Insure use of JEDEC routing topologies. For DDR3 fly-by topology should be used.
- Pitfall 8 Separate VDDQ/VDDIO : VDDQ and VDDIO are common on DDR DIMM Modules, not on controller.
- Pitfall 9 Must review application note AN3940
- Pitfall 10 Design not simulated.

SW Pitfalls

- Pitfall 1 Auto CPO: Auto CPO settings not set
- Pitfall 2 ClK_adjust: Value not optimized
- Pitfall 3 Writelevel_START: Value is not centered
- Pitfall 4 Burst Length: incorrect or miss-matched burst length selection
- Pitfall 5 ODT: Incorrect ODT timing, value selection
- Pitfall 6 Errata: Incorrect or missing errata implementation
- Pitfall 7 DRAM Datasheet: Incorrect timing parameter selection
- Pitfall 8 bounds: Incorrect or mismatched BNDS register values with LAW registers.
- Pitfall 9 Mode register: incorrect or mismatched values in mode register with same setting in other registers.
- QCS DDRv not used: It generates & optimizes DDR registers to customer board.

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IFC Overview

- The integrated flash controller (IFC) is used to interface with external asynchronous NAND flash, asynchronous NOR flash, SRAM, generic ASIC memories, and EPROM
- Eight chip-selects to which a maximum of eight flash devices can be attached, although only one can be accessed at any given time.
- Supports error and debug registers
- Functional muxing of pins between NAND, NOR, and GPCM
- Supports memory banks of sizes up to 32 MB
- Write-protection capability (only for NAND and NOR)

System Must Talk to Flash Memory Without Any Configuration

- A system must be able to talk to non-volatile memory without any
- software configuration steps
- IFC is the controller that does this initial booting job
  - IFC has three controllers:
    - NOR controller
      - Standard and page mode NOR flash
      - **Support Booting**
    - NAND flash control machine (FCM)
      - NAND memory for storage
      - **Support Booting**
    - GPCM
      - Normal GPCM: Legacy, standard NOR flash
      - Generic ASIC: FPGA
      - No Booting

eLBC, IFC Comparison

Machine	Features	IFC	eLBC
NAND Flash	Support for ONFI 2.0	Yes	No
	Error correction	4 & 8 bit	1- bit
	Flexible timing control allows interfacing with proprietary NAND devices.	Yes	Limited capability
	Max page size	4KB	2KB
	Provide cache, copy-back and multi-plane command support	Yes	No
	Programmable command and data transfer sequences	Up to 15	Up to 8
	BBI page position	Configurable between (2nd and last page)	First two pages of each block
	Configurable block size constraint to multiple of 32 pages, up to 1024 pages	Yes	No
	Internal SRAM size	16KB	5KB
	Max boot block size for NAND flash	8KB	4KB
	SRAM access while NAND operation is on	Not-Allowed	Allowed

eLBC, IFC Comparison (Cont.)

Machine	Features	IFC	eLBC
NOR Flash	Compatible with latest NOR flash interface	Yes	No
	Support true Address Data Muxed devices	Yes	No
	Flexible timing control allows interfacing with variety of NOR devices	Yes	Limited capability
Other	UPM	No	Yes
	Write protection feature	Yes	Minimal support
	GASIC	Yes	No
	GPCM	Yes (with enhanced timing control)	Yes

NAND Flash Connections

- The NAND FCM provides a glueless interface to 8- or 16-bit parallel-bus NAND Flash EEPROM devices.
- The figure below shows a simple connection between an 8-bit port size NAND Flash EEPROM and the IFC. In NAND FCM mode, commands, address bytes, and data are all transferred on AD[0:7].

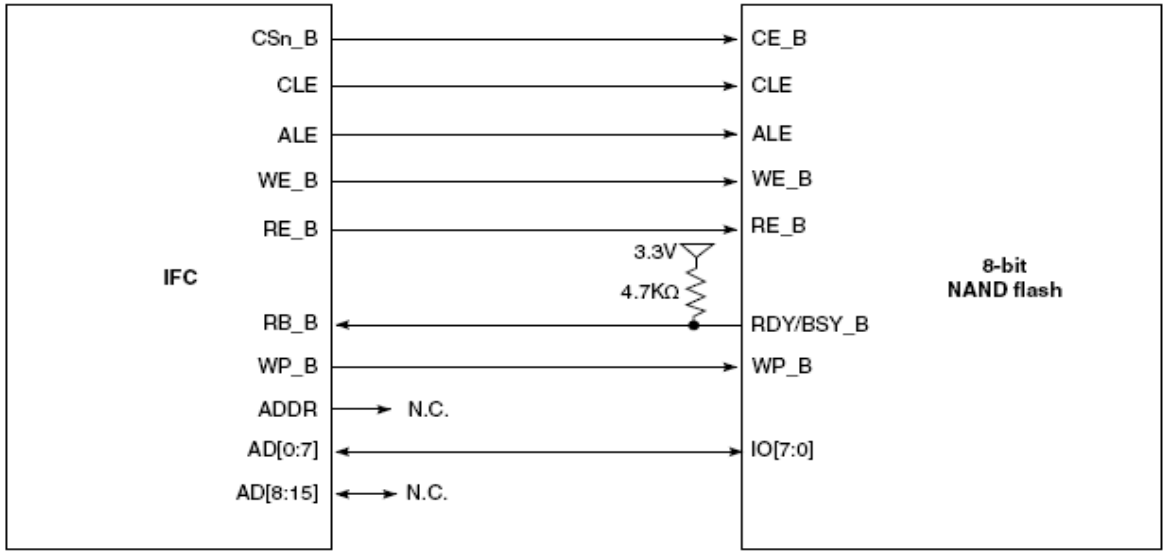


Figure 13-281. IFC to 8-bit asynchronous NAND device interface

NOR Flash Connections

- For 32-bit devices, ADDR[30:31] are irrelevant since these address bits are implicit in the byte lanes that carry data.
- If the bus width is 4 bytes, then ADDR[23:24] are don't cares and would not be connected

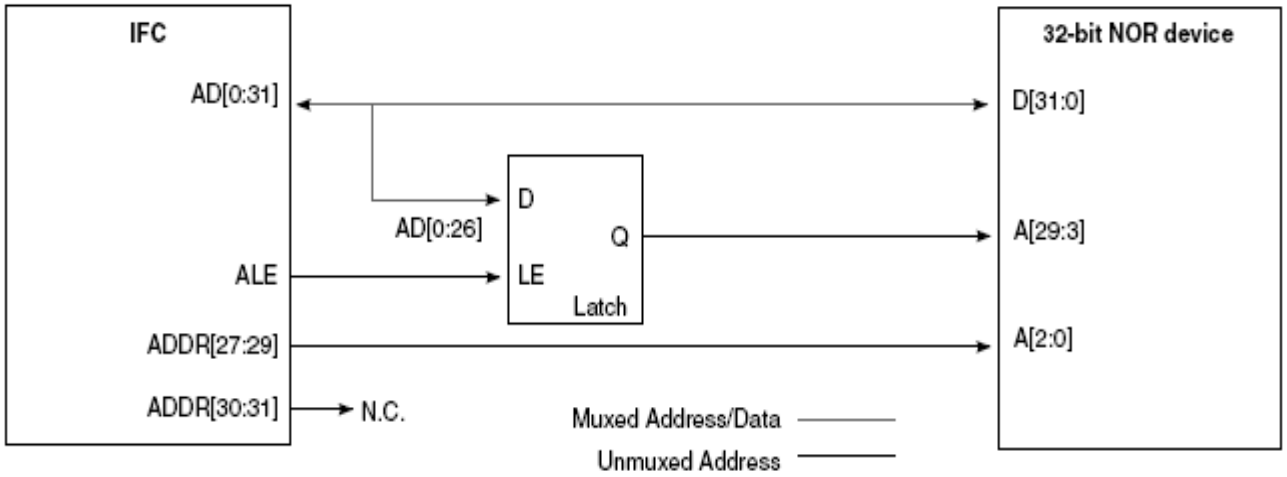


Figure 13-283. IFC to 32-bit NOR device interface

NOR Flash Connections – Cont'd

- Similarly, for 16-bit devices, ADDR[30] is used and ADDR[31] is irrelevant
- If the bus size is 2 bytes wide, then ADDR[24] is a don't care and would not be connected.

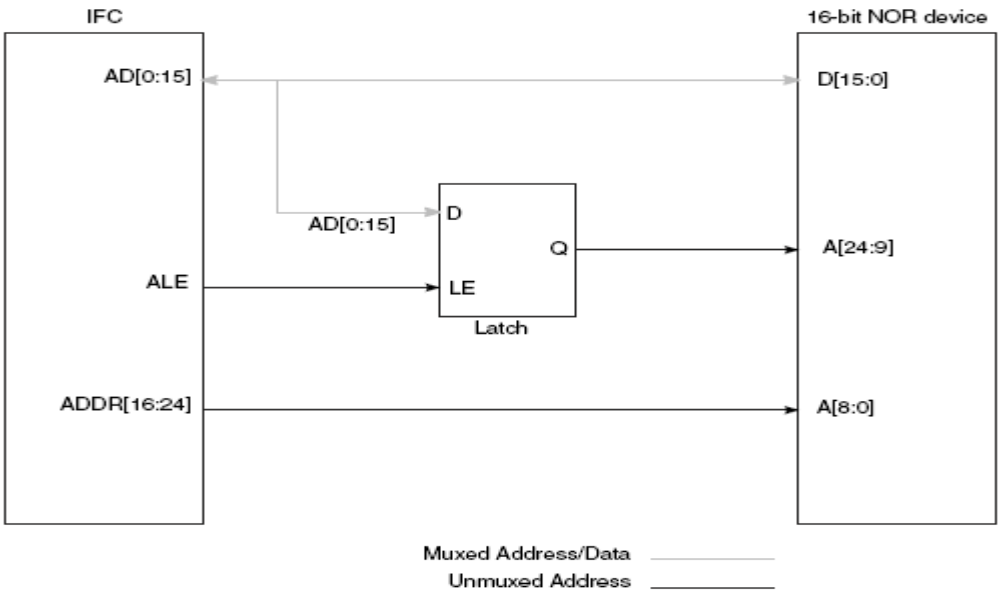


Figure 13-284. IFC to 16-bit NOR device interface

NOR Flash Connections – Cont'd

- for 8-bit devices, ADDR[30:31] are necessary.

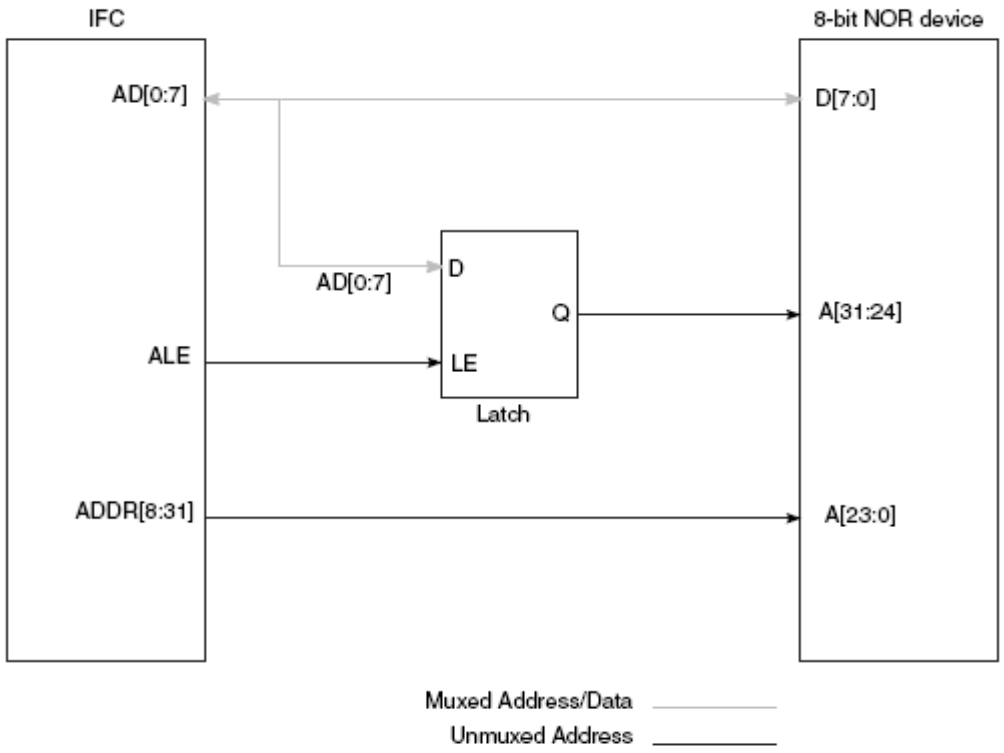


Figure 13-285. IFC to 8-bit NOR device interface

Generic ASIC

- A simple interface useful for talking to FPGA.
- IFC supports the following features on GASIC interface:
  - Support for x8-/16-bit device
  - Address and Data are shared on AD I/O bus. Dedicated address pins are not used
  - Following Address and Data sequences will be supported on I/O bus
    - 16-bit I/O: AADD
    - 8-bit I/O : AAAADDDD
  - Configurable Even/Odd Parity on Address/Data bus supported
  - Parity Error detection supported.

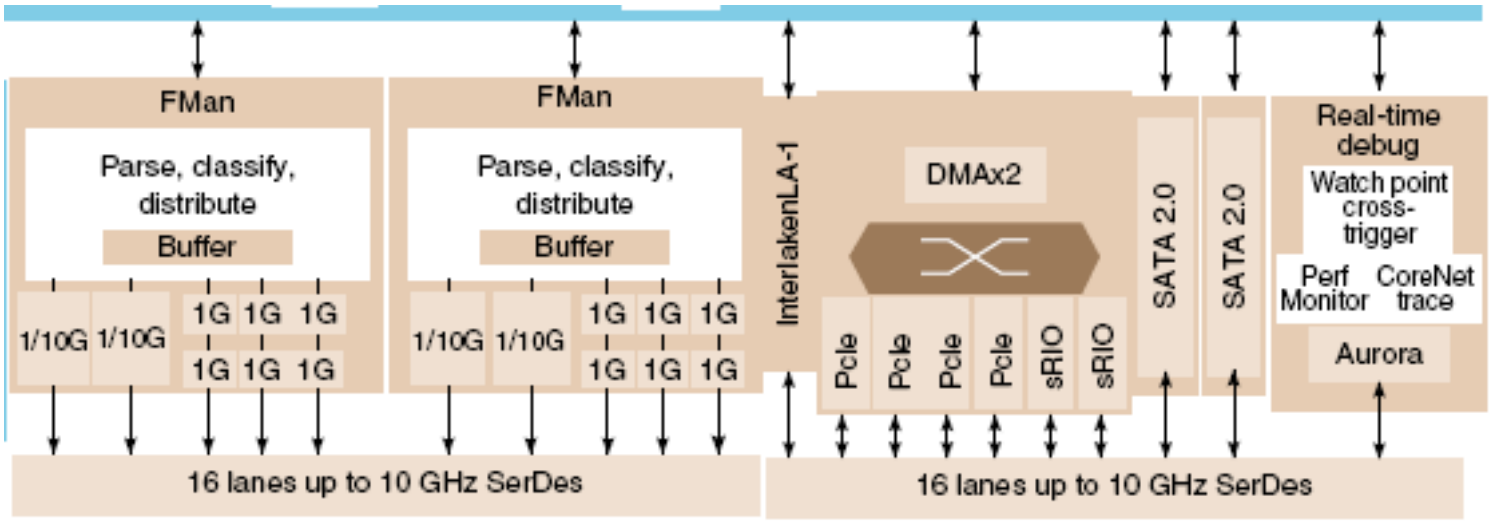
- GASIC interface does not support:
  - Boot from GASIC not supported
  - Burst transaction not supported

Design Checklist

- Power Design recommendation
- Power-on reset recommendations
- DDR controller recommendations
- IFC recommendations
- High-speed serial interfaces (HSSI) recommendations
- JTAG and Aurora configuration signals
- Thermal recommendations

Introduction

- The SerDes module implements link serialization/deserialization and PCS functions for high speed serial interfaces from 1.25 Gbaud to 10.3125 Gbaud.
- Each SerDes module (4 modules) includes eight data lanes and two PLLs



External Signals Description

Table 19-1. SerDes Interface Signals

Pin Name	Description	No. of Signals	I/O
SDn_TX_P[0:7]	Transmitter serial output, positive data	8	O
SDn_TX_N[0:7]	Transmitter serial output, negative data	8	O
SDn_IMP_CAL_TX	Tx Impedance Calibration	1	I
SDn_RX_P[0:7]	Receiver serial output, positive data	8	I
SDn_RX_N[0:7]	Receiver serial output, negative data	8	I
SDn_IMP_CAL_RX	Rx Impedance Calibration	1	I
x=1, 2			
SDn_REFx_CLK_P	Reference clock input to PLL*x*	1	I
SDn_REFx_CLK_N	Reference clock-bar input to PLL*x*	1	I

Misc SerDes Pin Termination

- The following table highlights a few miscellaneous pins used for calibration and test. Refer to section 8.1 of AN4559 for complete pin recommendations.

8.1 SerDes pin termination recommendations

Table 36. SerDes pin termination checklist[1, 2, 3]

Signal name	I/O type	Used	Not used	Completed
SD*n*_IMP_CAL_TX	I	Tie to X*n*V_{DD} through a 698 Ω 1% resistor.	If the SerDes interface is entirely unused, the unused pin must be left unconnected	
SD*n*_IMP_CAL_RX	I	Tie to S*n*V_{DD} through a 200 Ω 1% resistor.	If the SerDes interface is entirely unused, the unused pin must be left unconnected	
SD*n*_PLL*m*_TPA	O	Do not connect. This pin should be left floating		
SD*n*_PLL*m*_TPD	O	Do not connect. This pin should be left floating		

Networking Protocols (SerDes 1 and SerDes 2)

- **SerDes 1 and SerDes 2 support networking protocols and interconnect with the two Frame Managers supporting the following network protocols**

  - SGMII @ 1.25, 3.125 Gbaud:
  - XAUI @ 3.125 Gbaud:
  - HiGig/HiGig2 @ 3.125, 3.75 Gbaud:
  - QSGMII @ 5 Gbaud:
  - XFI/10GBASE-R and 10GBASE-KR @ 10.3125 Gbaud

Non-Networking Protocols (SerDes 3 and SerDes 4)

- **SerDes 3 and SerDes 4 support non-networking protocols and interconnect with the PEX, SRIO, Interlaken, SATA and Aurora controllers.**
- x1, x2, x4 or x8 PCI Express @ 2.5, 5, 8 Gbaud: SerDes instances 3 and 4
  - Note: 8 Gbaud is not supported with x8 link width, and is restricted in other configurations. See Section 19.4, “SerDes Lane Assignments and Multiplexing,” for details on the supported configurations for PEX gen3.
- x2 or x4 Serial RapidIO @ 2.5, 3.125, 5 Gbaud: SerDes instance 3 and 4
- Aurora @ 2.5, 3.125, 5 Gbaud: SerDes instance 4
- x4, x8 Interlaken-LA @6.25, 10.3125 Gbaud: SerDes instance 3
- SATA @ 1.5, 3 Gbaud: SerDes instance 4

Recommendations

- IBIS-AMI Modeling can continue to provide a highly portable, fast, efficient and accurate means to model High Speed SERDES devices.
- High Speed SERDES devices use forms of equalization at the transmitter (TX) and receiver (RX) to enable the bus to run at 5-10 Gbps.
- These forms of equalization can be modeled in IBIS-AMI to provide the models that can run in multiple simulators.
- Ask you local FAE or Sales Account Manager to provide models.
- For any unused SerDes lines it is recommended to power down those lines via RCW programming.

Design Checklist

- Power Design recommendation
- Power-on reset recommendations
- DDR controller recommendations
- IFC recommendations
- High-speed serial interfaces (HSSI) recommendations
- JTAG and Aurora configuration signals
- Thermal recommendations

Introduction

- TheT4240 provides two paths for connection to the cores; legacy JTAG and high speed Aurora.
- Aurora provides access to other chip functions and provides visibility for system debug as well as statistics and performance monitoring.
- If the Aurora interface is used or not used, Freescale recommends the legacy COP header be designed into the system for JTAG debug.

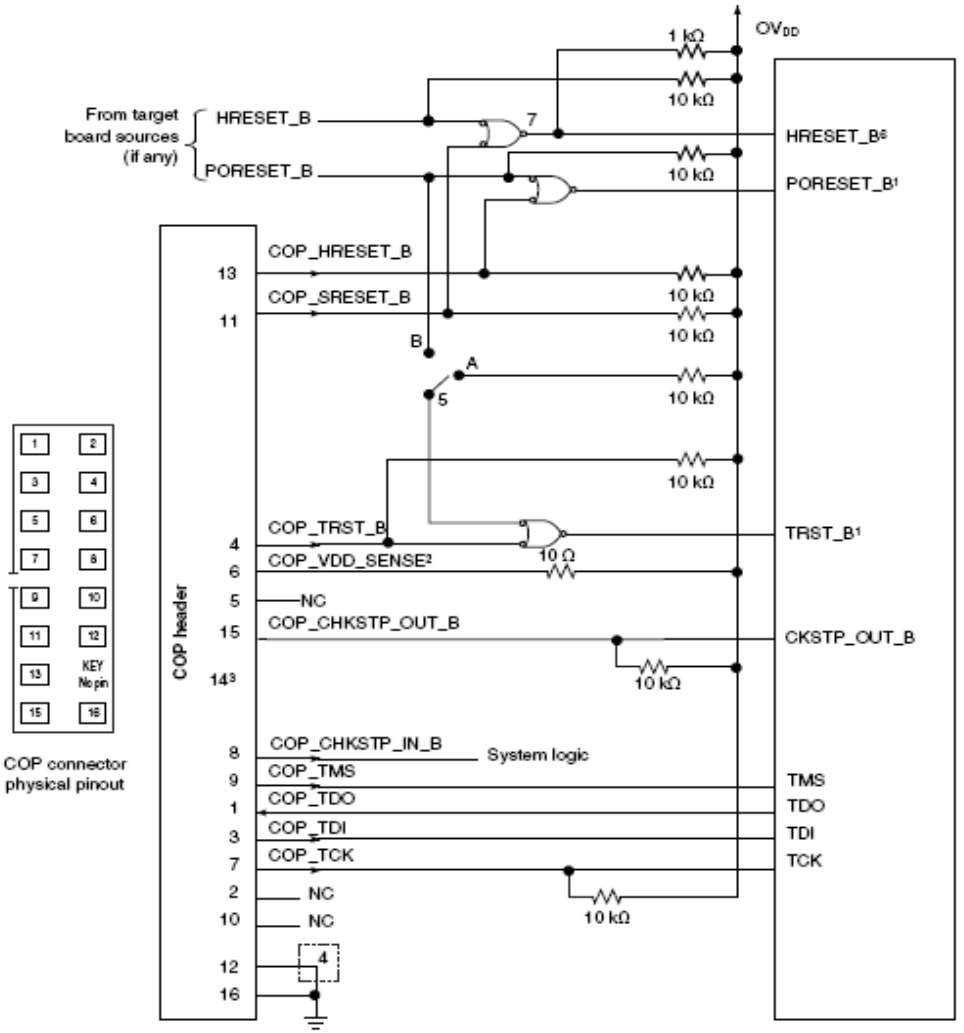
Legacy JTAG configuration

- Correct operation of the JTAG interface requires configuration of a group of system control pins.
- Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.
- The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor.
- The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals.
- The COP port requires the ability to independently assert PORESET_B or TRST_B in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

Legacy JTAG Interface Connection

Notes:

1. The COP port and target board should be able to independently assert PORESET_B and TRST_B to the processor in order to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a no-connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the TRST_B line. If BSDL testing is not being performed, this switch should be closed to position B.
6. Asserting HRESET_B causes a hard reset on the device
7. This is an open-drain output gate.



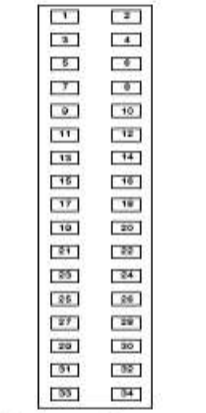
Aurora Interface

- Correct operation of the Aurora interface requires configuration of a group of system control pins
- Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.
- Freescale recommends that the Aurora 34 pin duplex connector be designed into the system or the 70 pin duplex connector be designed into the system

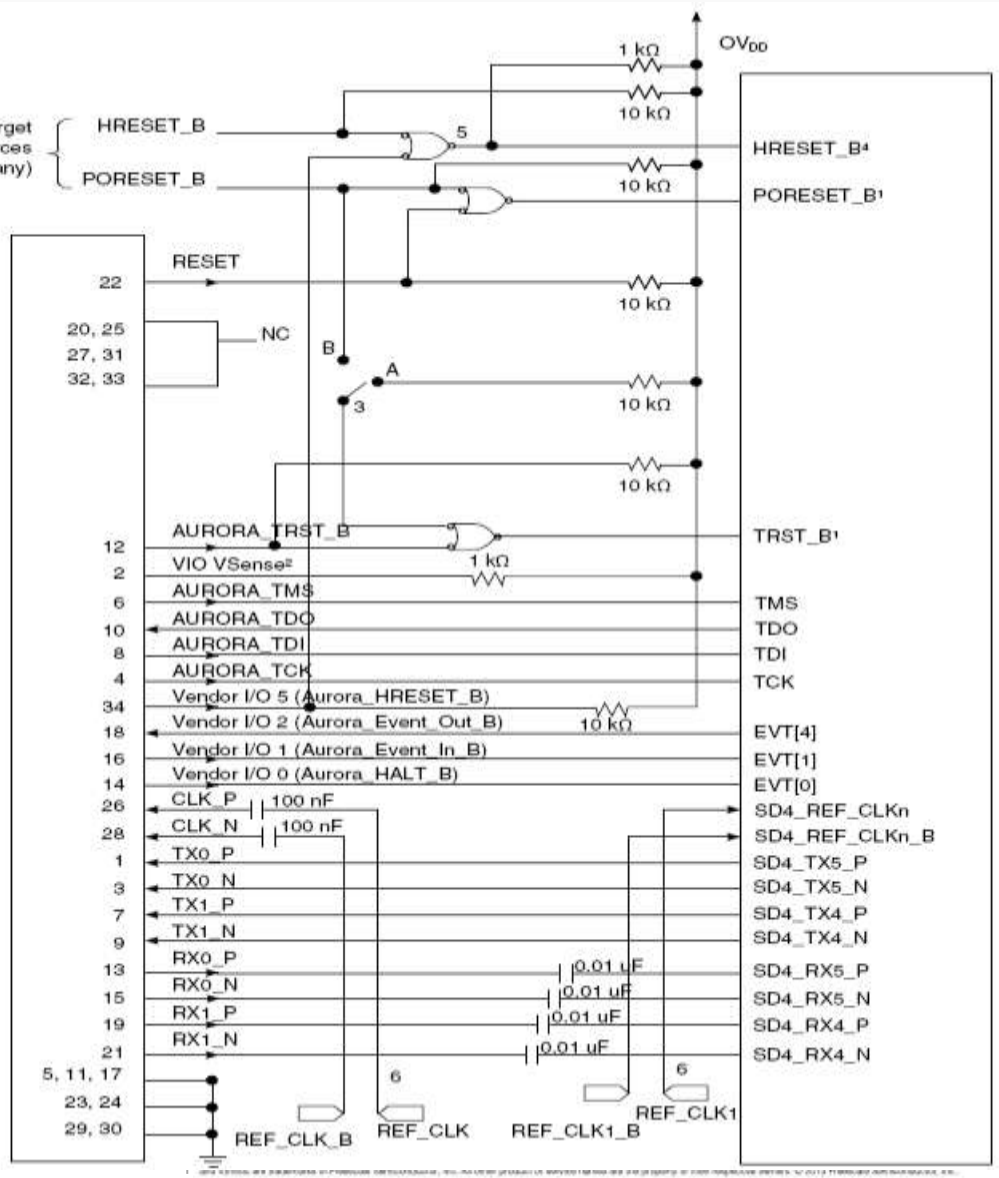
Aurora 34 pin connector duplex interface connection

Notes:

1. The Aurora port and target board should be able to independently assert PORESET_B and TRST_B to the processor in order to fully control the processor as shown here.
2. Populate this with a 1 kΩ resistor for short-circuit/current-limiting protection.
3. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the TRST_B line. If BSDL testing is not being performed, this switch should be closed to position B.
4. Asserting HRESET_B causes a hard reset on the device
5. This is an open-drain output gate.
6. REF_CLK/REF_CLK_B and REF_CLK1/REFCLK1_B are buffered clocks from the same common source.



Duplex 34 Connector Physical Pinout

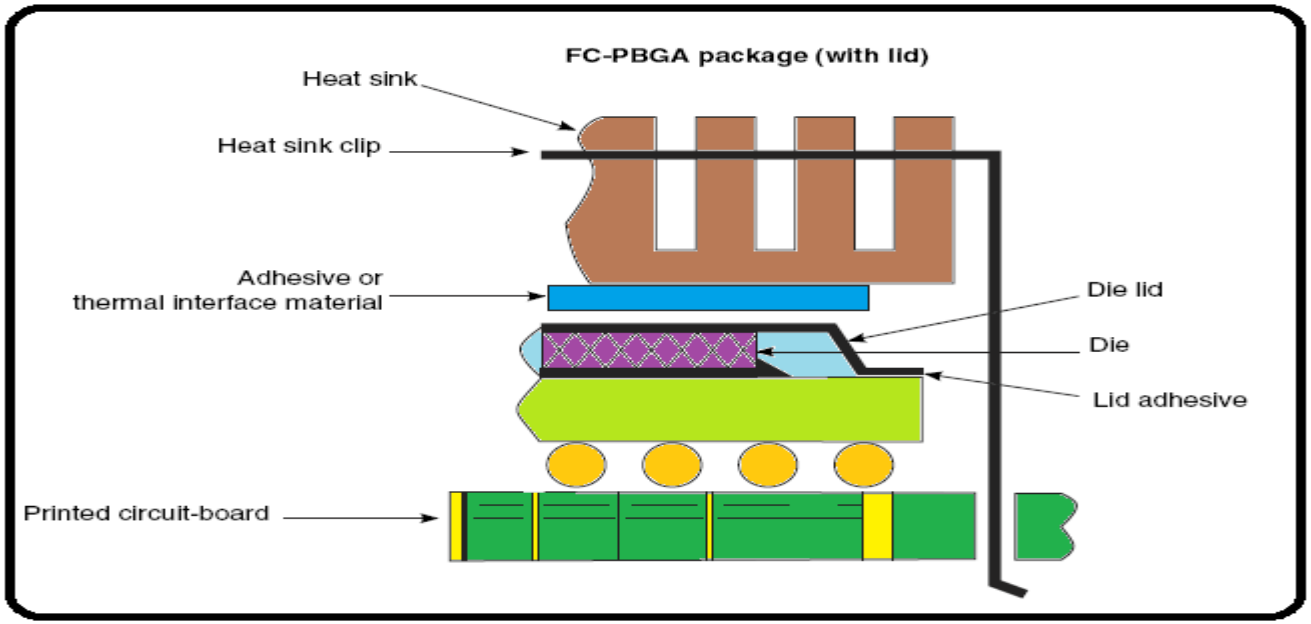


Design Checklist

- Power Design recommendation
- Power-on reset recommendations
- DDR controller recommendations
- IFC recommendations
- High-speed serial interfaces (HSSI) recommendations
- JTAG and Aurora configuration signals
- Thermal recommendations

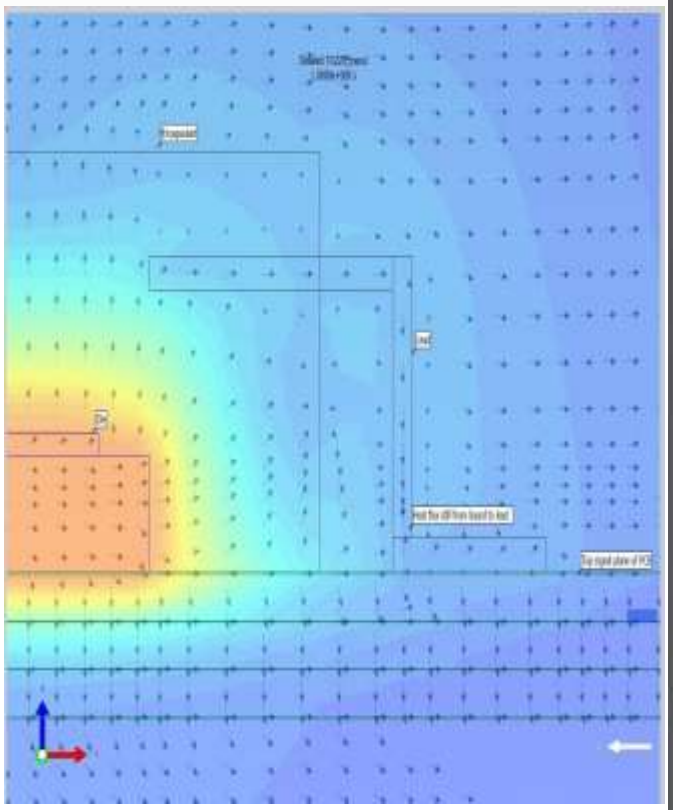
Thermal recommendations

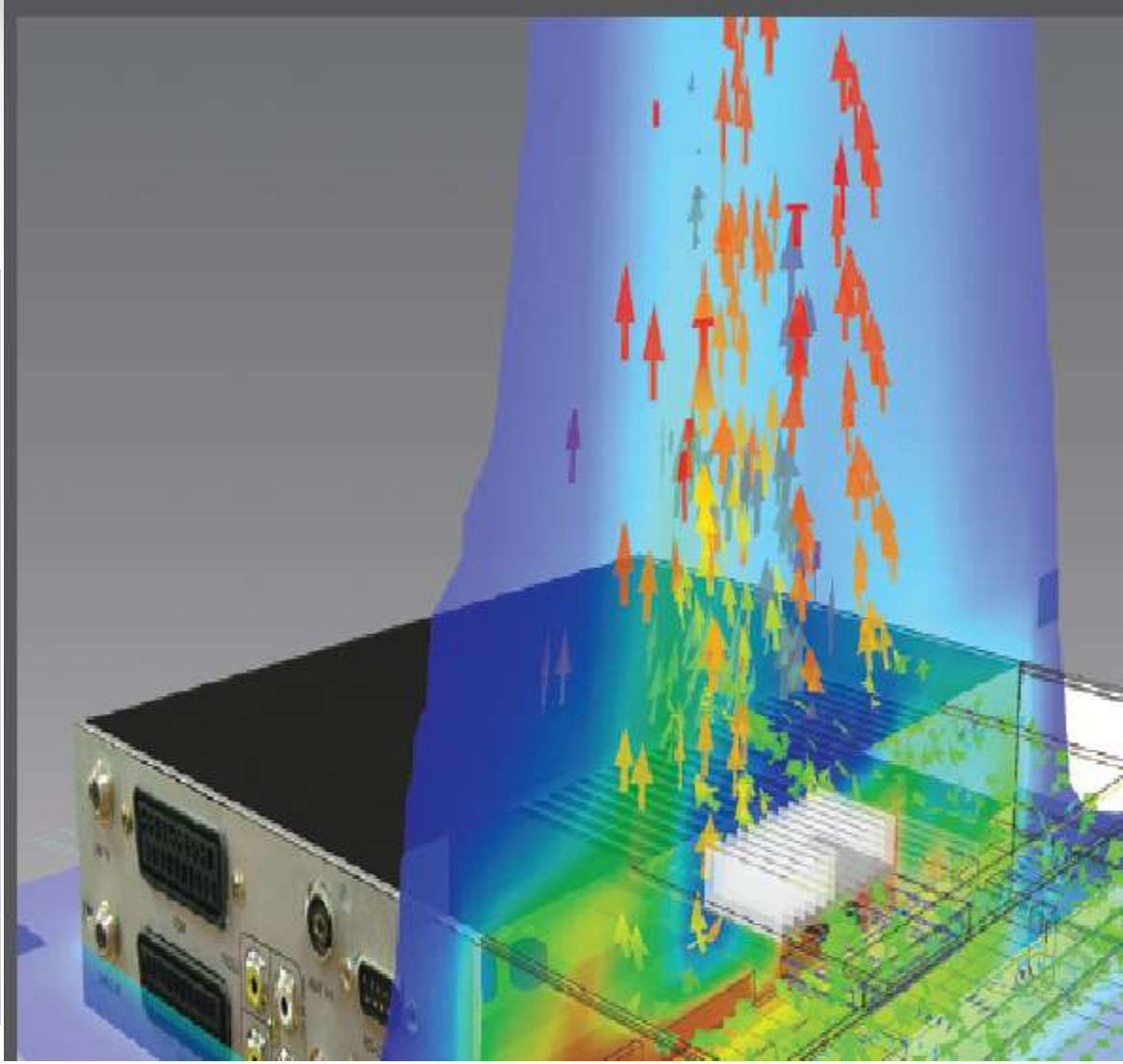
- Proper thermal control design is primarily dependent on the system level design-the heat sink, airflow and thermal interface material.
- Use the recommended thermal model, can be obtained from your local Freescale sales office.
- Use this recommended board attachment method to the heat sink



Thermal recommendations, continued

- Ensure the heat sink is attached to the printed-circuit board with the spring force centered over the package.
- the final selection of an appropriate heat sink depends on factors such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly and cost.
- Ensure the spring force does not exceed 10 pounds force
- A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance
- Ensure the method of mounting heat sinks on the package is by means of a spring clip attachment to the printed-circuit board.
- A thermal simulation is required to determine the performance in the application.





The Flotherm library files of the parts have a dense grid to accurately capture the laminar boundary layer for flow over the part in standard JEDEC environments, as well as the heat spreading in the board under the package.

Processor Expert Software

QorIQ Configuration Suite

Why QorIQ Configuration Suite?

- Configuration of QorIQ processors is increasing in complexity
  - Even more complexity is around the corner
  - We support many, many configuration settings
- Reference manuals are huge and intimidating to new customers
- Configuration problems during board bring-up are HARD and COSTLY
- Learning command line tools requires more training, etc.

- **Solution/Strategy to solve these problems:**
  - **Extensible suite of tools with a common user interface**
  - Consolidate into a common tools framework (Processor Expert)
  - Provide new device support aligned with silicon roadmap
  - Add more configuration tools over time
  - Allow customers to add their own configuration tools to extend what we offer …

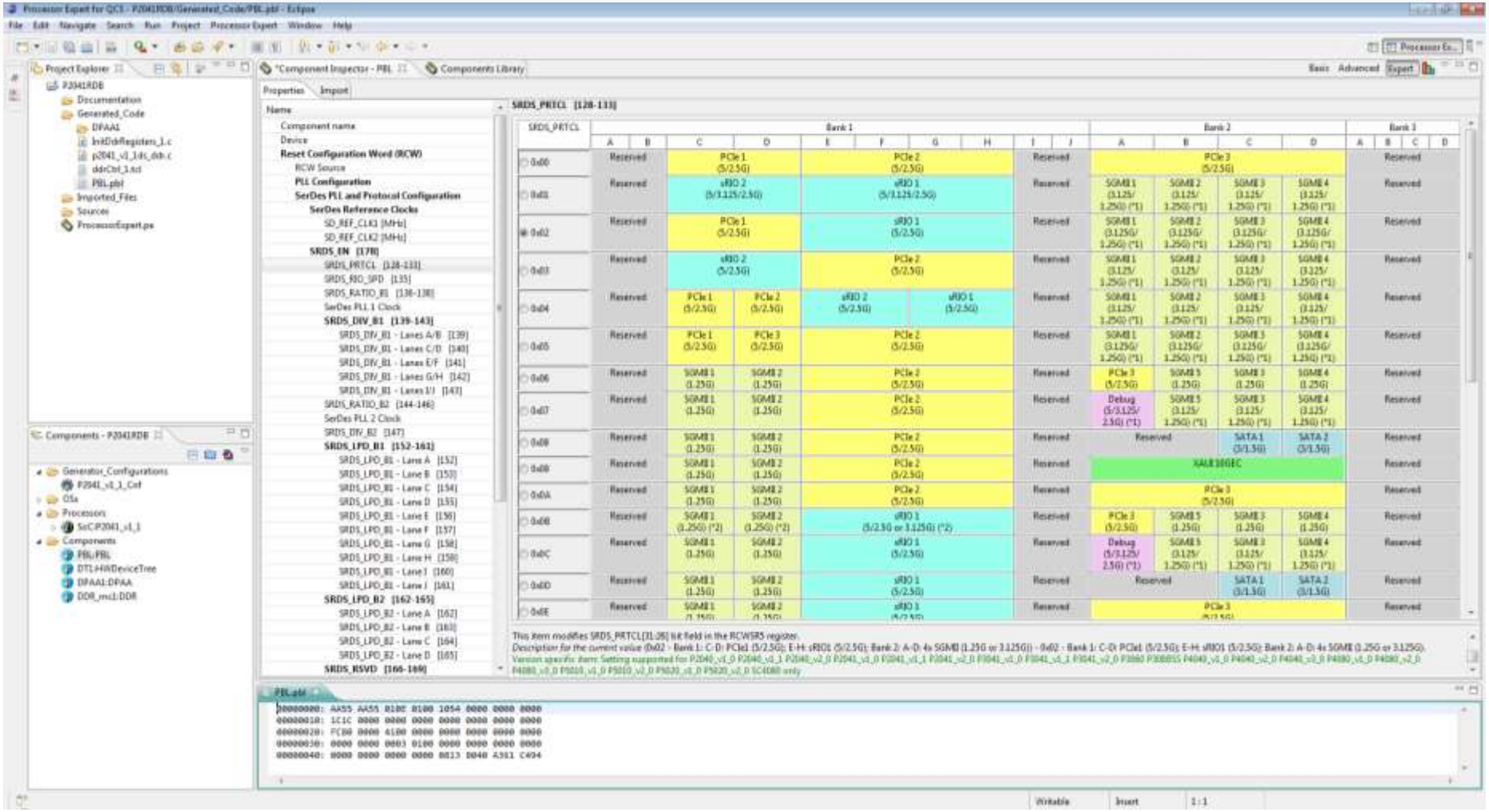
QorIQ Configuration Suite – Now Available!

- **QorIQ Configuration Suite v3.0.x is NOW AVAILABLE!!!**
  - Supports all QorIQ and Qorivva devices
  - Works with Eclipse 3.6, Eclipse 3.7, Eclipse 4.2 development tools
    - Pure Java solution for maximum choice of host system support
    - Add-in to CodeWarrior Development Studio for PA, v10.1 or later
  - Available from www.freescale.com/QCS – FREE DOWNLOAD*
- **Includes the following configuration tools all designed to collaborate on consistent configuration:**
  - PBL tool to define the Reset Control Word bit values and PBI data for the pre-boot
  - BOOTROM generator for those QorIQ without RCW functionality
  - DDR configuration supports setting the controller to a working state for any DDR
  - Data path graphical view helps to define data path configuration for the DPAA.
  - Hardware Device Tree editor supports references, synchronous GUI and XML editing, node validation based on specification bindings
  - Packaged as a separate product with installer and wizard functionality

* Must be a QorIQ customer or under QorIQ NDA for download permission

Actual URL is http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=PE_QORIQ_SUITE&tid=PEH

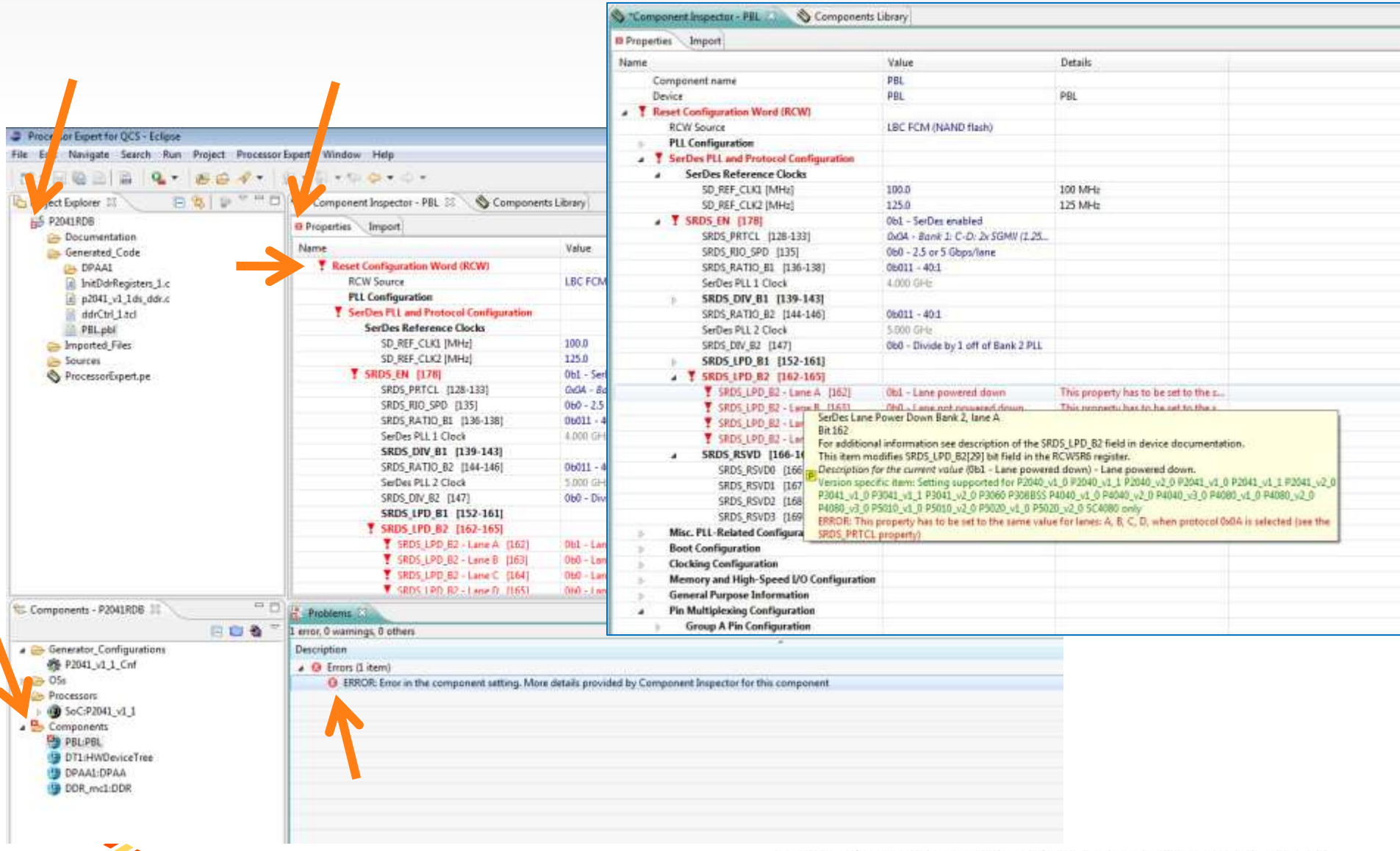
Processor Expert for QorIQ – Configuration Suite



Pre-boot Loader

RCW Configuration Tool

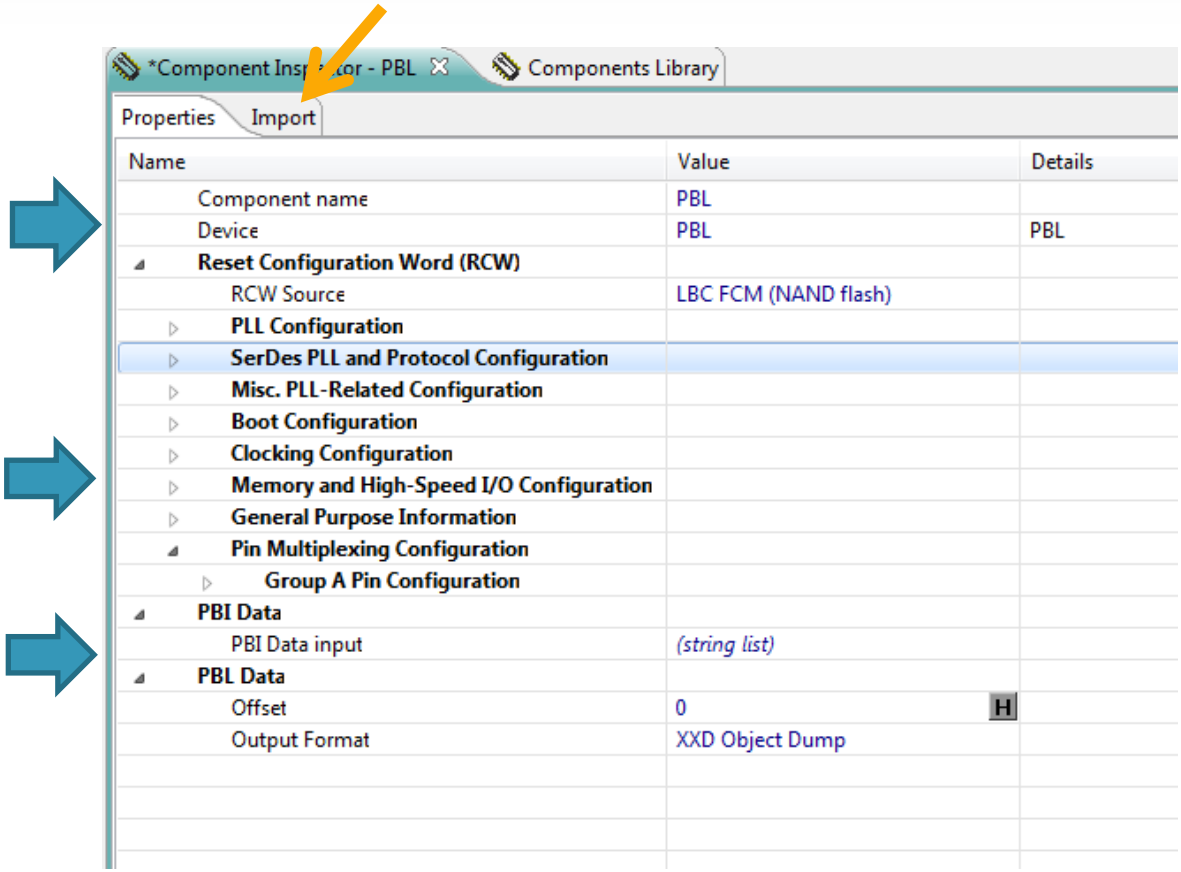
Pre-boot Loader (RCW) Configuration



Pre-boot Loader standard component interface

- PBL tool establishes all Reset Control Word settings
- PLL Configurations
- SerDes Configuration
- Pin Muxing Configuration
- Output format selection
- Possibility to add PBI data

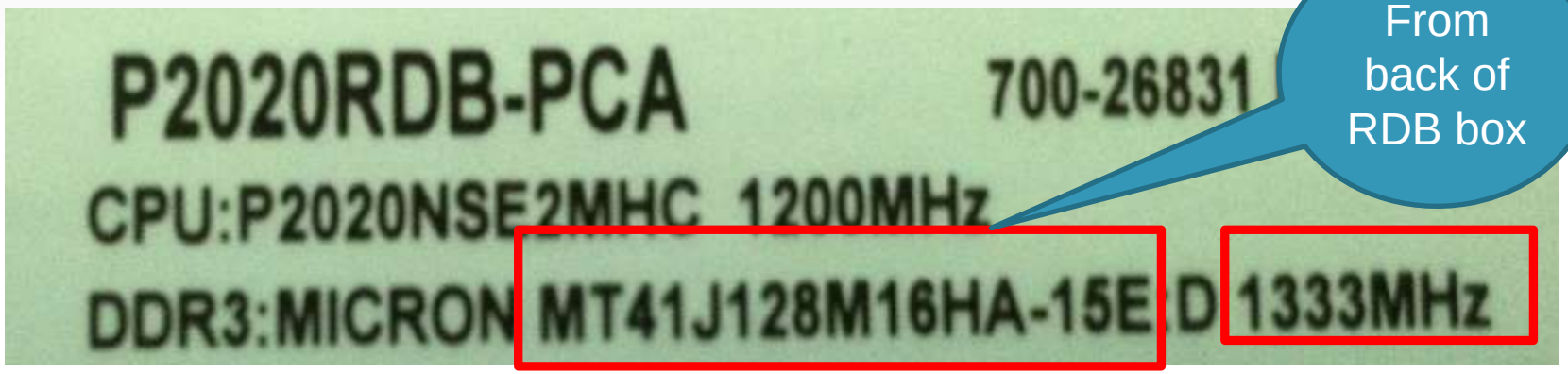
Possibility to import RCW settings



DDR Configuration

DDR Configuration Tool

Get DRAM information – P2020RDB-PCA



Micron

DDR3 SDRAM

MT41J512M4 – 64 Meg x 4 x 8 Banks

MT41J256M8 – 32 Meg x 8 x 8 Banks

MT41J128M16 – 16 Meg x 16 x 8 Banks

From DRAM datasheet

How about rest of the timing parameters?

Table 1: Key Timing Parameters

Speed Grade	Data Rate (MT/s)	Target ^{t}RCD-^{t}RP-CL	^{t}RCD (ns)	^{t}RP (ns)	CL (ns)
-093[1, 2, 3, 4]	2133	14-14-14	13.09	13.09	13.09
-107[1, 2, 3]	1866	13-13-13	13.91	13.91	13.91
-125[1, 2,]	1600	11-11-11	13.75	13.75	13.75
-15E[1,]	1333	9-9-9	13.5	13.5	13.5
-187E	1066	7-7-7	13.1	13.1	13.1

Features

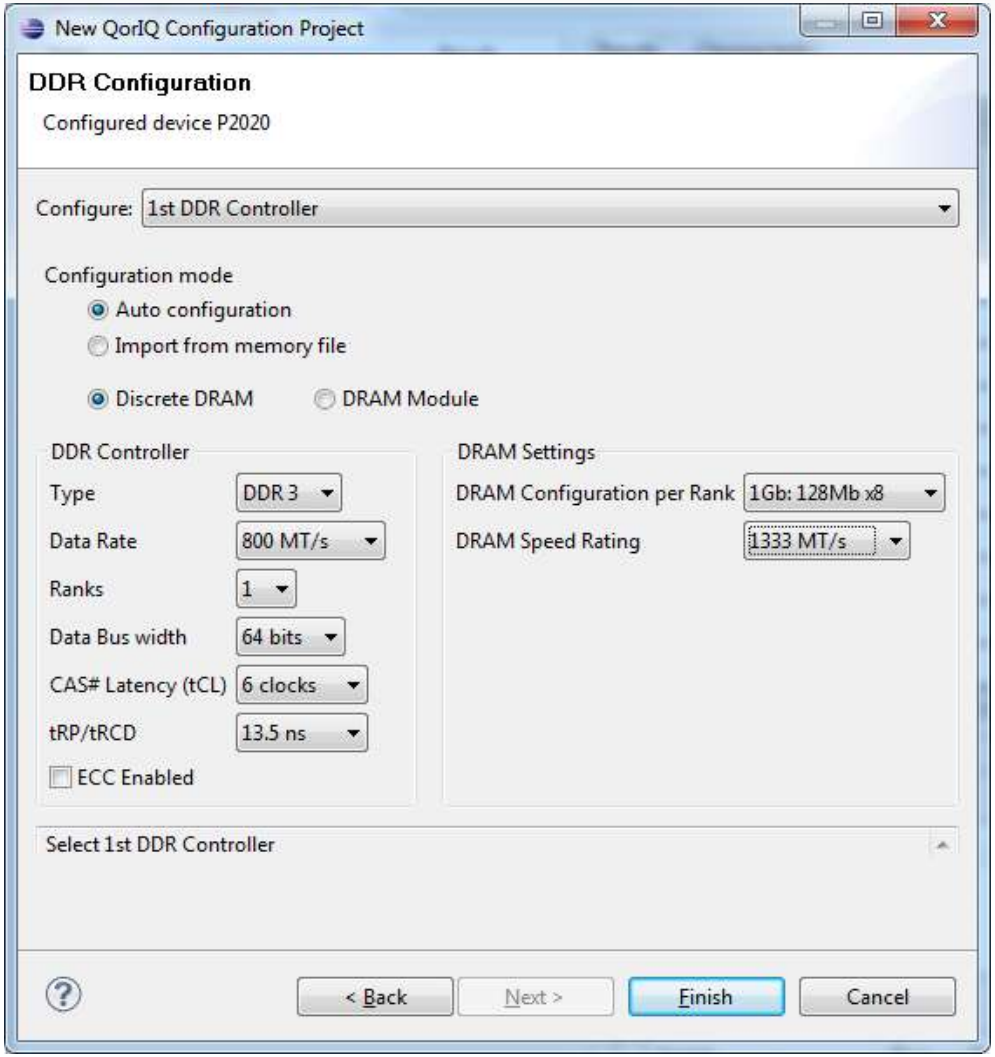
- $V_{DD} = V_{DDQ}$ = 1.5V ±0.075V
- 1.5V center-terminated push/pull I/O
- Differential bidirectional data strobe
- 8*n*-bit prefetch architecture
- Differential clock inputs (CK, CK#)
- 8 internal banks
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Programmable CAS READ latency (CL)
- Posted CAS additive latency (AL)
- Programmable CAS WRITE latency (CWL) based on ^{t}CK
- Fixed burst length (BL) of 8 and burst chop (BC) of 4 (via the mode register set [MRS])
- Selectable BC4 or BL8 on-the-fly (OTF)
- Self refresh mode
- T_C of 0°C to 95°C
  - 64ms, 8192 cycle refresh at 0°C to 85°C
  - 32ms, 8192 cycle refresh at 85°C to 95°C
- Self refresh temperature (SRT)
- Write leveling
- Multipurpose register
- Output driver calibration

Options[1]	Marking
• Configuration	
– 512 Meg x 4	512M4
– 256 Meg x 8	256M8
– 128 Meg x 16	128M16
• FBGA package (Pb-free) – x4, x8	
– 78-ball (8mm x 10.5mm) Rev. H,M,J,K	DA
– 78-ball (9mm x 11.5mm) Rev. D	HX
• FBGA package (Pb-free) – x16	
– 96-ball (9mm x 14mm) Rev. D	HA
– 96-ball (8mm x 14mm) Rev. K	JT
• Timing – cycle time	
– 938ps @ CL = 14 (DDR3-2133)	-093
– 1.071ns @ CL = 13 (DDR3-1866)	-107
– 1.25ns @ CL = 11 (DDR3-1600)	-125
– 1.5ns @ CL = 9 (DDR3-1333)	-15E
– 1.87ns @ CL = 7 (DDR3-1066)	-187E
• Operating temperature	
– Commercial (0°C ≤ T_C ≤ +95°C)	None
– Industrial (–40°C ≤ T_C ≤ +95°C)	IT
• Revision	:D/:H/:J/:K/ :M

Note: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on http://www.micron.com for available offerings.

- Tool automatically computes tRCD, tRP, and CL!
  - User can change these values if required.

DDR Wizard simplifies configuration



- From memory data sheet:
  - Maximum speed rating
  - Capacity

Generated files – CW, uboot, ddrinit.c

```
# DDR Controller 1 Registers

  # DDR_SDRAM_CFG
  mem [0xFF702110] = 0x47000008

  # CS0_BNDS
  mem [0xFF702000] = 0x3F

  # CS0_CONFIG
  mem [0xFF702080] = 0x80014202

  # CS0_CONFIG_2
  mem [0xFF7020C0] = 0x00

  # TIMING_CFG_3
  mem [0xFF702100] = 0x00030000

  # TIMING_CFG_0
  mem [0xFF702104] = 0x00330104

  # TIMING_CFG_1
  mem [0xFF702108] = 0x6E6B8846

  # TIMING_CFG_2
  mem [0xFF70210C] = 0x0FA8D0CC

  # DDR_SDRAM_CFG_2
  mem [0xFF702114] = 0x24401050

  # DDR_SDRAM_MODE
  mem [0xFF702118] = 0x00061421
```

```
#define DDR_1_INIT_EXT_ADDR_ADDR     0xFF70214C
#define DDR_1_SDRAM_RCW_1_ADDR       0xFF702180
#define DDR_1_SDRAM_RCW_2_ADDR       0xFF702184
#define DDR_1_DATA_INIT_ADDR         0xFF702128
#define DDR_1_SDRAM_MD_CNTL_ADDR     0xFF702120
#define DDR_1_DDRCDR_1_ADDR          0xFF702B28
#define DDR_1_DDRCDR_2_ADDR          0xFF702B2C

#define SDRAM_CFG_MEM_EN_MASK        0x80000000
#define SDRAM_CFG2_D_INIT_MASK       0x00000010

/* DDR Controller configured registers' values */
#define DDR_1_CS0_BNDS_VAL           0x3F
#define DDR_1_CS1_BNDS_VAL           0x00
#define DDR_1_CS2_BNDS_VAL           0x00
#define DDR_1_CS3_BNDS_VAL           0x00
#define DDR_1_CS0_CONFIG_VAL         0x80014202
#define DDR_1_CS1_CONFIG_VAL         0x00
```

```
#define PEX_CONFIG_DDR1_INIT_EXT_ADDR     0x00000000
#define PEX_CONFIG_DDR1_TIMING_4          0x00220001
#define PEX_CONFIG_DDR1_TIMING_5          0x02401400
#define PEX_CONFIG_DDR1_ZQ_CNTL           0x89080600
#define PEX_CONFIG_DDR1_WRLVL_CNTL        0x8655F614
#define PEX_CONFIG_DDR1_RCW_1             0x00000000
#define PEX_CONFIG_DDR1_RCW_2             0x00000000


/* DDR Controller 1 configuration global structures */
fsl_ddr_cfg_regs_t ddr_cfg_regs_0 = {
  .cs[0].bnds = PEX_CONFIG_DDR1_CS0_BNDS,
  .cs[1].bnds = PEX_CONFIG_DDR1_CS1_BNDS,
  .cs[2].bnds = PEX_CONFIG_DDR1_CS2_BNDS,
  .cs[3].bnds = PEX_CONFIG_DDR1_CS3_BNDS,
  .cs[0].config = PEX_CONFIG_DDR1_CS0_CONFIG,
  .cs[1].config = PEX_CONFIG_DDR1_CS1_CONFIG,
  .cs[2].config = PEX_CONFIG_DDR1_CS2_CONFIG,
```

DDR Validation Tool (DDRv)

Validating DDR Configuration

NOTES:

1. **THIS TOOL IS AN ADD-IN to QCS**
2. This tool is 995$ and requires a TAP to be purchased separately.
3. Current version is v1.3 and is available from the Freescale website – use Buy Direct to purchase online.

Centering of the clock - after ODT optimization

Results | Choose tests

WRLVL_START	CLK_ADJ								
	0 clocks	1/8 clocks	1/4 clocks	3/8 clocks	1/2 clocks	5/8 clocks	3/4 clocks	7/8 clocks	1 clocks
0 clock delay	0/3	3/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3
1/8 clock delay	0/3	3/3	3/3	3/3	0/3	0/3	0/3	0/3	0/3
1/4 clock delay	0/3	3/3	3/3	3/3	0/3	0/3	0/3	0/3	0/3
3/8 clock delay	0/3	3/3	3/3	3/3	3/3	3/3	0/3	0/3	0/3
1/2 clock delay	0/3	3/3	3/3	3/3	3/3	3/3	0/3	0/3	0/3
5/8 clock delay	0/3	3/3	3/3	3/3	3/3	3/3	3/3	3/3	0/3
3/4 clock delay	0/3	0/3	3/3	3/3	3/3	3/3	3/3	3/3	0/3
7/8 clock delay	0/3	0/3	0/3	3/3	3/3	3/3	2/3	3/3	0/3
1 clock delay	0/3	0/3	0/3	0/3	3/3	3/3	3/3	3/3	0/3
9/8 clock delay	0/3	0/3	0/3	0/3	0/3	3/3	3/3	3/3	0/3
5/4 clock delay	0/3	0/3	0/3	0/3	0/3	0/3	2/3	3/3	0/3
11/8 clock delay	0/3	0/3	0/3	0/3	0/3	0/3	0/3	3/3	0/3
3/2 clock delay	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3
13/8 clock delay	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3
7/4 clock delay	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3
15/8 clock delay	0/3	3/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3
2 clock delay	0/3	3/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3
17/8 clock delay	0/3	3/3	3/3	3/3	0/3	0/3	0/3	0/3	0/3
9/4 clock delay	0/3	3/3	3/3	3/3	0/3	0/3	0/3	0/3	0/3
19/8 clock delay	0/3	3/3	3/3	3/3	3/3	3/3	0/3	0/3	0/3
5/2 clock delay	0/3	3/3	3/3	3/3	3/3	3/3	0/3	0/3	0/3

- Centering of clock scenario was re-run after finding the right ODT values

Initial Bring-Up

Getting out of Reset!

Initial Board Power On/Validation

Top areas to check if not coming out of Reset:

- Voltage Rails:
  - Ensure the all the required voltage levels are provided and meet the specified levels and tolerances.
  - Ensure that the recommended power rail sequence.
- SYSCLK:
  - Ensure it is present and meets the voltage level, slew rate, frequency, duty cycle, and jitter requirements specified.
- Reset Signals
  - Ensure PORESET is driven for a minimum of 1 ms and that it is driven before the core and platform voltages are powered up.
  - If HRESET is driven externally, ensure it is released as expected; if driven just by the T4240, confirm it is released after PORESET deassertion.
- RCW
  - Confirm the RCW device is being read after ASLEEP is driven high. If not, check that the cfg_rcw_src signals are driven as expected when the PORESET signal is released.
  - Confirm RCW contents are as expected. The specifics of the RCW must match the system configuration.

Initial Board Power On/Validation

- **Connect Debug Tools**

- **Hardware JTAG probe:**

CodeWarrior Tap Kit

Initial Board Power On/Validation

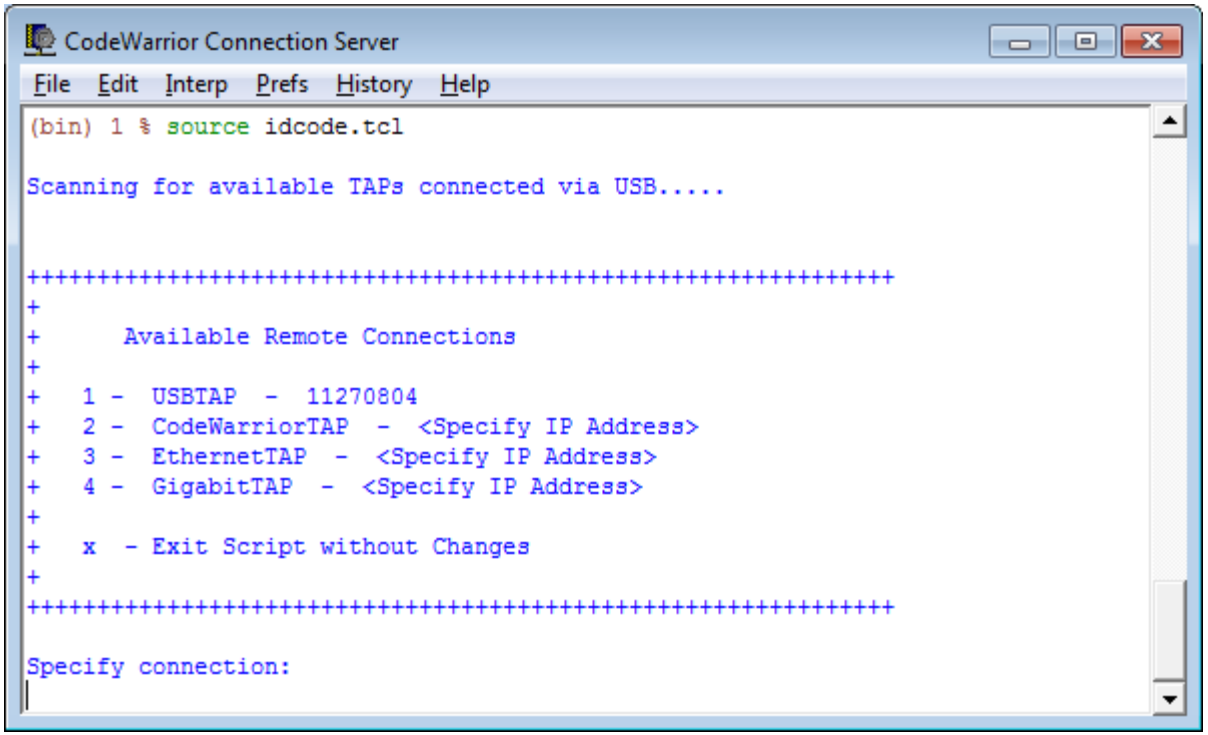
- **Connect Debug Tools**

- **Software Tools:**
  - Codewarrior 10.3.x IDE

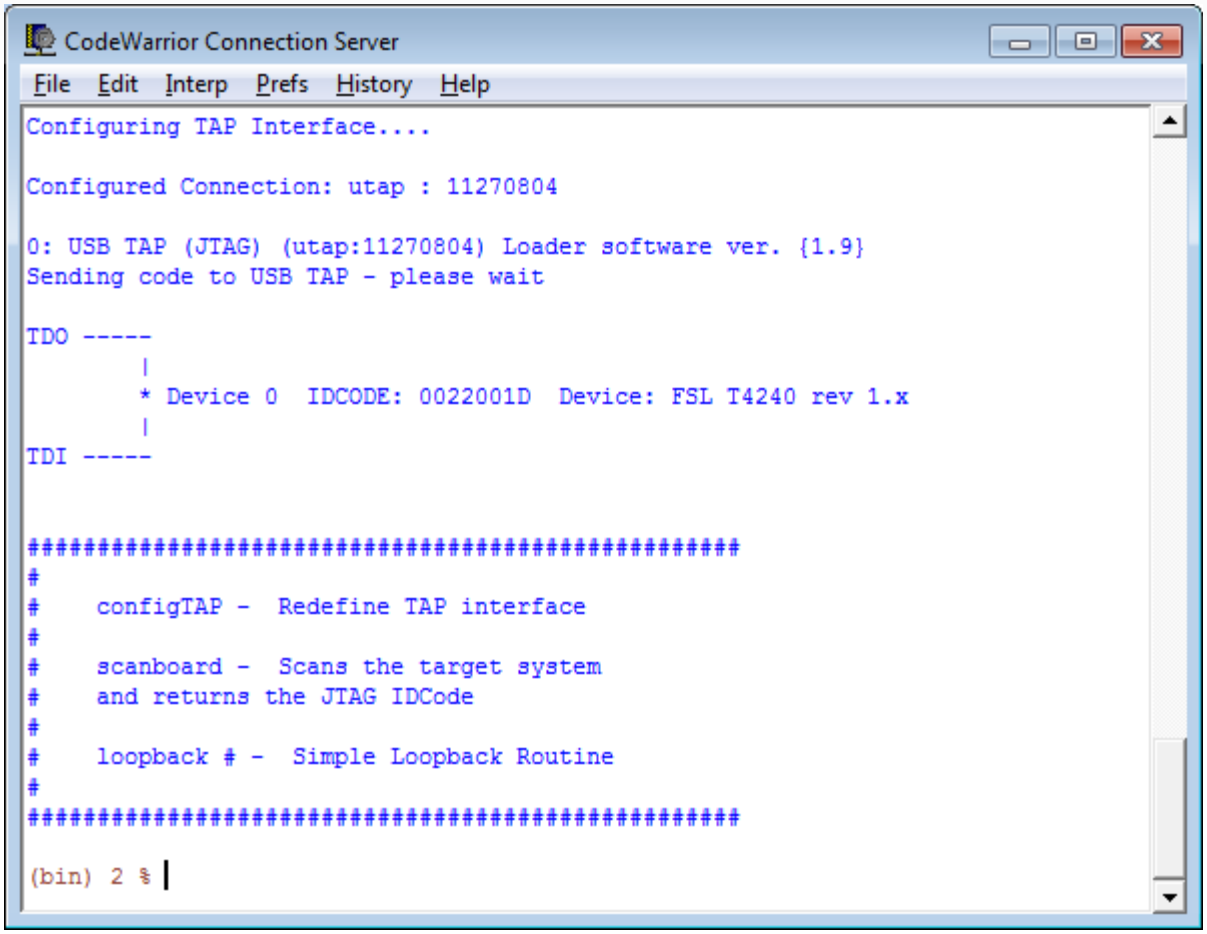
    http://www.freescale.com/webapp/sps/site/homepage.jsp?code=CW_HOME

    - ccs (part of Codewarrior)
      - Located .\PA\ccs\bin\ccs.exe
        - idcode.tcl

Verify JTAG connection



Verify JTAG connection



CW RCW Override

C:\Program Files\Freescale\CW PA v10.1.1\PA\PA_Support\Initialization_Files\jtag_chains

Below is an example of a JTAG configuration file for a T4240.

```
# Example file to allow overriding the whole RCW or only parts of it
#
# Syntax:
#  T4240 (2 RCW_option) (RCWn value) ...
#
# where:
#   RCW_option = 0 [RCW Override disabled]
#                1 [RCW Override enabled]
#                2 [Reset previous RCW Override parts]
#       0x80000001 [RCW Override + PLL Override]
#       NOTE: Enabling PLL Override could lead to hanging the chip
#
#   RCWn = 21000+n (n = 1 .. 16; index of RCW value)
#
#   value = 32bit value
```

T4240 (2 1) (210001 0x14180019) (210002 0x0c10190c) (210003 0x00000000) (210004 0x00000000) (210005 0x70023060) (210006 0x0055bc00) (210007 0x1c020000) (210008 0x09000000) (210009 0x00000000) (210011 0xee0000ee) (210012 0x00000000) (210013 0x000187fc) (210014 0x00000000) (210015 0x00000000) (210016 0x00000008)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