QorIQ Portfolio: Deeper Look at QorIQ T1040 and Its Integrated Switch

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Business Development

October 2013

AGENDA

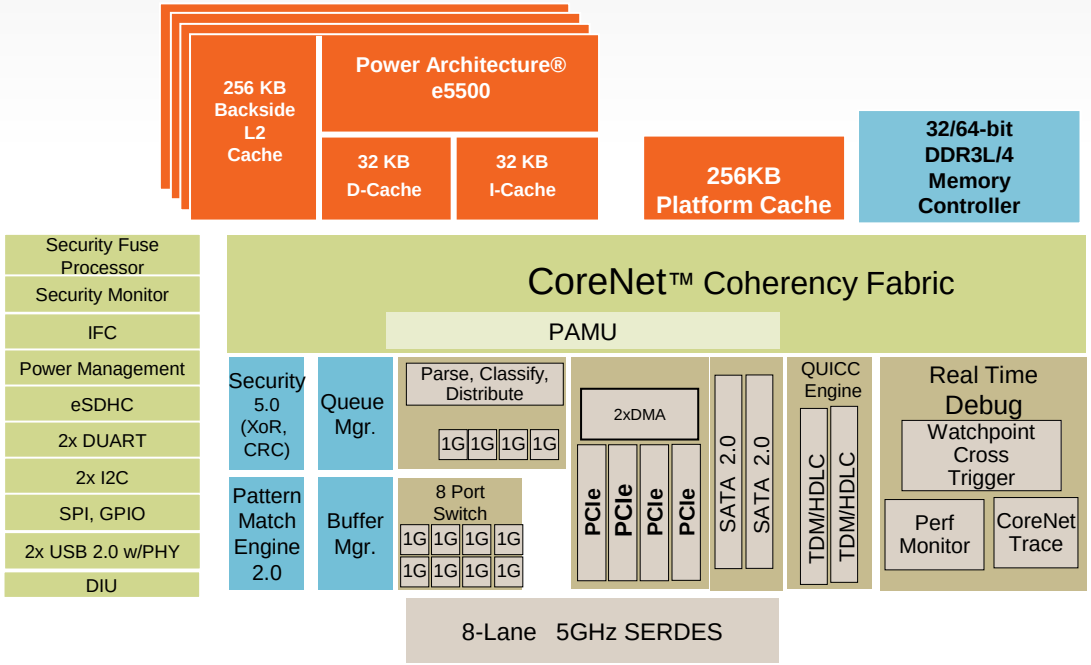
1. Introduction
2. New IP’s
3. Enhancements
4. HW related topics
5. T1040 to T2081 Migration

Introduction

INTRODUCTION

- Block Diagram
- Road Map
- Personality Comparison Chart
- Feature List
- Software and tools Support
- Use Cases

T1040



Device

- 780-pin FC-PBGA package
- 23x23mm, 0.8mm pitch

Power targets

- Enable Convection cooled system design

Datapath Acceleration

- SEC- crypto acceleration
- PME- Reg-ex Pattern Matcher

Processor

- 4x e5500, 64b, up to 1.4GHz
- Each with 256KB backside L2 cache
- 256KB Shared Platform Cache w/ECC
- Supports up to 64GB addressability (36 bit physical addressing)

Memory Subsystem

- 32/64b DDR3L/4 Controller up to 1600MHz

CoreNet Switch Fabric

High Speed Serial IO

- 4x PCIe Gen2 (5Gbps) Controllers
- 2x SATA 2.0, 3Gbps
- 2x USB 2.0 with PHY

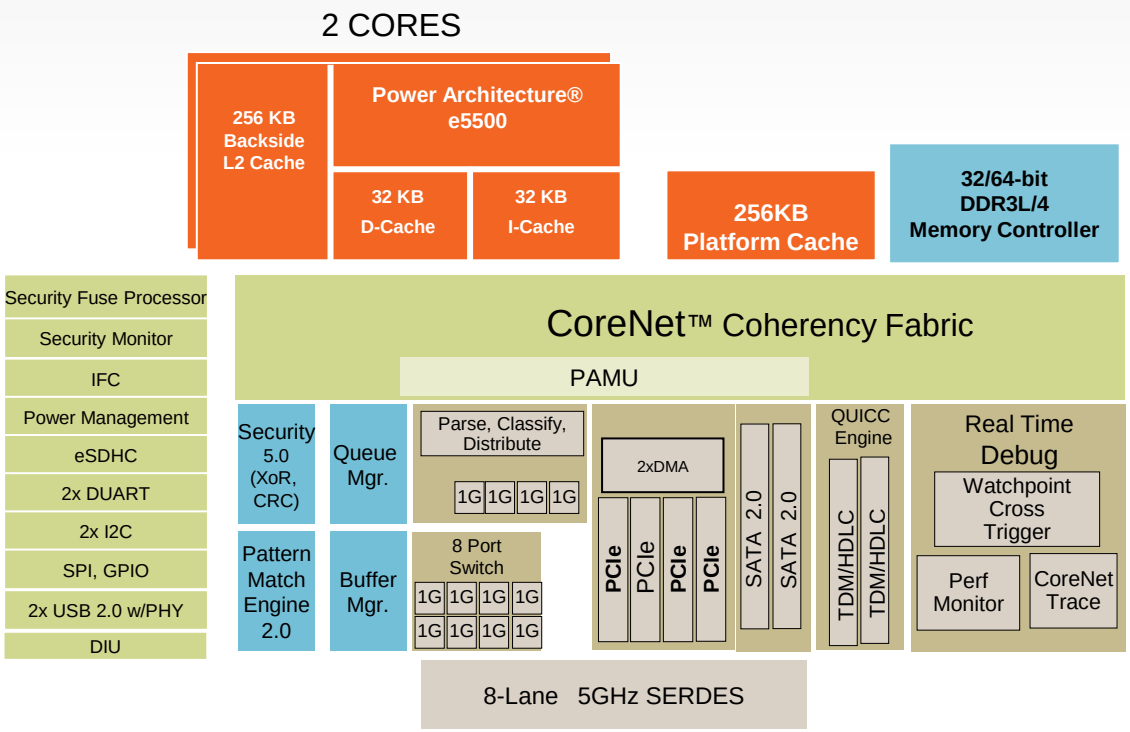
Network IO

- FMan packet Parse/Classify/Distribute
- Lossless Flow Control, IEEE 1588
- Up to 4x 10/100/1000 Ethernet Controllers
- **8-Port Gigabit Ethernet Switch**
- QUICC Engine
  - HDLC, 2x TDM

Green Energy Operation

- Fanless operation quad-core 1.4GHz
- Packet lossless deepsleep
  - Programmable wake-on-packet
  - Wake-on-timer/GPIO/USB/IRQ

T1020



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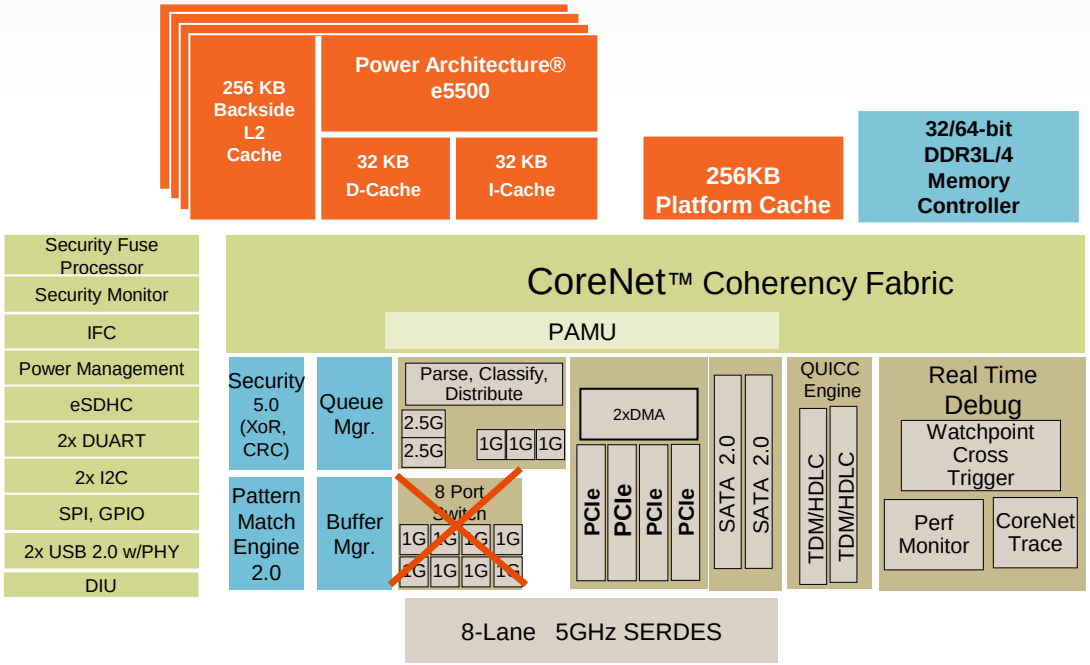
T1042



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- **Target Deep Sleep 150mW on special Part Numbers (1/2W AC System)**

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High Speed Serial IO

- 4 PCIe Gen2 Controllers
- SATA 2.0, 3Gbps
- 2 USB 2.0 with PHY

Network IO

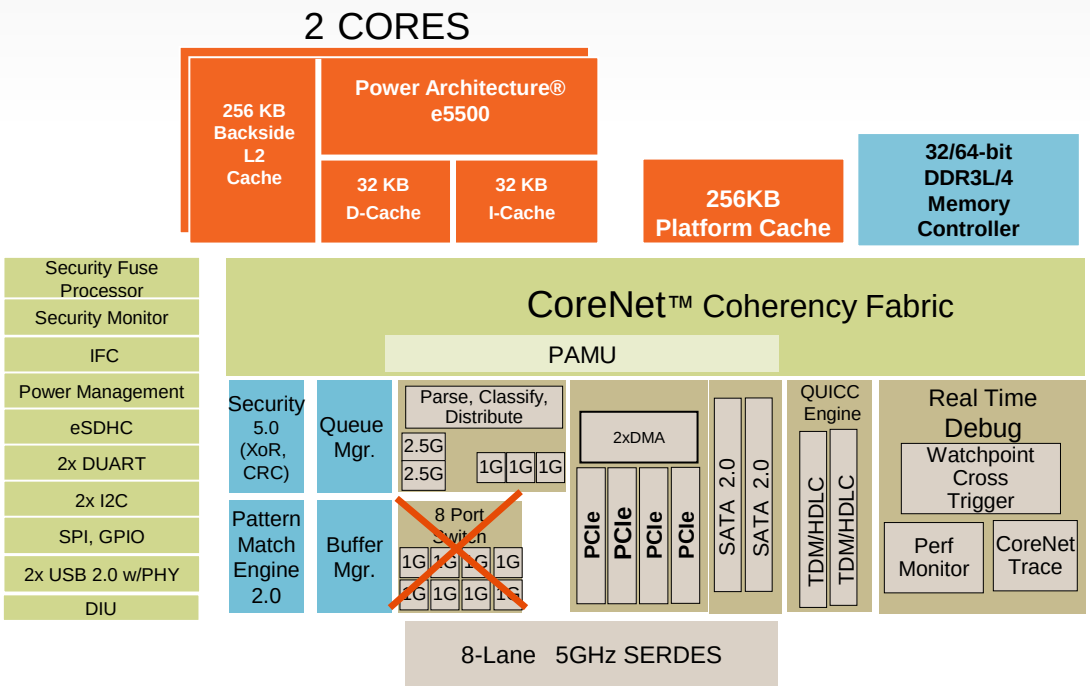
- FMan packet Parse/Classify/Distribute
- Lossless Flow Control, IEEE 1588
- 5x 10/100/1000 Ethernet Controllers
- QUICC Engine
  - HDLC, 2x TDM

Green Energy Operation

- Fanless operation quad-core 1.4GHz
- Packet lossless deepsleep
  - Programmable wake-on-packet
  - Wake-on-timer/GPIO/USB/IRQ

freescale™

T1022



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- SATA 2.0, 3Gb/s
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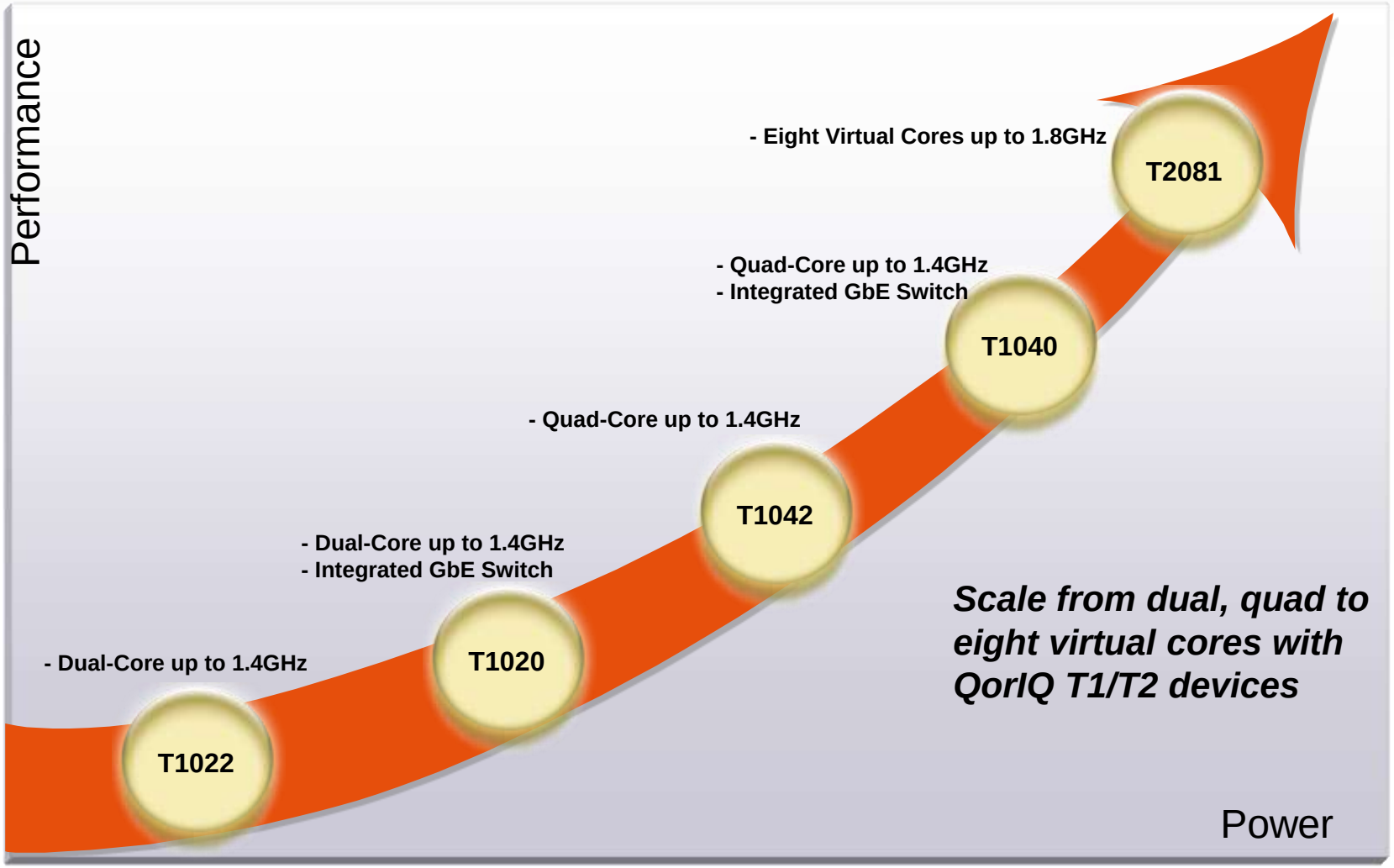
One of the Industry's Most Scalable, Pin-Compatible Communications Processor Family



Personality Comparison Chart

	P1020, P1011, P1021, P1012	P1022, P1013	T1020	T1022	T1040	T1042	T2081
CPU	1 to 2 x e500	1 to 2 x e500	2 x e5500	2 x e5500	4 x e5500	4 x e5500	4 x e6500/8 threads
	Up to 800MHz	Up to 1200MHz	1200-1400MHz	1200-1400MHz	1200-1400MHz	1200-1400MHz	1500 - 1800MHz
	32K I/D	32K I/D	32K I/D	32K I/D	32K I/D	32K I/D	32K I/D
L2 Cache	256KB	256KB	256KB/Core	256KB/Core	256KB/Core	256KB/Core	2MB shared
Platform Cache			256KB	256KB	256KB	256KB	512KB
DDR I/F Type/Width	DDR2/3	DDR2/3	DDR3L/4	DDR3L/4	DDR3L/4	DDR3L/4	DDR3/3L
	16/32-bit , 800MHz	32/64-bit, 800MHz	32/64-bit, 1600MT/s	32/64-bit, 1600MT/s	32/64-bit, 1600MT/s	32/64-bit, 1600MT/s	64-bit, 2133MT/s
10/100/1000 Ethernet (with IEEE1588v2)	3 x 10/100/1000	2 x 10/100/1000	4 x 10/100/1000	5 x 10/100/1000	4 x 10/100/1000	5 x 10/100/1000	2x 2.5/10G + 6x 1G
Ethernet Switch	--	--	8-Port GE Switch	No	8-Port GE Switch	No	No
TDM	Yes	Yes	Yes	Yes	Yes	Yes	No
QUICC Engine	In P1021/12	No	TDM and HDLC	TDM and HDLC	TDM and HDLC	TDM and HDLC	No
SERDES	4 lanes	6 lanes	8 lanes(5GHz)	8 lanes(5GHz)	8 lanes(5GHz)	8 lanes(5GHz)	8 lanes(10GHz)
PCI-Exp	2 (Gen-1)	3 (Gen-1)	4 (Gen-2)	4 (Gen-2)	4 (Gen-2)	4 (Gen-2)	3 (Gen2) and 1 (Gen3)
Package			Pin Compatible				

Personality Comparison Chart

	P1020, P1011, P1021, P1012	P1022, P1013	T1020	T1022	T1040	T1042	T2081
DIU	--	Yes	Yes	Yes	Yes	Yes	No
SATA	--	2 controller	2 controller	2 controller	2 controller	2 controller	No
		1.5 or 3Gbaud	1.5 or 3Gbaud	1.5 or 3Gbaud	1.5 or 3Gbaud	1.5 or 3Gbaud	No
USB2.0	2 ULPI controllers	2 ULPI controllers	2 with PHY	2 with PHY	2 with PHY	2 with PHY	2 with PHY
Memory Card	SD/MMC	SD/MMC	SD/MMC/SDXC	SD/MMC/SDXC	SD/MMC/SDXC	SD/MMC/SDXC	SD/MMC/SDXC
Accelerators	SEC3.3	SEC3.3	DPAA, PME SEC5.0 with Trust Architecture	DPAA, PME SEC5.0 with Trust Architecture	DPAA, PME SEC5.0 with Trust Architecture	DPAA, PME SEC5.0 with Trust Architecture	DPAA, PME, DCE, SEC5.2 with Trust Architecture
Power Management	Power Management	Power Management with Deep sleep	Power Management with Deep sleep	Power Management with Deep sleep	Power Management with Deep sleep	Power Management with Deep sleep	Power Management
Package			Pin Compatible				

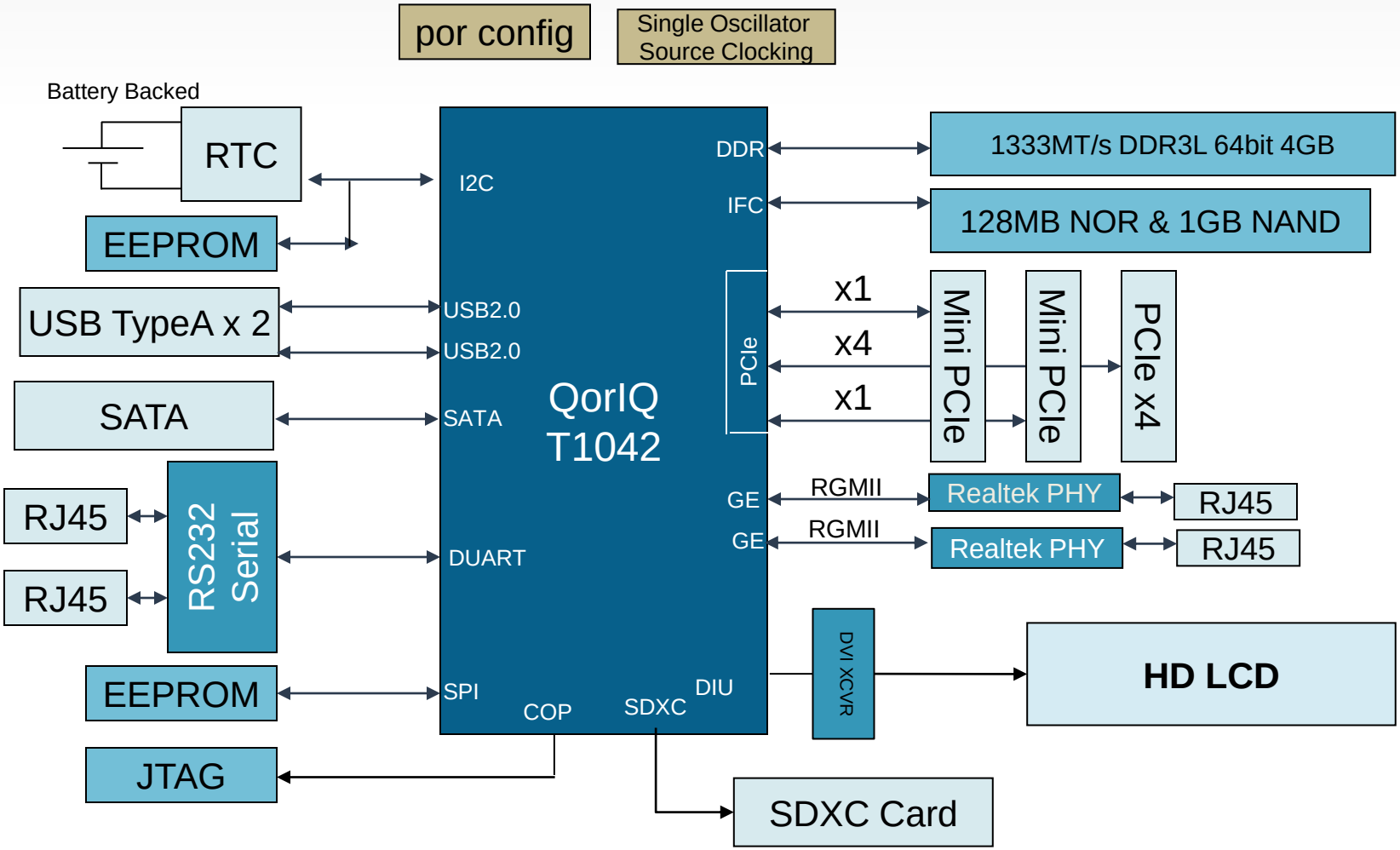
T1 Family Features & Benefits

Features	Benefits
Scalable Performance Pin compatible dual core to eight virtual cores	**Future Proofing** Upgrade to higher performance as needed >2x-4x the performance of existing P1 series
Gigabit Ethernet Switch Integrated Gigabit Ethernet Switch	**Lowers System Cost/Simplifies design** Eliminates cost of external GE switch Simplifies HW and SW implementation Reduces overall system power
Accelerators DPAA - Classification, Traffic Management Pattern Matching Security	**Reduce CPU cycles** Security policies based on application/services High performance HW based encryption VortiQa Security Appliance S/W and AppID
Hardware Assisted Virtualization Hypervisor level I/O MMU – controls memory I/Os can access Support for Topaz, KVM, Linux Containers,	**Higher performance (Vs. software emulation)** Enables virtualization layer to enforce system security Simplifies I/O virtualization and sharing Flexibility to use multiple options to meet system needs Support for S/W Hypervisor, KVM and Linux Containers
Power Management Best performance per watt Deep Sleep – proxy for sleeping hosts Enables ½ Watt AC	**Green Energy Efficient System Designs** Optimized for best performance and power Enables Compliance with Energy Consumption standards (ECC, EnergyStar, ECMA 393) Power Management software as part of SDK

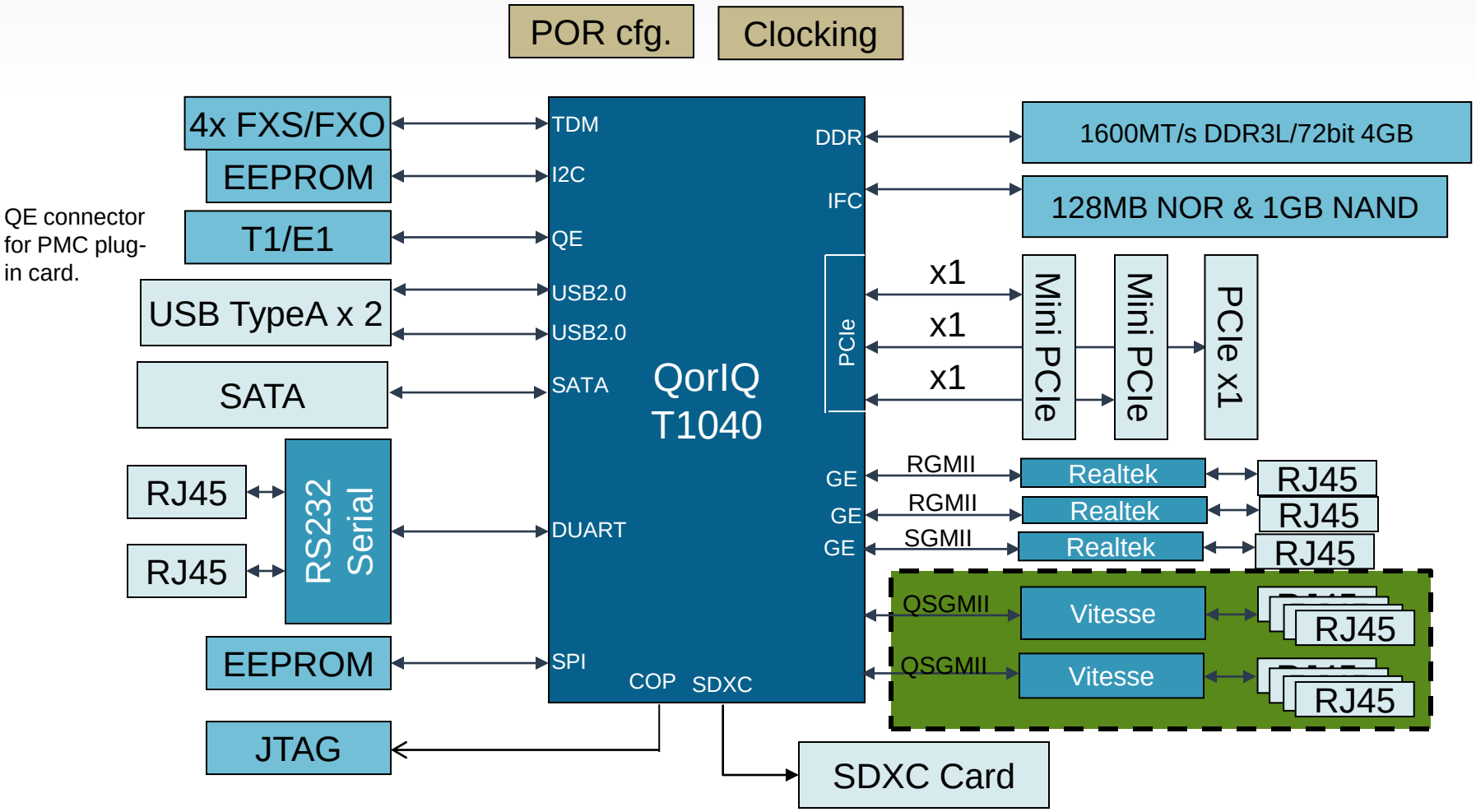
T1040 Software & Tools at a Glance

- Two Reference Design Boards
  - T1040RDB
  - T1042RDB
- Software Support
  - Yocto based SDK
  - SDK support includes
    - Legacy features (refer SDK 1.4 release notes)
    - New features
    - FMAN and QE microcode
    - Linux based QE drivers for TDM, UART and HDLC
- QorIQ Configuration Suite
- CodeWarrior based debugger, flash programmer

T1042RDB Block Diagram

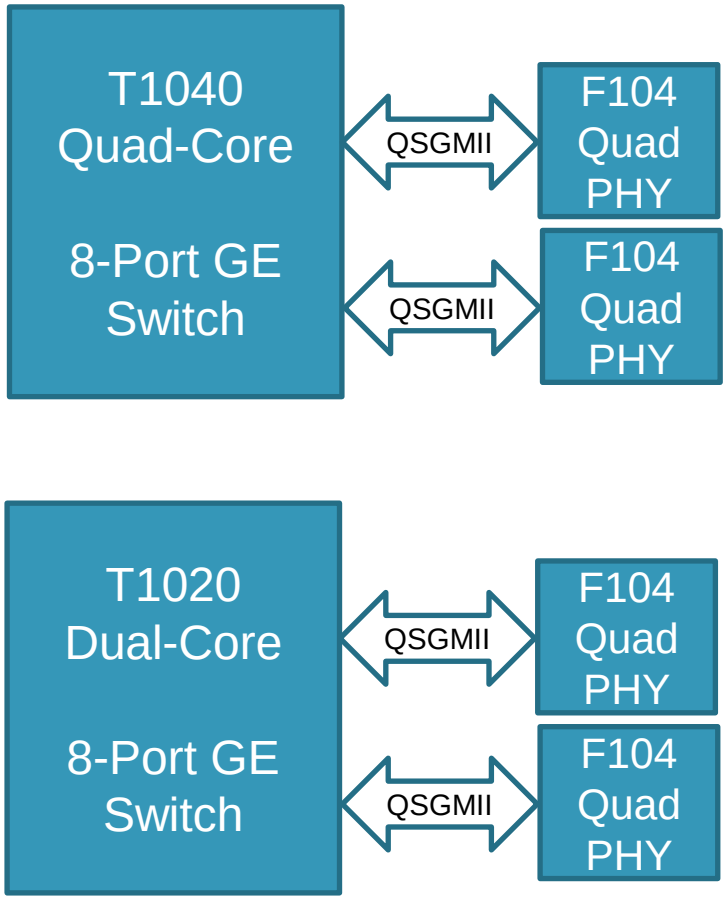


T1040RDB Block Diagram



T10xx Product Kit Options

Integrated Gigabit Ethernet Switch And bundled 2x QUAD PHYs



Without Gigabit Switch

T1042
Quad-Core

T1022
Dual-Core

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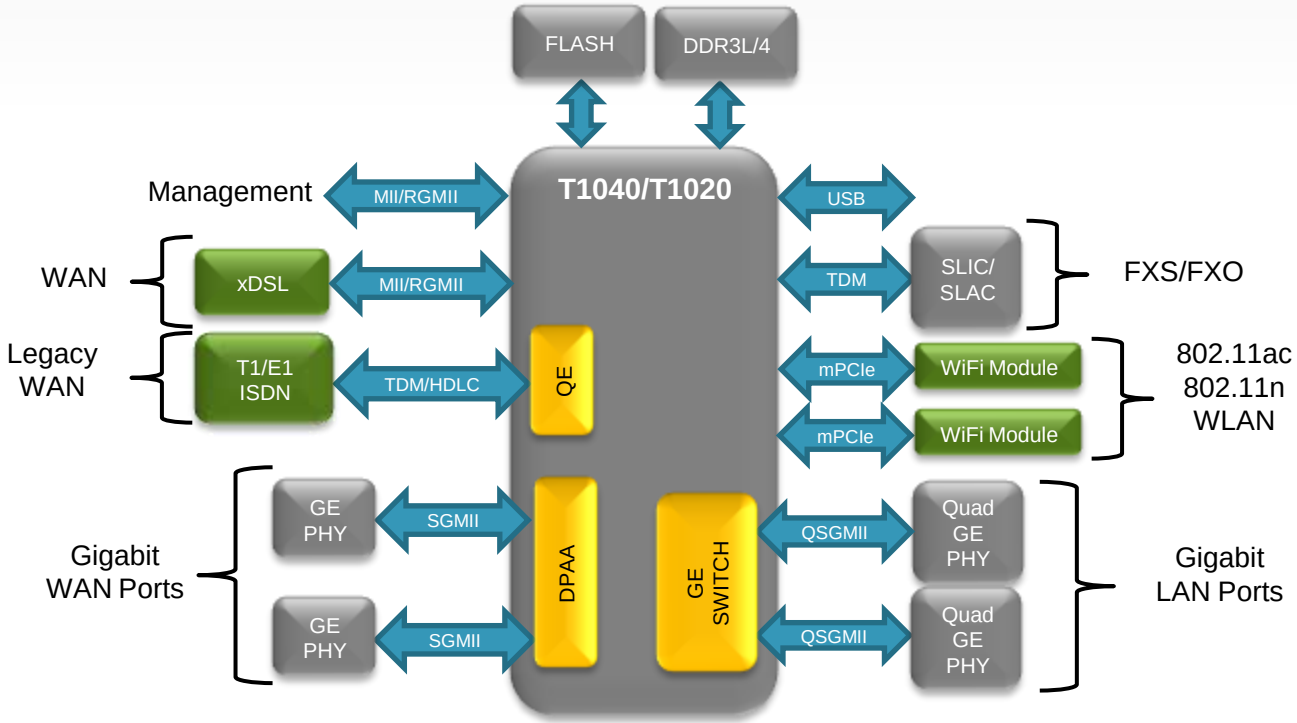
T10xx - Business Use cases

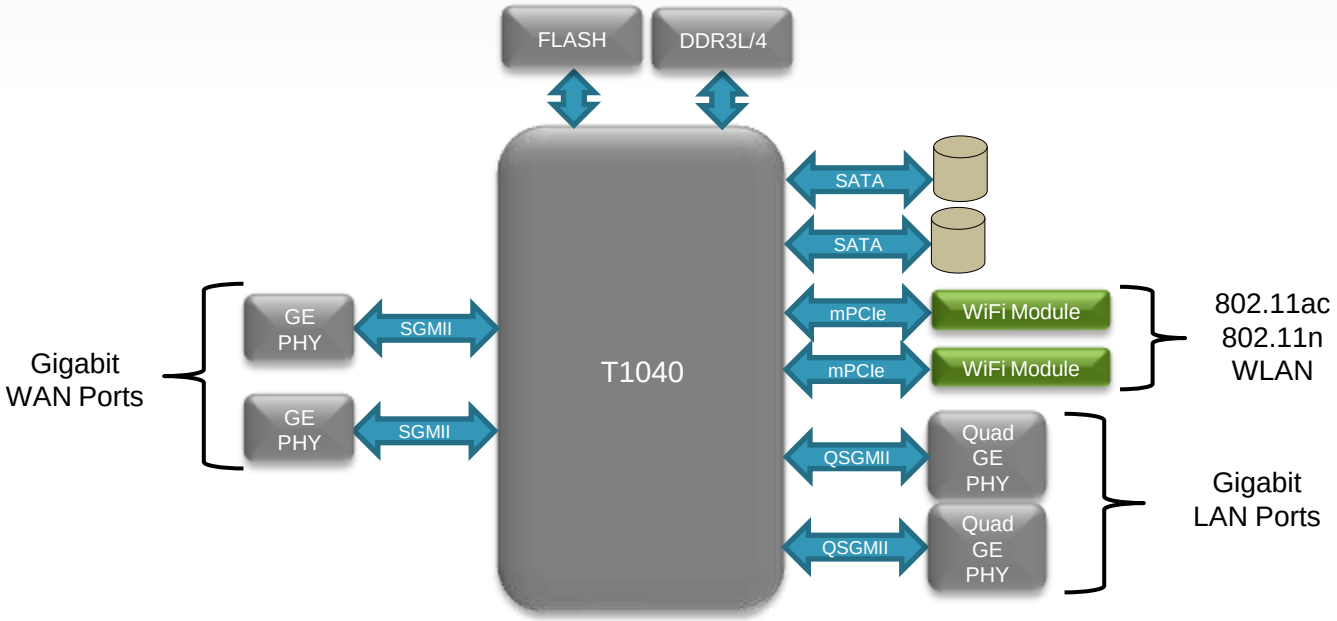
- Enterprise / Service Provider Router
- Security Appliance/UTM
- Network Multi Function Printer

Enterprise / Service Provider Router



- **Integrated GE LAN Switch to reduce system cost**
- **Quad-core CPU to support advanced services/applications**
- **Hardware based virtualization**
- **Datapath Architecture to offload packet processing**
- **Advanced Security and Trust Architecture**
- **Support for legacy T1/E1, ISDN and IP Services**

Security Appliance/UTM



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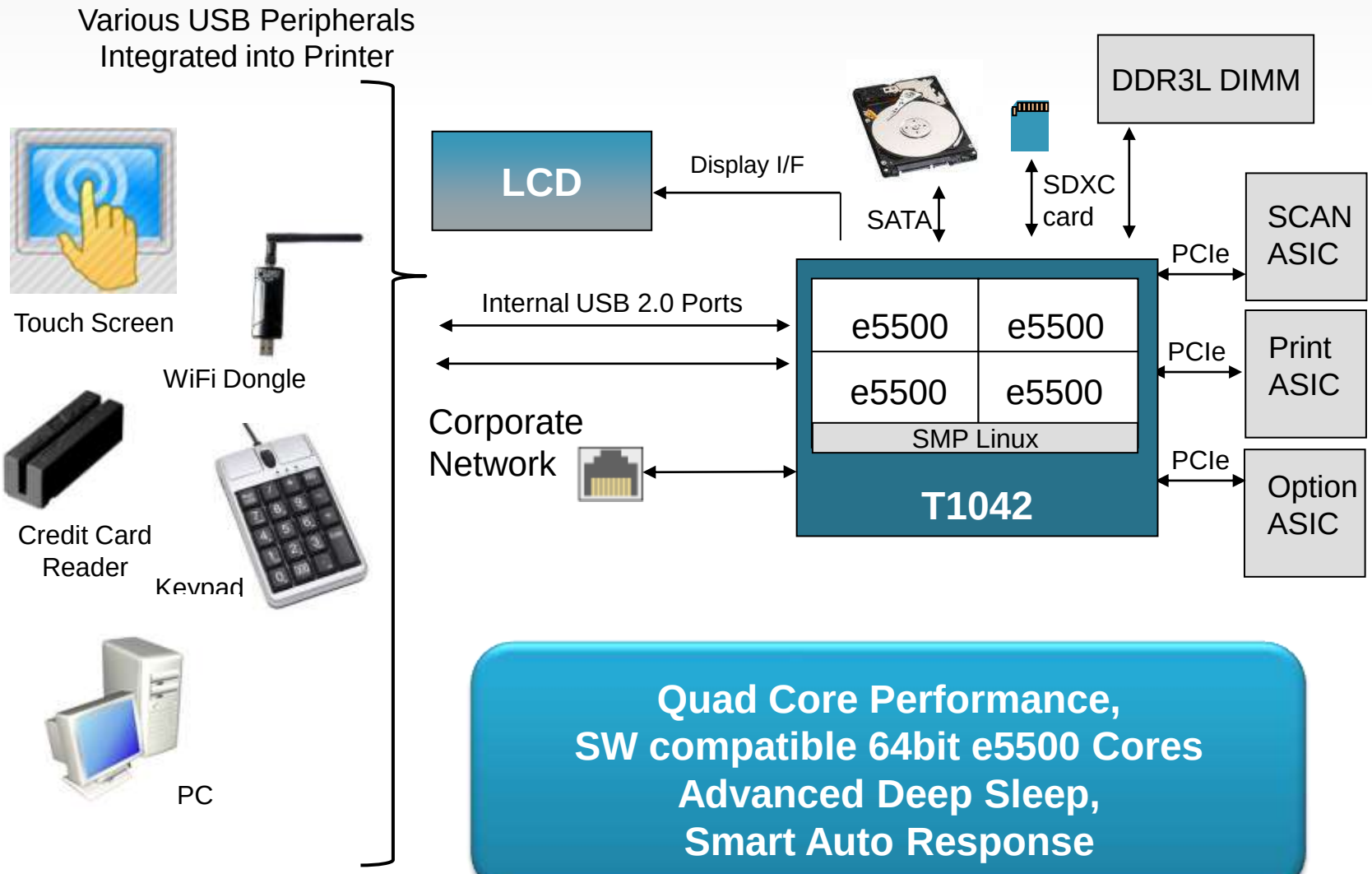
- **Quad-core CPU to support advanced services/applications**
- **Hardware based virtualization**
- **Datapath Architecture to offload packet processing**
- **Advanced Security and Trust Architecture**
- **Hardware based pattern matcher for high performance**

T1042 MFP System



Quad Core Performance,
SW compatible 64bit e5500 Cores
Advanced Deep Sleep,
Smart Auto Response

NEW IP's in T1040

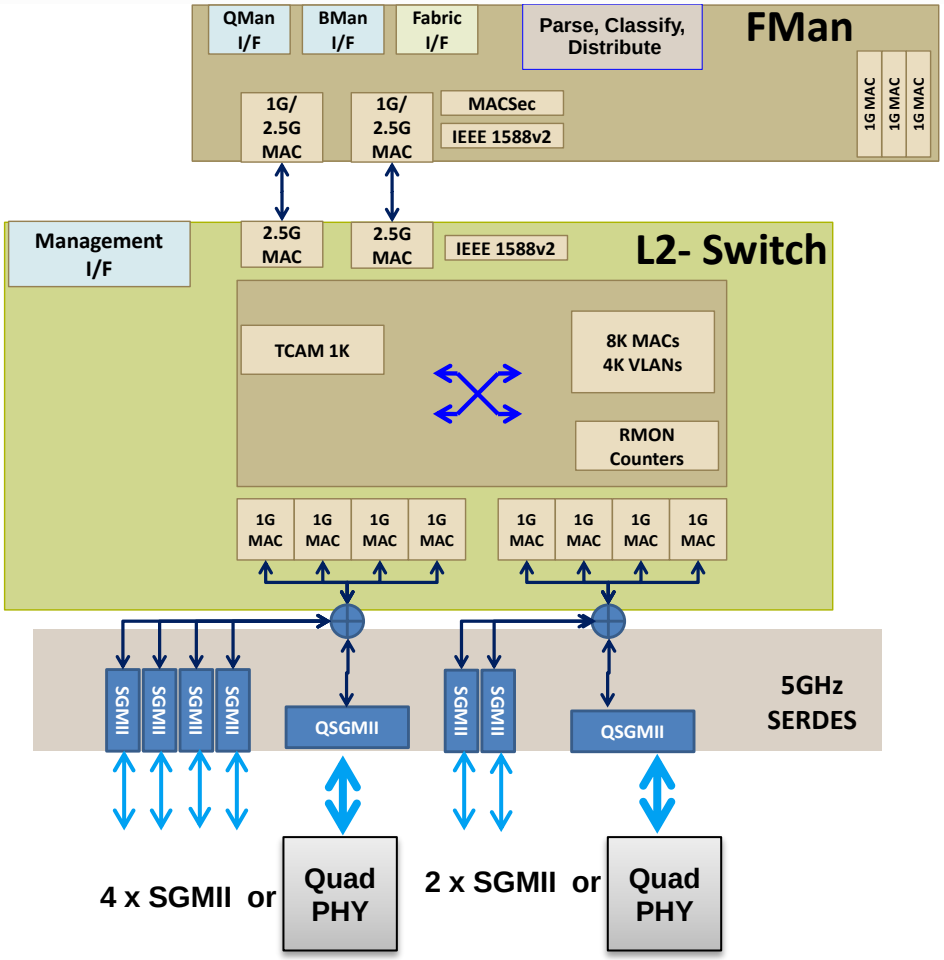
New IP's

Layer 2 Ethernet Switch

- Block Diagram
- Interface with FMAN

T1040: Gigabit Ethernet Switch

- Advanced Features
  - Priority flow control - lossless
  - Lower latency and shared buffer management
  - Advanced classification, shaping an policing
- Power savings
  - With support for latest standards including IEEE 802.3az Energy Efficient Ethernet (EEE)
- Cost savings
  - Through switch integration, low-pin count QSGMII connectivity and port count / cost optimization
- Increased ROI - Lower TTM and high re-use
  - Integrated solution kit with software reuse potential
- Support for Full featured L2 software stacks

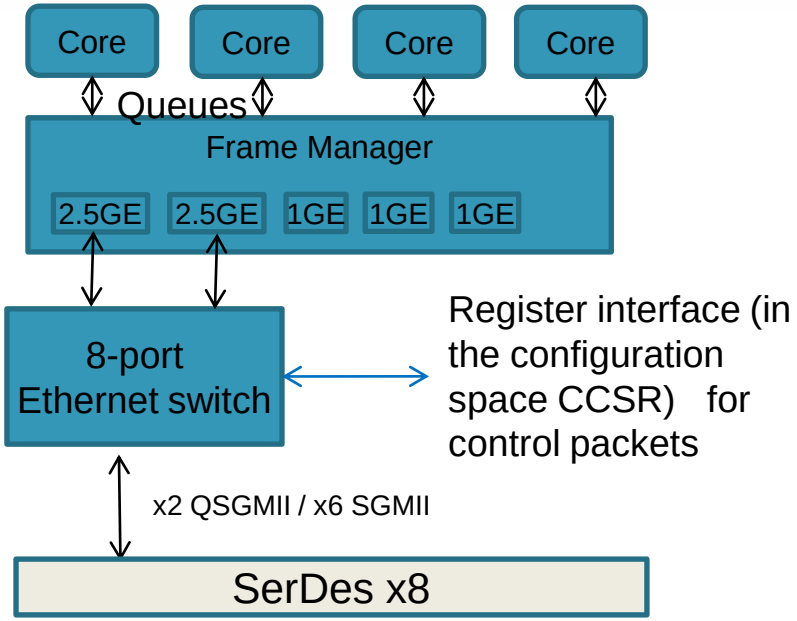


Ethernet Switch Block

The QorIQ cores (e5500) provide the management of the switch via a defined API

- **Layer 2 Switching**
  - IEEE 802.1Q VLAN switch
  - MAC addresses - 8K Entry Table
  - VLAN tags - 4K Entry Table
  - Push/pop up to two VLAN tags
  - Independent and shared VLAN learning (IVL, SVL)
  - Dynamic Learning – S/W or H/W (wire speed) : aging 1 – 220 sec
  - Static Address provisioning
  - Link aggregation (IEEE 802.3ad)
  - Policing with storm control and MC/BC protection
  - STP, RSTP and MSTP support
  - IPv4 and IPV6 multicast
  - Jumbo Frames 9.6KB
- **TCAM-based**
  - TCAM - 1K Entry Table
  - Normal - Service Classification, Translation, and Remarking
  - VLAN - Editing, Translation, and Remarking
  - ACL
- **VLAN and QoS Classification**
  - Hierarchical QoS (H-QoS) with DWRR scheduling at different levels
  - between ingress ports
  - between priorities
  - between services
- **Monitoring**
  - RMON counters per port

Ethernet Switch Interface with Frame Manager



- 8 L2-switch ports + 3 FMAN ports
- 2 ports of Ethernet switch is connected to FMAN and operating 2.5 Gbps (aggregating to 5 Gbps)

OR

- 8 L2-switch ports + 4 FMAN ports. 1 port of Ethernet switch is connected to FMAN @ 2.5 Gbps.

Control packets are queued on the Ethernet Switch CPU-register interface and can be accessed (receive and transmit) through any e5500 core. This space is memory mapped in T1040 (CCSR space).

Enhancements

Enhancements

- SERDES
- USB PHY
- DIU
- IFC
- eSDHC
- DDR4

Enhancements

SERDES

T104x SERDES

- T104x supports single 8 lane SerDes.

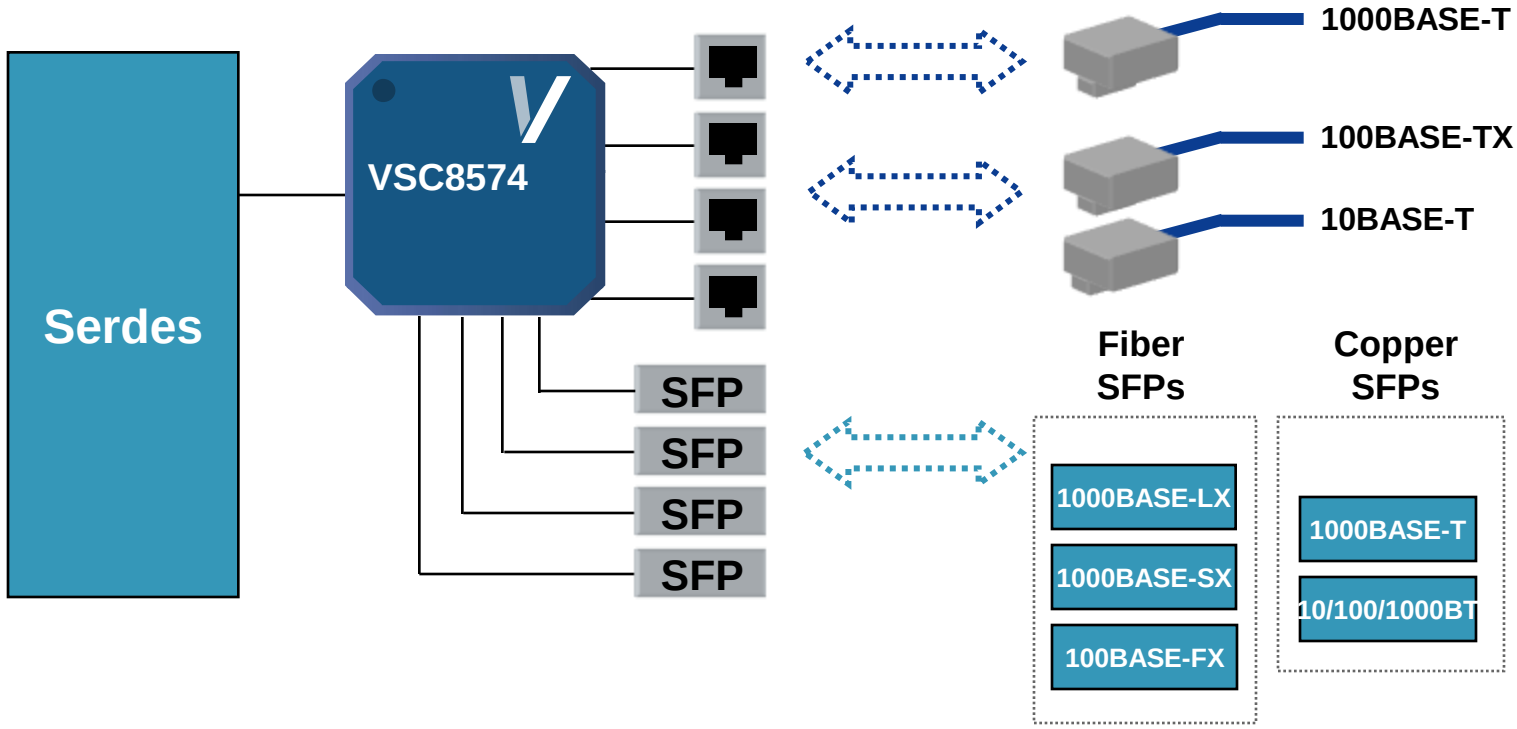
- There are two PLL's in the SerDes.
  - PLL1 provides clocking for lanes A:H
  - PLL2 provides clocking for Lanes C:H
  - PLL1 provides clocking for Ethernet switch

  - T104x supports the following network protocols through SerDes
    - QSGMII
    - 1000 Base-KX
    - SGMII 2.5x
    - SGMII

QSGMII (Quad Serial Gigabit Media Independent Interface)

The **QSGMII** is a method of combining four **SGMII** lines into a 5Gbit/s interface.

QSGMII uses significantly fewer signal lines than four **SGMII** busses



1000 Base-KX

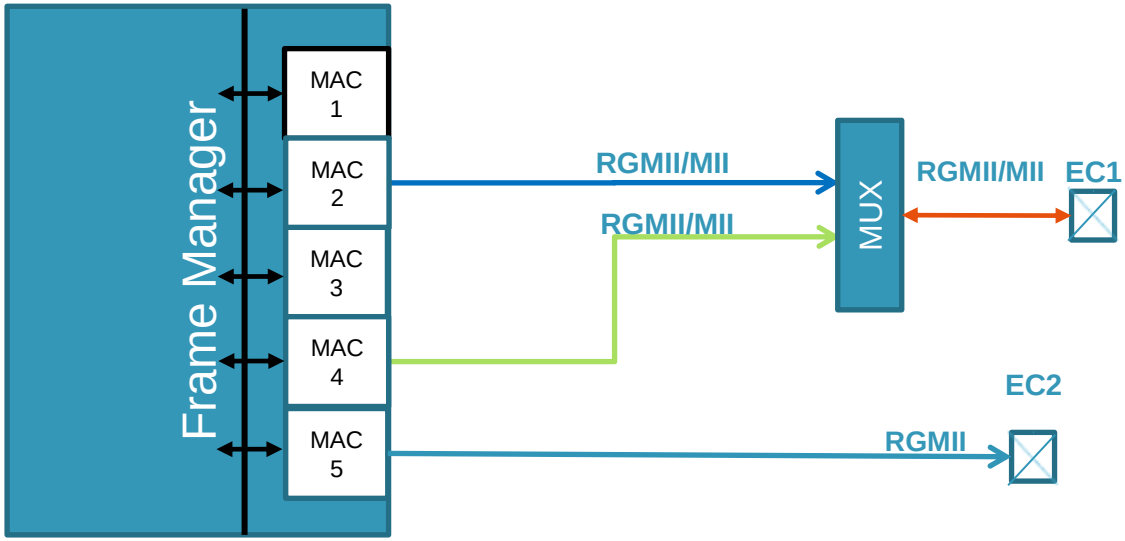
- IEEE 802.3ap standard for Ethernet Operation over Electrical Backplanes
- Supports Controlled impedance traces up to 1 m, including two connectors, on printed circuit boards
- Signaling speed - 1.25Gbaud on 2 lanes (TX and RX)
- 8B10B coding
- No transmitter or receiver equalization
- New Auto-Negotiation support
- No Forward Error Correction

SGMII 2.5x

- T1042 supports SGMII 2.5x on two FMAN ports, MAC1 and MAC2.
- 2.5 Gbps data rate is supported on SGMII 2.5x
- SGMII MAC runs at 312.5MHz for supporting 2500MHz data rate.

MAC Allocation for Parallel Interface - RGMII/MII

- 2x RGMII or 1x MII interface supported.
- MII/RGMII selection for EC1 via RCW**[EC1]** field.
- MAC2 or MAC4 selection for EC1 via RCW**[MAC2_GMII_SEL]** field
- RGMII interface enabled for EC2 via RCW**[EC2]** field.



T1040/20 SerDes Lane Multiplexing

With Ethernet switch

SRDS_PRTCL_S1 RCW[128:135]	Lane A	Lane B	Lane C	Lane D	Lane E	Lane F	Lane G	Lane H	Parallel Port Availability
69	PCIe1 (5/2.5)	SGMII (m3)	QSGMII (s1-4)	QSGMII (s5-8)	PCIe2 (5/2.5)	PCIe3 (5/2.5)	SGMII (m4)	SATA1	**RGMII (FMAN MAC#5) RGMII (FMAN MAC#2, MAC#5**
66	PCIe1 (5/2.5)	SGMII (m3)	QSGMII (s1-4)	QSGMII (s5-8)	PCIe2 (5/2.5)	PCIe3 (5/2.5)	PCIe4 (5/2.5)	SATA1	**2 RGMII (FMAN MAC #4 & #5)**
67	PCIe1 (5/2.5)	SGMII (m3)	QSGMII (s1-4)	QSGMII (s5-8)	PCIe2 (5/2.5)	PCIe3 (5/2.5)	PCIe4 (5/2.5)	SGMII (m5)	**1 RGMII (FMAN MAC #4)**
60	PCIe1 (5/2.5)	SGMII (m3)	QSGMII (s1-4)	QSGMII (s5-8)	PCIe2 (5/2.5)				**2 RGMII (FMAN MAC #4 & #5)**
8D	PCIe1 (5/2.5)	SGMII (s3)	SGMII (s1)	SGMII (s2)	PCIe2 (5/2.5)	SGMII (s6)	SGMII (s4)	SGMII (s5)	**2 RGMII (FMAN MAC #4 & #5)**
89	PCIe1 (5/2.5)	SGMII (s3)	SGMII (s1)	SGMII (s2)	PCIe2 (5/2.5)	PCIe3 (5/2.5)	SGMII (s4)	SATA1	**2 RGMII (FMAN MAC #4 & #5)**

- Ethernet switch connects with FMAN using MAC#1 and/or MAC#2
- MAC#2 used as additional RGMII port if Ethernet switch connected through MAC#1 only
- MAC#1 and MAC#2 are 2.5G ports.

LEGEND
"mn" indicates MAC# from FMan
"sn" indicates MAC# from Ethernet switch

T1042/22 SerDes Lane Multiplexing

- Without Ethernet switch

SRDS_PRTCL_S1 RCW[128:135]	Lane A	Lane B	Lane C	Lane D	Lane E	Lane F	Lane G	Lane H	Parallel Port availability
86	PCIe1 (5/2.5)	SGMII (m3)	SGMII (m1)	SGMII (m2)	PCIe2 (5/2.5)	PCIe3 (5/2.5)	PCIe4 (5/2.5)	SATA1	2 RGMII (FMAN MAC #4 & #5)
87	PCIe1 (5/2.5)	SGMII (m3)	SGMII (m1)	SGMII (m2)	PCIe2 (5/2.5)	PCIe3 (5/2.5)	PCIe4 (5/2.5)	SGMII (m5)	1 RGMII (FMAN MAC #4)
A7	PCIe1 (5/2.5)	SGMII (m3)	SGMII (m1) 2.5G	SGMII (m2) 2.5G	PCIe2 (5/2.5)	PCIe3 (5/2.5)	PCIe4 (5/2.5)	SGMII (m5)	1 RGMII (FMAN MAC #4)
AA	PCIe1 (5/2.5)	SGMII (m3)	SGMII (m1) 2.5G	SGMII (m2) 2.5G	PCIe2 (5/2.5)	PCIe3 (5/2.5)	SGMII (m4)	SGMII (m5)	0 RGMII
40	PCIe1 (5/2.5)		SGMII (m1)	SGMII (m2)	PCIe2 (5/2.5)				2 RGMII (FMAN MAC #4 & #5)
06	PCIe1 (5/2.5)				PCIe2 (5/2.5)	PCIe3 (5/2.5)	PCIe4 (5/2.5)	SATA1	2 RGMII (FMAN MAC #4 & #5)
08	PCIe1 (5/2.5)				PCIe2 (5/2.5)	PCIe3 (5/2.5)	SATA2	SATA1	2 RGMII (FMAN MAC #4 & #5)
8F	PCIe1 (5/2.5)	SGMII (m3)	SGMII (m1)2.5G	SGMII (m2)2.5G			SGMII (m4)	SGMII (m5)	0 RGMII
85	PCIe1 (5/2.5)	SGMII (m3)	SGMII (m1)	SGMII (m2)	PCIe2 (5/2.5)		SGMII (m4)	SGMII (m5)	0 RGMII
A5	PCIe1 (5/2.5)	SGMII (m3)	SGMII (m1) 2.5G	SGMII (m2) 2.5G	PCIe2 (5/2.5)		SGMII (m4)	SGMII (m5)	0 RGMII
00	PCIe1 (5/2.5)				PCIe2 (5/2.5)				2 RGMII (FMAN MAC #4 & #5)

LEGEND
"mn" indicates MAC# from FMan

T104x SerDes supported protocols

Product	QSGMII	SGMII	SGMII 2.5x	PCIe (2.0)	SATA	1000Base-Kx
T1040	2	6	-	4	2	Supported
T1042	-	5	2	4	2	Supported
T1020	2	6	-	4	2	Supported
T1022	-	5	2	4	2	Supported

- QSGMII support only on Ethernet switch ports.
- SGMII support on both Ethernet switch and FMAN MAC
- Numbers indicate the maximum that can be supported.

PCIe

PCIe Controller	Gen1 rate	Gen 2 Rate
PCIe1	RC/EP x4, x2, x1	
PCIe 2	RC/EP x4, x2, x1	
PCIe 3	RC/EP x1	
PCIe 4	RC/EP x1	

SATA

- Two SATA controllers supporting 1.5G/3.0G

Exceptions of Serdes protocol muxing

- SGMII 2.5x and SATA are mutually exclusive.
- QSGMII and SGMII from switch are mutually exclusive
- Spread spectrum is not supported on SGMII and SATA. When mixing any non spread spectrum protocol with PCIe, Spread spectrum should not be used.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