May, 2010

Migrating from PowerQUICC II Pro to QorIQ P1 / P2 and H/W Design Guide

Haim Cohen
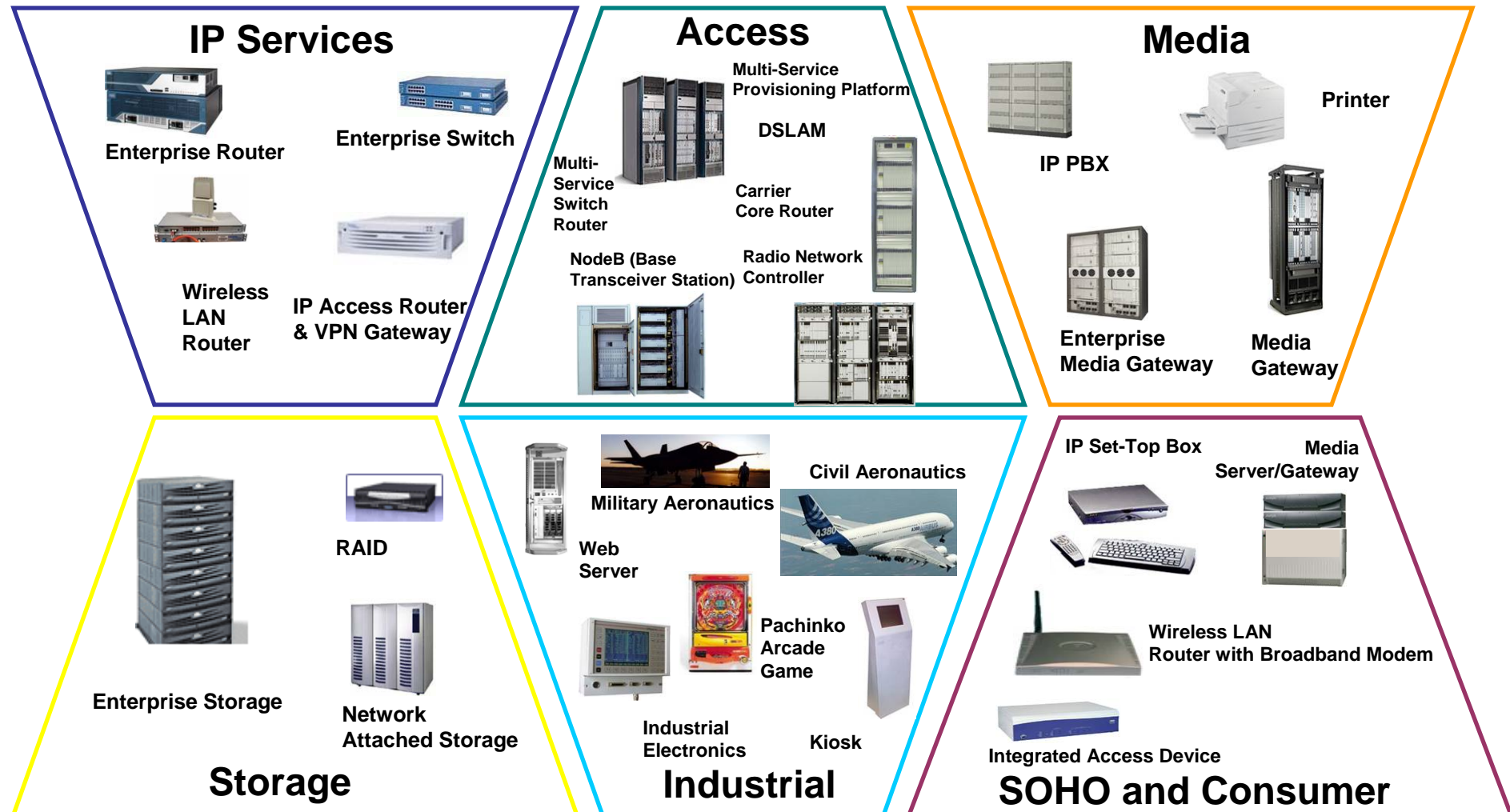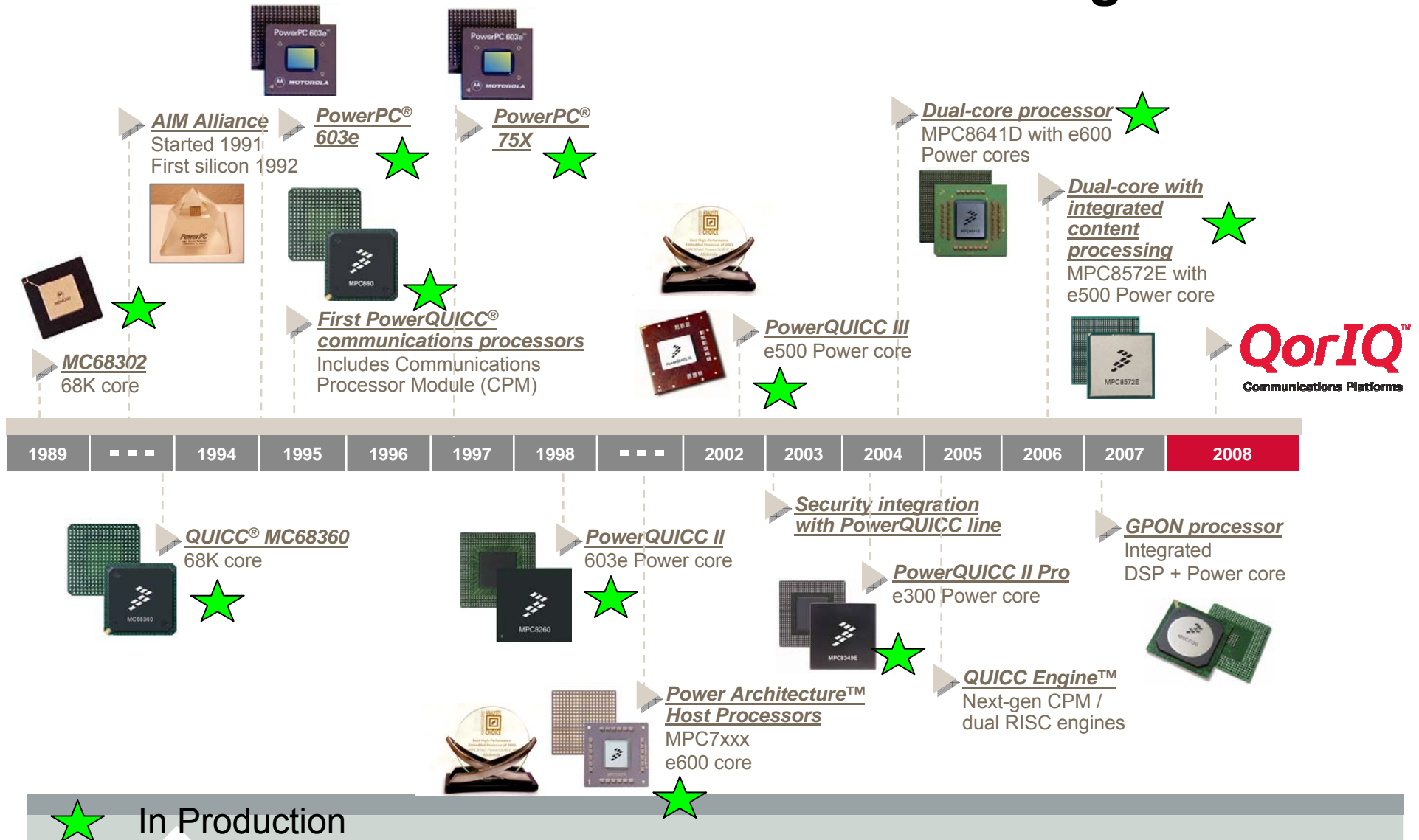
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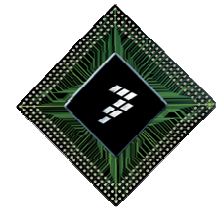
Session Objectives

This session will:

- Provide overview and highlight the new features introduced with the QorIQ™ P1 and P2 device family of processors

- Provide the detail and guidance on migrating designs from PowerQUICC II Pro™ to the QorIQ™ family

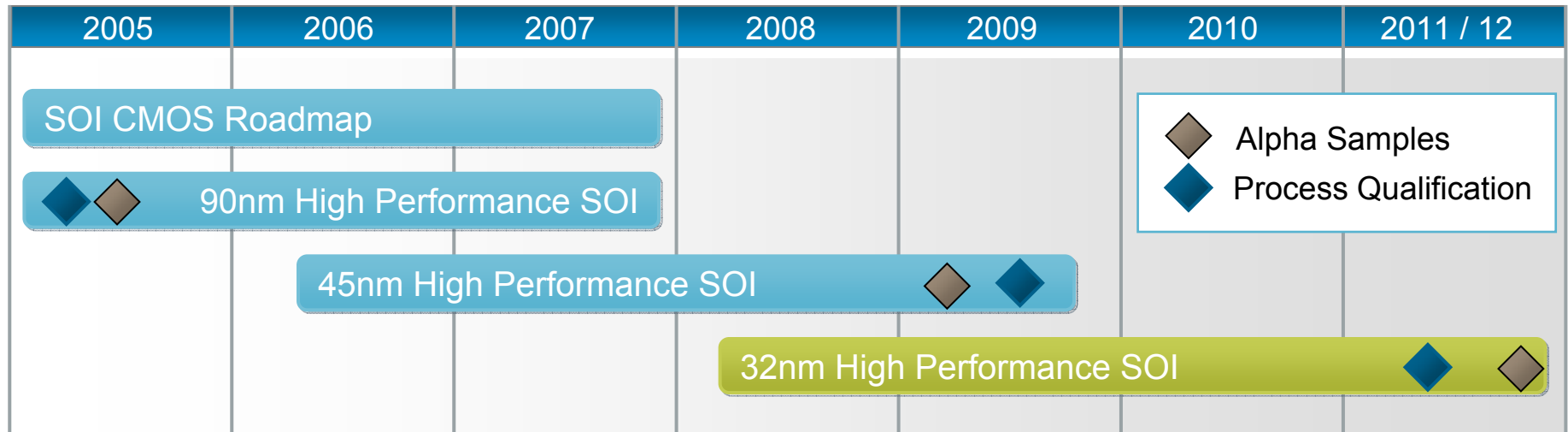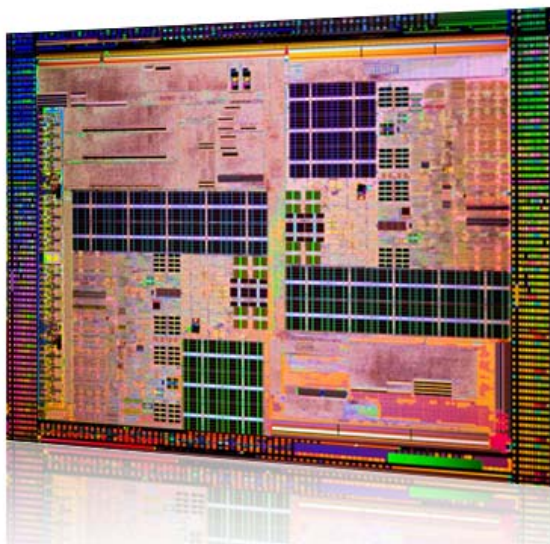- Provide overview on H/W design guide for QorIQ™ P2020

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Focus Freescale Market Segments

IP Services

Enterprise Router

Enterprise Switch

Wireless LAN Router

IP Access Router & VPN Gateway

Access

Multi-Service Provisioning Platform

DSLAM

Multi-Service Switch Router

Carrier Core Router

NodeB (Base Transceiver Station)

Radio Network Controller

Media

IP PBX

Printer

Enterprise Media Gateway

Media Gateway

Storage

RAID

Enterprise Storage

Network Attached Storage

Industrial

Military Aeronautics

Civil Aeronautics

Web Server

Pachinko Arcade Game

Industrial Electronics

Kiosk

SOHO and Consumer

IP Set-Top Box

Media Server/Gateway

Wireless LAN Router with Broadband Modem

Integrated Access Device

20 Years of Communications Processing Evolution

AIM Alliance
Started 1991
First silicon 1992

PowerPC® 603e

PowerPC® 75X

Dual-core processor
MPC8641D with e600 Power cores

Dual-core with integrated content processing
MPC8572E with e500 Power core

MC68302
68K core

First PowerQUICC® communications processors
Includes Communications Processor Module (CPM)

PowerQUICC III
e500 Power core

QorIQ™
Communications Platforms

1989	- - -	1994	1995	1996	1997	1998	- - -	2002	2003	2004	2005	2006	2007	2008

QUICC® MC68360
68K core

PowerQUICC II
603e Power core

Security integration with PowerQUICC line

PowerQUICC II Pro
e300 Power core

GPON processor
Integrated
DSP + Power core

Power Architecture™ Host Processors
MPC7xxx
e600 core

QUICC Engine™
Next-gen CPM /
dual RISC engines

⭐ In Production

SOI CMOS Technology Roadmap

2005	2006	2007	2008	2009	2010	2011 / 12

SOI CMOS Roadmap

◆ ◆ 90nm High Performance SOI

45nm High Performance SOI ◆ ◆

32nm High Performance SOI ◆ ◆

◆ Alpha Samples
◆ Process Qualification

90nm Dual Core Processor

45nm Dual Core
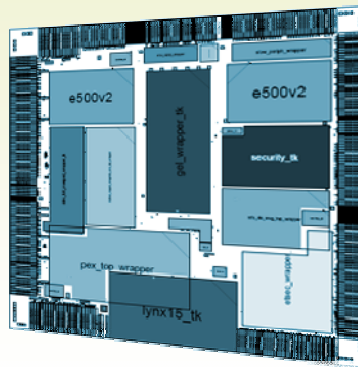
Same functionality and performance delivered today in C90SOI is 50% lower power in 45SOI

32nm Dual Core
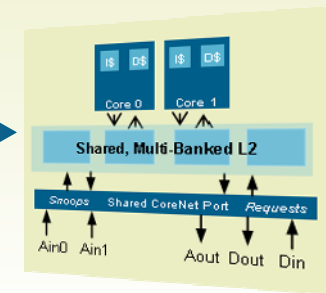
Same functionality and performance in 45SOI is 50% lower power in 32SOI

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QorIQ Platform Levels

PLATFORMS / PRODUCTS	DESCRIPTION	APPLICATION EXAMPLES		
QorIQ P5 PRODUCTS: To be announced	**Highest-performing embedded processors**	Service Provider Routers	Network Admission Control	Storage Networks
QorIQ P4 PRODUCTS: P4080 P4040	**Tap the full potential of multicore with this "many-core" platform**	Metro Carrier Edge Router / IMS Controller	Radio Network Control	Serving Node Router (GSN)
QorIQ P3 PRODUCTS: To be announced	**Your first step into true multicore performance**	Converged Media Gateway	SSL, IPSec, Firewall	Access Gateway
QorIQ P2 PRODUCTS: P2020 P2010	**Unprecedented performance per watt in this highly integrated platform**	Unified Threat Management / VoIP Carrier-Class Media Gateway	Wireless Media Gateway	Basestation
QorIQ P1 PRODUCTS: P1020 P1011 P1021 P1012 P1022 P1013	**A highly integrated, cost-effective, low power platform**	Integrated Services Router	Network Attached Storage	Home Media Hub

PowerQUICC Migration to QorIQ™ Platforms
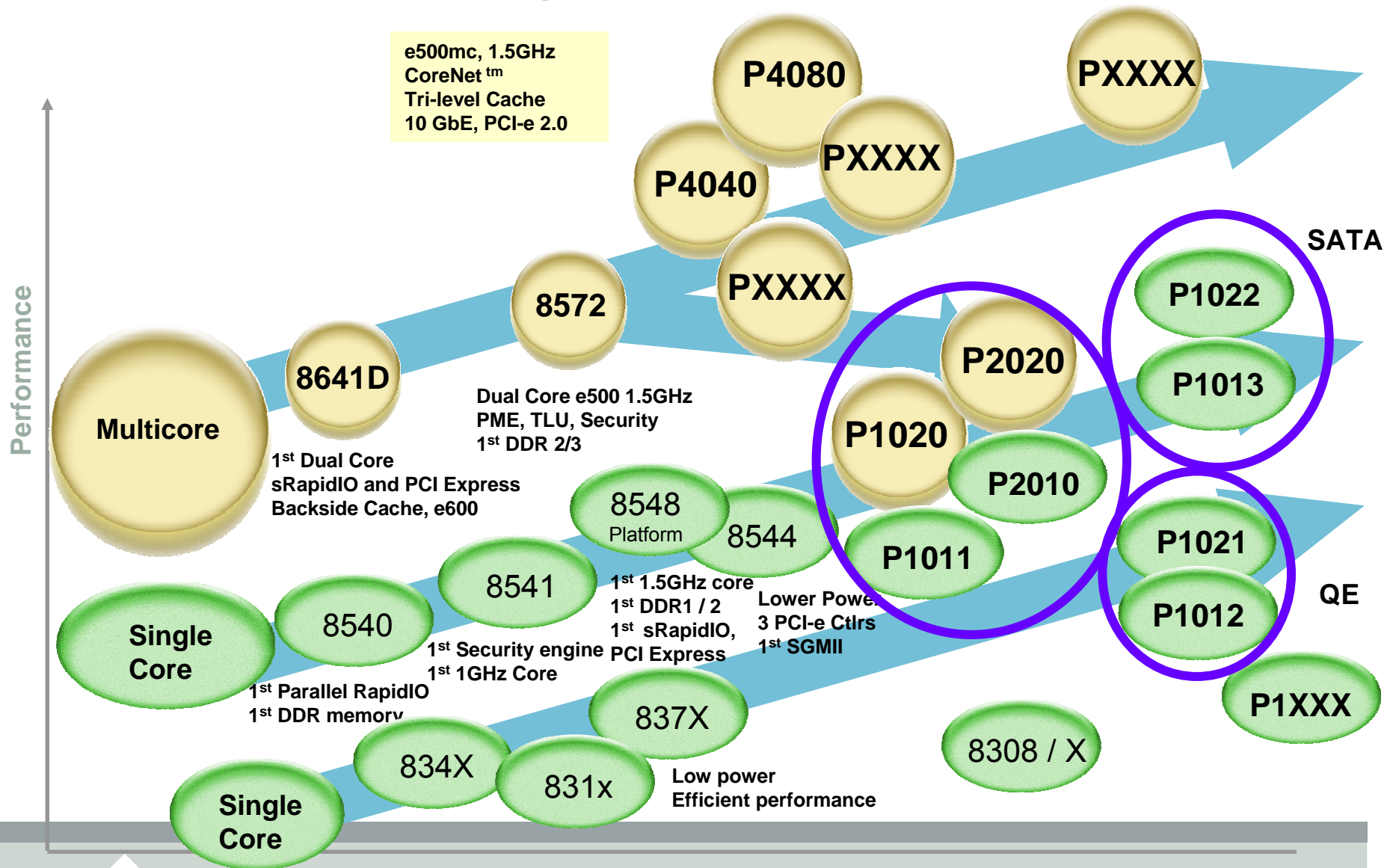
PowerQUICC II Pro to QorIQ Evolution

Performance & Power

Legend
- 45nm
- 90nm
- 130nm

MPC8349E

MPC8347E

MPC8343E

266-667MHz
2 x GigE
2 x PCI
USB, DDR1/2,
Security
<5.0W @ 667MHz

MPC8313E

333MHz
2 x GigE (SGMII)
PCI, USB, DDR1/2,
Security
<2.0W @ 333MHz

MPC8378E

MPC8379E

MPC8377E

400-800MHz
2 x GigE (SGMII)
PCI , PCI-Exp
USB, DDR1/2,
Security, SATA
<5.0W @ 667MHz

MPC8315E

MPC8314E

400MHz
2 x GigE (SGMII)
PCI, PCI-Exp
USB, DDR1/2,
Security
<2.0W @ 400MHz

P2020E

P2010E

e500 @800MHz-1200MHz
Dual-core / Single core
512KB L2 Cache,
3 x GigE (SGMII), 2x PCI-Exp,
2x SRIO, 2 x USB,
DDR2/3, SD FLASH, Security,
8W @ DC 1200MHz

P1020E

P1011E

e500 @533MHz-800MHz
Dual-core / Single-core
256KB L2 Cache
3 x GigE (SGMII), PCI-Exp, 2 x USB,
DDR2/3, SD FLASH, Security, TDM
5.0W for Dual-Core 800MHz

4 Devices – All pin compatible

2006   2007   2008   2009   2010   2011

Proposal   Planning   Execution   Production

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Introducing Freescale's QorIQ platforms

Designed to enable the development of the next era of networking applications by delivering

- Improved Processing Performance - High-performance Power® Architecture based multicore solutions
- Power-Efficiency - 45nm process technology for industry-leading power-to-performance solution
- Programmability - Programming tools, ecosystem partners, common software and pin compatible processors

P2020
Wire Bond TEPBGA-II
~100M transistors
>1B vias and contacts
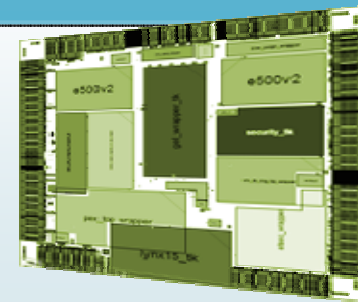
1st silicon in house

Teams validating part at component and board level

Alpha samples launched in February 2009

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QorIQ P2020/10 Block Diagram

P2020 only

Security Accel / XOR

e500 Core — 32KB I-Cache, 32KB D-Cache

512KB L2

e500 Core — 32KB I-Cache, 32KB D-Cache

Coherency Module

System Bus

DDR2/DDR3, SDRAM Controller — 64b

Enhanced Local Bus — 16b

Perf Mon, DUART, MPIC 2x I2C, Timers

USB2.0

SD/MMC

eSPI

3x GE MAC

On-Chip Network

2x DMA | PCI Express | PCI Express | PCI Express | Serial RapidIO | Serial RapidIO

SGMII

x4 SerDes

Red = New
Green = Enhanced
Blue = Same
(Compared to PQ2 Pro)
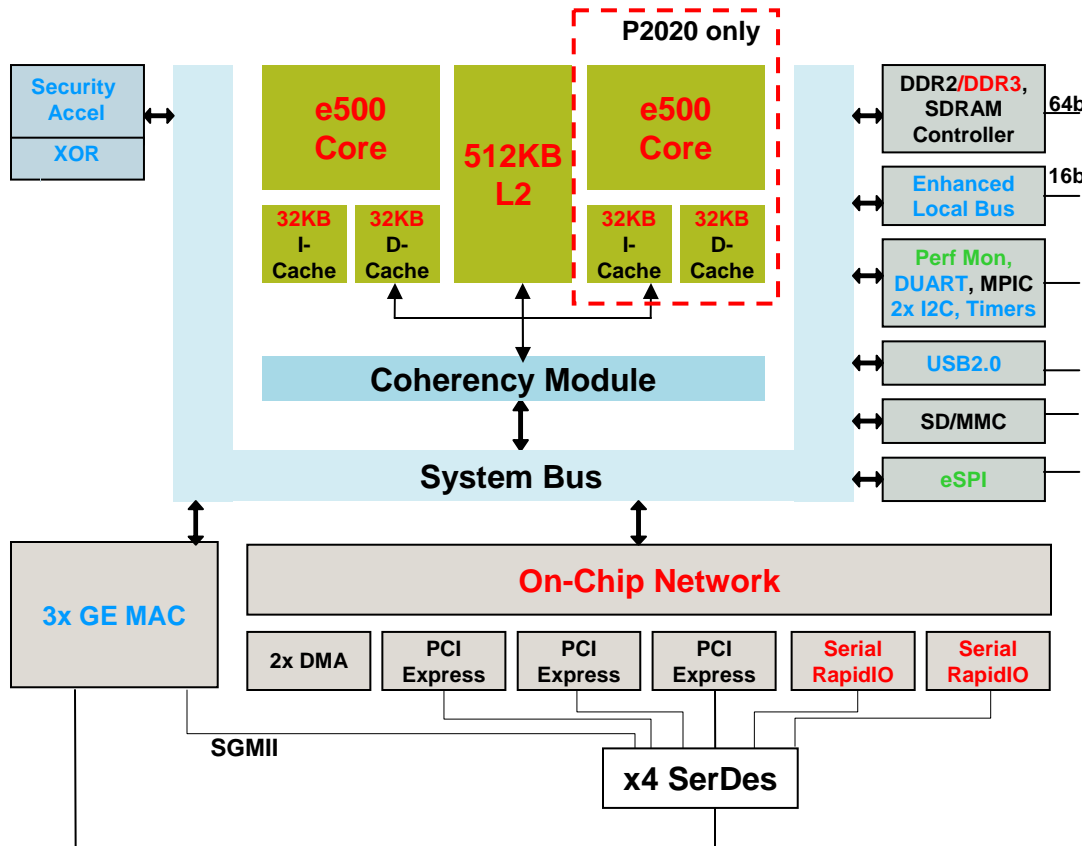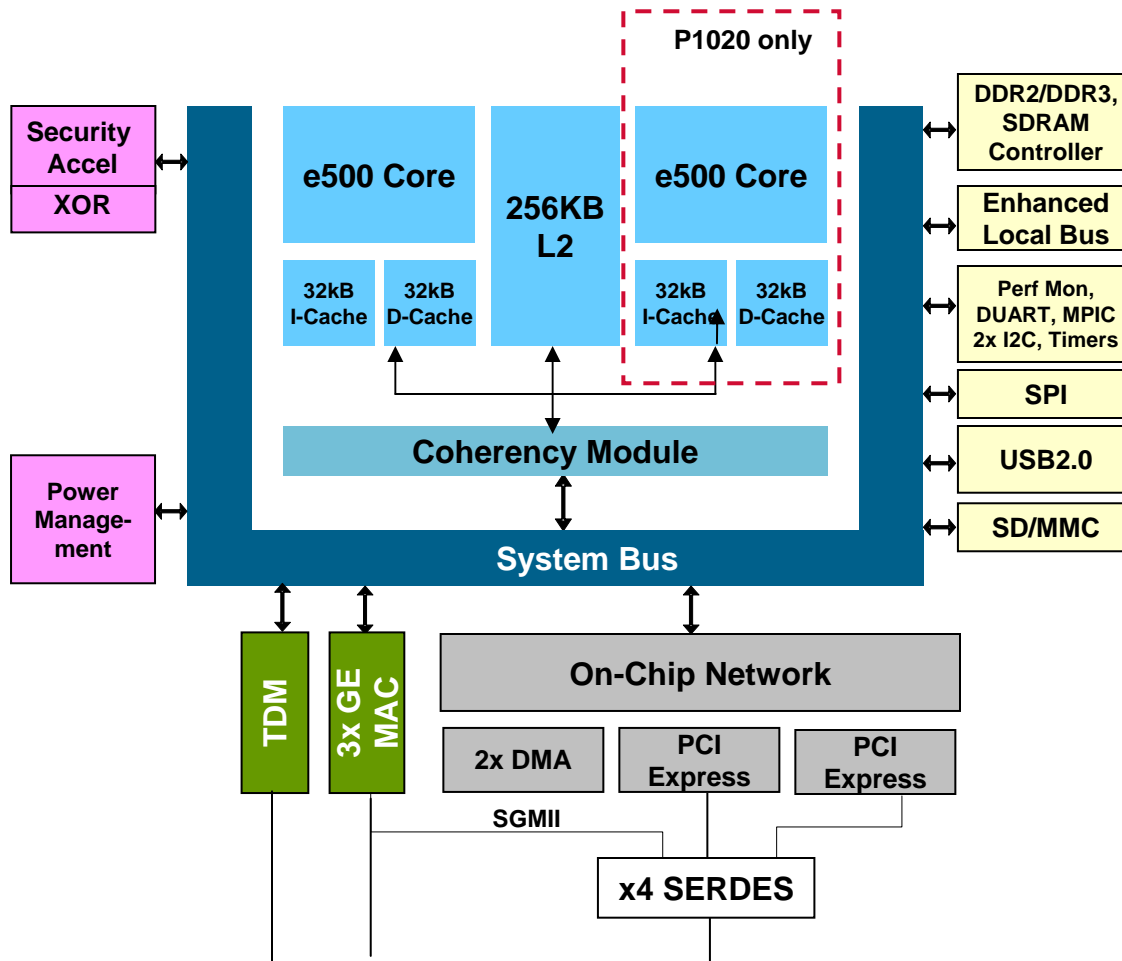
- **Single/Dual e500 Power Architecture™ core**
  - 800 - 1200 MHz
  - 512KB Frontside L2 cache w/ECC, HW cache coherent
  - 36 bit physical addressing, DP-FPU
- **System Unit**
  - 64/32b DDR2/DDR3 with ECC
  - Integrated SEC 3.1 Security Engine
  - Open-PIC Interrupt Controller, Perf Mon, 2x I2C, Timers, 16 GPIO's, DUART
  - 16-bit Enhanced Local Bus supports booting from NAND Flash
  - One USB 2.0 Host Controller with ULPI interface
  - eSPI controller supporting booting from SPI serial Flash
  - SD/MMC card controller supporting booting from Flash cards
  - Three 10/100/1000 Ethernet Controllers (eTSEC) w/ Jumbo Frame support, SGMII interface
    - Enhanced features: Parser/Filer, QOS, IP-Checksum Offload, Lossless Flow Control
    - IEEE 1588v2 support
  - Two Serial Rapid I/O Controllers with integrated message unit operating up to 3.125GHz
  - Three PCI Express 1.0a Controllers operating at 2.5GHz
- **Process & Package**
  - 45nm SOI, 1.05V +/- 50mV, 0C to 125C Tj
    - with -40C to 125C Tj option
  - 689-pin TePBGAII, 31x31mm
- **8.0 W (Est) - Dual Core at 1.2GHz**

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QorIQ1020 / P1011 Block Diagram

- **Single / Dual e500 Power Architecture® core; 533 - 800 MHz**
  - 256KB Frontside L2 cache w/ECC, HW cache coherent
  - 36 bit physical addressing, DP-FPU
- **System Unit**
  - 32-bit DDR2/DDR3, 667 MHz data rate w/ECC
  - Integrated SEC 3.3 Security Engine
  - Open-PIC Interrupt Controller, Perf Mon, 2x I2C, Timers, 16 GPIO's, DUART
  - 16-bit Enhanced Local Bus supports booting from NAND Flash
  - Two USB 2.0Controllers Host/Device support
  - SPI controller supporting booting from SPI serial Flash
  - SD/MMC card controller supporting booting from Flash cards
  - TDM interface
  - Three 10/100/1000 Ethernet Controllers (eTSEC) w/ Jumbo Frame support, SGMII interface
    - Enhanced features: Parser/Filer, QOS, IP-Checksum Offload, Lossless Flow Control with Interface options:
      - IEEE1588v2 Support
  - Two PCI Express 1.0a Controllers operating up to 2.5Gbps
  - Power Management
- **Process & Package**
  - 45nm SOI, 0.95V+/-50mV, -40C to 125C Tj
  - 689-pin TePBGAII

- **5.0 W (Est) – Dual Core @ 800MHz**

MPC834x/831x to QorIQ P1 Migration

Feature	MPC8343E	MPC8313E	MPC8314E/ MPC8315E	P1020E / P1011E
Core	e300	e300	e300	Dual / Single e500v2
CPU Speed	Up to 400MHz	Up to 400 MHz	Up to 400 MHz	533MHz - 800MHz
L1 I/D Cache	32K I/D	16K I/D	16K I/D	32K I/D
L2 Cache	-	-	-	256K I/D
Memory Controller	32/64 bit DDR2 up to 333MHz	16/32 bit DDR/2 up to 333MHz	16/32 bit DDR/2 up to 266MHz	32 bit DDR2/3 ,up to 667MHz
Ethernet	2-10/100/1000 (MII, RGMII & RTBI only)	2-10/100/1000 with SGMII	2-10/100/1000 with SGMII	3-10/100/1000 with SGMII
Local Bus	8/16/32-bit ROM boot	8/16-bit/66MHz w/ NAND & NOR Boot	8/16-bit/66MHz w/ NAND & NOR Boot	8/16/32-bit 83MHz w/ NOR, 8/16-bit NAND Boot
PCIE	-	-	x2 supported	2 Controllers, up to x4 lanes
SATA	-	-	x2 (MPC8315E only)	-
USB	Hi-Speed Host or Device	1 -2.0 Host or Device w/PHY	1 -2.0 Host or Device w/PHY	2 x 2.0 Host or Device
Security	E version only	SEC 2.2	SEC 3.3	SEC 3.3.1
Other	1x 32Bit / 66MHz PCI, Dual I2C, DUART, SPI Interrupt Controller	1x 32Bit / 66MHz PCI, Dual I2C, DUART, SPI Interrupt Controller, 2 SERDES Lanes	1x 32Bit / 66MHz PCI, Dual I2C, DUART, SPI Interrupt Controller, 2 SERDES Lanes	SD/MMC Support, TDM, DUART, Dual I2C, SPI, Interrupt controller 4 SERDES Lanes
Package	620 PBGA	516 TePBGA	620 TePBGA	689 TePBGA II
Power	<5W @ 667MHz	~2W @ 333MHz	~2W	~ 5 W (typ) @ 800MHz Dual Core
Samples	Now	Now	Now	May 2010
Production	Now	Now	Feb 2009	Q4 2010
Process	130nm	90nm	90nm	45nm

MPC837x to QorIQ P1 /P2 Migration

	MPC8379E	MPC8378E	MPC8377E	P1020 / P1011	P2020 / P2010
Core	e300	e300	e300	Dual e500v2 / Single e500v2	Dual e500v2 / Single e500v2
CPU Speed	Up to 800 MHz	Up to 800 MHz	Up to 800 MHz	533MHz - 800MHz	800MHz / 1200 MHz
L1 I/D Cache	32KI/ 32KD	32KI/32KD	32KI/32KD	32K I/D	32K I/D
L2 Cache				256K I/D	512K I/D
Memory Controller	32/64 bit DDR/2 up to 400MHz	32/64 bit DDR/2 up to 400MHz	32/64 bit DDR/2 up to 400MHz	32 bit DDR2/3 up to 667MHz	32/64 bit DDR2/3 up to 800MHz
Local bus	32 bit w/NAND boot support	32 bit w/NAND boot support	32 bit w/NAND boot support	8/16/32-bit 83MHz w/ NOR, 8/16-bit NAND Boot Support	8/16-bit/ 150MHz w/ NAND & NOR Boot
PCI	1-32 bit up to 66MHz (2.3)	1-32 bit up to 66MHz (2.3)	1-32 bit up to 66MHz (2.3)	-	-
PCI Express	-	2-x1	2-x1	2 PCIE (1.0a) Controllers Up to x4 Lanes	3 PCIE (1.0a) Controllers Up to x4 Lanes
SATA	4x1 SATA 2.0 w/PHY	-	2x1 SATA 2.0 w/PHY	-	-
Ethernet	2-10/100/1000 (RGMII, RTBI, RMII, MII)	2-10/100/1000 (SGMII, RGMII, RTBI, RMII, MII)	2-10/100/1000 (RGMII, RTBI, RMII, MII)	3-10/100/1000 with SGMII support	3-10/100/1000 with SGMII support
USB	1- 2.0 Host or Device	1-2.0 Host or Device	1- 2.0 Host or Device	2 x 2.0 Host or Device	1 x 2.0 Host or Device
Security	SEC 3.0	SEC 3.0	SEC 3.0	SEC 3.3.1	SEC 3.1
Other	Dual UART Dual I2C Interrupt Controller	Dual UART Dual I2C Interrupt Controller	Dual UART Dual I2C Interrupt Controller	SD/MMC, TDM, Dual UART Dual I2C Interrupt Controller	SD/MMC, Dual UART, Dual I2C Interrupt Controller
Package	Te PBGA	Te PBGA	Te PBGA	689 TePBGA II	689 TePBGA II
General Samples	Oct 2007	Oct 2007	Oct 2007	May 2010	Now
Production	NOW	NOW	NOW	Q4 2010	July 2010

QorIQ™ P1 Series Comparison

	P1011	P1020	P1012	P1021	P1013	P1022
CPU	e500 Up to 800MHz 32K I/D	e500 Up to 800MHz 32K I/D	e500 Up to 800MHz 32K I/D	e500 Up to 800MHz 32K I/D	e500 Up to 1000MHz 32K I/D	e500 Up to 1000MHz 32K I/D
L2 Cache	256KB	256KB	256KB	256KB	256KB	256KB
DDR I/F Type/Width	DDR2/3 32-bit	DDR2/3 32-bit	DDR2/3 32-bit	DDR2/3 32-bit	DDR2/3 32/64-bit	DDR2/3 32/64-bit
10/100/1000 (with IEEE1588v2	3 w/(2) SGMII	3 w/(2) SGMII	3 w/(2) SGMII	3 w/(2) SGMII	2 w/(2) SGMII	2 w/(2) SGMII
TDM/I2S	Yes	Yes	Yes	Yes	Yes	Yes
PCI Express 1.0a	2 controllers w/ 4 SERDES	2 controllers w/ 4 SERDES	2 controllers w/ 4 SERDES	2 controllers w/ 4 SERDES	3 controllers w/ 4 SERDES	3 controllers w/ 4 SERDES
USB 2.0	2	2	1	1	2	2
Memory Card	SD/MMC	SD/MMC	SD/MMC	SD/MMC	SD/MMC	SD/MMC
GPIO	16	16	16	16	87	87
SATA	-	-	-	-	Yes	Yes
LCD Controller	-	-	-	-	Yes	Yes
Other Interfaces	SPI, 2x I2C, DUART	SPI, 2x I2C, DUART	SPI, 2x I2C, DUART	SPI, 2x I2C, DUART	SPI, 2x I2C, DUART	SPI, 2x I2C, DUART
QUICC Engine	-	-	Yes	Yes	-	-
Accelerators	SEC3.3	SEC3.3	SEC3.3	SEC3.3	SEC3.1	SEC3.1
Power Management	Doze, Nap, Sleep	Doze, Nap, Sleep	Doze, Nap, Sleep	Doze, Nap, Sleep	Doze, Nap, Sleep, Jogm Oacket-lossless Deepsleep	Doze, Nap, Sleep, Jogm Oacket-lossless Deepsleep
Typical Power	3W	3.5W	3.2W	3.7W	3W	<4W
Package	689 TePBGAII	689 TePBGAII	689 TePBGAII	689 TePBGAII	689 TePBGAII	689 TePBGAII

Challenges of Migration

Before we move on, lets consider what are some of the challenges of design migration…

Hardware design
- Power supply design
- What level of actual re-design is required?
    - Can I use existing interfaces?
    - What are the requirements for new interfaces?
- Power management and thermal performance
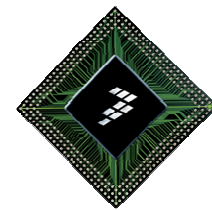- Future-proofing and design re-use for other platforms

Software design
- Code set migration. Instructions set, library and function support
- Operating system and tool support
- Software portability and level of re-coding for new features

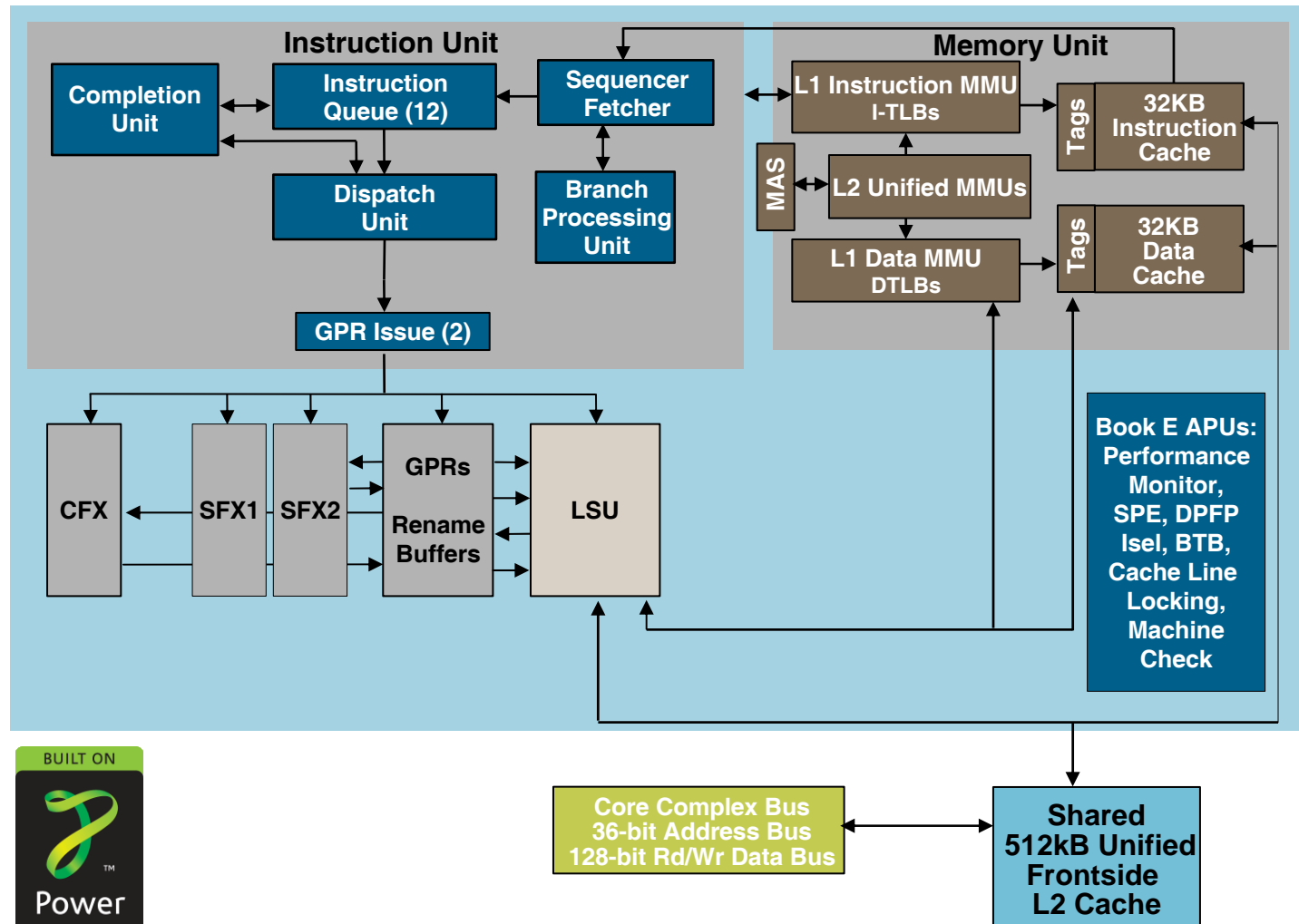Migrating to dual and multi-core

QorIQ P1 / P2 Device Features

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e500v2 Core Architecture

- Up to 1.2 GHz
- L1: 32KB, 8-way set associative, Parity
- L2: 512KB, Front Side: 8-way set associative, ECC
- Cache line locking supported
- MESI cache coherence
- Peak IPC 2 Instructions plus 1 branch
- Out of Order Execution
- Multiple Book E APUs
- 16 TLB variable page sizes
- 512-entry 4K Pages
- 36-bit Physical Address

Instruction Unit

- Completion Unit
- Instruction Queue (12)
- Sequencer Fetcher
- Dispatch Unit
- Branch Processing Unit
- GPR Issue (2)

CFX — SFX1 — SFX2 — GPRs Rename Buffers — LSU

Memory Unit

- L1 Instruction MMU I-TLBs
- MAS
- L2 Unified MMUs
- L1 Data MMU DTLBs
- Tags — 32KB Instruction Cache
- Tags — 32KB Data Cache

Book E APUs: Performance Monitor, SPE, DPFP Isel, BTB, Cache Line Locking, Machine Check

Core Complex Bus
36-bit Address Bus
128-bit Rd/Wr Data Bus

Shared 512kB Unified Frontside L2 Cache

BUILT ON Power

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L2 Cache Controller

Shared 256KB / 512 KB unified front-side L2 cache

Eight-way associatively (each way: 64 KB)

Assignment Granularity :
- One, two, four, or all eight "ways" of the cache can be assigned as the following:
- SRAM
- Stash-Only
- CPU0 L2 Only
- CPU1 L2 Only
- Both CPU0 and CPU1 L2

Stash-Only regions can now be defined
- Prevents stash data from polluting processor data and vice-versa
- One, two or four "ways" of the cache can be dedicated as Stash-Only

Stash Allocate Disable mode added
- Allows update of all resident cache lines without allocation of new lines

Example
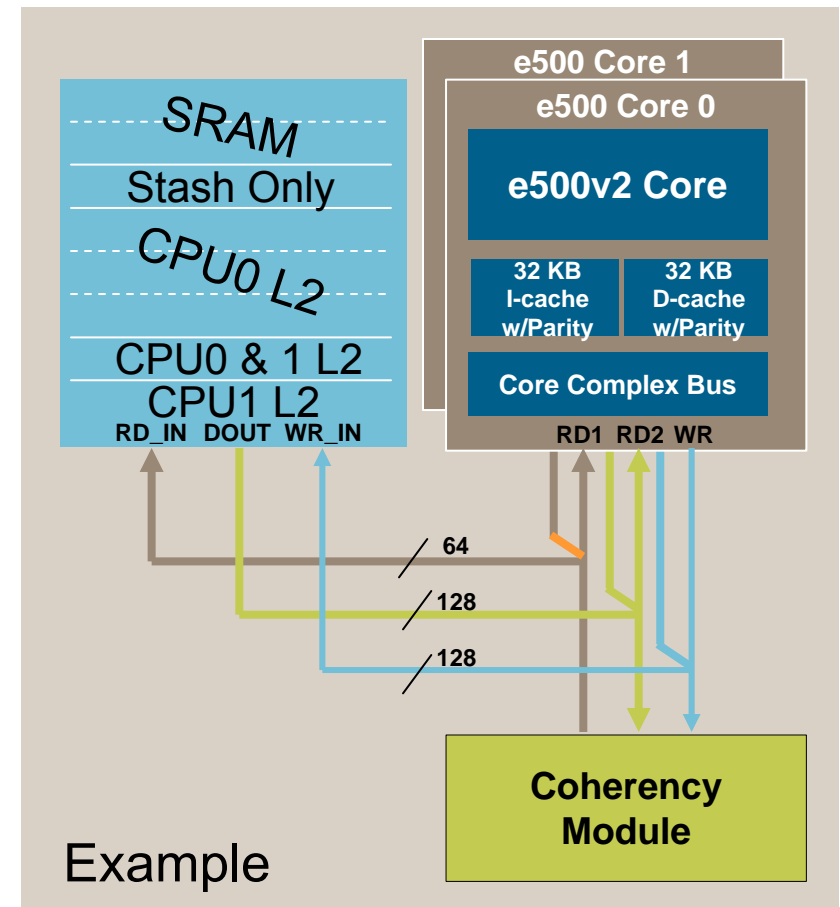
e500 Internal Busses

e300 uses internal coherent system bus CSB to interconnect cores and interfaces

Core Complex Bus (CCB) is evolution of CSB bus
- Offers extended addressing and enhanced data flow performance
- Used to connect e500 cores and caches together to the rest of device via ECM module

e500 Coherency Module (ECM)
- Module used to ensure coherency between e500 cache and external interfaces on the board
- Functions include queuing & buffering functions for CCB, arbitration across CCB and I/O masters, and transaction processing
  - Low-latency path between DDR controllers and cores / caches

On-Chip Network (OCeaN) Switch Fabric
- A multi-port, on-chip, non-blocking crossbar switch fabric designed for high-speed interconnects
  - 2.7GByte/s peak bandwidth per port

DDR Controller

QorIQ P1 / P2 platforms offer DDR2 & DDR3 support
- No DDR support – change from PowerQUICC II Pro

QorIQ P1020 / P1011
- Support 32-bit data bus configuration with ECC
- Support up to 667MHz DDR interface speed.
- Support for up to 4Gb devices, x8, x16, x32 configurations
- Max memory support of 8GB, with 2 memory banks supported

QorIQ P2020/P2010
- Support 64-bit and 32-bit data bus configuration with ECC.
- Support up to 800MHz DDR interface speed.
- Support for up to 4Gb devices, x8, x16, x32 configurations
- Max memory support 16GB, with 4 memory banks supported

Other common features
- Supports self-refresh mode
- Battery backup
- Initialization bypass
- Chip-select interleaving
- Automatic DRAM initialization
- Error injection
- On die termination

e500 Core | e500 Core

DDR2/DDR3, SDRAM Controller

ECM

System Bus

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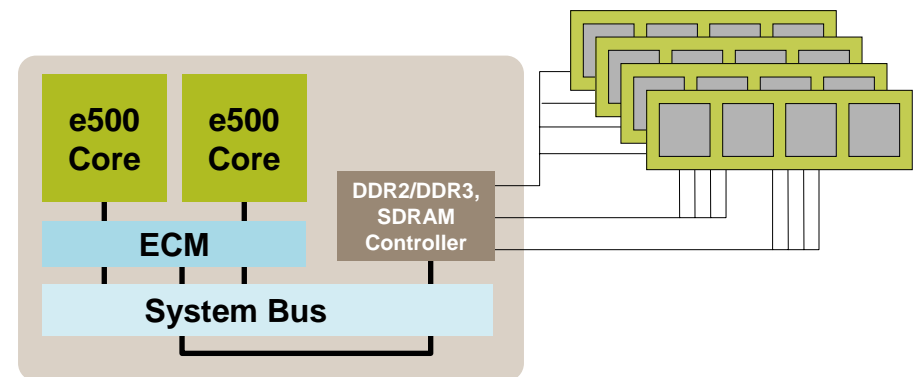
DDR Controller

DDR 3 – New feature

- Lower power performance – ~25% compared to DDR2 (Source - JEDEC)
- Supply voltage reduced from 1.8V to 1.5V.
- Support for "Fly by" routing,
  - Results in fewer stubs and improved signal integrity for faster clock speeds
- Introduced additional registers for write-levelling control for DDR3
- Asynchronous reset pin for cold or warm reset of memories
- Separate voltage reference pins for address and data signals for noise reduction
- Improved pin-out for signal integrity and reduced skew.
- Dynamic ODT for also aids signal integrity

DDR clocking – ability to asynchronously clock from platform clock supported for higher speed memory devices

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Enhanced Three-Speed Ethernet (eTSEC) Controllers

eTSEC MAC controllers support 10Mbps, 100Mbps, 1Gbps Ethernet /IEEE 802.3 interfaces
- Similar in specification to MPC831x & MPC837x devices

Backwards compatible with TSEC controllers used on MPC834x

Support following PHY interfaces
- GMII, RGMII, MII, TBI, RMII, RTBI, SGMII, & 8/16-bit FIFO mode
- SGMII interfaces share available SERDES lanes

Advanced functions part of enhanced controller:
- TCP/IP acceleration
- QOS support for up to 8 queues
- MAC address recognitions
- CRC generation & checking
- Extraction and allocation of data to L2 cache
- Remote monitoring statistics support

IEEE® 1588 Timer support

Interrupt virtualisation added to P1 devices
- eTSEC controllers and interrupts can be grouped, to be assigned to a particular core by software
- Further available information in software section

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Security

Embedded security block (SEC) used for off-loading computationally intensive security functions

Existing SEC architecture migrated to QorIQ P1 / P2 devices.

SEC block contains specialised execution unit for different encryption algorithms

- PKE – Public Key Encryption Unit
- AES – Advanced Encryption Standard Unit
- DES – Data Encryption Standard Execution Unit
- CRC – Cyclic Redundancy Check Unit
- MDE – Message Digest Execution Unit
- RNG – Random Number Generator
- SNOW3G & KASUMI - 2G/GSM & 3G encryption

Execution unit support varies depending on target silicon application

Backwards compatible driver support across various SEC engine versions
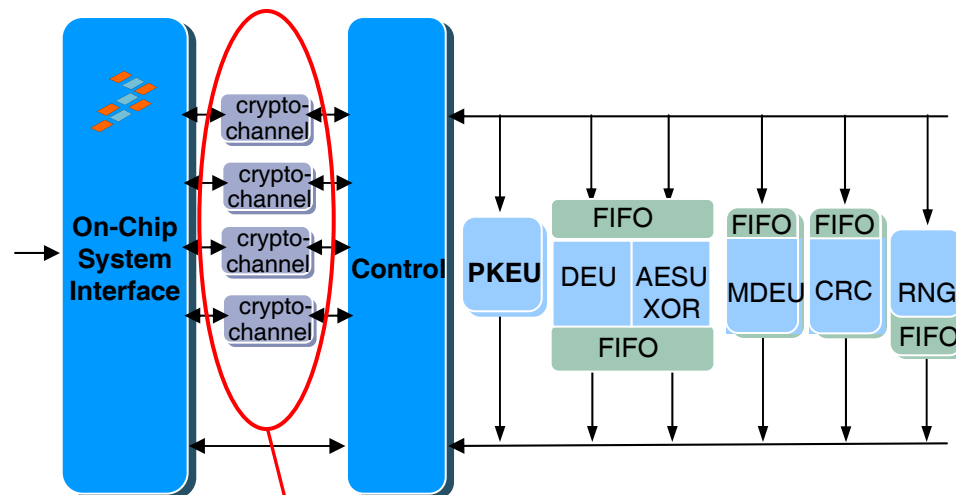
4 Crypto-channels are initiators and data fetchers for the SEC block

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SERDES Interfaces

SERDES interface is consistent with MPC831x / MPC837x devices
- Additional SERDES support added to QorIQ P1 & P2 devices
- 4 SERDES lanes shared across PCIe, SGMII, & SRIO controllers

PCI Express v1.0a
- Up to x4 lane support on P1 & P2 devices, supports 8Gbps(half-duplex) max data rate - as per PowerQUICC II Pro
- Up to 3 PCIe controllers available on P2 devices, for multiple configurations

Serial RapidIO – (P2 devices Only)
- New high-speed switched fabric for embedded systems
- Supports multiple lane configurations & speeds (1.25/2.5/3.125Gbauds)
- Max data rate of 10Gbps (half-duplex, 4x)

SGMII – Up to 2 SGMII interfaces **with** PCIe / SRIO support

PCI Express® Interface

PCI Express 1.0a compatible

Supports x1, x2, and x4 link widths @ 2.5 Gbaud, 2.0 Gb/s
- Auto-detection of number of connected lanes

Selectable as root complex or endpoint at initialization

32- and 64-bit addressing into PCI Express address space

Root complex inbound support for MSI and INTx

Endpoint support for outbound MSI

Reads/writes carried across ports, but not a switch

256 byte maximum payload size

One virtual channel

Strong and relaxed ordering rules

8 non-posted, 6 posted transactions

3 inbound + 1 configuration window
- Translates upper 52b of PCI addr to upper 24b of local addr
- Window sizes of 4 KB to 64 GB
- Settings: read/write type, prefetchable, and target
- 1 MB Config window maps to CCSR region

4 outbound + 1 default window
- Translates upper 24b of local addr to upper 52b of PCI addr
- Select I/O or memory for reads and writes
- Window sizes of 4 KB to 64 GB
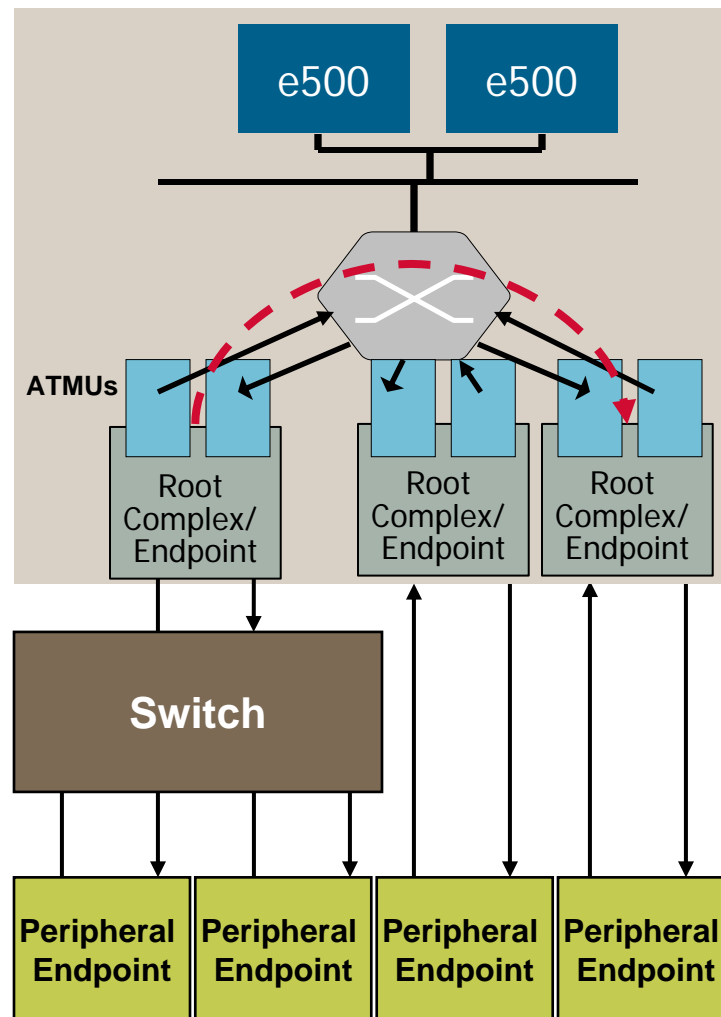
Enhanced Secure Digital Host Controller (eSDHC)

Memory card interface available on QorIQ Platforms
- Similar in specification to the eSDHC on MPC837x

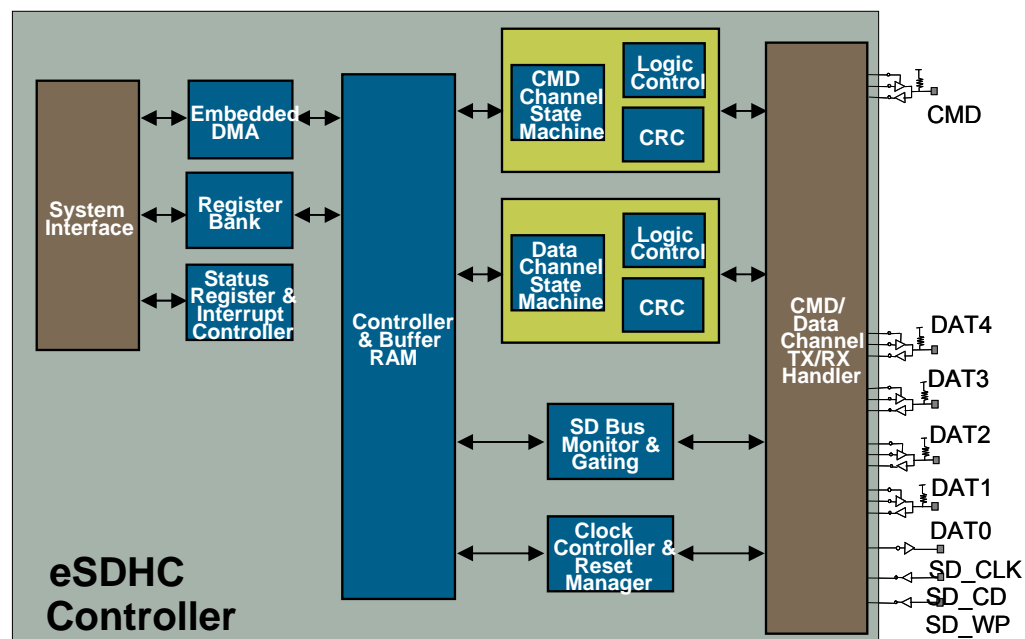Provides high-speed, flexible data storage capability to a system

Designed to work with various SD & MMC card formats
- SD, SDHC, miniSD, SD Combo, MMC, MMC*plus* & RS-MMC cards

Supports capacities of up to 32GB, with different speeds

Boot interface support – new feature
- On-chip ROM used to load device driver prior to loading of boot data from the card.

Programmable Interrupt Controller (PIC)

- Interrupts added between cores and for SRIO
- Interrupts based on OpenPIC architecture
- 16 interrupt priority levels (15 is highest)
  - Priority level is the reversed from PowerQUICC II Pro
- Critical interrupts

Performance monitoring

- Core performance monitoring available from PowerQUICC II Pro
- Device performance monitoring available as well on QorIQ / PowerQUICC III devices
- Debug and monitor events on DDR, DMA, ECM bus, PCIe & other interfaces

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Additional Interfaces (Continue)

DMA Controller

- 4 channel DMA controller located on OCeaN switched fabric
- Used for internal data movement and external movement to/from the device
- Accessible by all cores, all internal interfaces and external masters
- 2 DMA controllers available on P2020 for additional I/O performance

USB

- High-speed USB 2.0 interface, with host or device support
  - USB on-the-go capability supported as well.
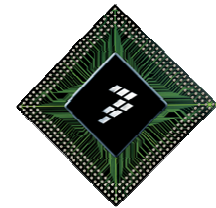- Supports ULPI interface to an external PHY

eSPI controller

- Interface consistent with PowerQUICC II Pro device family

Local Bus – Enhanced local bus controller

- Supports 8-bit / 16-bit interface with NAND / NOR Flash support

Hardware Design Considerations

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Hardware Design
Electrical Specifications

Description	Symbols	MPC831x	MPC837x	QorIQ P1	QorIQ P2
Core	VDD	1.0V	1.0V	0.95V	1.05V
PLL supply	AVDD	1.0V	1.0V	0.95V	1.05V
SERDES Core Supply	SVDD / XCOREVDD	1.0V	1.0V / 1.05V***	0.95V	1.05V
SERDES pad supply	XVDD / XPADVDD	1.0V	1.0V / 1.05V***	0.95V	1.05V
DDR2 / DDR3 I/O	GVDD	1.8V / -	1.8V / -	1.8V / 1.5V	1.8V / 1.5V
Ethernet I/O	LVDD	3.3V / 2.5V	3.3V / 2.5V	3.3V / 2.5V	3.3V / 2.5V
DUART, system control, I²C, GPIO, JTAG	OVdd / NVdd	3.3V	3.3V	3.3V	3.3V
Local Bus	BVDD / NVDD	3.3V	3.3V / 2.5V /1.8V	3.3V / 2.5V /1.8V	3.3V / 2.5V /1.8V
USB, eSPI, eSDHC*	CVDD / USB_VDD	3.3V	3.3V / 2.5V /1.8V	3.3V / 2.5V /1.8V	3.3V / 2.5V /1.8V

* eSDHC not available on MPC831x

** SPI interface shares same supply as I2C & JTAG on MPC831x / MPC837x

*** SERDES supply specs for 600MHz / 800MHz devices respectively

Power Sequencing

Power sequencing is different from PowerQUICC II Pro

P1/P2 devices requires power rails to be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows for power-up:

- VDD, AVDD_n, BVDD, LVDD, OVDD,CVDD, XVDD_SRDS and XVDD_SRDS

- GVDD

- NOTE: Items on the same line have no ordering requirement with respect to one another.

- NOTE: If any of the I/O power supplies ramp prior to VDD core supplies, the associated I/O supply may drive a logic one or zero during power- up thus causing excessive current to be drawn by the device.

All supplies must be at their stable values within 50 ms.

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POR Configuration Inputs

P1/P2 platforms have power on reset (POR) signals used for device configuration

- Signals are muxed with existing I/O pins

The settings for the following POR pins will determine CPU boot enable, PLL ratios and boot device selection:

- LA[29:31] - cfg_sys_pll[0:2]
- LBCTL, LALE, LGPL2 - cfg_core0_pll[0:2]
- LWE0, UART_SOUT1, READY_P1 - cfg_core1_pll[0:2]
- TSEC1_TXD[6:4],TSEC1_TX_ER - cfg_rom_loc[0:3]
- LA[27] - cfg_cpu0_boot
- LA[16] - cfg_cpu1_boot

- LGPL3, LGPL5 - cfg_boot_seq[0:1]

Further configuration signals may be used in the future to control functionality. It is advised that boards are built with the ability to pull-up or pull-down these pins.

- LA[20] - cfg_eng_use[00]
- LA[21] - cfg_eng_use[01]
- LA[22] -cfg_eng_use[02]
- UART_SOUT[00]- cfg_eng_use[03]
- TRIG_OUT -cfg_eng_use[04]
- MSRCID[01] -cfg_eng_use[05]
- MSRCID[04]- cfg_eng_use[06]
- DMA1_DDONE[00]- cfg_eng_use[07]

POR signals are sampled on HRESET negation

POR Configuration Pins Termination Requirements

The following pins must NOT be pulled down during power-on reset, otherwise it may trigger the internal test mode:

- DMA1_DACK[00]

- USB1_STP

- HRESET_REQ

- MSRCID[2:3]

- MDVAL

- ASLEEP

DDR Interface Design

DDR2 interface requirements consistent with PowerQUICC II Pro family

Refer to Application Note AN2910:
- "Hardware and Layout Design Considerations for DDR2 SDRAM Memory Interfaces"

DDR3 guidelines available from AN108
- "Designing for DDR3 Memory on Freescale Microprocessors"

DDRCLK input
- Input is only required when the DDR controller is running in asynchronous mode.
- Not required if DDR controller is selected to work in synchronous mode, via POR setting cfg_ddr_pll[0:2]=111.
- It is recommended to tie it off to GND when DDR controller is running in synchronous mode.
- DDR3 is only supported in asynchronous mode

eTSEC Pin Termination

Addition termination requirements for eTSECs compared to PowerQUICC II Pro

- When eTSEC1 and eTSEC2 are used as parallel interfaces, pins TSEC1_TX_EN and TSEC2_TX_EN requires an external 4.7-kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.

- TSEC2_TXD[01] is used as cfg_dram_type. It must be valid at power-up, even before HRESET assertion.

Unused eTSEC pin termination

- For I/Os, tie signals high or low through a resistor. Recommended resistor values are 2–10K ohm.
- For inputs, tie signals to their inactive state through a resistor; clock inputs may be tied high or low. Recommended resistor values are 2–10 K ohm.
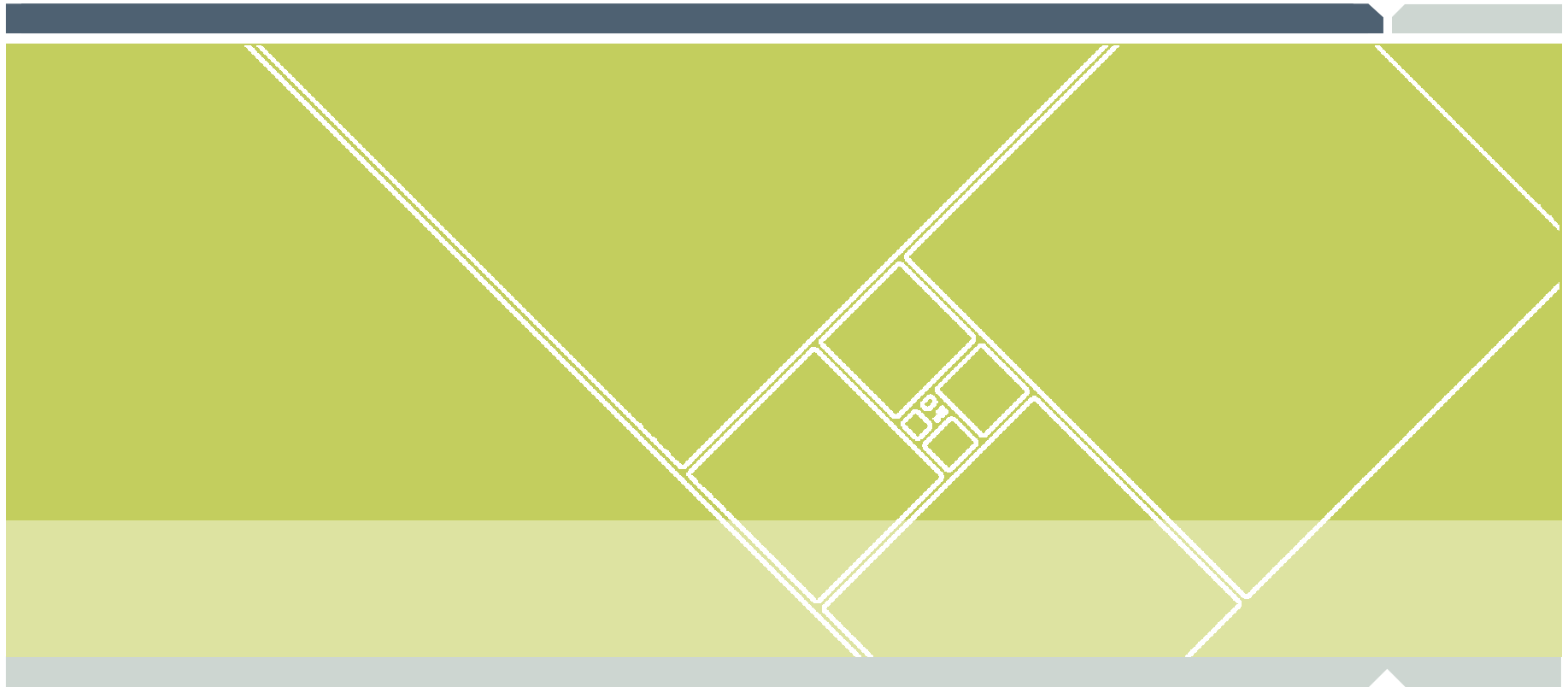
Termination is not needed on output signals.

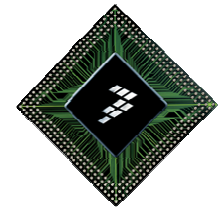For bidirectional I/Os, tie signals high or low though a resistor. Recommended resistor values are 2–10 K ohm

For inputs, tie signals to their inactive state through a resistor. Recommended resistor values are 2–10 K ohm.

Reset Configuration and Clocking

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POR Configuration

QorIQ P1 / P2 devices use power-on reset (POR) configuration pins, which are sampled during the assertion of HRESET_B.

- PowerQUICC II Pro devices load reset configuration words to initialize various device functions

All POR configuration pins are typically multiplexed with the output signals

All POR configuration pins have internal pull-up resistor (~20 KΩ) and those resistors are activated only during the POR configuration;

- POR pins can be pulled high or low by external resistors for configuration.
- Signals can also be driven by CPLD / FPGA device

During HRESET, all other signal drivers connected to these POR configuration signals must be in the high-impedance state.

- Reason: If other devices also drive POR pin during HRESET, device may sample the wrong POR configuration information from the POR pin.

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Power-On Reset

Power-On reset sequence is significantly different from PowerQUICC II Pro family

- HRESET#   - Now input only and replaces PORESET# input
- HRESET_REQ# - Output, used to request reset
- SRESET#   - Input only
- READY_P0 / TRIG_OUT – Core 0 ready output / external trigger output
- READY_P1 – Core 1 ready output (if available)

Signals no longer available

- CFG_RESET_SOURCE[0:3] – Used to load configuration words. Function replaced by POR configuration pins
- CFG_CLKIN_DIV# - Clock division selection is carried out by POR PLL config pins

Clocking Quick Reference

Functional Block	Clocked by…	Restrictions
Local Bus	CCB_clk / [4, 8, 16]	LBIU PLL bypass mode is recommended when LBIU frequency is at or below 83 MHz; When LBIU operates above 83 MHz, LBIU PLL is recommended to be enabled
PCI Express® and Serial RapidIO® digital logic	CCB_clk/2	
SerDes for PCIe, sRIO and SGMII	SD_REF_CLK/SD_REF_CLK_B	100 MHz ref clk for PCIe 1.25 Gbps and 2.5 Gbps 100 MHz ref clk for SRIO 1.25 Gbps and 2.5 Gbps 125 MHz ref clk for SRIO 3.125 Gbps 100 MHz ref clk for SGMII 1.25 Gbps For PCIe, CCB_clk > (527 MHz x PCI Express link width) / 8 For sRIO, CCB_clk > 2 × (0.80) × (Serial RapidIO interface frequency) × (Serial RapidIO link width) /64
I²C	CCB_clk / (2* I2CFDR[FDR]ratio)	
Real Time Clock (RTC)	External source or CCB_clk	The minimum pulse width of the RTC signal should be greater than 2x the period of the CCB clock; The minimum RTC frequency is zero.

Clocking Quick Reference (continued)

Functional Block	Clocked by…	Restrictions
e500 core and L1 cache	Core-complex-bus clock (CCB_clk) times a multiplier	533 MHz=< core freq =<1.2 GHz
L2 cache and ECM	CCB_clk	266 MHz=< CCB_clk (platform clock) =<600 MHz
SYSCLK	External clock source	SYSCLK 66.66 MHz=min, & 100 MHz=max
DDR	CCB_clk / 2	400 MHz=< DDR data rate =<800 MHz; For DDR3: the minimum data rate is 667 MHz **Note:For asynchronous operation the DDR clock speed is derived from the DDR_CLK input**
eTSECs	eTSEC logic layer is clocked by CCB_clk /2; MAC layer is clocked by 125 MHz from PHY or External;	EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK.
eTSEC FIFO mode	TSECn_RX_CLK and TSECn_TX_CLK	For FIFO GMII mode: FIFO TX/RX clock frequency <= platform clock frequency / 4.2 For FIFO encoded mode: FIFO TX/RX clock frequency <= platform clock frequency / 3.2

e500 Clock Control Architecture and Low Power States
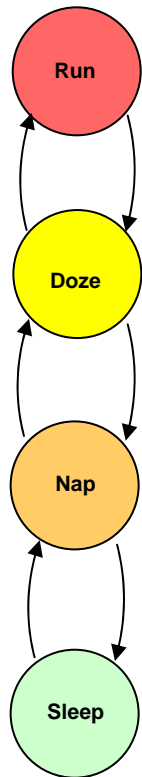
Processor Clocks	Snoops Respond to	Interrupts Respond to	Comments
On	Yes	Yes	All units operating normally. Dynamic Power Management (DPM) may be enabled
On	Yes	Yes	The core has halted instruction fetching, but all other functional blocks in the core and device are running.
Off except time base	No	Yes	The core has halted instruction fetching. Snooping of the L1 caches is disabled. All of the core's functional units except the timer are shut down. All functional blocks in the device are running.
Off	No	Yes	Instruction fetching is halted. snooping of L1 caches is disabled. Most functional blocks are shut down in both the e500 cores and the system logic, except to the interrupt controller (PIC) unit and eTSEC

Run

Doze

Nap

Sleep

Possible Boot interfaces

- Local bus
- DDR2 / DDR3 memory controller
- PCI Express interface
- Serial RapidIO (P2020)
- eSPI interface
- eSDHC interface

New boot interfaces supported on P1 & P2

Boot sequencer – Migrated from PowerQUICC II Pro

Boot hold-off – registers used to suspend core booting

- Used when booting two cores. CPU0 boots while CPU1 waits
- Used when external master boots device over eg. RapidIO or PCIe

Reset - e500 begins execution from fixed location of 0xFFFF_FFFC

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Runtime Power Management

- **Dynamic power management**
  - Withholds clocks to e500's unused execution units, MMUs, caches, and other blocks without performance impact
- **Programmable power mode**
  - Programmable transition (per core) between e500 modes: full power, doze, nap, and sleep
  - Three external pins track power mode of cores
  - POWMGTCR puts device into sleep or doze
- **Memory Controller**
  - Dynamic power management
    - Doesn't clock DRAM when no transactions
  - Sleep/doze mode. DRAM put into self-refresh mode, controller goes into sleep mode
- **I/O power management**
  - eTSEC's Magic Packet support: specially defined Ethernet packet received on eTSEC wakes chip from sleep

Configuration Power Management

- **Multiplier flexibility to optimize core, internal bus, and DDR performance and power**
- **Disable unused blocks through DEVDISR register**
  - e500 (each individually)
  - PCI Express (all three individually)
  - Local bus
  - Security block
  - USB
  - eSDHC
  - SPI
  - DMAs (both individually)
  - eTSECs (each individually)
  - DDR controller
  - I2C (both together)
  - DUART
  - Timers (both sets individually)

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Software Design Considerations

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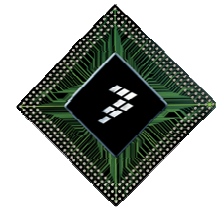
Memory Map

e500v2 based QorIQ devices deploy a 36-bit local address space

- PowerQUICC II Pro, e300 based, devices deploy a 32-bit local addressing scheme

Local Access Windows (LAWs)

- Support multiple access windows like e300 devices
- Maximum window size increased from 2GBytes to 32GBytes

ATMU - Address Translation & Mapping Unit

- Used for translating between local & external address spaces
- Further ATMUs added on QorIQ platforms for additional PCIe controllers & SRIO

CCSR – Command, Configuration & Status Registers

- Replacement to IMMR space registers on PowerQUICC II Pro
- All registers of the SoC are contained within a 1MByte address region
- Offers additional flexibility – can be relocated, and provides easier external access

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eTSEC Updates - Memory mapping

P2020

eTSEC 1.x

4k Block ⟷ Core 0

⟷ Core 1

P1020

eTSEC 2.x

4k Block Group 0

4k Block for MDIO ⟷ Core 0

4k Block Group 1 ⟷ Core 1

New eTSEC features introduced to P1 devices
- P2 and earlier devices have eTSEC 1.x
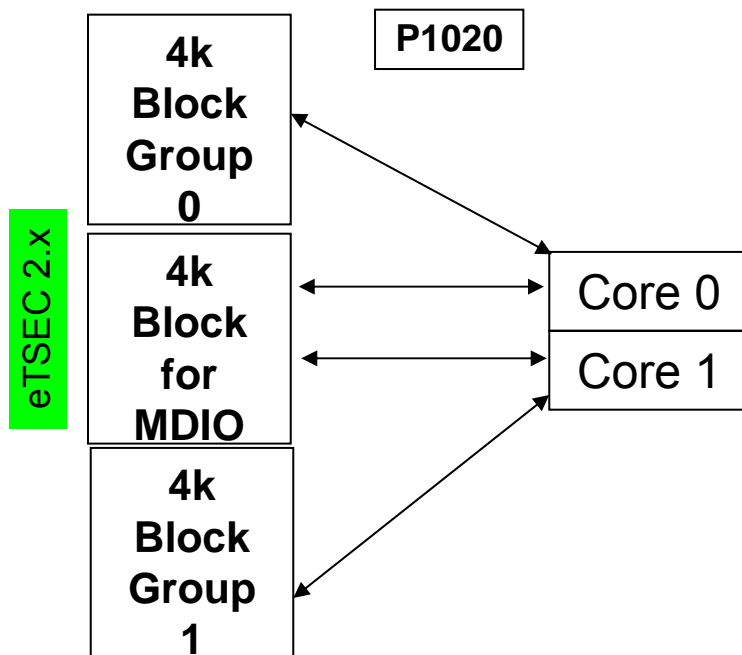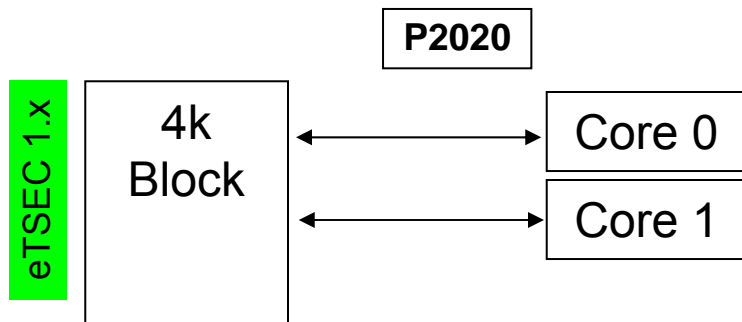- P1 devices have eTSEC 2.x

eTSEC 1.x has one common 4k block of common registers which can be used by any core

In eTSEC 2.x, the Ethernet traffic can be categorized in two groups

Separate 4k block of status & control registers are for each groups. These 4k blocks can be associated to each of the cores

Another 4k block, common to both the core, is available for management

eTSEC Updates - Interrupt steering

Interrupt routing in eTSEC 1.x | P2020 |
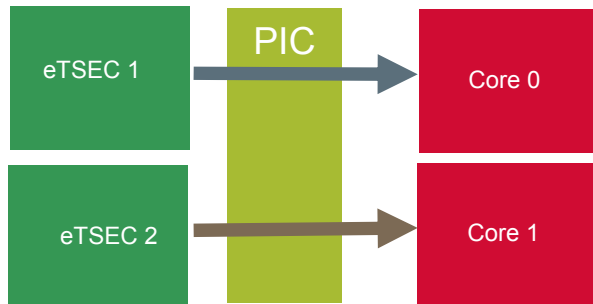
In eTSEC 1.x, all the Rx and Tx interrupts are routed to any one core through PIC

Interrupt routing in eTSEC 2.x | P1020 |
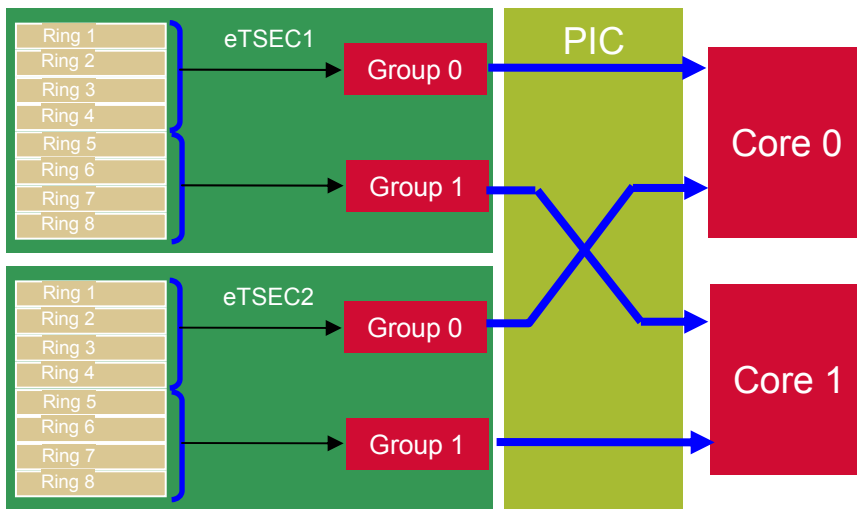
In eTSEC 2.x, the hardware queues can be mapped to any of the two groups.
The interrupt controller gets two Rx and two Tx interrupts from each eTSECs.
These interrupts can be routed to either of the cores.

Power Architecture cores operates in either of the following two modes

- ***Supervisor Mode***: This is the highest privilege mode where entire programming model is available for the software. Operating systems and boot loaders operate on this mode.

- ***User mode***: Resources, which can affect whole system, are not available in this mode. User-level applications or non-trustable programs operate on this mode.

e500v2

e300

0   31 32   63

| GPR0 |
GPR1
GPR30
GPR31

General Purpose Registers

FPU Registers

FPSCR

| CR |
| CTR |
| LR |
| XER |

Instruction Accessible Registers

0   63

| FPR0 |
FPR1
FPR30
FPR31

L1 Cache (Read Only)

L1CFG0

L1CFG1

SPE Register

SPEFSCR

ACC

User General SPR

USPRG0

| ATBL | | TBL |
| ATBU | | TBU |

Time-Base Registers
(Read Only)

General SPRs (Read Only)

SPRG3
SPRG4
SPRG5
SPRG6
SPRG7

| PMGC0 |
| PMC0 |
| PMC1 |
| PMC2 |
| PMC3 |

Performance Monitor Registers
(Read Only)

Branch Buffer Registers

BBEAR

BBTAR

PMLCb0	PMLCa0
PMLCb1	PMLCa1
PMLCb2	PMLCa2
PMLCb3	PMLCa3

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e500v2 L1 Cache

L1CSR0
L1CSR1

Branch Buffer Registers

BBEAR
BBTAR
BUCSR

PIR

Miscellaneous

MSR
PVR
SVR
HID0
HID1

TCR | DEC
TSR | DECAR

Time-Base
Registers

TBL
TBU

Performance
Monitor
Registers

PMGC0
PMC0
PMC1
PMC2
PMC3

General SPRs

SPRG0
SPRG1

SPRG7

PMLCb0 | PMLCa0
PMLCb1 | PMLCa1
PMLCb2 | PMLCa2
PMLCb3 | PMLCa3

e300

Debug

DABR
DABR2
IABR
IABR2
IBCR
DBCR

MMU

PID0
PID1
PID2
MMUCSR0
MAS0
MAS1

MAS7
MMUCFG
TLB0CFG
TLB1CFG

Debug

DBCR0
DBCR1
DBCR2
DBSR
IAC1
IAC2
DAC1
DAC2

IVOR0
IVOR1
* * *
IVOR15
IVOR32
* * *
IVOR35
MCAR
MCARU

MCSRR0
MCSSR1
MCSR
ESR
DEAR
IVPR

Interrupt Registers

SRR0
SRR1
CSRR0
CSSR1

DAR
DSISR

MMU

SR0
SR1
* * *
SR15

IBAT0U
IBAT0L
* * *
IBAT7U
IBAT7L
DBAT0U
DBAT0L
* * *
DBAT7U
DBAT7L

SDR1
DMISS
IMISS
HASH1
HASH2
DCMP
ICMP
RPA

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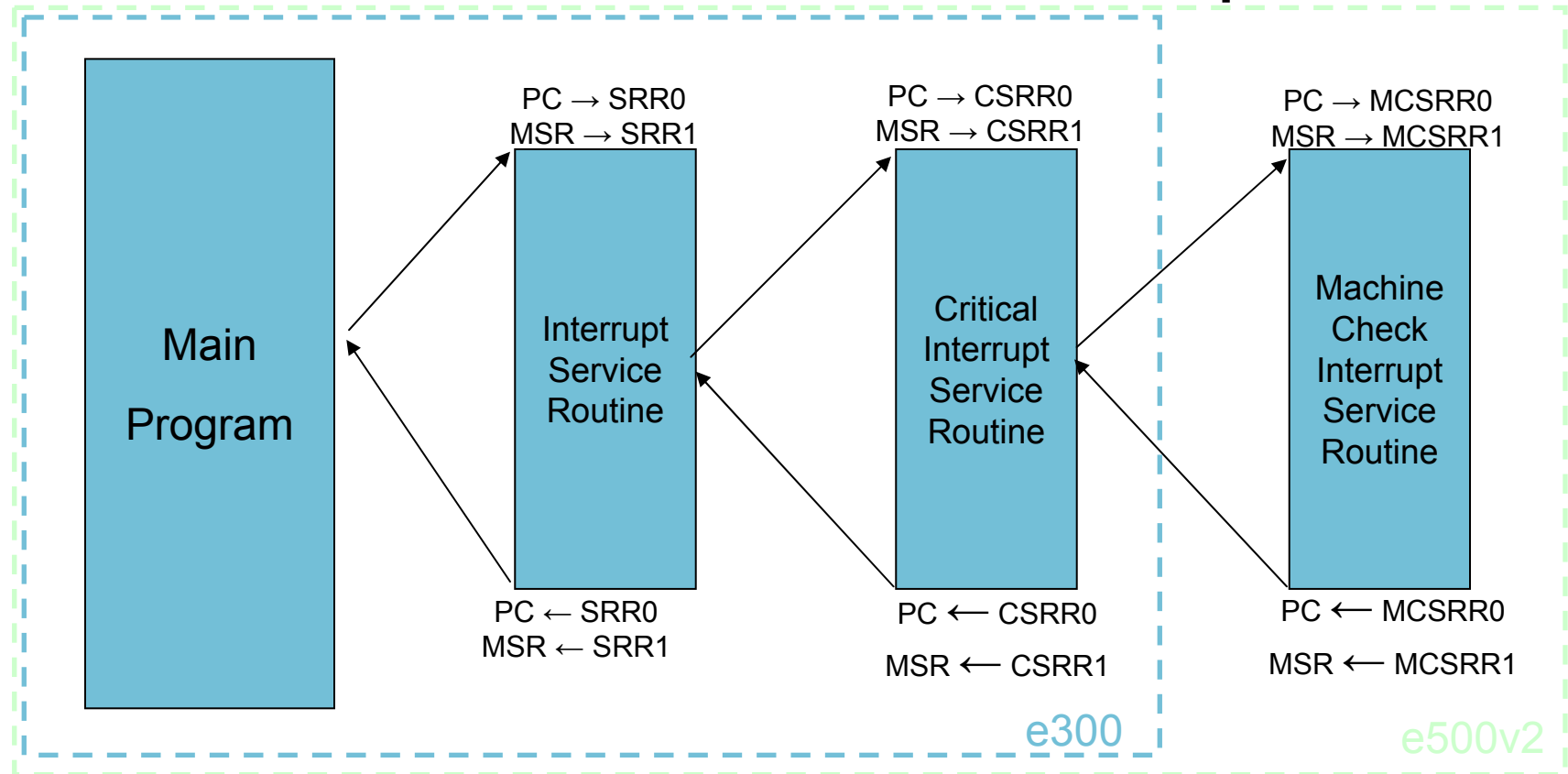*semiconductor*

While exceptions had fixed vector addresses in e300, they are programmable in e500v2 except reset vector.

In e300, reset vectors at 0x0000_0100 while it vectors at 0xFFFF_FFFC in e500v2

e500v2 has a new category of exception. Machine check

PC → SRR0
MSR → SRR1

PC → CSRR0
MSR → CSRR1

PC → MCSRR0
MSR → MCSRR1

Main
Program

Interrupt
Service
Routine

Critical
Interrupt
Service
Routine

Machine
Check
Interrupt
Service
Routine

PC ← SRR0
MSR ← SRR1

PC ← CSRR0
MSR ← CSRR1

PC ← MCSRR0
MSR ← MCSRR1

e300

e500v2

A new category of Machine check interrupt has been added in e500v2

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e300 supports BAT and page translations while e500v2 has 512 entries of fixed 4k pages and 16 entry variable size pages

e300 endian mode is controlled on system basis while e500v2 allows endian confirguration per page basis

Unlike e300, MMU is always on in e500v2

After reset, a default entry in MMU maps logical address 0xffff_f000 to physical address 0xffff_f000

Cache

e300 has 16/32k L1 I/D cache while e500v2 has 32k L1 I/D cache and 256k L2 cache(P1)/512k L2 cache(P2).

e300 supports way-locking while e500v2 supports line-locking

e500v2 has non-blocking caches (cache access is allowed even after a miss)

e500v2 supports stashing on L2

Software Migration Considerations
Operating System Migration

e500v2 imposes numerous changes to classic PowerPC operating systems

Areas affected include:

- Instruction set use
- Context switching
- Exception handling
- MMU operation
- Reset

Necessary changes have already been made by PowerPC OS vendors

Linux BSPs with gcc based toolchain available from Freescale

- http://www.freescale.com/linux

Software Migration Considerations
Migrating to Dual Core

Dual core systems support for AMP & SMP architectures

SMP – Symmetric Multi-Processing architecture

- Configuration where two or more identical cores can connect to a single shared memory space. Equal access to memory and resources

AMP – Asymmetric Multi-Processing architecture

- Configuration where the processing elements in a multi-core processor can be used to run separate tasks. Processing elements are treated separately with own resources and memory space.

AMP & SMP BSPs available from Freescale for P2020

Selection of architecture depends upon application

Symmetric Multi-processing (SMP)

SMP is a multi-processor homogeneous computer architecture where two or more identical processors are connected to a globally shared main memory…

Processors could be separate devices, all on 1 device or a mix

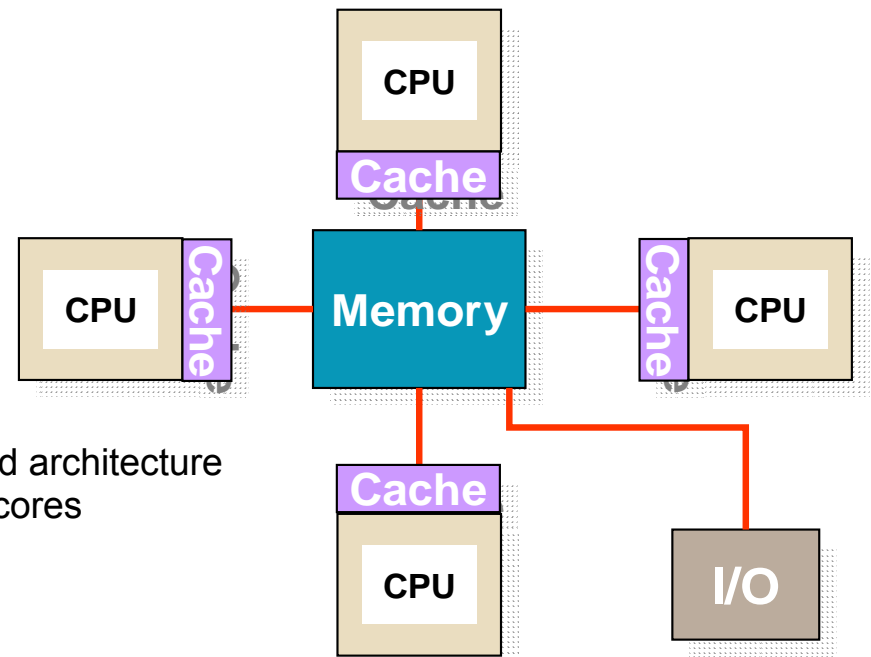Typically all CPUs share memory, I/O and are run one OS instance

Each processor can run independent processes and threads

Any idle processor can be assigned any task

Issues / challenges
- Challenges of migrating legacy code to multithreaded architecture
- Additional overhead with scheduling and managing cores

Performance speed-up depends on application
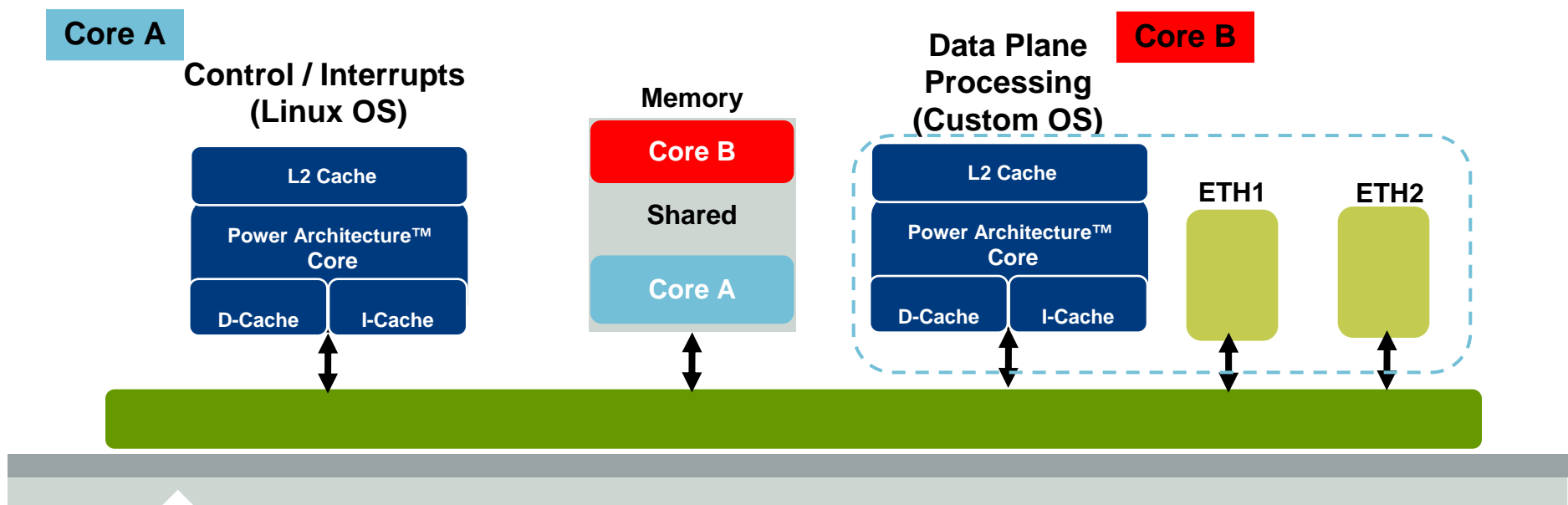
Asymmetric Multi-processing (AMP)

A _multi-processing usage model_ in which individual processors are dedicated to particular tasks, such as running the operating system or performing user requests

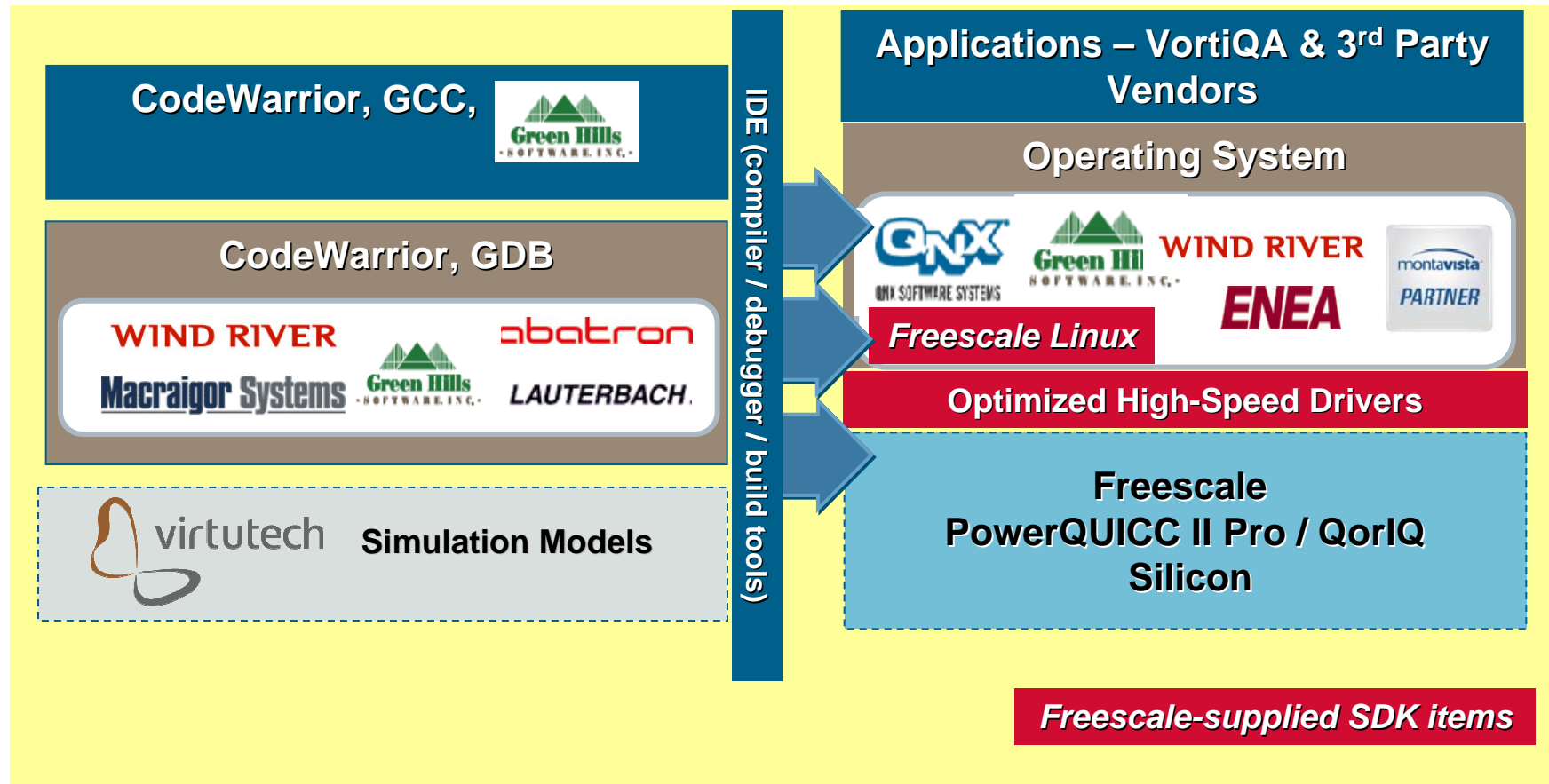Each core has its own dedicated resources, no scheduling required with other devices

Software will run as it does on a single core environment

Issues / Challenges:
- System design - deciding how to partition resources between cores
- Cannot take advantage of idle time on another CPU

Development System & Ecosystem

CodeWarrior, GCC, Green Hills Software, Inc.

CodeWarrior, GDB

WIND RIVER, abatron, Macraigor Systems, Green Hills Software, Inc., LAUTERBACH.

virtutech Simulation Models

IDE (compiler / debugger / build tools)

Applications – VortiQA & 3rd Party Vendors

Operating System

QNX Software Systems, Green Hills Software, Inc., WIND RIVER, ENEA, montavista PARTNER

Freescale Linux

Optimized High-Speed Drivers

Freescale PowerQUICC II Pro / QorIQ Silicon

Freescale-supplied SDK items

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Application Case Studies
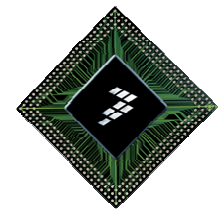
- **Networking (switches and routers)**
  - Line card controller
  - Mid-range line card control plane
  - Low-end line card combined control and data plane
  - Shelf controller
  - Business gateway
  - Multiservice router
  - Wireless access points
- **Telecom**
  - AMC card
  - Controller on ATCA Carrier Card
  - Channel and control card for NodeB, BTS, WCDMA, 4G LTE, WiMax
  - General-purpose compute blade
- **Industrial**
  - Robotics
  - Test/measurement Networking/telecom
  - Multifunction printer
  - Single board computers
  - Industrial applications
- **Key Advantages**
  - High single-threaded performance
  - Enables performance without complexity of partitioning across multiple cores or threads
  - Highly suitable for control plane applications whose sequential nature means efficiency is lost with scaling to many cores
  - Pin compatibility over 4.5x frequency range enables BOM-based product differentiation
  - Low power

NAS Storage Application – PowerQUICC II Pro
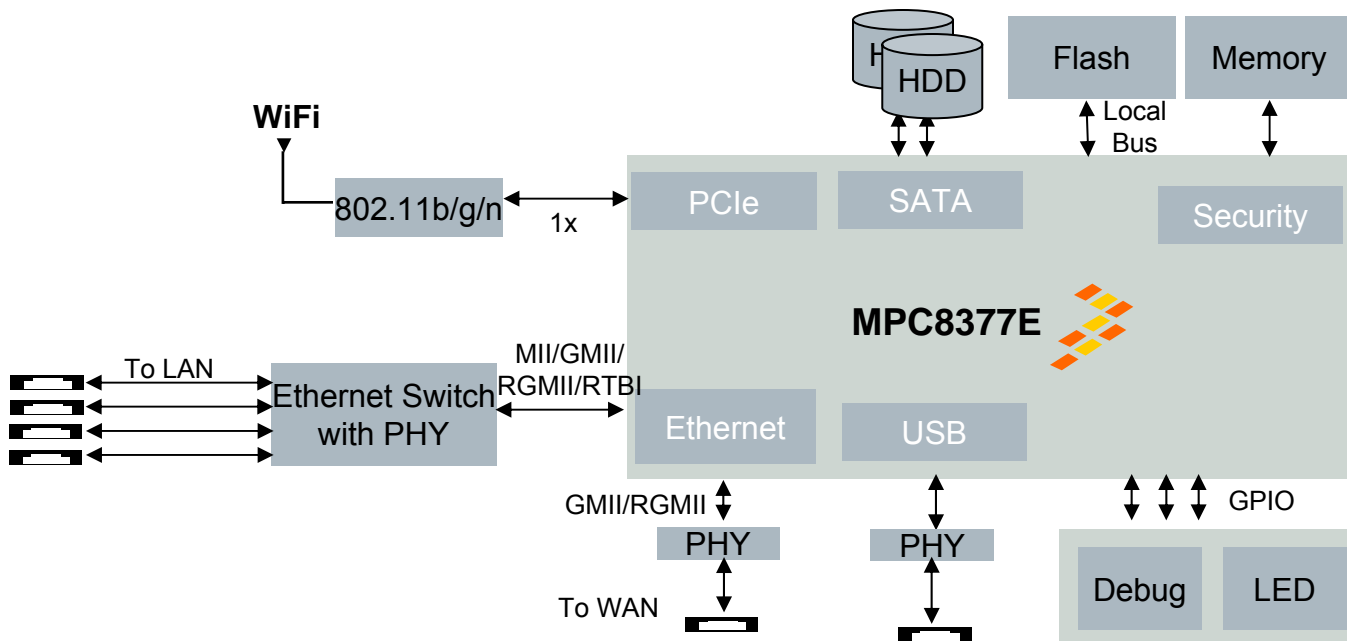
e300 based platform, up to 800MHz performance, 1.92 DMIPS/MHz performance, <5W @ 800MHz

Integrated SATA controller used to connect up to 2x HDD

Gigabit Ethernet LAN and WAN interface

Wireless capability available through PCIe express card

USB interface accessible through external PHY

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NAS Storage Application – QorIQ P1 / P2

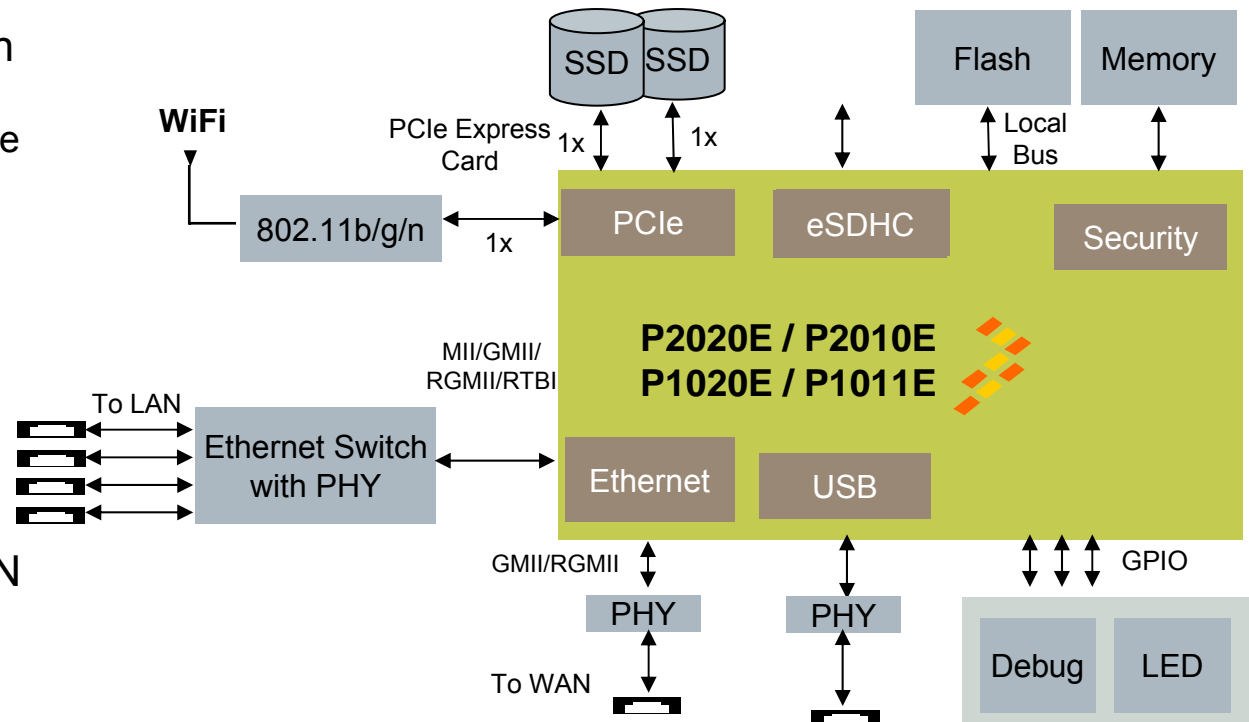Performance improvement with e500 core
- Up to 1200MHz performance per CPU
- 2.4DMIPS/MHz per CPU

L2 cache available to improve Ethernet packet processing

Storage capability:
- SSD on PCIe express
- eSDHC interface

Gigabit Ethernet LAN and WAN interface maintained

Potential to add additional services using extra CPU processing capability

Target CPU power
- P2020 – 8W @ 1200MHz
- P1020 – 5W @ 800MHz

WiFi

SSD SSD

Flash   Memory

PCIe Express Card   1x   1x   Local Bus

802.11b/g/n   1x

PCIe   eSDHC   Security

P2020E / P2010E
P1020E / P1011E

MII/GMII/ RGMII/RTBI

To LAN

Ethernet Switch with PHY

Ethernet   USB

GMII/RGMII   GPIO

PHY   PHY

To WAN

Debug   LED

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Application Migration - Hardware

New board design required for QorIQ device

Issue	Solution with QorIQ P1 /P2
Power supply	Same voltage architecture. Adjustable supplies will ease migration from 1.1V on PowerQUICC II Pro to 0.95V for QorIQ P1
Existing interfaces	Re-use design for existing interfaces such as Ethernet, DDR2, eSPI, JTAG and USB
New interfaces	Use application notes, evaluation boards and other resources from http://www.freescale.com.
Power performance	Best-in-class power performance, enable fan-less "green" design. Advanced power management.
Simulation	IBIS models available for all devices
Future expansion	Pin compatibility between P1011, P1020, P2020 and P2010 devices simple migration to a higher performance or lower power application

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Application Migration – Software

Migration from e300 to e500 based platform

Issue	Solution with QorIQ P1 /P2
Code base migration	General code compatibility with exceptions in certain areas – floating point, interrupts, supervisor instructions. See resources at www.freescale.com
Operating systems & tools	Established ecosystem of operating systems BSPs, tools and drivers for e500 based platforms, thus reducing development time
Software compatibility for reused interfaces	Code used for existing interfaces such as Ethernet and security block will migrate
New interfaces and features	Driver-level source code available for Freescale evaluation platforms from www.freescale.com

Application – Migrating to Dual Core

Consider why?
- Achieve increased performance of existing application
- Accommodate new services and functions
- Integration of external functions to achieve lower cost

Do you choose AMP or SMP?
- How will the application be partitioned?
- Consider memory and resource access on device

Is the existing application single threaded or multi-threaded
- <u>Single threaded</u>
    - AMP – Run existing code as is on single core
    - SMP – Run multiple versions of existing code
- <u>Multi-threaded</u>
    - SMP – Run single instance of un-modified application

Profile existing code and recode critical spots, make use of parallel processing to optimise performance

QorIQ™ P1 and P2 Series Summary

Features	Benefits
Best in class ecosystem	Faster time to market
Migration path	Improved performance/watt/$ migrating from PowerQUICC II, PowerQUICC II Pro, and PowerQUICC III
High performance e500 2.4MIPS/MHz Power Architecture™ core	High efficiency and frequency cores means fewer cores to get the job done
Best-in-class power	Enables fan-less, "green" and low cost designs, improves reliability
Integrated Ethernet, TDM, USB, SD Flash controller, IEEE1588, PCI-Express, Serial Rapid IO	Flexibility to address a wide range of applications and reduced system cost
4.5x performance range in a single package (533MHz to 2x1200MHz)	Common hardware platform to enable wide range of system performance
Dual and single cores	Move to dual core at your own pace without hardware changes

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