FS85/FS84 FAQ

Frequently Asked Questions

April 13th, 2026
Version: 2.1

Navigation section

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FS85/FS84 series selection

FS85/FS84 series selection

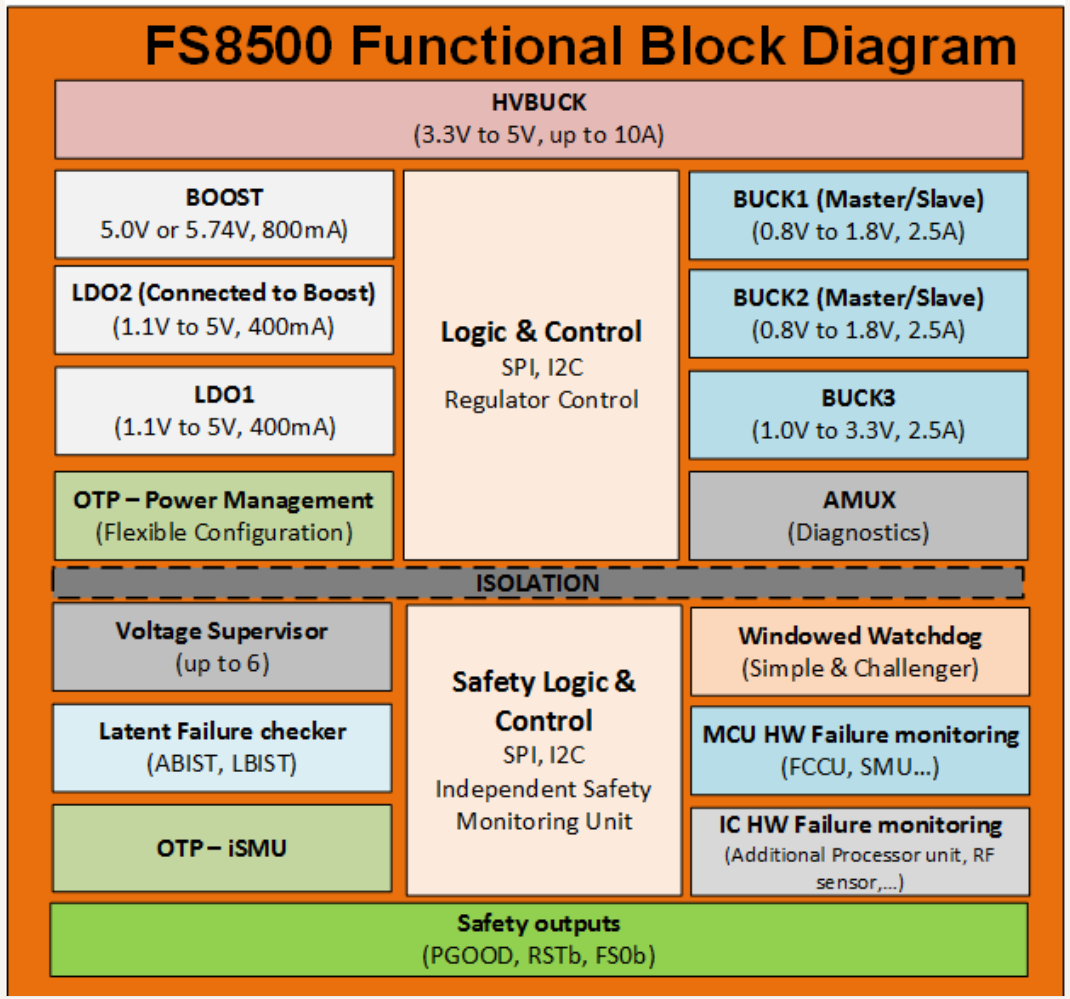
FS85 Family introduction

Power Management

- Input supply up to 60V – 12V and 24V systems.
- **HVBUCK** , adjustable 3.3V to 5V, scalable output current up to 10A.
  - Synchronous Buck, 455kHz or 2.22MHz, ext. MOS.
- **BUCK1/2**, adjustable 0.8V to 1.8V, up to 2.5A DC – 3.6A peak
  - Synchronous Buck, up to 3MHz, int. MOS
  - Can operate in multi-phase delivering 5A
  - SVS capability on Buck1.
- **BUCK3**, adjustable 1.0V to 3.3V, up to 2.5A DC – 3.6A peak
  - Synchronous Buck, up to 3MHz, int. MOS.
- **BOOST** 5V or 5.74V, up to 800mA DC- 1.5A peak, int. MOS.
- **LDO1/2**, configurable 1.1V to 5V, up to 400mA.
- Synchronization signal for dual device operation / Power GOOD output.
- Frequency Synchronization Fin/Fout.

System Features

- Independent Safety Monitoring Unit
- Control via 32 bits SPI and I2C (including CRC).
- Low Power Mode : 10µA in LPOFF, wake up via WAKE1/2 pins
- AMUX: Battery, Internal Safety critical voltages, Vref and Temperature
- Emulation and Programming capability offered in Engineering mode only : Voltage, Frequency, Phase shift, Power sequencing.
- EMC: Spread Spectrum, Freq. Synch., Vpre Slew Rate control, Freq. Tuning



FS85/FS84/VR5500/FS5502 package pins are pin to pin compatible

- Classified according to functional safety level: FS85 is ASIL-D, FS84 is ASIL-B and VR5500 and FS5502 are QM.
- FS85/FS84 are divided into different sub-Part Numbers according to the BUCK used, such as FS8530 and FS8510.

<table>
<tr><th>Part Number</th><th>Buck 1</th><th>Buck 2</th><th>Buck 3</th><th>Safety Level</th></tr>
<tr><td>VR5500</td><td rowspan="10">0.8V – 1.8V
2.5A
Multi Phase
& SVS option</td><td>0.8V – 1.8V</td><td>1.0V – 3.3V</td><td>Quality Mgt (QM)</td></tr>
<tr><td>FS8400</td><td></td><td></td><td>Fit for ASIL B</td></tr>
<tr><td>FS8500</td><td></td><td></td><td>Fit for ASIL D</td></tr>
<tr><td>FS5502</td><td></td><td rowspan="3">1.0V – 3.3V
2.5A</td><td>Quality Mgt (QM)</td></tr>
<tr><td>FS8410</td><td></td><td>Fit for ASIL B</td></tr>
<tr><td>FS8510</td><td></td><td>Fit for ASIL D</td></tr>
<tr><td>FS8420</td><td rowspan="4">0.8V – 1.8V
2.5A
Multi Phase
& SVS option</td><td rowspan="2">N/A</td><td>Fit for ASIL B</td></tr>
<tr><td>FS8520</td><td>Fit for ASIL D</td></tr>
<tr><td>FS8430</td><td rowspan="2">1.0V – 3.3V
2.5A</td><td>Fit for ASIL B</td></tr>
<tr><td>FS8530</td><td>Fit for ASIL D</td></tr>
</table>

Notes and sources

Differences in FuSa features of FS85/FS84/VR5500/FS5502

- Functional safety can be tailored, and the appropriate series must be selected according to functional safety requirements.

ITEMS		VR55/FS55 – QM	FS84 – ASIL B	FS85 – ASIL C/D
Documentation & Safety analysis	FTA	-	-	✓
	DFA	-	-	✓
	FMEDA	-	✓	✓
	Fault Injection T Report	-	-	✓
	Safety Manual	-	✓	✓
Safety Outputs	PGOOD	✓	✓	✓
	RSTb	✓	✓	✓
	FS0b	-	✓	✓
Safety Functions	Voltage Monitoring	2 (VR55)/ 3 (FS55)	4	6
	Watchdog	No	Simple	Challenger
	External IC Monitoring – single pin	No	No	YES
	MCU Monitoring (single and dual pins) - FCCU	No	No	YES
	Analog BIST	No	YES	YES
	Logical BIST	No	No	YES
	MCU Fault Recovery Strategy Compliance	No	No	YES

Notes and sources

Part numbering for FS85 series products

MC 3x FS 8 x x y x y ES / R2

Type:
MC : Standard for mass production
SC : Customized for mass production
PC : Samples for prototype

Temperature range:
33 T_a = -40°C to 125°C
35 T_a = -40°C to 150°C

Device family code:
FS : NXP SBCs / VIN Battery
PF: NXP PMICs / VIN <=5V

Series
84 series – ASIL B
85 series – ASIL D

Tape and reel packaging code:
Without R2: Tray packaging
With R2: Tape and reel packaging

Package form:
ES : WF-Type HVQFN56
EP : E-Type HVQFN56

OTP version number:
For example, A1 means that it is the A1 version of OTP
A corresponding configuration for each OTP version

Sub-model

	Have BUCKx
00	BUCK1 only
10	BUCK1 and BUCK3, No BUCK2
20	BUCK1 and BUCK2 No BUCK3
30	BUCK1 /BUCK2/BUCK3

Notes and sources

02

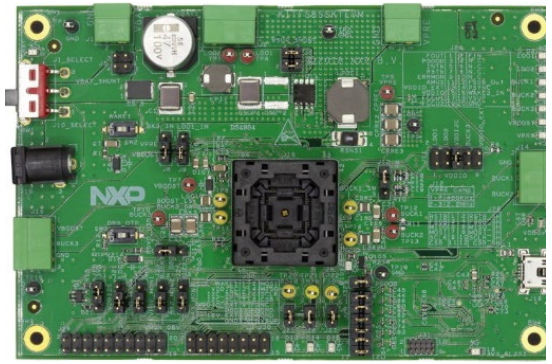
OTP introduction/version

FS85 series enables configuration flexibility via OTP

Green= can be modified
Red=cannot be modified

The configurations that can be achieved through OTP are as follows

- Buck/LDO/Boost voltage value
- Power up sequence
- Functional safety configuration
- Other functional configurations



- NXP can provide the OTP programming tool as shown above, which is only used for customer evaluation.

*OTP= One Time Programmable

Note: Empty samples such as FS8530A0 and FS8430G0 have no power output after power up.

FS85 series

Power Management

Voltage, Sequence, Enable
I_Lim , Switching Frequency
Phase shifting
VPRE/VBOOST Slew Rate
VPRE/VBOOST slop compensation
Behavior in case of TSD
PSYNC, VSUP power-up Threshold
Deep Fail Safe(autoretry)

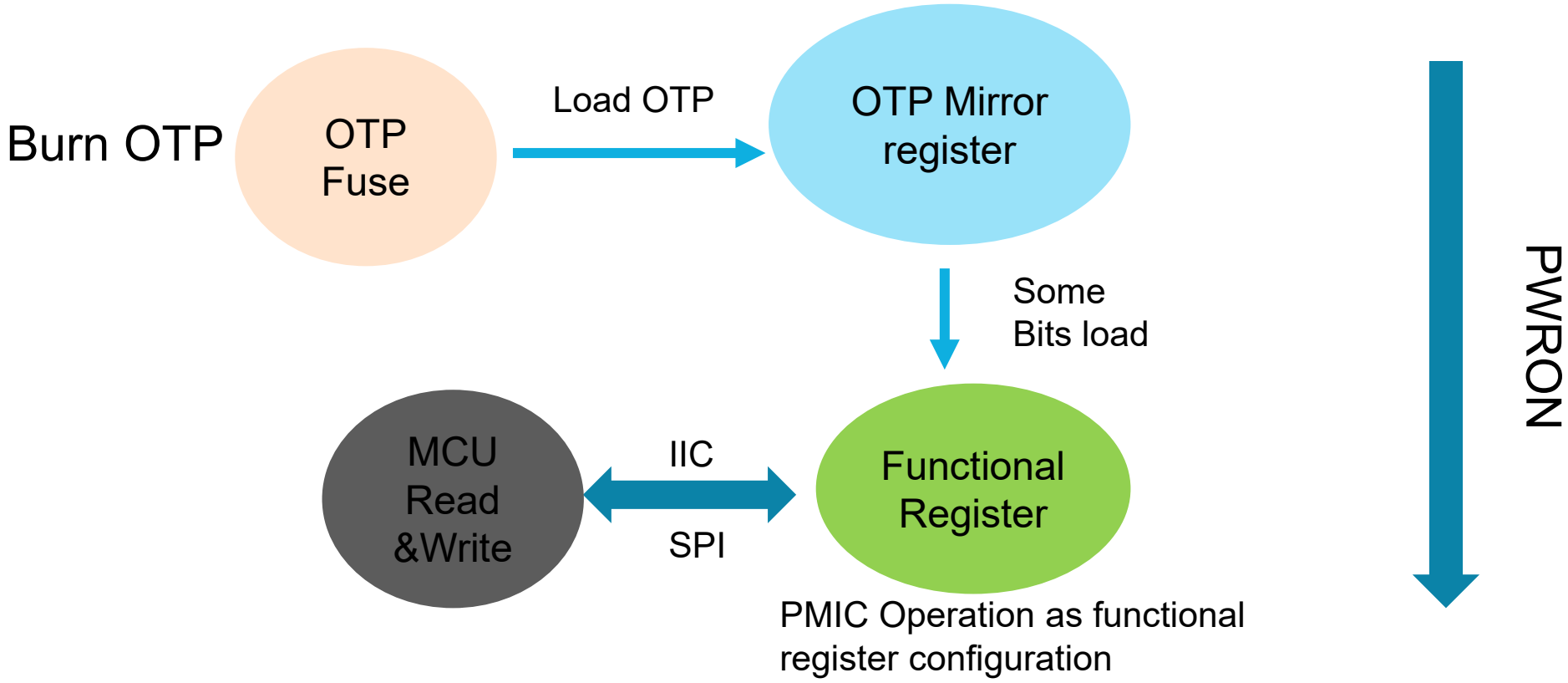
Monitoring

OV/UV Threshold
OV/UV filtering time
VCOR/VDDIO Monitor Voltage

Safety

PGOOD Assignment
ABIST1 Assignment
Safety Enable: VMON1~4, ERRMON, WATCHDOG, FCCU, FLT_RECOVERY

FS85/FS84/VR5500/FS5502 package pins are pin to pin compatible



Notes and sources

FS85_FS84 OTP register

- Functional and Mirror registers

  FS85 family **has Functional registers map & OTP mirror register map**

  - During the power up ,SBC will load OTP fuse and work by default as OTP mirror register map configuration.
  - During SBC operation, SBC can be read and configurated basing Functional register map.

- Which OTP registers are available via SPI/I2C after power up?

  - For Main OTP registers, regulator behavior in case of TSD and VPRE and VBOOST slew rates (**parameters in bold**) can be changed later by SPI/I2C.
  - For Fail-safe OTP registers, all parameters can not be changed by SPI/I2C.

Table 75. Main OTP_REGISTERS

Name [1]	Address	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OTP_CFG_VPRE_1	14	0	0	VPREV[5:0]					
OTP_CFG_VPRE_2	15	0	0	VPRESC[5:0]					
OTP_CFG_VPRE_3	16	VPREILIM[1:0]		1	0	**VPRESRLS[1:0]**		**VPRESRHS[1:0]**	
OTP_CFG_BOOST_1	17	0	0	0	0	VBSTV[3:0]			
OTP_CFG_BOOST_2	18	BOOSTEN	VBSTTONTIME[1:0]		VBSTSC[4:0]				
OTP_CFG_BOOST_3	19	0	0	0	0	0	1	**VBSTSR[1:0]**	
OTP_CFG_BUCK1_1	1A	VB1V[7:0]							
OTP_CFG_BUCK1_2	1B	0	0	0	VB1INDOPT[1:0]		VB1SWILIM[1:0]		VB12M ULTIPH
OTP_CFG_BUCK2_1	1C	VB2V[7:0]							
OTP_CFG_BUCK2_2	1D	0	VB2INDOPT[1:0]		BUCK2EN	VB2SWILIM[1:0]		0	0
OTP_CFG_BUCK3_1	1E	BUCK3EN	VB3INDOPT[1:0]		VB3V[4:0]				
OTP_CFG_BUCK3_2	1F	VB2GMCOMP[2:0]			VB1GMCOMP[2:0]			VB3SWILIM[1:0]	
OTP_CFG_LDO	20	LDO2ILIM	LDO2V[2:0]			LDO1ILIM	LDO1V[2:0]		
OTP_CFG_SEQ_1	21	0	0	VB2S[2:0]			VB1S[2:0]		
OTP_CFG_SEQ_2	22	0	0	LDO2S[2:0]			LDO1S[2:0]		
OTP_CFG_SEQ_3	23	0	0	0	0	0	VB3S[2:0]		
OTP_CFG_CLOCK_1	24	0	0	VPRE_ph[2:0]			1	0	0
OTP_CFG_CLOCK_2	25	0	0	BUCK1_ph[2:0]			VBST_ph[2:0]		
OTP_CFG_CLOCK_3	26	0	0	BUCK3_ph[2:0]			BUCK2_ph[2:0]		
OTP_CFG_CLOCK_4	27	BUCK3_ clk_sel	BUCK2_ clk_sel	BUCK1_ clk_sel	VBST_clk_sel	VPRE_clk_sel	PLL_sel	0	1
OTP_CFG_SM_1	28	0	0	**conf_TSD[5:0]**					
OTP_CFG_SM_2	29	0	0	0	VPRE_off_dly	Autoretry_ infinite	Autoretry_en	PSYNC_CFG	PSYNC_EN
OTP_CFG_VSUP_UV	2A	0	0	0	0	0	0	0	VSUPCFG
OTP_CFG_I2C	2B	0	0	0	0	M_I2CDEVADDR[3:0]			
OTP_CFG_OV	2C	0	0	0	0	0	VDDIO_REG_ASSIGN[2:0]		
OTP_CFG_DEVID	2D	DeviceID[7:0]							

Table 77. Fail-safe OTP_REGISTERS

Name	Address	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OTP_CFG_UVOV_1	0A	VCORE_V[7:0]							
OTP_CFG_UVOV_2	0B	VDDIOOVTH[3:0]				VCOREOVTH[3:0]			
OTP_CFG_UVOV_3	0C	0	0	VDDIO_V	VCORE_SVS_CLAMP[4:0]				
OTP_CFG_UVOV_4	0D	VMON2OVTH[3:0]				VMON1OVTH[3:0]			
OTP_CFG_UVOV_5	0E	VMON4OVTH[3:0]				VMON3OVTH[3:0]			
OTP_CFG_UVOV_6	0F	VDDIOUVTH[3:0]				VCOREUVTH[3:0]			
OTP_CFG_UVOV_7	10	VMON2UVTH[3:0]				VMON1UVTH[3:0]			
OTP_CFG_UVOV_8	11	VMON4UVTH[3:0]				VMON3UVTH[3:0]			
OTP_CFG_PGOOD	12	0	PGOOD_ RSTB	PGOOD_ VMON4	PGOOD_ VMON3	PGOOD_ VMON2	PGOOD_ VMON1	PGOOD_ VDDIO	PGOOD_ VCORE
OTP_CFG_ABIST1	13	0	0	ABIST1_ VMON4	ABIST1_ VMON3	ABIST1_ VMON2	ABIST1_ VMON1	ABIST1_ VDDIO	ABIST1_ VCORE
OTP_CFG_ASIL	14	WD_DIS	WD_Selection	ERRMON_EN	FCCU_EN	VMON4_EN	VMON3_EN	VMON2_EN	VMON1_EN
OTP_CFG_I2C	15	0	0	0	FLT_ RECOVERY_ EN	FS_I2CDEVADDR[3:0]			
OTP_CFG_DGLT_DUR_1	16	0	0	VCORE_UV_DGLT[1:0]		VCORE_ OV_DGLT	VDDIO_UV_DGLT[1:0]		VDDIO_ OV_DGLT
OTP_CFG_DGLT_DUR_2	17	0	0	0	0	0	VMONx_UV_DGLT[1:0]		VMONx_ OV_DGLT

OTP version options

Standard version

- A0 and G0 empty samples (require programming OTP version)
- Standard OTP versions, listed in the datasheet, correspond to different MCUs and application designs (or reference designs).
- Standard price

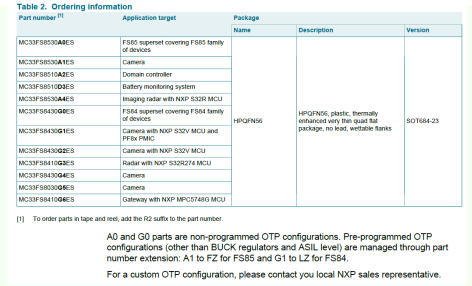


Table 2. Ordering information

Part number [1]	Application target	Package		
		Name	Description	Version
MC33FS8530**A0**ES	FS85 superset covering FS85 family of devices	HPQFN56	HPQFN56, plastic, thermally enhanced very thin quad flat package, no lead, wettable flanks	SOT684-23
MC33FS8530**A1**ES	Camera			
MC33FS8510**A2**ES	Domain controller			
MC33FS8510**D3**ES	Battery monitoring system			
MC33FS8530**A4**ES	Imaging radar with NXP S32R MCU			
MC33FS8430**G0**ES	FS84 superset covering FS84 family of devices			
MC33FS8430**G1**ES	Camera with NXP S32V MCU and PF8x PMIC			
MC33FS8430**G2**ES	Camera with NXP S32V MCU			
MC33FS8410**G2**ES	Radar with NXP S32R274 MCU			
MC33FS8430**G4**ES	Camera			
MC33FS8030**G6**ES	Camera			
MC33FS8410**G6**ES	Gateway with NXP MPC5748G MCU			

[1] To order parts in tape and reel, add the R2 suffix to the part number.

A0 and G0 parts are non-programmed OTP configurations. Pre-programmed OTP configurations (other than BUCK regulators and ASIL level) are managed through part number extension: A1 to FZ for FS85 and G1 to LZ for FS84.

For a custom OTP configuration, please contact you local NXP sales representative.

Customized version

- NXP supports customer-customized OTP (customized PNs), Volume > 250ku/y
- Purchase products with customized OTP programmed directly from NXP
- The price is slightly higher than the standard version

DISTI

- Major agents provide OTP programming (in their logistic centre)
- Customers purchase products with OTP programmed from agents
- The price is slightly higher than the standard version

CUSTOMER

- Customers can burn OTP by themselves, which is only used for debugging and development phases. There is relevant documentation to guide and support it.
- Not recommended for mass production

Notes and sources

FS85_FS84 OTP versions of standard model

Table 2. Ordering information

Part number [1]	Application target	Package		
		Name	Description	Version
MC33FS8530**A0**ES	FS85 superset covering FS85 family of devices	HPQFN56	HPQFN56, plastic, thermally enhanced very thin quad flat package, no lead, wettable flanks	SOT684-23
MC33FS8530**A1**ES	Camera			
MC33FS8510**A2**ES	Domain controller			
MC33FS8510**D3**ES	Battery monitoring system			
MC33FS8530**A4**ES	Imaging radar with NXP S32R MCU			
MC33FS8430**G0**ES	FS84 superset covering FS84 family of devices			
MC33FS8430**G1**ES	Camera with NXP S32V MCU and PF8x PMIC			
MC33FS8430**G2**ES	Camera with NXP S32V MCU			
MC33FS8410**G3**ES	Radar with NXP S32R274 MCU			
MC33FS8430**G4**ES	Camera			
MC33FS8030**G5**ES	Camera			
MC33FS8410**G6**ES	Gateway with NXP MPC5748G MCU			

[1] To order parts in tape and reel, add the R2 suffix to the part number.

A0 and G0 parts are non-programmed OTP configurations. Pre-programmed OTP configurations (other than BUCK regulators and ASIL level) are managed through part number extension: A1 to FZ for FS85 and G1 to LZ for FS84.

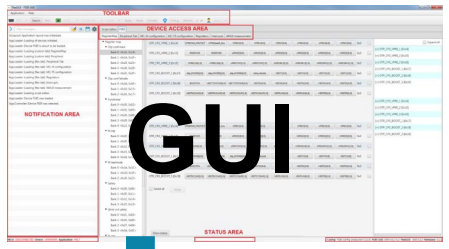
For a custom OTP configuration, please contact you local NXP sales representative.

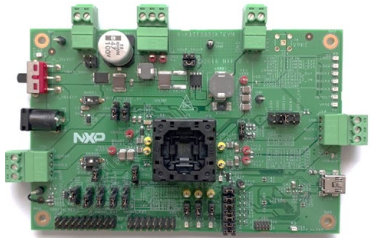
- All details of the OTP configuration's standard versions can be found in the datasheet.
- In the model on the left, A1, G1 and other boldface characters are the OTP version IDs.
- Assign A1~FZ as the FS85's OTP ID field. Assign G1~LZ as the FS84's OTP ID field
- A0 and G0 are the models of FS85 and FS84 respectively that have not been programmed with any OTP version, that is, empty samples. Can be used to program customer-customized OTP during the evaluation phase.
- In order to distinguish between B0 and C0 Silicon versions, please use PC33FS8530C0ES to apply for the C0 version FS85 blank sample.

Notes and sources

Customized OTP process

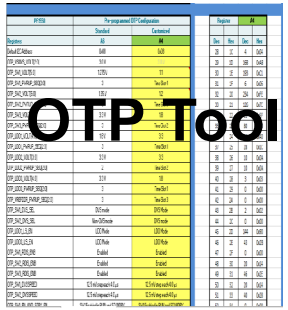
CUSTOMER





Define & Validate OTP on Lab tool

Custom sequence ID assigned



OTP File

OTP Prog

10 Eng samples

Validation of OTP in preproduction

Email approval

Production test + OTP prog

Custom PN set up

Production

3 weeks

3 Months

FS85 series engineering sample application process

- For application for FS85 engineering samples, agents can apply through NXP sales according to customer needs.
- For existing OTP versions, it will take at least three weeks to apply for engineering samples.
- For the OTP version customized for customers. After confirming the OTP configuration with NXP, it is needed to reserve at least 4 weeks to apply for samples. AE is responsible for determining the customized OTP version model, and the agent needs to provide the customer's project specific information.
- The applied engineering samples are only provided to customers for engineering prototype verification and cannot be provided to customers for the production of mass production products
- NXP company sales can apply for engineering samples through the company's PMIC Webtool. The sample PN is 14 digits large, such as: PC33FS8530C0ES. The sample application address is: https://web.powerapps.com/apps/67d76bf8-9b37-4fc3-878a-92d2bc87cdfc

- Agents and customers can apply for or purchase programming tools on the official website and use PC33FS8530A0ES (this blank chip) for programming. For specific programming methods, please refer to relevant documents and the "OTP programming process and GUI application" chapter of this document. Link to the official website of the programming tool: https://www.nxp.com/design/development-boards/analog-toolbox/fs84-fs85-safety-sbc-programming-board:KITFS85SKTEVM

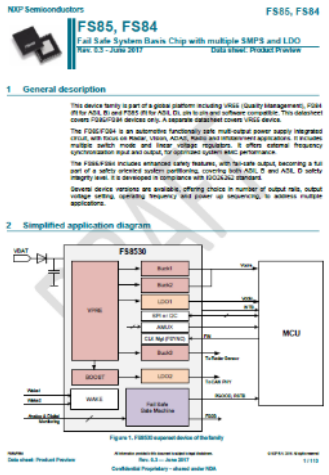
Notes and sources

03

FS85 documentation/tool support

FS84/FS85 – Documentation & Application Support

✓ Data Sheet


NXP Semiconductors FS85, FS84

FS85, FS84

Fail Safe System Basis Chip with multiple SMPS and LDO

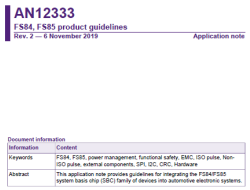
1 General description

2 Simplified application diagram

FS8530

MCU

✓ Application Note


AN12333

FS84, FS85 product guidelines

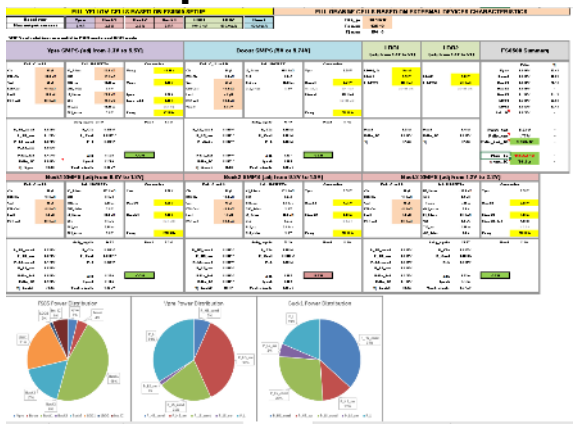
Rev. 2 — 6 November 2019

Application note

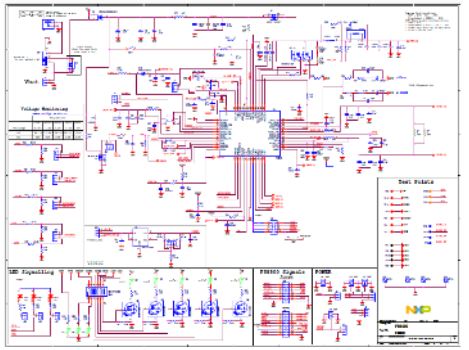
Document information

Information	Content
Keywords	FS84, FS85, power management, functional safety, EMC, ISO pulse, Non-ISO pulse, external components, SPI, I2C, CRC, Hardware
Abstract	This application note provides guidelines for integrating the FS84/FS85 system basis chip (SBC) family of devices into automotive electronic systems.

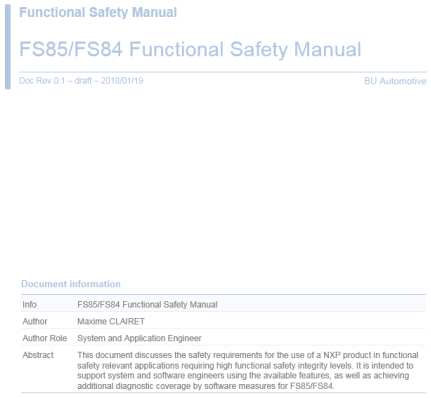
✓ Thermal Tool
✓ Including VPRE/VBOOST ext. components calculation



✓ PCB Schematic



✓ Safety Manual


Functional Safety Manual

FS85/FS84 Functional Safety Manual

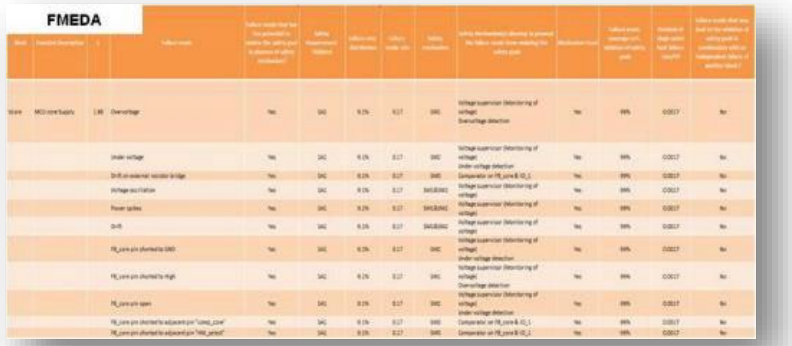
Doc Rev 0.1 – draft – 2019/01/19

BU Automotive

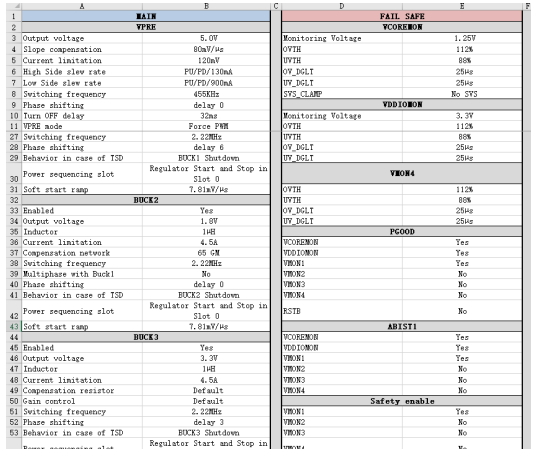
Document information

Info	FS85/FS84 Functional Safety Manual
Author	Maxime CLAIRET
Author Role	System and Application Engineer
Abstract	This document discusses the safety requirements for the use of a NXP product in functional safety relevant applications requiring high functional safety integrity levels. It is intended to support system and software engineers using the available features, as well as achieving additional diagnostic coverage by software measures for FS85/FS84.

✓ SafeAssure – FMEDA

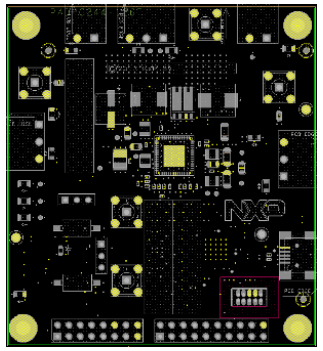

FMEDA

✓ OTP Configuration Tool



	MAIN		FAIL SAFE	
	VPRE		VCOREMON	
	Output voltage	5.0V	Monitoring Voltage	1.25V
	Slope compensation	80mV/µs	OVTH	112%
	Current limitation	120mV	UVTH	88%
	High Side slew rate	PU/PD/130mA	OV_DGLT	25µs
	Low Side slew rate	PU/PD/900mA	UV_DGLT	25µs
	Switching frequency	455KHz	SYS_CLAMP	No SYS
	Phase shifting	delay 0	VDDIOMON	
	Turn OFF delay	32ns	Monitoring Voltage	3.3V
	TPRE mode	Force PWM	OVTH	112%
	Switching frequency	2.22MHz	UVTH	88%
	Phase shifting	delay 6	OV_DGLT	25µs
	Behavior in case of TSD	BUCK1 Shutdown	UV_DGLT	25µs
	Power sequencing slot	Regulator Start and Stop in Slot 0	VMON4	
	Soft start ramp	7.81mV/µs	OVTH	112%
	BUCK2		OVTH	88%
	Enabled	Yes	OV_DGLT	25µs
	Output voltage	1.0V	UV_DGLT	25µs
	Inductor	1µH	PGOOD	
	Current limitation	4.5A	VCOREMON	Yes
	Compensation network	65 GM	VDDIOMON	Yes
	Switching frequency	2.22MHz	VMON1	Yes
	Multiphase with Buck1	No	VMON2	No
	Phase shifting	delay 0	VMON3	No
	Behavior in case of TSD	BUCK2 Shutdown	VMON4	No
	Power sequencing slot	Regulator Start and Stop in Slot 0	RSTB	No
	Soft start ramp	7.81mV/µs	ABIST1	
	BUCK3		VCOREMON	Yes
	Enabled	Yes	VDDIOMON	Yes
	Output voltage	3.3V	VMON1	Yes
	Inductor	1µH	VMON2	No
	Current limitation	4.5A	VMON3	No
	Compensation resistor	Default	VMON4	No
	Gain control	Default	Safety_enable	
	Switching frequency	2.22MHz	VMON1	Yes
	Phase shifting	delay 3	VMON2	No
	Behavior in case of TSD	BUCK3 Shutdown	VMON3	No
	Power sequencing slot	Regulator Start and Stop in		

✓ PCB Layout Recommendations



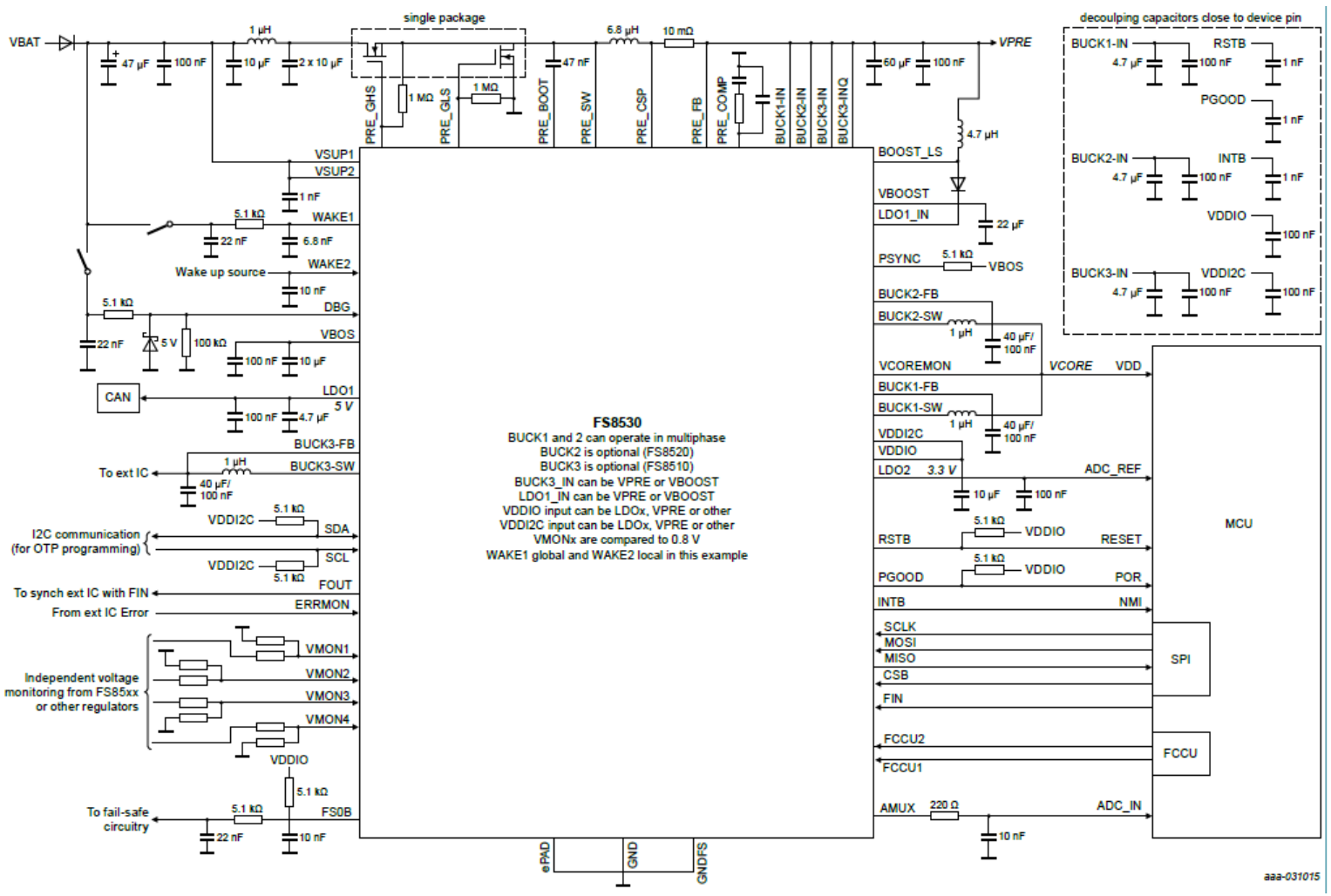
FS85 series already has information and links

NO	Document and tool information	Link to get the Tool
1	Latest version Datasheet for FS85_F84	Datasheet
2	Latest version Datasheet for VR5500	Datasheet
3	FS85 VPRE stability application note	AN12540
4	Hardware design application note	AN12333
5	FS85_FS84 Functional Safety Manual	SM537310（NDA required）
6	FS8500 Dynamic FMEDA	FM537415（NDA required）
7	FlexGUI for FS85_FS84 Family (REV 0.7.4)	Flex GUI
8	OTP Configuration tool	OTP Tool
9	KITFS85SKTEVM: FS84/FS85 safety SBC programming board	Summary UM11183 SCH-29627
10	KITFS85AEEVM:FS84/FS85 24 V/36 V safety SBC evaluation board for truck	Summary UM11193 SCH29774
11	KITFS85FRDMEVM: FS84/FS85 12 V safety SBC evaluation board for automotive	Summary UM11157 SCH-29838
12	FS85_FS84 Embedded Software Driver	Overview

04

Schematic design/OTP configuration

Schematic design and LAYOUT

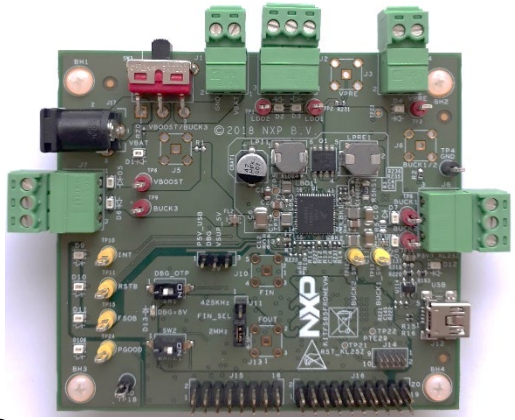


1. Customer schematics can be designed by referring to the Datasheet or the Application diagram of AN12333.
2. You can also refer to the NXP FS85_FS84 DEMO board designs. NXP can provide DEMO board .dsn format schematic diagram.
3. For device selection and BOM table, refer to Chapter 6 of AN12333.
4. Customers can check the schematic diagram item by item according to the "FS85 Schematic Diagram Self-Inspection Form“.
5. For layout, please refer to the Layout and PCB guidelines chapter of Datasheet and the EMC performance chapter of AN12333. NXP can provide .brd format Layout files for customer reference.

Notes and sources

FS8500 customers can refer to the DEMO boards

KITFS85FRDMEVM



Main Purpose

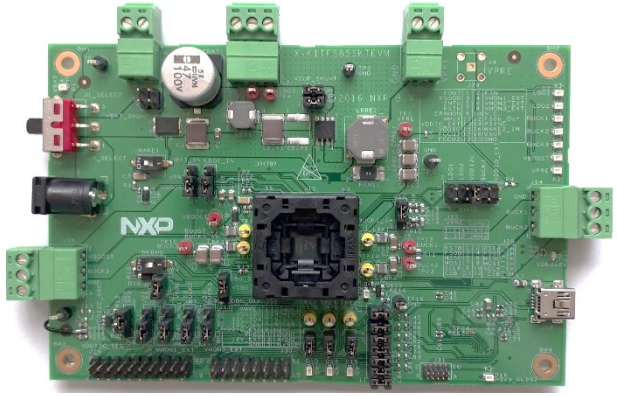
- **Automotive** evaluation
- Vpre evaluation up to 40V / 6A
- 12V Operation

Documentation

- Datasheet
- FlexGUI User Guide
- Board User Guide
- Schematic

APN Code: 29838 / Rev.C

KITFS85SKTEV



Main Purpose

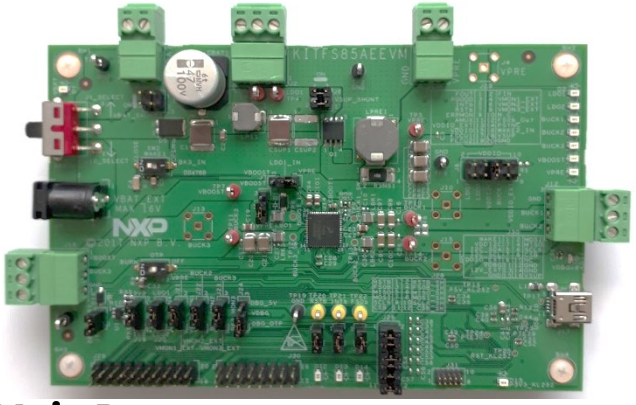
- OTP Configuration **Programming**
- Basic Tests & Evaluation

Documentation

- Datasheet
- FlexGUI User Guide
- Board User Guide
- Schematic

APN Code: 29627 / Rev.C

KITFS85AEEVM



Main Purpose

- **Truck** high voltage evaluation
- Vpre evaluation up to 60V / 10A
- 24V / 36V operation

Documentation

- Datasheet
- FlexGUI User Guide
- Board User Guide
- Schematic

APN Code: 29774 / Rev.C

- You can apply to download the corresponding schematic file on the NXP official website.

VPRE device selection – MOSFET selection

- Logical level NMOS, gate drive comes from VBOS (5.0 V)
- VDS > 60 V for 24 V truck and bus applications
- VDS > 40 V for 12 V automotive applications
- Qg < 15 nC at Vgs = 5.0 V is recommended for 455 kHz
- Qg < 7 nC at Vgs = 5.0 V is recommended for 2.22MHz

- Power dissipation is linked to RDSon and Qg:

RDSon	Qg	Pdis
↓	↑	High switching losses
↑	↓	High conduction losses

➔ Balance the dissipation between conduction and switching

- Qg takes current from VPRE driver, which takes current from VBOS with 50mA max current.

Applications	Fpre	Ipre < 2.0 A	Ipre < 4.0 A	Ipre < 6.0 A	Ipre < 10 A
12 V	455 kHz	BUK9K25-40E, BUK9K18-40E	BUK9K25-40E, BUK9K18-40E	BUK9K18-40E	BUK9K18-40E, NVTFS5C471NLWFTAG, HS = BUK9M9R5-40H, LS = BUK9M3R3-40H
	2.22 MHz	BUK9K25-40E, BUK9Y29-40E	BUK9K25-40E, BUK9Y29-40E	BUK9K25-40E, BUK9Y29-40E	N/A
24 V	455 kHz	BUK9K35-60E, BUK9K52-60E	BUK9K35-60E, BUK9K52-60E	BUK9K35-60E	BUK9K12-60E

Notes and sources

VPRE related calculations - loop and slope compensation calculations

Parameter	Symbol	Calculation		Value	EVB components value
Error amplifier gain	EA_{Gain}	$10^{\log\frac{Bw}{Fgbw}}$	(11)	0.94	—
Compensation network resistor	Rcomp	$\frac{Vout*EA_{Gain}}{gm\_EA}$	(12)	3.14 KΩ	3.57 KΩ
Capacitor In series	Ccomp	$\frac{1}{(2\pi*Fz*Rcomp)}$	(13)	9.8 nF	6.8 nF
Capacitor in parallel	Chf	$\frac{1}{(2\pi*Fp*Rcomp)}$	(14)	195 pF	150 pF
Slope compensation ramp	Se	$\frac{Vout*Rshunt*Ilim_{Gain}}{Lpre}$	(15)	Se > 35,1 mV/µs	Se > 40 mV/µs

- For details on the loop stability principle, please refer to AN12540.
- NXP provides the VPRE_VBOOST_Components calculation tool. Just fill in the relevant blue parts in the table on the right to automatically calculate the recommended values of the compensation circuit components and the minimum value required for slope compensation.
- The calculation formulas are as shown in the table above.

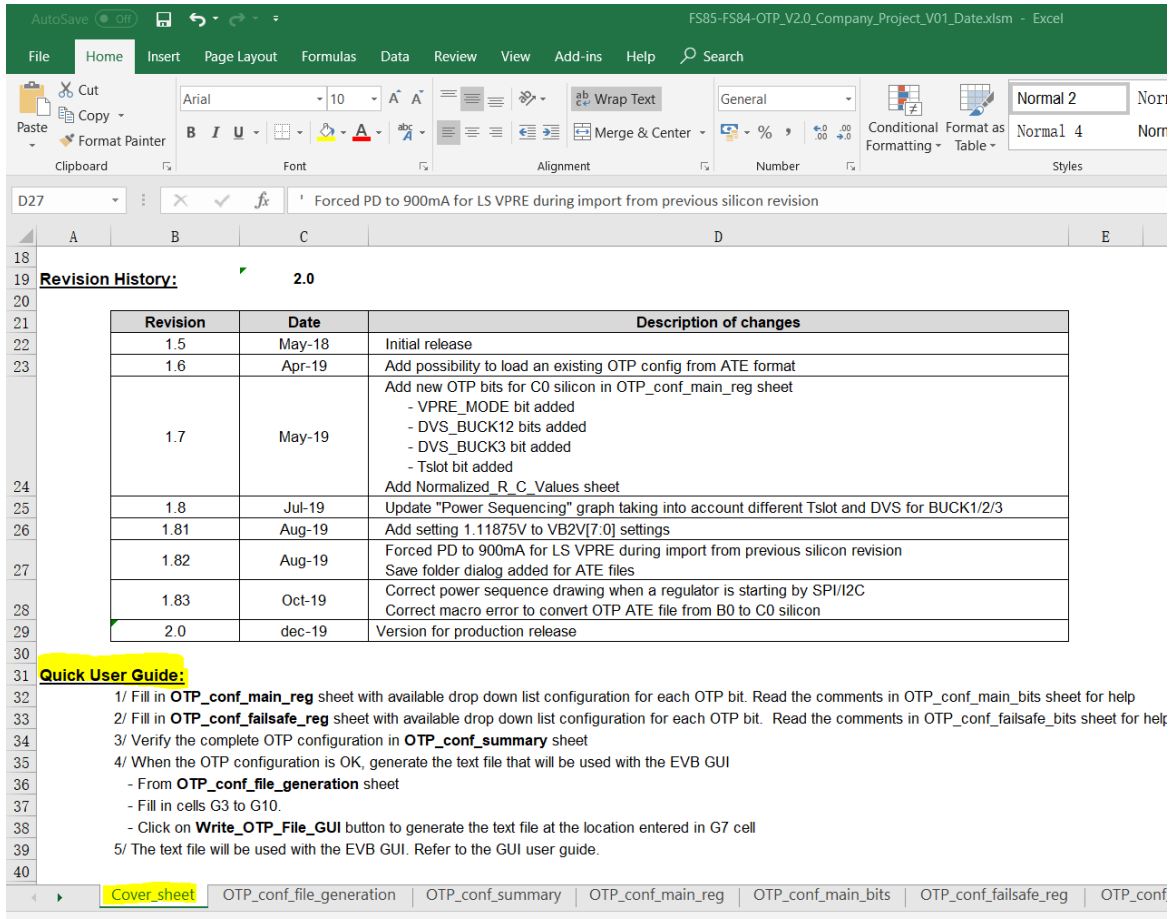
VPRE - 455KHz		
Vin (VSUP)	14	V
Vout (3.3 or 4.1 or 5.0V)	4.1	V
Duty Cyle (Eff=1)	0.29	
Fsw (455KHz or 2.22MHz)	455000	Hz
I_PRE_average	3	A
I_PRE_peak (in the inductor)	3.47	A
Inductor Current Ripple desired	30	%
Output Voltage Ripple desired	20	mV
Max dV desired	100	mV
Max dI desired	1.5	A
L_PRE_calculated	7.08	uH
L_PRE_selected from (4.7uH - 10uH @450KHz)	**6.80**	**uH**
Inductor Current Ripple Calculated	31.24	%
Cout_PRE_min (for ripple)	12.36	uF
Cout_PRE_min (for transient) Cout = dI / (2π x Fbw x dV)	52.47	uF
Cout_PRE_selected	**88.00**	**uF**
Max dV Calculated	60	mV
Cout_PRE_ESR	10.00	mΩ
Output Voltage Ripple Calculated	12.30	mV
Rsense (10 - 20)	20	mΩ
Bandwidth target (Fbw ~Fsw/10)	45500	Hz
Fz = Fbw/10 = 1/(2π x Rcomp x Ccomp)	4550	Hz
Fp = Fsw/2 = 1/(2π x Rcomp x Chf)	227500	Hz
EA transconductance (gmEA_PRE)	1.50	mS
Fgbw = 1/(Rsense x Acs x 2π x Cout)	18086	Hz
EA gain = (Vref/Vout) x gmEA x Rcomp	2.52	
Rcomp_Calculated	6.88	KΩ
Rcomp_selected	**6.8**	**KΩ**
Ccomp_calculated (min)	5.14	nF
Ccomp_selected	**4.7**	**nF**
Chf_calculated	102.73	pF
Chf_selected	**100**	**pF**
Discharge slope m=(Vout/L)	603	mA/us
Slope compensation to select SC > m x Rsense x Acs	60.29	mV/us
Current Limit to select must be >	69.37	mV

VPRE - 2.22MHz		
Vin (VSUP)	14	V
Vout (3.3 or 4.1 or 5.0V)	3.3	V
Duty Cyle (Eff=1)	0.24	
Fsw (455KHz or 2.22MHz)	2220000	Hz
I_PRE_average	3	A
I_PRE_peak (in the inductor)	3.26	A
Inductor Current Ripple desired	30	%
Output Voltage Ripple desired	20	mV
Max dV desired	100	mV
Max dI desired	1.5	A
L_PRE_calculated	1.26	uH
L_PRE_selected from (1.5uH - 4.7uH @2.22MHz)	**2.20**	**uH**
Inductor Current Ripple Calculated	17.21	%
Cout_PRE_min (for ripple)	2.53	uF
Cout_PRE_min (for transient) Cout = dI / (2π x Fbw x dV)	16.13	uF
Cout_PRE_selected	**22.00**	**uF**
Max dV Calculated	73	mV
Cout_PRE_ESR	20.00	mΩ
Output Voltage Ripple Calculated	11.65	mV
Rsense (10 - 20)	10	mΩ
Bandwidth target (Fbw ~Fsw/15)	148000	Hz
Fz = Fbw/10 = 1/(2π x Rcomp x Ccomp)	14800	Hz
Fp = Fsw/4 = 1/(2π x Rcomp x Chf)	555000	Hz
EA transconductance (gmEA_PRE)	1.50	mS
Fgbw = 1/(Rsense x Acs x 2π x Cout)	144688	Hz
EA gain = (Vref/Vout) x gmEA x Rcomp	1.02	
Rcomp_Calculated	2.25	KΩ
Rcomp_selected	**4.3**	**KΩ**
Ccomp_calculated (min)	2.50	nF
Ccomp_selected	**2.7**	**nF**
Chf_calculated	66.69	pF
Chf_selected	**68**	**pF**
Discharge slope m=(Vout/L)	1500	mA/us
Slope compensation to select SC > m x Rsense x Acs	75.00	mV/us
Current Limit to select must be >	32.58	mV

Notes and sources

FS85 series OTP configuration

- The customer did not find an OTP version suitable for the application among the standard versions listed in the Datasheet. When customer OTP customization is required, the FS85_FS84_OTP_Config.xlsm configuration tool must be used for configuration.
- Customers can follow the quick user guide in the Cover Sheet of the OTP configuration tool to configure the OTP file.
- The document "OTP Settings Guide" has a detailed description of the recommended values of OTP configuration information.



05

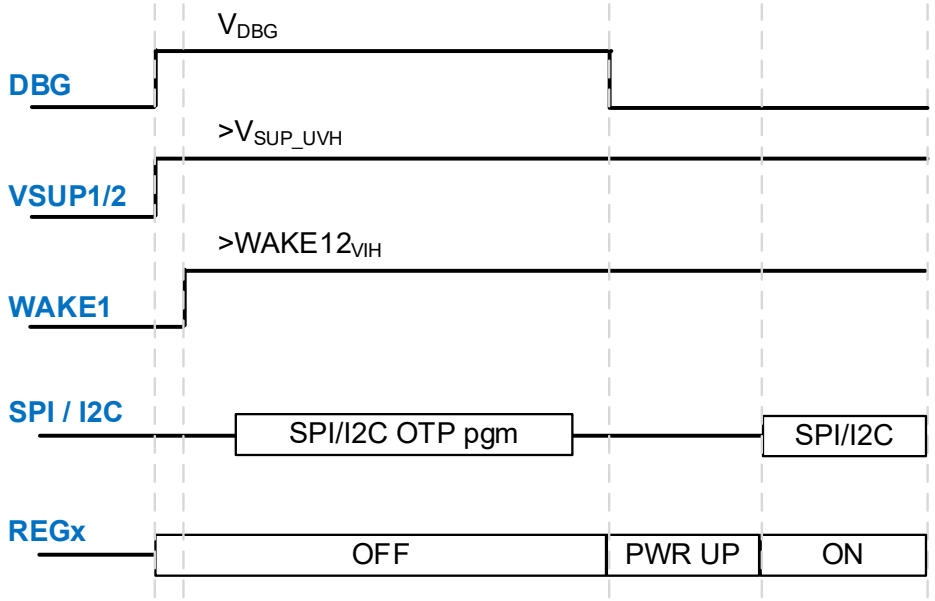
Debug mode/Deep Fail-safe mode

Debug mode

FS85/FS84 needs to meet the timing to enter DEBUG mode:

1. DBG pin = VDBG =5V and VSUP > VSUP_UVH > 6V
2. WAKE1 > WAKE12VIH > 4V

VDBG and VSUP can come up at the same time as long as WAKE1 or WAKE2 comes up the last.



Powering up in DEBUG mode allows the SBC to continue powering the MCU before the MCU program is debugged, and the power supply will not be interrupted due to repeated startup of the SBC due to reasons such as bad Watchdog refresh. Therefore, during the debugging process of FS85, the first power up and software debugging stages need to be started in Debug mode. After software debugging is OK, normal mode can be used to power up.

The DBG pin remains at 5V, and the power supply has no voltage output. The DBG pin must be 5V first and then 0V before powering up in Debug mode.

Debug debugging mode:

- Watchdog window becomes completely opened, and there is no limit on the Watchdog window period
- Fail-safe state machine (DFS=1) Deep Fail-safe request mode is not enabled
- RSTB's 8s monitoring function is turned off
- FS0B output pin cannot be released
- Allows the use of empty chips for OTP emulation and programming

Under what circumstances will DEEP-FS mode be entered?

1. VPRE_FB_OV detected (threshold is fixed at 6V)
2. Over-temperature protection TSD (Thermal Shut Down) and TSD assigned to DEEP-FS by OTP
3. The Fail-safe state machine sends the instruction DFS=1 to enter the deep fail-safe request
4. FLT_ERR_CNT reaches the limit set by FLT_ERR_CNT_LIMIT[1:0].
5. RSTB continues down for 8s.

Exit DEEP-FS mode

1. Wake1 is pulled low for more than 1ms
2. OTP_Autorety_en function enabled by OTP to automatically restart after 4 seconds.
3. If OTP_Autorety_en is enabled, OTP_Autoretry_infinite also enabled by OTP to be restarted countless times. If it is not enabled, it is only allowed to restart 15 times.

Notes and sources

06

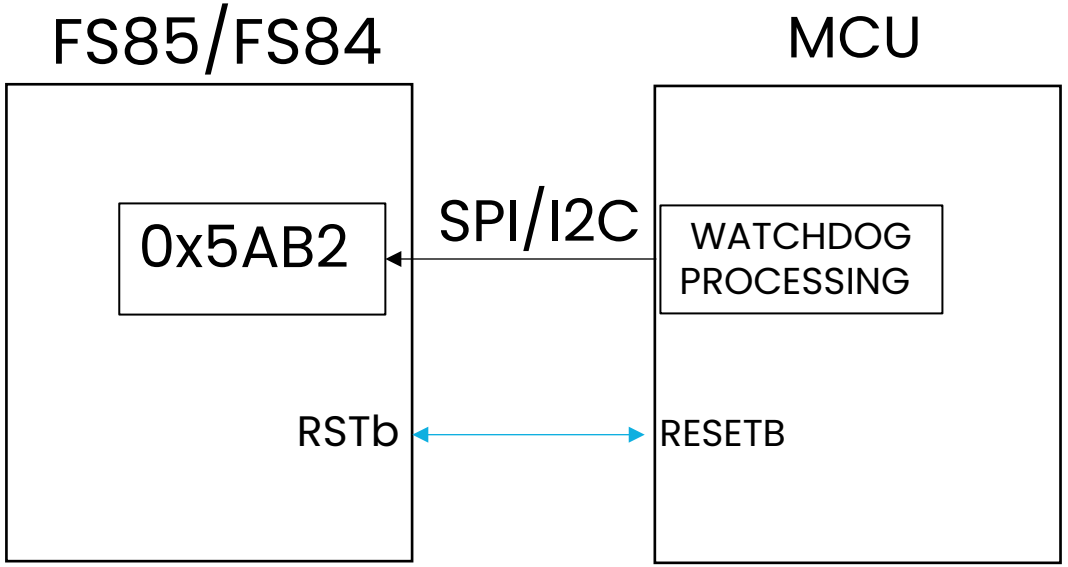
Watchdog mechanism

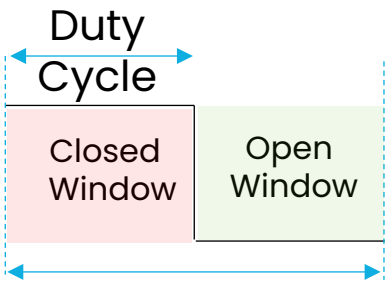
Watchdog mechanism

- Two Watchdog types available (Simple and Challenger) – set via OTP

Simple Watchdog

- The Watchdog's seed is constant: 0x5AB2 (default value).
- MCU can also change the WD_SEED.





Duty Cycle [2:0]	Value	
	Closed Window	Open Window
Duty Cycle [2:0]=000	31.25%	68.75%
Duty Cycle[2:0]=001	37.5%	62.5%
Duty Cycle[2:0]=010	50%	50%
Duty Cycle[2:0]=011	62.5%	37.5%
Duty Cycle[2:0]=100	68.75%	31.25%
Others	50%	50%

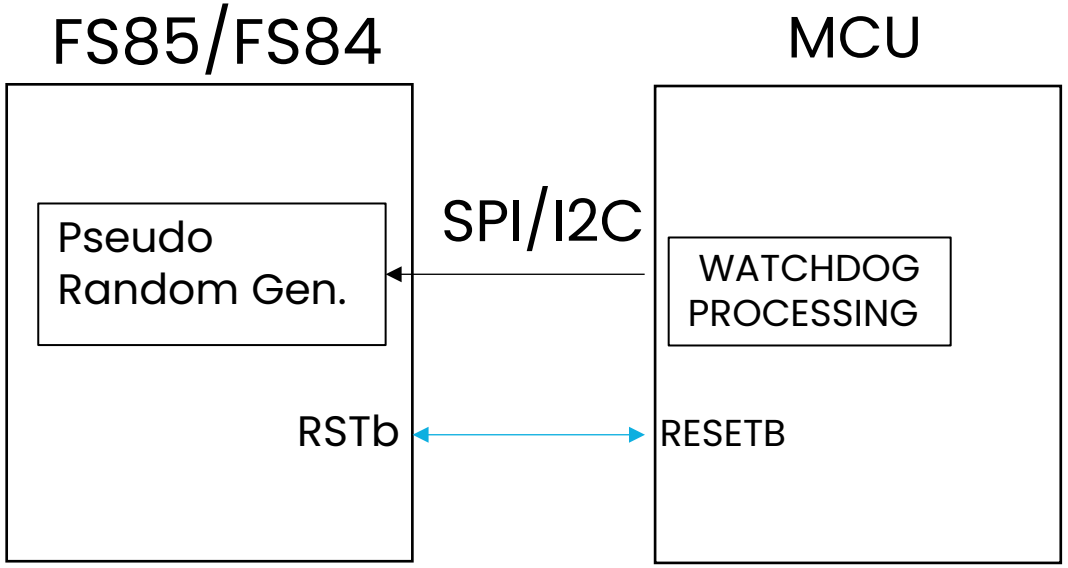
Parameter	Value
WD_WINDOW[3:0]=0000	DISABLE
WD_WINDOW[3:0]=0001	1 ms
WD_WINDOW[3:0]=0010	2 ms
WD_WINDOW[3:0]=0011	3 ms
WD_WINDOW[3:0]=0100	4 ms
WD_WINDOW[3:0]=0101	6 ms
WD_WINDOW[3:0]=0110	8 ms
WD_WINDOW[3:0]=0111	12 ms
WD_WINDOW[3:0]=1000	16 ms
WD_WINDOW[3:0]=1001	24 ms
WD_WINDOW[3:0]=1010	32 ms
WD_WINDOW[3:0]=1011	64 ms
WD_WINDOW[3:0]=1100	128 ms
WD_WINDOW[3:0]=1101	256 ms
WD_WINDOW[3:0]=1110	512 ms
WD_WINDOW[3:0]=1111	1024 ms

Notes and sources

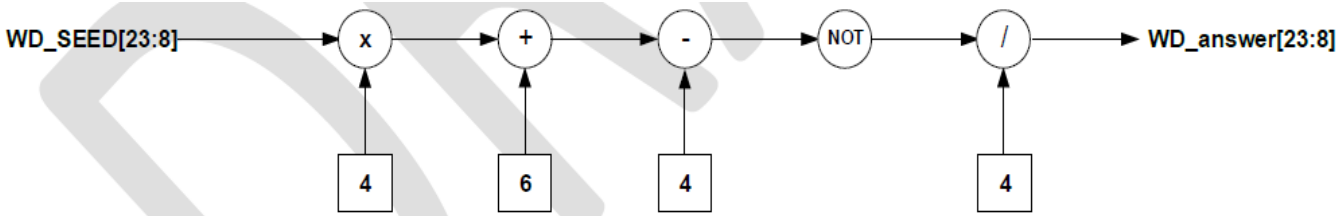
Watchdog mechanism

Challenger Watchdog

- Challenger Watchdog seed (WD_seed) is based on a 16-bit pseudo-random number
- After the MCU sends a good WD answer, FS85 automatically generates a new WD seed (WD_seed)
- Based on the algorithm (lower right), the WD answer is math by the MCU and FS85 (WD_answer)
- MCU sends calculation results to FS85/FS84 (Watchdog answer)
- FS85/FS84 compares the two results. If they are consistent, it is considered a good WD answer.



1 – MCU reads new Watchdog seed (WD_seed)
2 – MCU and PMIC respectively calculate WD answer



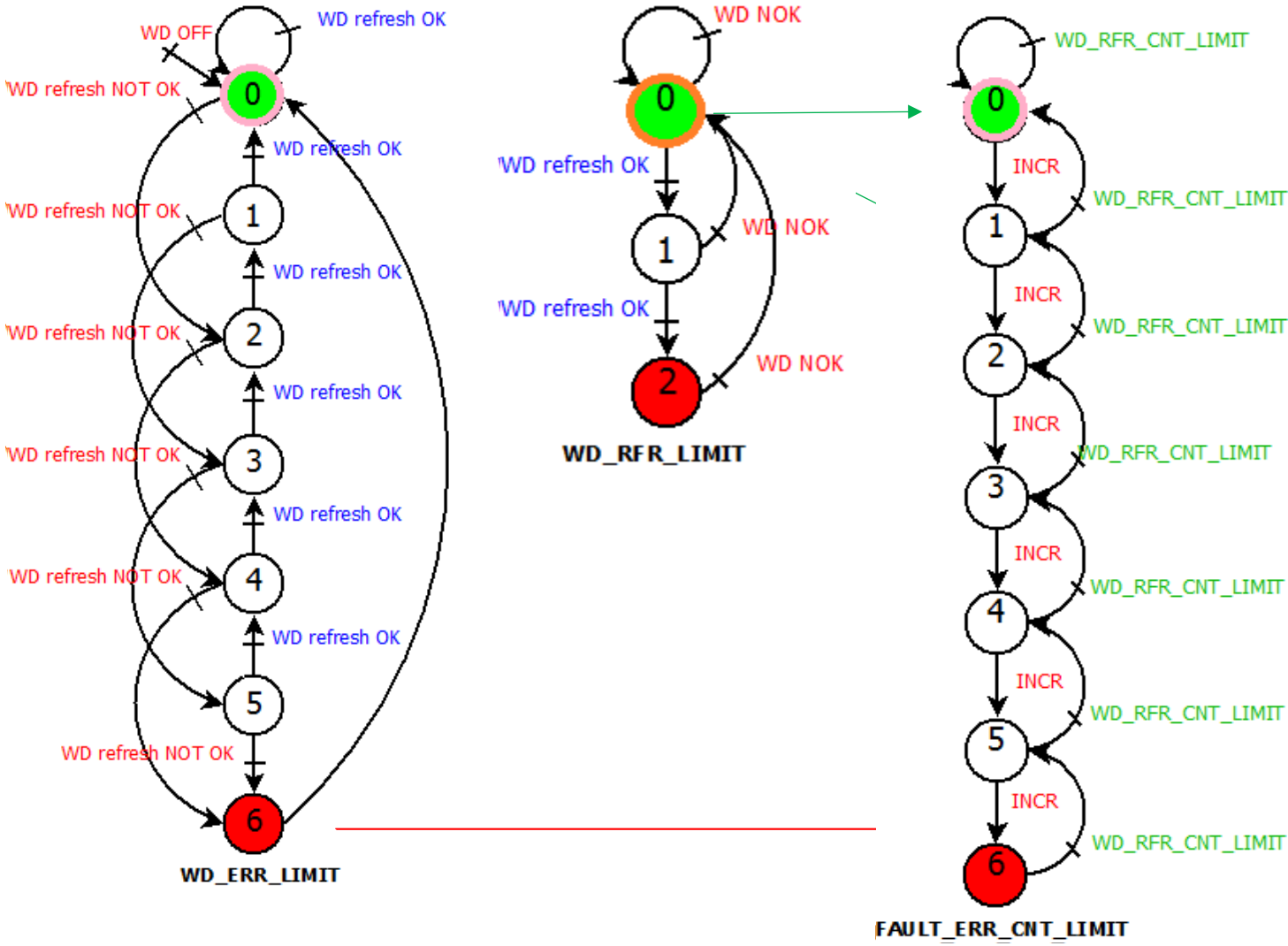
3 – MCU sends WD answer to FS85/FS84

Notes and sources

Watchdog mechanism example

- SBC configuration is as follows:
  - WD error counter max level = 6
  - WD Refresh counter max level = 2
  - Fault error counter max level = 6

- Result:
  - When there is once a bad WD refresh, the WD Error Counter increases by 2 and the WD Refresh Counter returns to zero.
  - After 3 bad WD refreshes, the WD Error Counter increases to 6, reaching the set threshold, and the Fault Error Counter increases by 1.
  - When the WD is once refreshed correctly, the WD Refresh Counter increases by 1 and the WD Error Counter decreases by 1.
  - Good 2 WD refreshes, the WD Refresh Counter will accumulate to 2 and reach the set threshold value. If there is another good WD refresh, the Fault Error Counter will decrease by 1.



GOOD WD REFRESH

Watchdog debugging considerations

1. The first debugging should be performed in debug mode for Watchdog debugging. After powering up in Debug mode, there is no cycle requirement for Watchdog refresh, and other Watchdog functions are still retained. WD Error Counter and WD Refresh Counter can be used to monitor whether the WD refreshes correctly.
2. The first WD refresh is the instruction to end the INIT_FS phase. It is different from WD refresh in the subsequent windows. If the first WD refresh is wrong, RSTB is pulled low and the Fault Error Counter is increased by 1.
3. If the bad WD refresh causes RSTB to be pulled low, it should first be checked whether the WD type selected by the OTP is consistent with the WD type selected by the MCU program to calculate the WD answer.
4. In Normal mode, if it is needed to temporarily turn off the Watchdog after powering up, it is needed to set the WD window WDW_PERIOD to 0b'0000 during the INIT_FS state after powering up.
5. If the Goto_Standby instruction is going to be used to return to the INIT_FS state to reconfigure the initialization register, it should be executed immediately after finishing a dog feeding session.

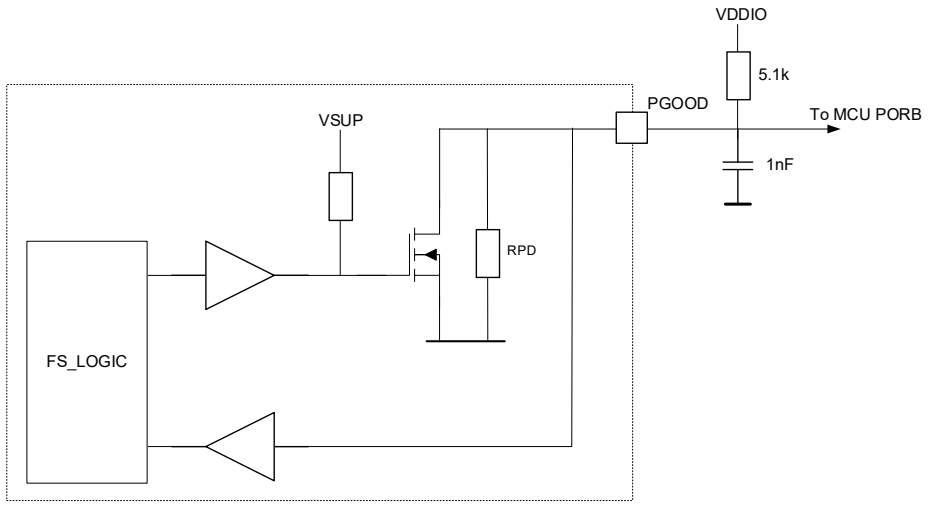
Notes and sources

07

Faults management and device reaction

PGOOD assertion fault list

	Fault Source	OTP function activation (Mask Level 1)
PGOOD ASSERTION	VCOREMON OV	OTP_PGOOD_VCORE
	VDDIO OV	OTP_PGOOD_VDDIO
	VMON1 OV	OTP_PGOOD_VMON1
	VMON2 OV	OTP_PGOOD_VMON2
	VMON3 OV	OTP_PGOOD_VMON3
	VMON4 OV	OTP_PGOOD_VMON4
	VCOREMON UV	OTP_PGOOD_VCOREMON
	VDDIO UV	OTP_PGOOD_VDDIO
	VMON1 UV	OTP_PGOOD_VMON1
	VMON2 UV	OTP_PGOOD_VMON2
	VMON3 UV	OTP_PGOOD_VMON3
	VMON4 UV	OTP_PGOOD_VMON4
	Deep Fail Safe	1



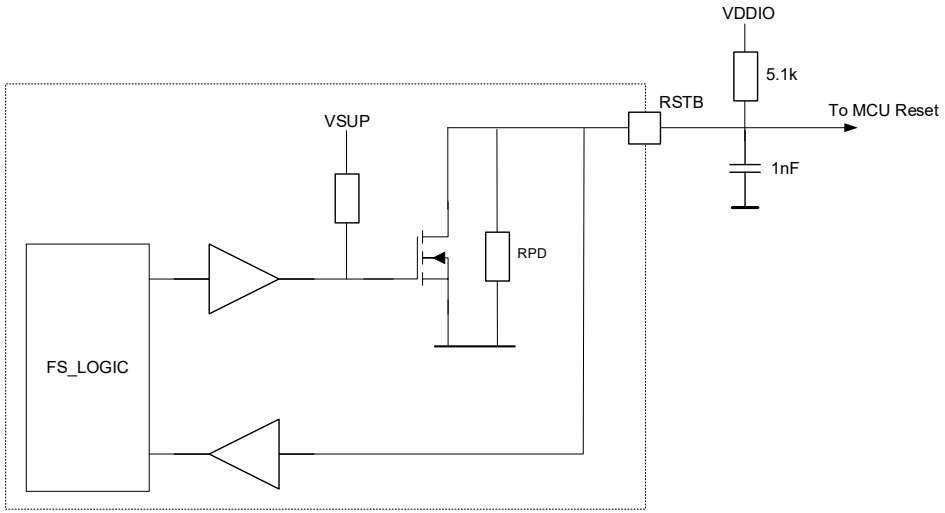
Assign PGOOD output and configure voltage monitoring through OTP.

➢Only the power monitoring results of the assigned circuit will cause PGOOD assertion when OV or UV occurs

RSTB assertion fault list

	Fault source
RSTb ASSERTION	WD error counter = max value
	BAD WD refresh (DATA) during INIT Phase
	Timeout INIT Phase (>256ms)
	VCOREMON OV or UV
	VDDIO OV or UV
	VMON1 OV or UV
	VMON2 OV or UV
	VMON3 OV or UV
	VMON4 OV or UV
	FCCU12 input (by pair)
	FCCU1 input (single)
	FCCU2 input (single)

	Fault source
RSTb ASSERTION	ERRMON
	FS0b Short to high
	Fault error counter level (severity)
	RSTb pulse requested by MCU
	External RESET out of extended RSTb

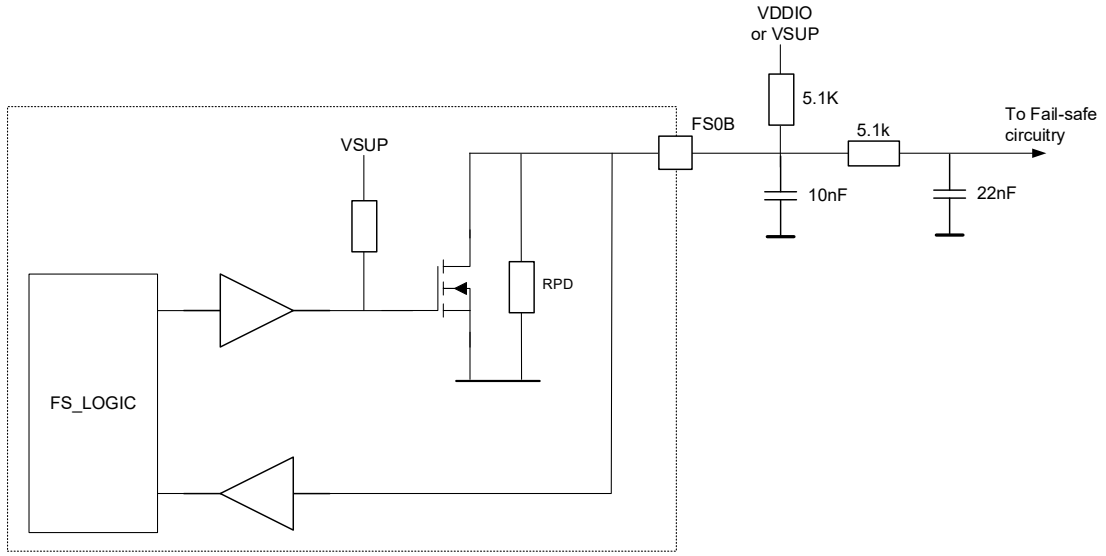


Notes and sources

FS0B assertion fault list

	Fault Source
FS0b assertion	WD error counter = max value
	VPRE OV (Buck 1 IN)
	VCOREMON OV or UV
	VDDIO OV or UV
	VMON1 OV or UV
	VMON2 OV or UV
	VMON3 OV or UV
	VMON4 OV or UV
	FCCU12 inputs (pin configuration by pair)
	FCCU1 input (single pin configuration)
	FCCU2 input (single pin configuration)

	Fault Source
FS0b assertion	ERRMON
	Fault error counter level (severity)
	FS0b Request by the MCU
	REG_CORRUPT
	OTP_CORRUPT



Notes and sources

Summary of Faults and SBC Reac

- Assign PGOOD output and configure voltage monitoring through OTP. The orange part is not configurable, green part can be configured via OTP for PGOOD or via SPI/I2C in INIT_FS stage for RSTB/FS0B
- If OTP_PGOOD_RSTB = '0' (default configuration), the RSTB and PGOOD pins work independently according to the table on the right. If OTP_PGOOD_RSTB = '1', all faults that cause RSTB assertion will also cause PGOOD assertion, unless RSTB is pulled high externally.

- PGOOD/RSTb/FS0B outputs are different safety levels.
- PGOOD safety level is 1. If PGOOD asserts (low), RSTB and FS0B must assert.
- RSTB safety level is 2. If RSTB asserts, FS0B will must assert, but PGOOD may not assert.
- FS0B safety level is 3. If FS0B is asserted, RSTB and PGOOD may not be asserted.
- The release (high) of RSTB is determined by the voltage monitoring assigned to PGOOD and ABIST1 (by OTP).

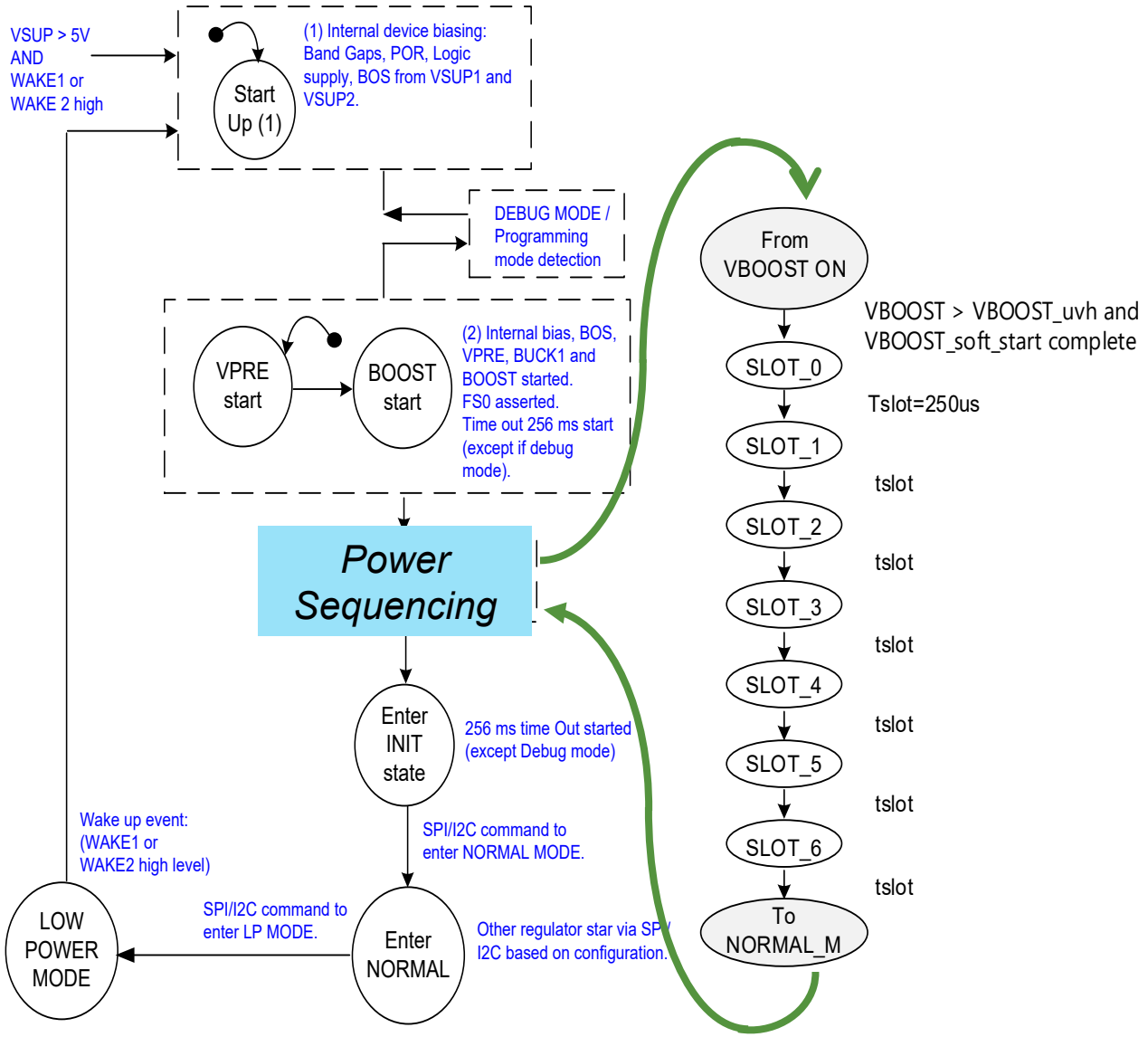
Apps related fail-safe faults	FLT_ERR_CNT increment	FS0B assertion	RSTB assertion	PGOOD assertion
VCOREMON_OV	+1	VCOREMON_OV_FS_IMPACT[0]	VCOREMON_OV_FS_IMPACT[1]	OTP_PGOOD_VCORE
VDDIO_OV	+1	VDDIO_OV_FS_IMPACT[0]	VDDIO_OV_FS_IMPACT[1]	OTP_PGOOD_VDDIO
VMONx_OV	+1	VMONx_OV_FS_IMPACT[0]	VMONx_OV_FS_IMPACT[1]	OTP_PGOOD_VMONx
VCOREMON_UV	+1	VCOREMON_UV_FS_IMPACT[0]	VCOREMON_UV_FS_IMPACT[1]	OTP_PGOOD_VCORE
VDDIO_UV	+1	VDDIO_UV_FS_IMPACT[0]	VDDIO_UV_FS_IMPACT[1]	OTP_PGOOD_VDDIO
VMONx_UV	+1	VMONx_UV_FS_IMPACT[0]	VMONx_UV_FS_IMPACT[1]	OTP_PGOOD_VMONx
FCCU12 (pair)	+1	FCCU12_FS_IMPACT	FCCU12_FS_IMPACT	No
FCCU1 (single)	+1	FCCU1_FS_IMPACT	FCCU1_FS_IMPACT	No
FCCU2 (single)	+1	FCCU2_FS_IMPACT	FCCU2_FS_IMPACT	No
ERRMON	+1	ERRMON_FS_IMPACT	ERRMON_FS_IMPACT	No
WD error counter = max value	+1	WD_FS_IMPACT[0]	WD_FS_IMPACT[1]	No
Fault error counter impact at intermediate Value	No	FLT_ERR_IMPACT[0]	FLT_ERR_IMPACT[1]	No
Wrong WD refresh in INIT_FS	+1	Yes	Yes	No
No WD refresh in INIT_FS	+1	Yes	Yes	No
External RESET (out of extended RSTB)	+1	No	Yes (low externally)	OTP_PGOOD_RSTB
RSTB pulse request by MCU	No	No	Yes	No
RSTB short to high	+1	Yes	No (high externally)	No
FS0B short to high	+1	No (high externally)	FS0B_SC_HIGH_CFG	No
FS0B request by the MCU	No	Yes	No	No
REG_CORRUPT = 1	+1	Yes	No	No
OTP_CORRUPT = 1	+1	Yes	No	No
GOTO_INITFS request by MCU	No	Yes	No	No

Notes and sources

08

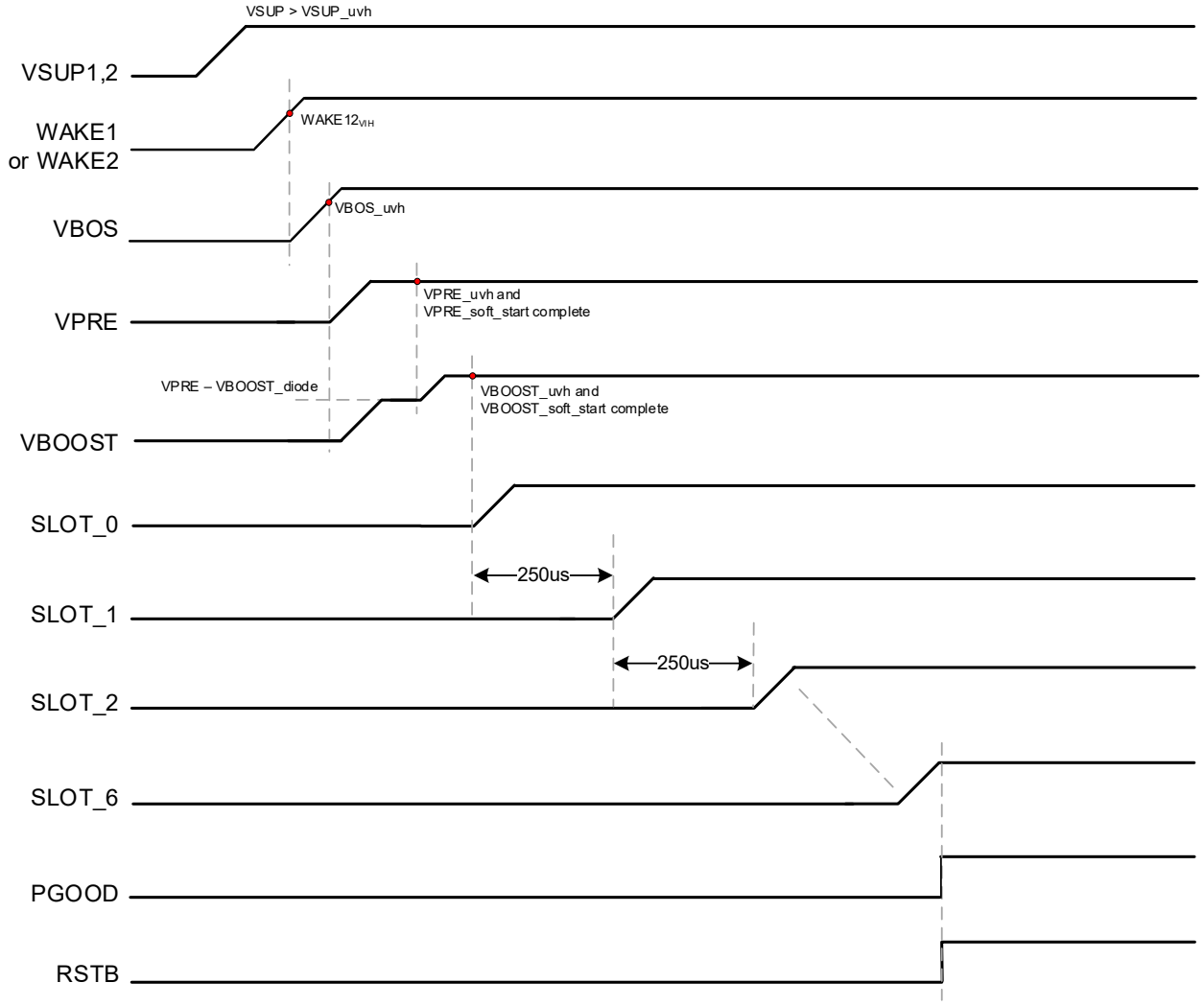
Start-up sequence

FS0B assertion fault list



OTP configuration

- VB1S[2:0] : Slot selection for LVBUCK1
- VB2S[2:0] : Slot selection for LVBUCK2
- VB3S[2:0] : Slot selection for LVBUCK3
- LDO1S[2:0] : Slot selection for LDO1
- LDO2S[2:0] : Slot selection for LDO2



➔ **Slot 7 is used for NOT automatically start up regulator. Regulator in this slot can be started later if needed by SPI/I2C.**

Power up and timing

- Question: How long does it take to power up until all supplies are powered on, or until RSTB is released?

1. RSTB release

RSTB is released when ABIST1 is done, so RSTB release time depends on ABIST1 OTP configuration. ABIST1 starts when the latest regulator assigned to ABIST1 is started, so it depends on the power-up sequence configured by OTP.

Typical power-up sequence starts as soon as VSUP > VSUP_UVH:

1. VBOS start up (max 1 ms)
2. When VBOS > VBOS_POR, LBIST execution (max 6 ms)
3. When LBIST done, VPRE start up (max 0.75 ms)
4. When VPRE > VPRE_UVH, VBOOST start up (max 0.75 ms)
5. When VBOOST > VBOOST_UVH, VREGx power-up sequence (OTP dependent, max 2 ms)
6. When last REGx assigned to ABIST1 is started, ABIST1 execution (max 1.2 ms)
7. When ABIST1 done, RSTB release (max 11.7 ms)

2. Verify

1. Verify LBIST and ABIST1 are pass
2. Verify Debug mode is not activated
3. Verify there is no OTP CRC error
4. Verify PGOOD was released

Notes and sources

Power on and timing

- Question: Which parameters need to be configured during the initialization phase? Which is the execution process after initialization is completed?

3. Configure FS_I and FS_I_NOT registers

1. Configure VCOREMON_OV_UV impact on RSTB and FS0B
2. Configure VDDIO_OV_UV impact on RSTB and FS0B
3. Configure VMONx_OV_UV impact on RSTB and FS0B
4. Configure ABIST2 assignment
5. Configure the WD window period, the WD window duty cycle, the WD counters limits and its impact on RSTB and FS0B. Ensure the configuration does not violate the FTTI requirement at system level.
6. Configure the Fault Error Counter limit and its impact on RSTB and FS0B at intermediate value
7. Configure the RSTB pulse duration
8. Configure MCU FCCU error monitoring and its impact on RSTB and FS0B
9. Configure Ext. IC error monitoring and its impact on RSTB and FS0B
10. Configure FS0B short to high impact on RSTB

4. Execute

1. Close INIT_FS by sending the first good WD refresh
2. Execute ABIST2 and verify it is pass
3. Clear all the flags by writing in FS_DIAG_SAFETY and FS_OVUVREG_STATUS
4. Clear the fault error counter to 0 with consecutive good WD refresh
5. Perform RSTB path check (steps 1 to 4 must be redo after RSTB is released)
6. Release FS0B pin
7. Perform FS0B safety path check
8. Refresh the WD according to its configuration
9. Check FS_GRL_FLAGS register after each WD refresh

The FS85/FS84 is now ready. If everything is ok for the MCU, it can release its own safety path and the ECU starts.

Notes and sources

09

Software debugging and diagnostics

Initialization phase configuration, how to re-enter INIT_FS state?

Initialization Phase (INIT_FS)

After power up, wake up from Standby or RSTB assertion, the INIT_FS is opened for 256 ms maximum when RSTB pin is released. FS85/FS84 is ready for safety initialization. To secure the writing process during INIT_FS, in addition to CRC computation during SPI/I2C transfer, the MCU must perform the following sequence for all INIT_FS registers:

1. Write the desired data in the FS_I_Register_N (DATA)
2. Write the opposite in the FS_I_NOT_Register_N (DATA_NOT)

As soon as the INIT_FS is closed, a real-time comparison process (XOR) is performed by the FS85/FS84 to ensure DATA FS_I_Register_N = DATA NOT FS_I_NOT_Register_N. If the comparison result is wrong, the REG_CORRUPT bit is set to 1 in FS_STATES register and FS0B pin is asserted.

INIT_FS must be closed by the first good watchdog refresh before the 256 ms timeout.

As soon as INIT_FS is closed, the MCU must refresh the Watchdog periodically.

The FS85/FS84 will go back to INIT_FS after the following two conditions:

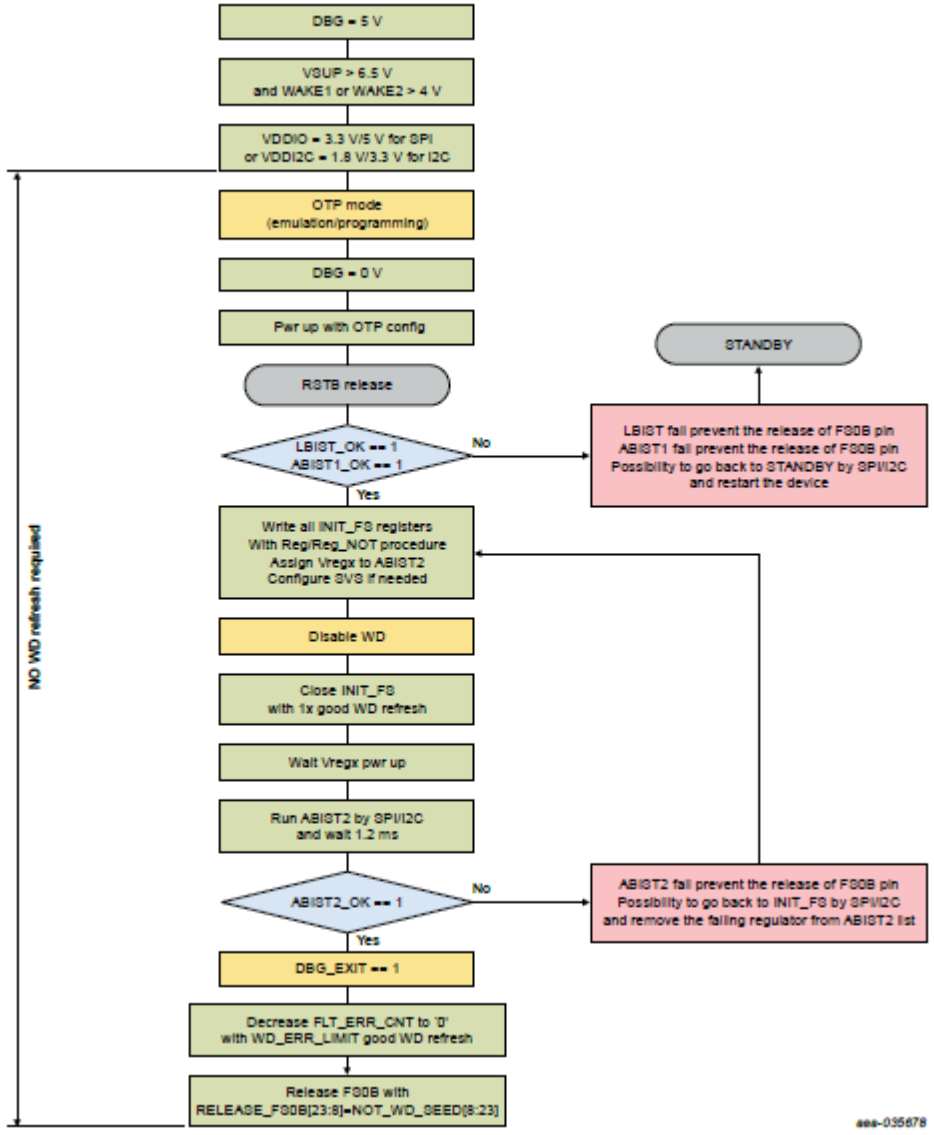
- RSTB pin assertion (internal or external)
- SPI/I2C request by the MCU with the bit GoTo_INITFS in FS_SAFE_IOs register

Notes and sources

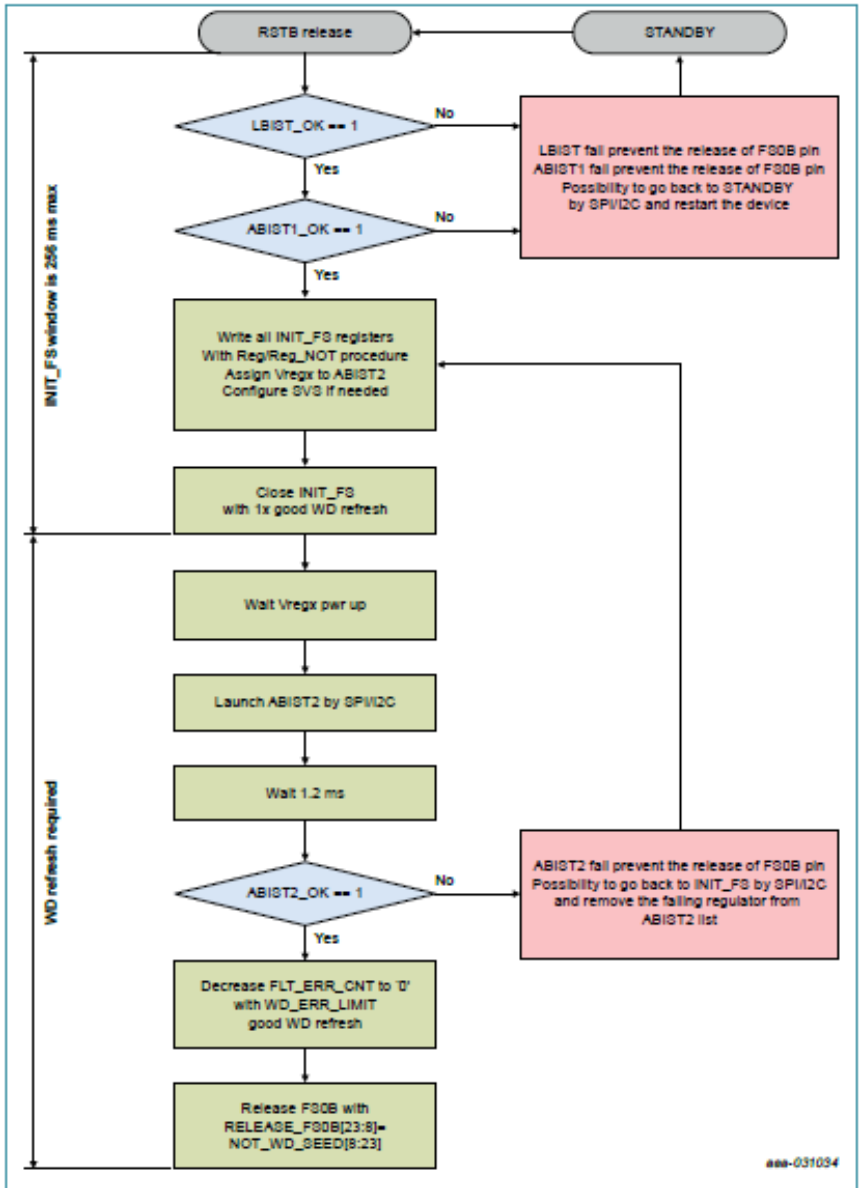
The simplest software debugging process

Reference data sheet 14.6 Flow cha

Debug mode debugging process



Normal mode starts the debugging process



FS0B release (simple steps)

FS0B release sequence after POR from Debug mode			
Simple WD		Challenger WD	
Register Name	Data	Register Name	Data
FS_WD_WINDOW	0x0200	FS_WD_WINDOW	0x0200
FS_NOT_WD_WINDOW	0xF50F	FS_NOT_WD_WINDOW	0xFDFF
FS_WD_ANSWER	0x5AB2	FS_WD_ANSWER	0xA54D
FS_STATES	0x4000	FS_STATES	0x4000
FS_WD_ANSWER	0x5AB2	FS_WD_ANSWER	0x4A9A
FS_WD_ANSWER	0x5AB2	FS_WD_ANSWER	0x9535
FS_WD_ANSWER	0x5AB2	FS_WD_ANSWER	0x2A6A
FS_WD_ANSWER	0x5AB2	FS_WD_ANSWER	0x54D4
FS_WD_ANSWER	0x5AB2	FS_WD_ANSWER	0xA9A9
FS_WD_ANSWER	0x5AB2	FS_WD_ANSWER	0x5353
FS_RELEASE_FS0B	0xB2A5	FS_RELEASE_FS0B	0x6565

1. Configure the watchdog period WDW_PERIOD [3:0] to 0 and disable the watchdog.
2. Exit DEBUG mode.
3. The initial value of FLT_ERR_CNT is 1. Send 6 good WD answer to clear it to 0.
4. Write the complement of WD_SEED to FS_RELEASE_FS0B. If there is no fault, FS0B can be released at this time
5. Software debugging should be started in Debug mode for debugging. After debugging the watchdog and FS0B release instructions without failure, start from Normal mode.

Notes and sources

Software diagnostic

Detailed SPI diagnostics are available by reading FS_DIAG_SAFETY register:

- SPI_FS_CLK bit reports an error in the number of SPI clock cycles
- SPI_FS_REQ bit reports an invalid Fail-safe SPI access (Wrong Write or Read, Write to INIT registers in normal mode, wrong address)
- SPI_FS_CRC bit reports an error in the CRC

Detailed I2C diagnostics are available by reading FS_DIAG_SAFETY register:

- I2C_FS_REQ bit reports and Invalid Fail-Safe I2C access (Wrong Write or Read, Write to INIT registers in normal mode, wrong address)
- I2C_FS_CRC bit reports an error in the CRC

Generic Fail-safe diagnostics are available by reading FS_GRL_FLAGS register:

- FS_COM_G bit reports an error in the communication (SPI or I2C). If this bit is set, read the FS_DIAG_SAFETY register for a detailed diagnostic
- FS_WD_G bit reports an error on the Watchdog refresh. If this bit is set, read the FS_DIAG_SAFETY register for a detailed diagnostic
- FS_IO_G bit reports an error in one of the Fail-safe IOs. If this bit is set, read the FS_SAFE_IOs register for a detailed diagnostic
- FS_REG_OVUV_G bit reports an error in one of the voltage monitoring (OV or UV). If this bit is set, read the FS_OVUVREG_STATUS register for a detailed diagnostic.

Notes and sources

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Other FAQs

What are the thermal resistance parameters?

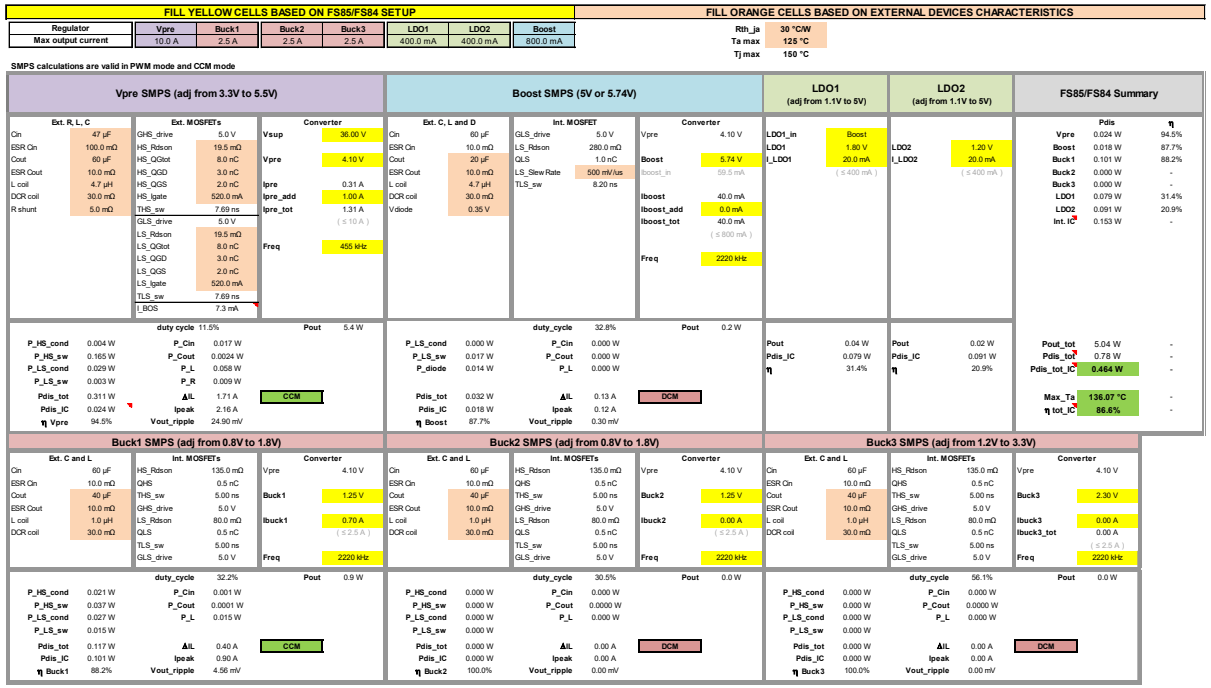
Table 6. Thermal ratings

Symbol	Parameter	Conditions	Min	Max	Unit
$R_{\theta JA}$	Thermal resistance junction to ambient	2s2p circuit board [1]	—	31	°C/W
$R_{\theta JA}$	Thermal resistance junction to ambient	2s6p circuit board [1]	—	23	°C/W
$R_{\theta JB}$	Thermal resistance junction to board	2s2p circuit board [1]	—	15	°C/W
$R_{\theta JB}$	Thermal resistance junction to board	2s6p circuit board [1]	—	10	°C/W
$R_{\theta JC\_BOT}$	Thermal resistance junction to case bottom	between the die and the solder pad on the bottom of the package [1]	—	1	°C/W
$R_{\theta JP\_TOP}$	Thermal resistance junction to package top	between package top and the junction temperature [1]	—	3	°C/W
T_A	Ambient temperature (Grade 1)		−40	125	°C
T_J	Junction temperature (Grade 1)		−40	150	°C
T_{STG}	Storage temperature		−55	150	°C

- Note: 2s2p is a 4-layer board, 2 signal layers and 2 power layers.

Notes and sources

How to evaluate heat dissipation?



FILL YELLOW CELLS BASED ON FS85/FS84 SETUP

FILL ORANGE CELLS BASED ON EXTERNAL DEVICES CHARACTERISTICS

Regulator	Vpre	Buck1	Buck2	Buck3	LDO1	LDO2	Boost
Max output current	10.0 A	2.5 A	2.5 A	2.5 A	400.0 mA	400.0 mA	800.0 mA

Rth_ja 30 °C/W
Ta max 125 °C
Tj max 150 °C

SMPS calculations are valid in PWM mode and CCM mode

Vpre SMPS (adj from 3.3V to 5.5V)

Ext. R, L, C: Cin 47 µF; ESR Cin 100.0 mΩ; Cout 60 µF; ESR Cout 10.0 mΩ; L coil 4.7 µH; DCR coil 30.0 mΩ; R shunt 5.0 mΩ

Ext. MOSFETs: GHS_drive 5.0 V; HS_Rdson 19.5 mΩ; HS_QGtot 8.0 nC; HS_QGD 3.0 nC; HS_QGS 2.0 nC; HS_Igate 520.0 mA; THS_sw 7.69 ns; GLS_drive 5.0 V; LS_Rdson 19.5 mΩ; LS_QGtot 8.0 nC; LS_QGD 3.0 nC; LS_QGS 2.0 nC; LS_Igate 520.0 mA; TLS_sw 7.69 ns; I_BOS 7.3 mA

Converter: Vsup 36.00 V; Vpre 4.10 V; Ipre 0.31 A; Ipre_add 1.00 A; Ipre_tot 1.31 A (≤ 10 A); Freq 455 kHz

duty cycle 11.5%; Pout 5.4 W

P_HS_cond 0.004 W; P_HS_sw 0.165 W; P_LS_cond 0.029 W; P_LS_sw 0.003 W; Pdis_tot 0.311 W; Pdis_IC 0.024 W; η Vpre 94.5%

P_Cin 0.017 W; P_Cout 0.0024 W; P_L 0.058 W; P_R 0.009 W; ΔIL 1.71 A; Ipeak 2.16 A; Vout_ripple 24.90 mV; CCM

Boost SMPS (5V or 5.74V)

Ext. C, L and D: Cin 60 µF; ESR Cin 10.0 mΩ; Cout 20 µF; ESR Cout 10.0 mΩ; L coil 4.7 µH; DCR coil 30.0 mΩ; Vdiode 0.35 V

Int. MOSFET: GLS_drive 5.0 V; LS_Rdson 280.0 mΩ; QLS 1.0 nC; LS_Slew Rate 500 mV/us; TLS_sw 8.20 ns

Converter: Vpre 4.10 V; Boost 5.74 V; Iboost_in 59.5 mA; Iboost 40.0 mA; Iboost_add 0.0 mA; Iboost_tot 40.0 mA (≤ 800 mA); Freq 2220 kHz

duty_cycle 32.8%; Pout 0.2 W

P_LS_cond 0.000 W; P_LS_sw 0.017 W; P_diode 0.014 W; Pdis_tot 0.032 W; Pdis_IC 0.018 W; η Boost 87.7%

P_Cin 0.000 W; P_Cout 0.000 W; P_L 0.000 W; ΔIL 0.13 A; Ipeak 0.12 A; Vout_ripple 0.30 mV; DCM

LDO1 (adj from 1.1V to 5V): LDO1_in Boost; LDO1 1.80 V; I_LDO1 20.0 mA (≤ 400 mA)

Pout 0.04 W; Pdis_IC 0.079 W; η 31.4%

LDO2 (adj from 1.1V to 5V): LDO2 1.20 V; I_LDO2 20.0 mA (≤ 400 mA)

Pout 0.02 W; Pdis_IC 0.091 W; η 20.9%

FS85/FS84 Summary

	Pdis	η
Vpre	0.024 W	94.5%
Boost	0.018 W	87.7%
Buck1	0.101 W	88.2%
Buck2	0.000 W	-
Buck3	0.000 W	-
LDO1	0.079 W	31.4%
LDO2	0.091 W	20.9%
Int. IC	0.153 W	-

Pout_tot 5.04 W; Pdis_tot 0.78 W; Pdis_tot_IC 0.464 W; Max_Ta 136.07 °C; η tot_IC 86.6%

Buck1 SMPS (adj from 0.8V to 1.8V)

Ext. C and L: Cin 60 µF; ESR Cin 10.0 mΩ; Cout 40 µF; ESR Cout 10.0 mΩ; L coil 1.0 µH; DCR coil 30.0 mΩ

Int. MOSFETs: HS_Rdson 135.0 mΩ; QHS 0.5 nC; THS_sw 5.00 ns; GHS_drive 5.0 V; LS_Rdson 80.0 mΩ; QLS 0.5 nC; TLS_sw 5.00 ns; GLS_drive 5.0 V

Converter: Vpre 4.10 V; Buck1 1.25 V; Ibuck1 0.70 A (≤ 2.5 A); Freq 2220 kHz

duty_cycle 32.2%; Pout 0.9 W

P_HS_cond 0.021 W; P_HS_sw 0.037 W; P_LS_cond 0.027 W; P_LS_sw 0.015 W; Pdis_tot 0.117 W; Pdis_IC 0.101 W; η Buck1 88.2%

P_Cin 0.001 W; P_Cout 0.0001 W; P_L 0.015 W; ΔIL 0.40 A; Ipeak 0.90 A; Vout_ripple 4.56 mV; CCM

Buck2 SMPS (adj from 0.8V to 1.8V)

Ext. C and L: Cin 60 µF; ESR Cin 10.0 mΩ; Cout 40 µF; ESR Cout 10.0 mΩ; L coil 1.0 µH; DCR coil 30.0 mΩ

Int. MOSFETs: HS_Rdson 135.0 mΩ; QHS 0.5 nC; THS_sw 5.00 ns; GHS_drive 5.0 V; LS_Rdson 80.0 mΩ; QLS 0.5 nC; TLS_sw 5.00 ns; GLS_drive 5.0 V

Converter: Vpre 4.10 V; Buck2 1.25 V; Ibuck2 0.00 A (≤ 2.5 A); Freq 2220 kHz

duty_cycle 30.5%; Pout 0.0 W

P_HS_cond 0.000 W; P_HS_sw 0.000 W; P_LS_cond 0.000 W; P_LS_sw 0.000 W; Pdis_tot 0.000 W; Pdis_IC 0.000 W; η Buck2 100.0%

P_Cin 0.000 W; P_Cout 0.0000 W; P_L 0.000 W; ΔIL 0.00 A; Ipeak 0.00 A; Vout_ripple 0.00 mV; DCM

Buck3 SMPS (adj from 1.2V to 3.3V)

Ext. C and L: Cin 60 µF; ESR Cin 10.0 mΩ; Cout 40 µF; ESR Cout 10.0 mΩ; L coil 1.0 µH; DCR coil 30.0 mΩ

Int. MOSFETs: HS_Rdson 135.0 mΩ; QHS 0.5 nC; THS_sw 5.00 ns; GHS_drive 5.0 V; LS_Rdson 80.0 mΩ; QLS 0.5 nC; TLS_sw 5.00 ns; GLS_drive 5.0 V

Converter: Vpre 4.10 V; Buck3 2.30 V; Ibuck3 0.00 A; Ibuck3_tot 0.00 A (≤ 2.5 A); Freq 2220 kHz

duty_cycle 56.1%; Pout 0.0 W

P_HS_cond 0.000 W; P_HS_sw 0.000 W; P_LS_cond 0.000 W; P_LS_sw 0.000 W; Pdis_tot 0.000 W; Pdis_IC 0.000 W; η Buck3 100.0%

P_Cin 0.000 W; P_Cout 0.0000 W; P_L 0.000 W; ΔIL 0.00 A; Ipeak 0.00 A; Vout_ripple 0.00 mV; DCM

Power Dissipation tool usage

1. NXP can provide Power dissipation tools to evaluate the power consumption on the chip to determine the heat generation during FS8x applications.
2. Customers can fill in the input and output voltage, load current of each rail, operating temperature and other information into the tool according to the application, and the tool will automatically calculate the power consumed on the PMIC chip.
3. When using the Power dissipation tool, confirm that the on-chip power consumption Pdis_tot_IC does not exceed 2.5W to ensure that the chip temperature is not too high.

How to improve the extra power on Pdis_tot_IC chip

1. LDO1 can select an input with a smaller voltage difference from the output.
2. If the LDO power loss is too large, consider using an external LDO instead.

Notes and sources

FS8x series quiescent current calculation: low power consumption design

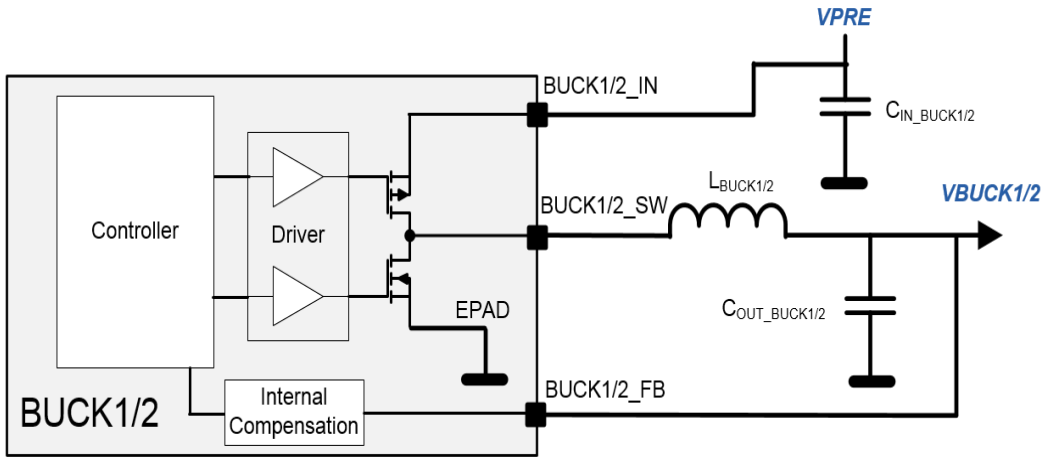
Symbol	Parameter	Min	Typ	Max	Unit
Power supply					
I_{SUP_NORMAL}	Current in Normal mode, all regulators ON (I_{OUT} = 0)	—	15	25	mA
$I_{SUP\_STANDBY}$	Current in Standby mode, all regulators OFF except VBOS	—	5	10	mA
I_{SUP_OFF1}	Current in OFF mode (Power Down), T_A < 85 °C	—	10	15	µA
I_{SUP_OFF2}	Current in OFF mode (Power Down), T_A = 125 °C	—	—	25	µA
V_{SUP_UV7}	VSUP undervoltage threshold (7.0 V)	7.2	7.5	7.8	V
V_{SUP_UVH}	VSUP undervoltage threshold high (during power up and Vsup rising) OTP_VSUP_CFG = 0	4.7	—	5.1	V
	VSUP undervoltage threshold high (during power up and Vsup rising) OTP_VSUP_CFG = 1	6.0	—	6.4	V
V_{SUP_UVL}	VSUP undervoltage threshold low (during power up and Vsup falling) OTP_VSUP_CFG = 0	4.0	—	4.4	V
	VSUP undervoltage threshold low (during power up and Vsup falling) OTP_VSUP_CFG = 1	5.3	—	5.7	V
T_{SUP_UV}	V_{SUP_UV7}, V_{SUP_UVH} and V_{SUP_UVL} filtering time	6.0	10	15	µs

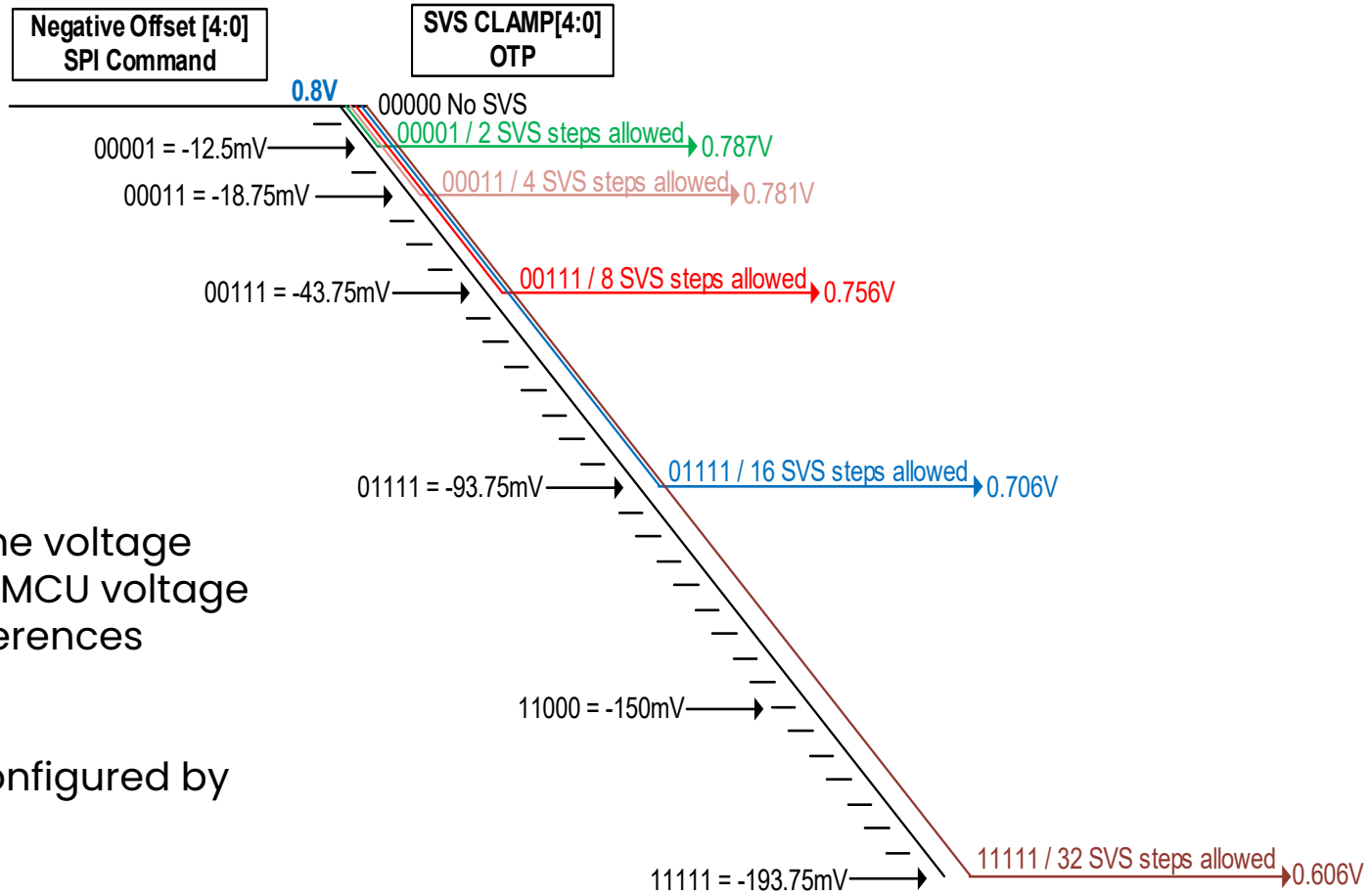
1. The different modes' static power consumption is as above. Isup_off is the Iq when FS8x enters Power Down mode. At ambient temperature (25°C), the typical value is 10uA.
2. If the system requires a low-power design, GoTo_STBY can be sent through the MCU and pull Wake1/2 low to make the device enter Power Down mode (to save power consumption).

Notes and sources

After power up, can the rails voltage be changed using the MCU?

- For safety reasons, only BUCK1/2 can adjust the static voltage downward to a certain range. The mechanism is as follows. Other circuit voltages cannot be changed.





- Static voltage scaling function allows to reduce the voltage configured by OTP after power up to optimize the MCU voltage operating point and compensate for process differences between various parts.
- The maximum range allowed for adjustment is configured by OTP VCORE_SVS_CLAMP[4:0].
- The actual negative voltage offset applied is implemented by SPI/I2C (SVS_OFFSET [4:0]). Each step corresponds to -6.25mV.

Notes and sources

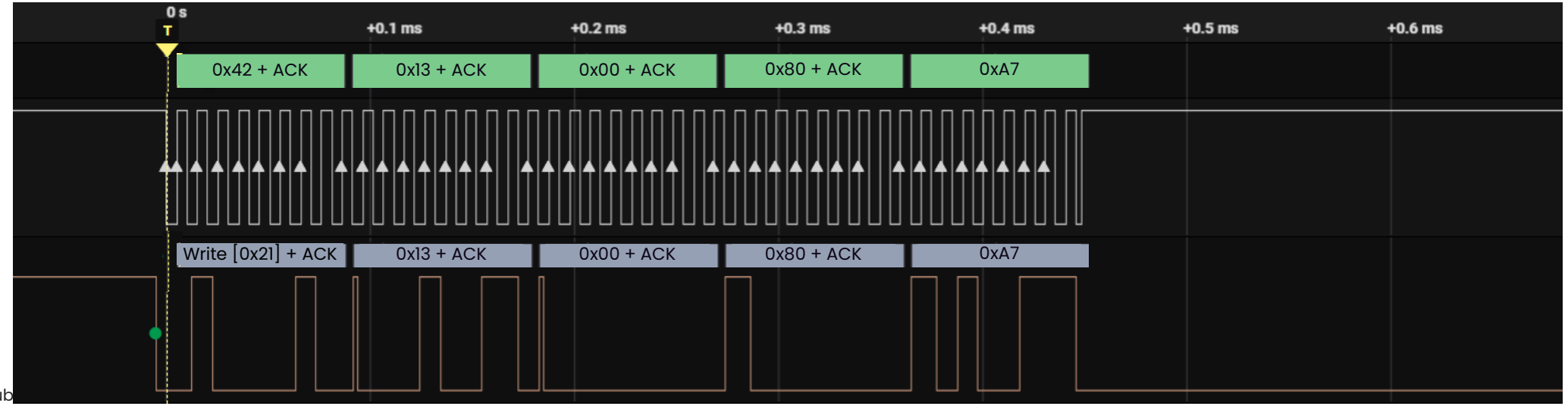
I2C communication stuck after sending RSTB_REQ

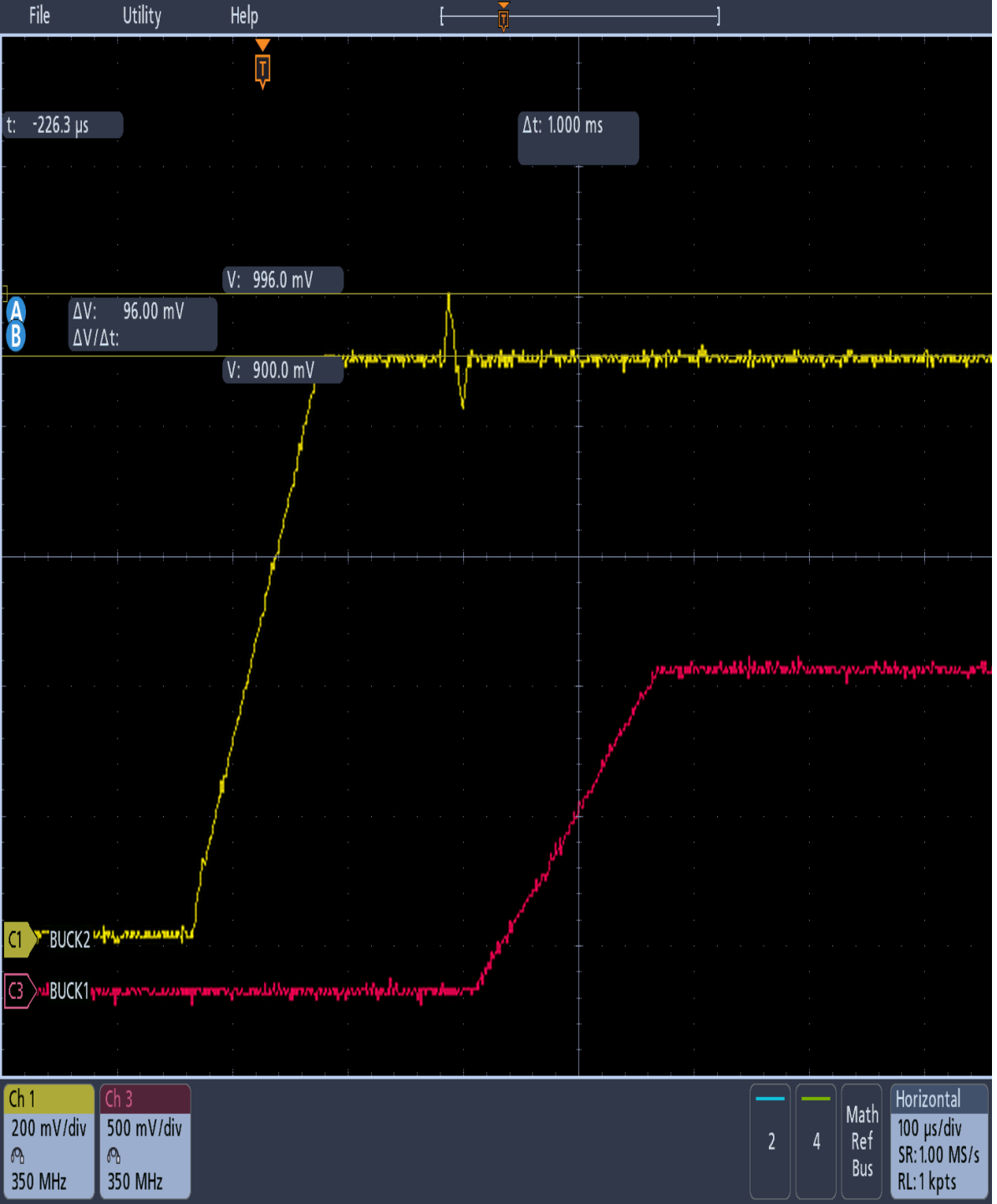
Customer may meet I2C stuck after sending the RSTB_REQ command, the stuck means SDA is pulled low and SCL is kept high status, and the communication of I2C cannot work anymore.

After sending the RSTB_REQ, the master will reset immediately after receiving the command (before the slave sends the acknowledge). Since SDA data from Slave is '0' for the acknowledge, slave will wait master to take away the '0' by one SCL falling edge, but the SCL is always keeping in high status, so the I2C Bus will stuck.

To solve the 2C stuck and make Bus recovery, there are 2 ways which can be tried to use:

1) Reset Slave device when I2C stuck through Hard WD reset by WDI or restart WAKEx
2) Operate I2C BUS Clear, If the data line (SDA) is stuck in LOW, the master should send nine clock pulses. The device that held the bus LOW should release it sometime within those nine clocks. If no, then use the HW reset or cycle power to clear the bus.





BUCKx over/undershoot when another BUCK is enabled

When a LVBUCK is enabled, there is a peak in its bias current before stabilizing. This bias current peak induces, through coupling, a drop in the bias current of another BUCK block, resulting in a voltage overshoot/undershoot on this affected BUCK's output.

The affected BUCKs and their respective aggressors are listed below:

When BUCKx enabled	Affected BUCK
BUCK1	BUCK2
BUCK2	BUCK1
BUCK3	BUCK2

BUCKx over/undershoot when another BUCK is enabled

Over/undershoot was found to be as high as **±96 mV** at the conditions listed below:

- V_{BUCK1} = 1.25 V
- V_{BUCK2} = 0.9 V
- No load
- C_{OUT_BUCK2} = 44 µF
- Temperature = 25 °C
- Standard BOM

These tests were performed with BUCK1 as the aggressor and BUCK2 as the affected regulator

Note: When a load is added, the over/undershoot decreases.

With 1.25 A load at BUCK1 and 1 A at BUCK2, over/undershoot was found to be as high as **±56 mV**.

Notes and sources

BUCKx over/undershoot when another BUCK is enabled

Work-around:

1. The overshoot / undershoot is reduced with a higher output capacitance.
2. Ensure that the aggressor is turned On before or in the same slot as the affected regulator.
3. Do not toggle the aggressor Off and On during normal operation.

Notes and sources

VBOOST = 4.4 V when FS85/84 goes to DFS at low loads

The device's VBOOST stays at 4.4 V when it goes to DFS under the condition in which the BOOST load is very low ($I_{BOOST\_OUT} \leq 4.3$ mA approximately).

This happens because an internal RCP (Reverse Current Protection) is activated at low loads to protect the internal VBOS circuitry. This causes that the BOOST output capacitors are unable to discharge since the current cannot flow anymore, making VBOOST stay at 4.4 V.

Notes and sources

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Diagnosis of board anomalies

Diagnosis of FS85 series power up abnormalities

After the SBC is powered up, all power supplies have not output

- Check the status of Vsup and Wake, and based on this, check whether VBOS is stable at 5V. If everything is normal and the power supply has not output, then it is most likely that the PMIC and the OTP are blank. Remove the chip and send it to the chip agent or NXP to confirm whether the OTP has not been programmed into the chip.

After the SBC is powered up, the output voltage switches periodically. Possible reasons:

1. For FS85 and FS84, the WD is enabled and the MCU does not send a WD answer periodically or the WD answer is wrong.
2. FCCU is enabled by OTP, but FCCU status monitoring fails.
3. Check whether the voltage monitoring circuit level enabled by OTP is correct. Whether VCOREMON is connected to BUCK1 output and the voltage value is correct. Whether the VDDIO level is consistent with the OTP configuration level. Whether the voltage of the power rail monitored by the enabled VMONx channel divided by the resistor bridge to the VMONx pin is 0.8V.
4. Check the external load. This problem may be caused by OV, UV or overcurrent of some power supplies. The diagnosis method is to detect the interrupt flag bits of these faults through I2C to determine whether there are corresponding faults.

Notes and sources

RSTB reset cause diagnosis

After power-on, RSTB is always at low level and cannot be released:

1. RSTB is not pulled up to VDDIO. RSTB is open drain and must be pulled up externally.
2. Check whether PGOOD cannot be released. If so, check whether the voltage rail assigned to PGOOD is normal.
3. The monitoring power rail assigned to ABIST1 by OTP is abnormal, or the VMONx voltage dividing resistor value is incorrect.
4. There is a fault on the MCU side, and RSTB is continuously pulled low externally. If the MCU pin can be disconnected, the cause can be determined.

Notes and sources

RSTB reset cause diagnosis

RSTB can be released to a high level as soon as it is powered, but it is reset and pulled low later:

1. After power up, there is not a WD answer within 256ms after RSTB is released, or there is a wrong WD answer.
2. OV, UV fault occurs in the voltage monitoring with monitoring enabled.
3. FCCU is enabled, but the FCCU level is in fault state
4. ERRMON is enabled, but ERRMON detects a fault
5. Fault Error Counter reaches half of the set maximum value
6. RSTB is externally pulled low
7. MCU issues RSTB request
8. When FS0B is shorted to high, RSTB detects a fault.
9. PGOOD is a higher security level, so a PGOOD action (pull low) leads to a RSTB action.

Apps related fail-safe faults	FLT_ERR_CNT increment	FS0B assertion	RSTB assertion	PGOOD assertion
VCOREMON_OV	+1	VCOREMON_OV_FS_IMPACT[0]	VCOREMON_OV_FS_IMPACT[1]	OTP_PGOOD_VCORE
VDDIO_OV	+1	VDDIO_OV_FS_IMPACT[0]	VDDIO_OV_FS_IMPACT[1]	OTP_PGOOD_VDDIO
VMONx_OV	+1	VMONx_OV_FS_IMPACT[0]	VMONx_OV_FS_IMPACT[1]	OTP_PGOOD_VMONx
VCOREMON_UV	+1	VCOREMON_UV_FS_IMPACT[0]	VCOREMON_UV_FS_IMPACT[1]	OTP_PGOOD_VCORE
VDDIO_UV	+1	VDDIO_UV_FS_IMPACT[0]	VDDIO_UV_FS_IMPACT[1]	OTP_PGOOD_VDDIO
VMONx_UV	+1	VMONx_UV_FS_IMPACT[0]	VMONx_UV_FS_IMPACT[1]	OTP_PGOOD_VMONx
FCCU12 (pair)	+1	FCCU12_FS_IMPACT	FCCU12_FS_IMPACT	No
FCCU1 (single)	+1	FCCU1_FS_IMPACT	FCCU1_FS_IMPACT	No
FCCU2 (single)	+1	FCCU2_FS_IMPACT	FCCU2_FS_IMPACT	No
ERRMON	+1	ERRMON_FS_IMPACT	ERRMON_FS_IMPACT	No
WD error counter = max value	+1	WD_FS_IMPACT[0]	WD_FS_IMPACT[1]	No
Fault error counter impact at intermediate Value	No	FLT_ERR_IMPACT[0]	FLT_ERR_IMPACT[1]	No
Wrong WD refresh in INIT_FS	+1	Yes	Yes	No
No WD refresh in INIT_FS	+1	Yes	Yes	No
External RESET (out of extended RSTB)	+1	No	Yes (low externally)	OTP_PGOOD_RSTB
RSTB pulse request by MCU	No	No	Yes	No
RSTB short to high	+1	Yes	No (high externally)	No
FS0B short to high	+1	No (high externally)	FS0B_SC_HIGH_CFG	No
FS0B request by the MCU	No	Yes	No	No
REG_CORRUPT = 1	+1	Yes	No	No
OTP_CORRUPT = 1	+1	Yes	No	No
GOTO_INITFS request by MCU	No	Yes	No	No

Notes and sources

RSTB reset reason query steps

1. First, in Debug mode, check whether the RSTB assertion still occurs. Since Debug mode is activated, there is no need to send a WD answer periodically. If RSTB no longer operates in Debug mode, that means that RSTB assertion is caused by the WD. BAD_WD_DATA and BAD_WD_TIMING of FS_DIAG_SAFETY bits can be also read to determine whether there is a WD failure.
2. Check whether PGOOD is also low level. If so, first check whether there is an OV/UV fault on the assigned circuit of PGOOD. Read the FS_OVUVREG_STATUS register to know the source of the fault. It should be noted that the default value of UV power up is 1, so it is needed to write 1 after power up to clear the initial fault.
3. If FCCU is enabled by OTP and RSTB assertion is assigned to this fault, check whether the FCCUx bit in FS_DIAG_SAFETY reports the FCCU fault.
4. If ERRMON is enabled by OTP and RSTB is assigned to this, check whether the ERRMON bit in FS_DIAG_SAFETY reports the ERRMON fault.
5. Read the FLT_ERR_CNT[3:0] in the FS_I_FSSM register to see if it exceeds half of the set maximum value.
6. Ensure the MCU does not write 1 to the RSTB_REQ bit of the FS_SAFE_IO register to request a reset.

Notes and sources

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Reference power tree and Part Number

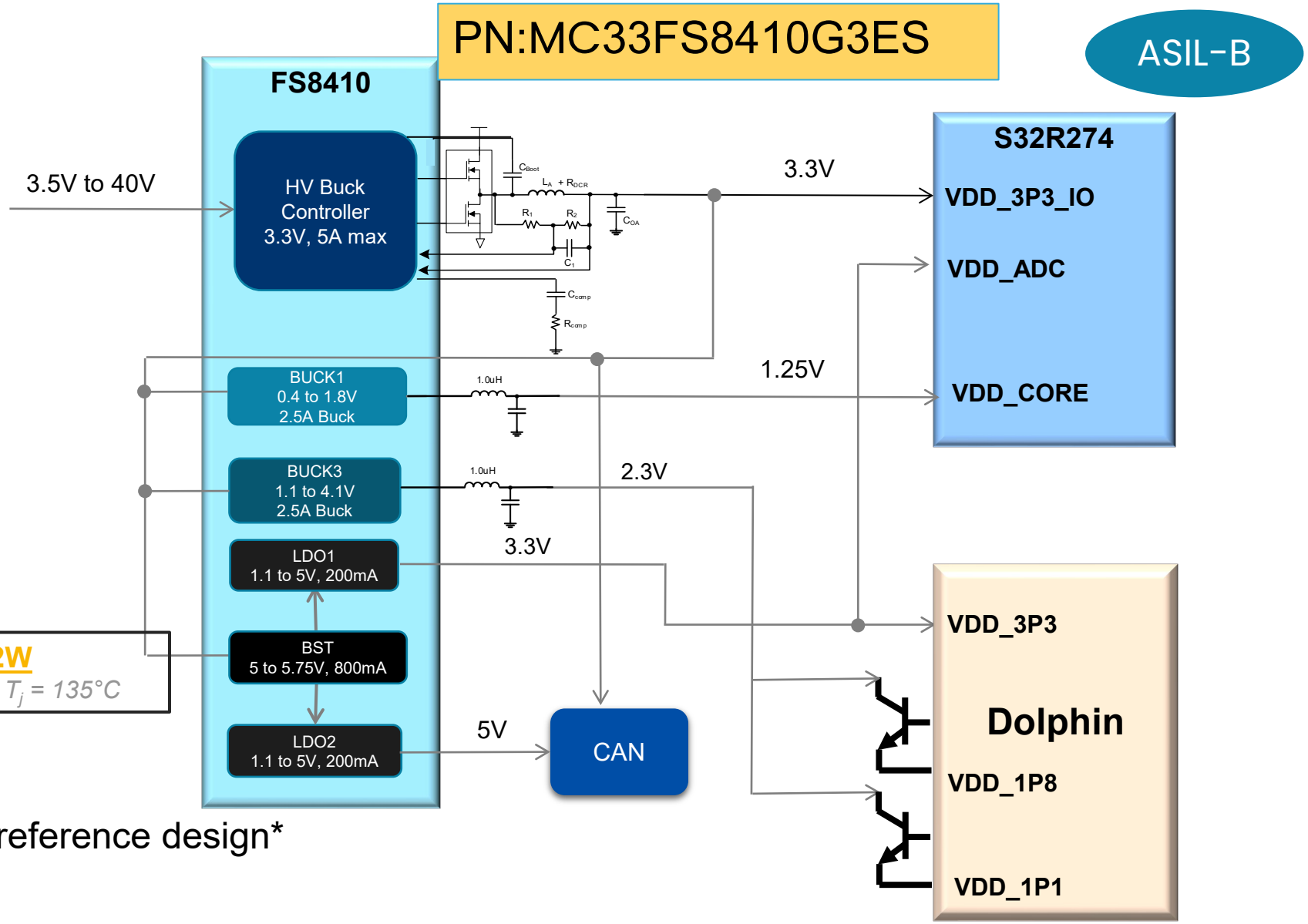
SRR Solution with RRU (S32R274), Dolphin & FS8410 *(Cocoon 2.0 board)*

Power Rail [V]	RRU Current
1.25V CORE	1.2A Average 1.5 A max
3.3V ADC, I/O	75 mA

Power Rail [V]	Dolphin Current
2.3V Rail	650mA average 1.5 A max
3.3V Rail	33 mA

Total Input Power Consumption = **4.2W**

Average Power at 1Tx @ 50% Duty Cycle, T_j = 135°C



Contact NXP to obtain this reference design

Notes and sources

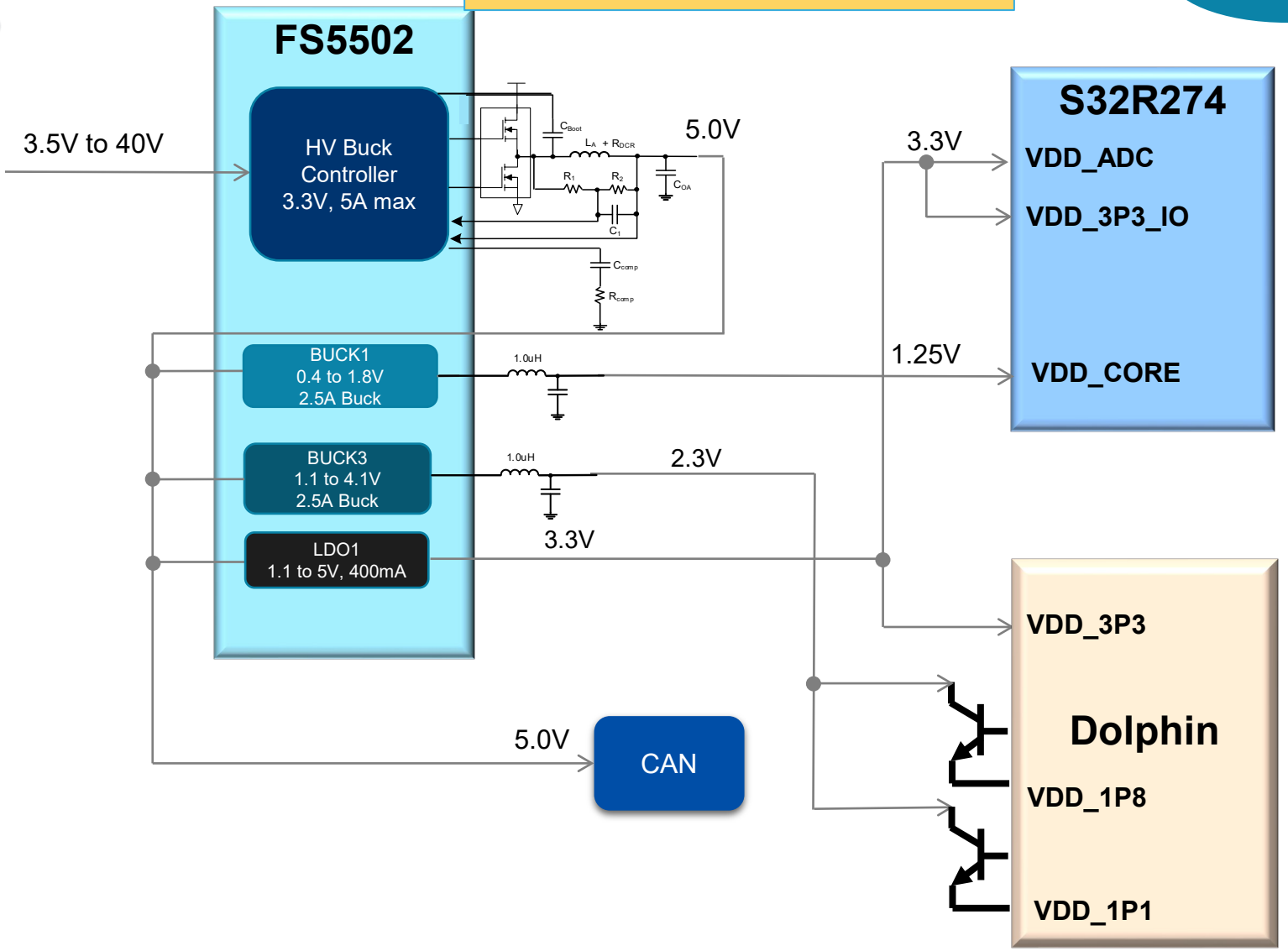
Automotive QM/ Industrial Radar with RRU (S32R274), Dolphin & FS5502

PN:PC33FS5502Y2ES

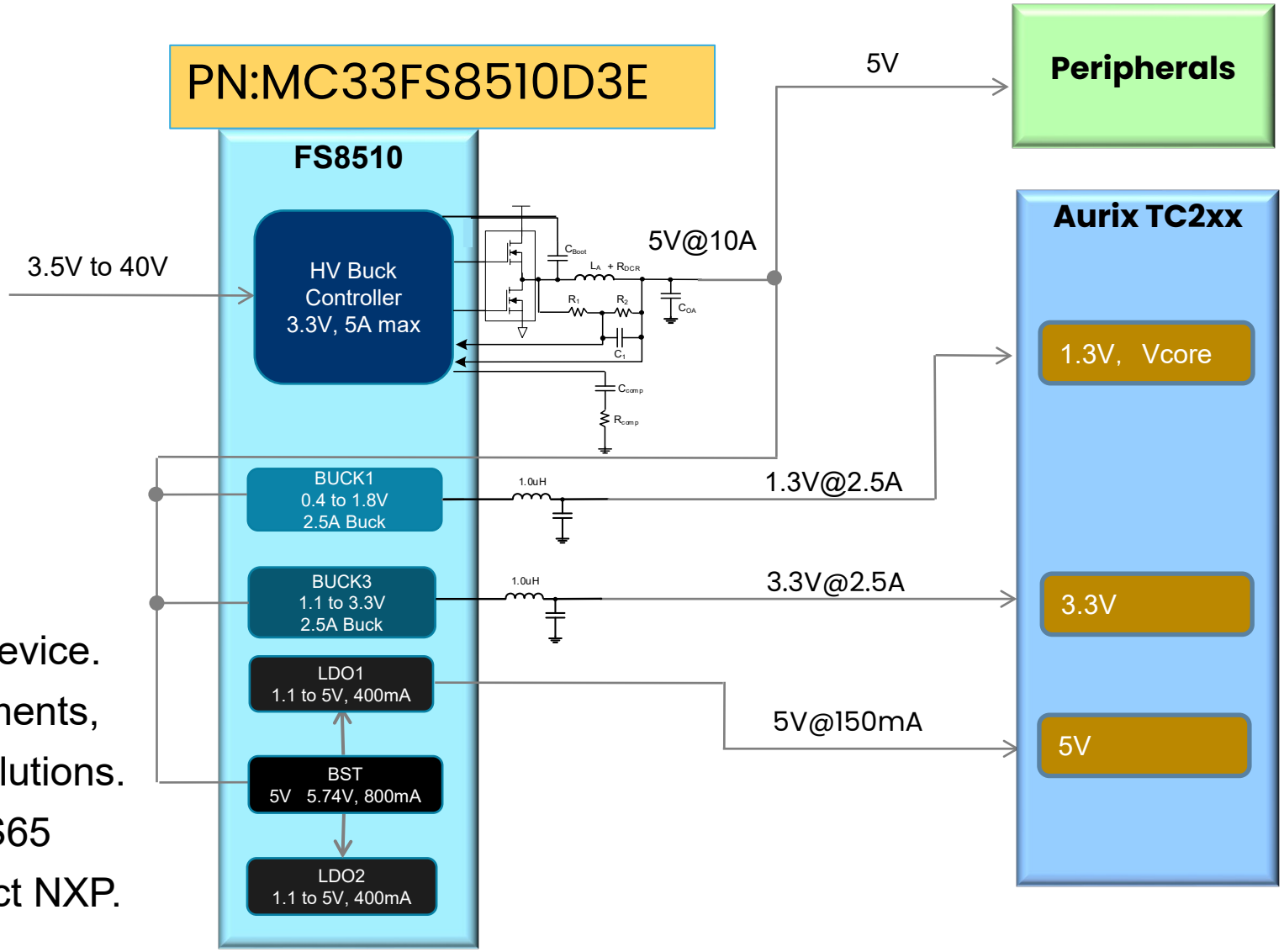
QM

Key Feature of OTP

- QM FS5502
- VPRE=5V
- No BOOST
- No LDO2



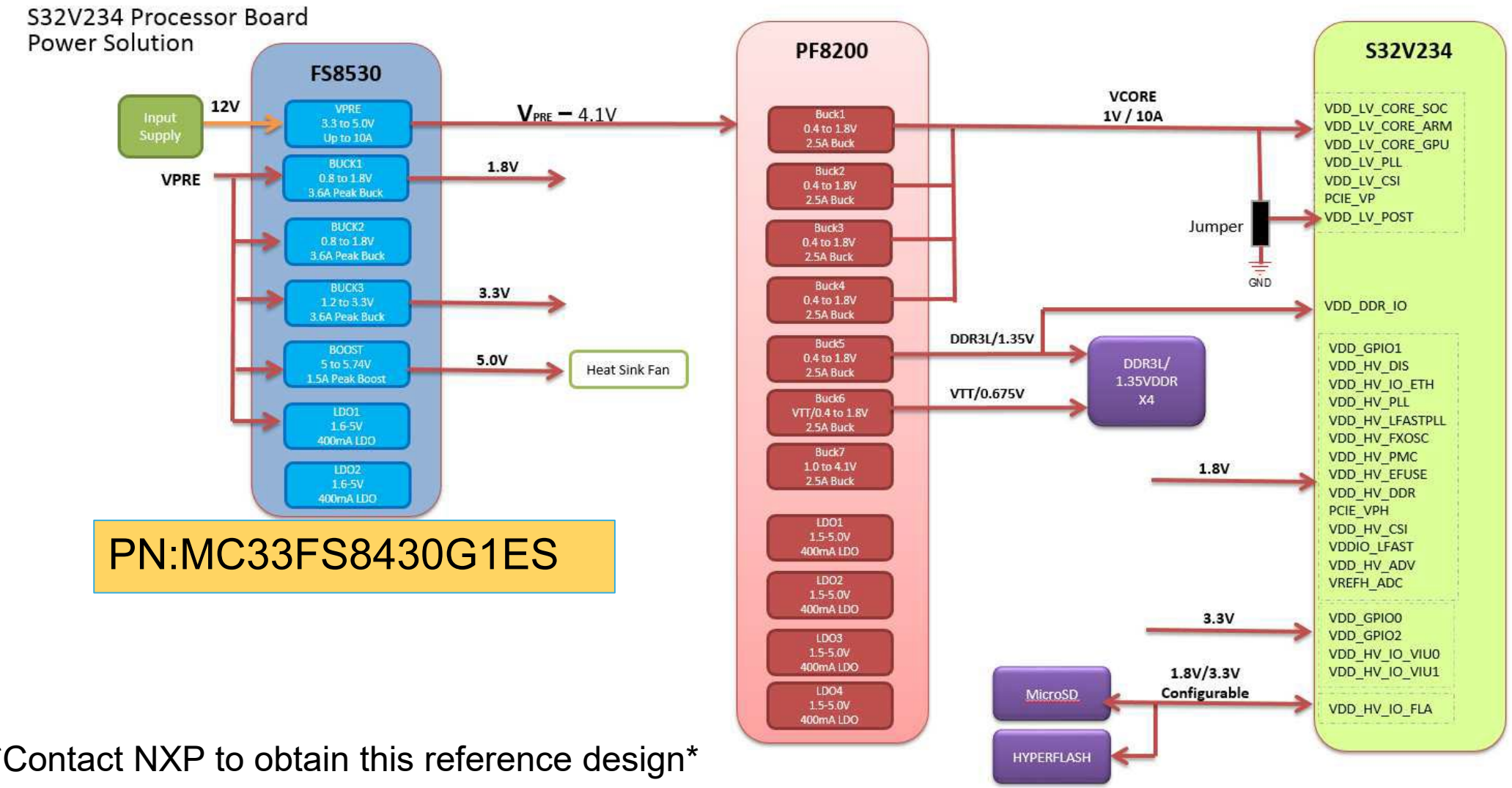
Aurix TC2xx



*FS85 is an OTP configurable device. For other power supply requirements, please contact NXP for other solutions.

*To obtain the TC2xx/TC3xx+FS65 series power tree, please contact NXP.

Camera Solutions – ASIL B based on FS84 + PF82 + S32V2x



PN:MC33FS8430G1ES

Contact NXP to obtain this reference design

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