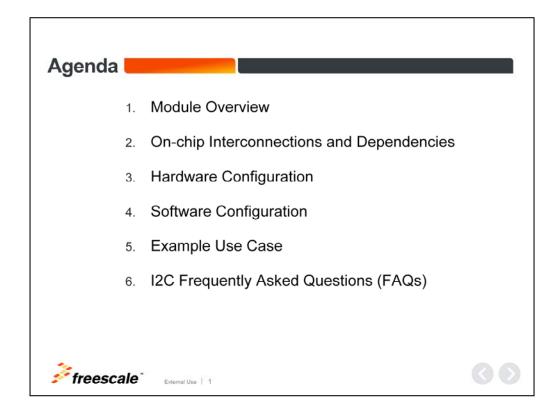




Hello and welcome to this presentation of the I2C, or inter-integrated circuit, module for Kinetis MCUs. In this session, you'll learn about the I2C's main features and the application benefits of leveraging this function.





In this presentation, we'll cover:

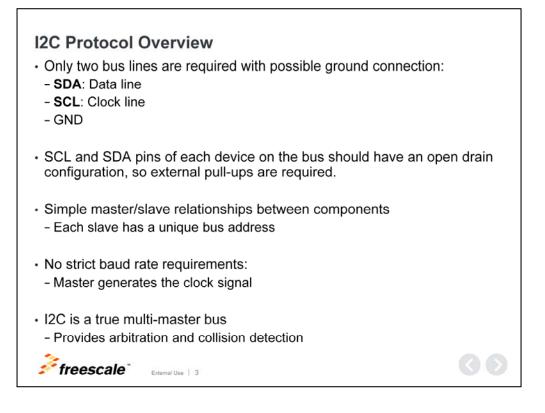
- An overview of the module
- The on-chip interconnections and inter-module dependencies
- Hardware and software configurations
- An example use case for reference
- And a few frequently asked questions





First, let's take a brief look at the I2C protocol and overall features of the Kinetis MCU I2C module.





I2C Protocol Overview

I2C is a widely used communication protocol to transfer data between devices.

It uses only 2 bus lines: SCL (or clock) and SDA (or data). Note that your system may also require a ground connection if a master and slave device do not reference the same ground connection.

Data transfer is made in a simple master-slave relationship between components with each slave possessing its own, unique bus address.

The protocol does not define a strict baud rate, but the standard transfer rates are up to 1 MHz. The master device determines the frequency.

It is possible to have multiple I2C devices in a multi-master or multi-slave bus configuration with arbitration loss and collision detection.



I2C Module Main Features

- · Compatible with the I2C bus specification
- Multimaster operation
- · Software programmable for one of 64 clock frequencies
- · Arbitration lost interrupt with automatic mode switch from master to slave
- · General call recognition
- 10-bit addressing
- · Support for SMBUS specification, version 2

External Use | 4

- Programmable input glitch filter
- · Range slave address support
- Supports clock stretching

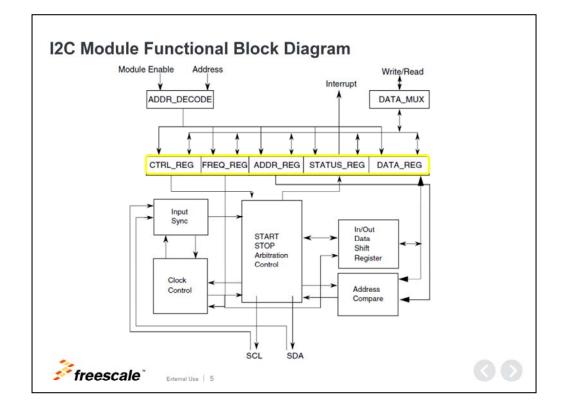
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I2C Module Main Features

The key features of the I2C module in Kinetis MCUs include:

- I2C bus specification support
- Support for 10-bit addressing scheme
- SMBUS version 2 specification support
- Programmable input filter to absorb and eliminate glitches on the bus
- and the ability to wake up the MCU with a slave address match

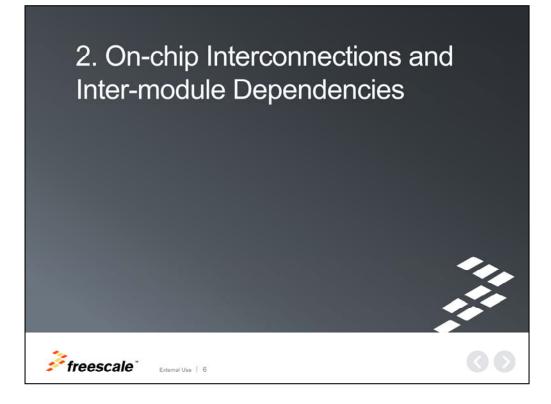




I2C Module Functional Block Diagram

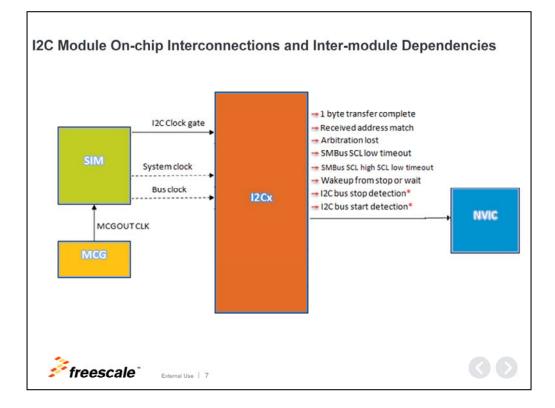
This is a general block diagram of the I2C module. The most relevant parts are the register blocks – outlined in yellow here. The registers provide status flags that serve as an interface to configure the module. The data register provides an interface for the application to send or receive data to or from the I2C bus.





Next, let's discuss on-chip interconnection and inter-module dependencies.





I2C Module On-chip Interconnections and Inter Module Dependencies

This diagram displays the I2C interconnections and it's relationship with other peripherals or systems.

On left, we see the path for the I2C module source clock. The clock is initially generated by the MCG module, passing then to the SIM module which delivers an equal or divided frequency. Note the doted lines for system and bus clocks; this means that the I2C clock source will depend on the specific Kinetis device and the specific I2C module instance. Please refer to your Kinetis MCU reference manual for help determining the exact clock source.

From the SIM module, it is very important to enable the I2C clock gate before accessing the I2C registers.

On the right, the possible interrupt triggers are displayed. The triggers marked with a red star are not present in all Kinetis devices. Refer to your device specific reference manual for details. All of the interrupts in an I2C module instance share a single interrupt vector mapped to the NVIC module. There are two required steps to enable interrupts:

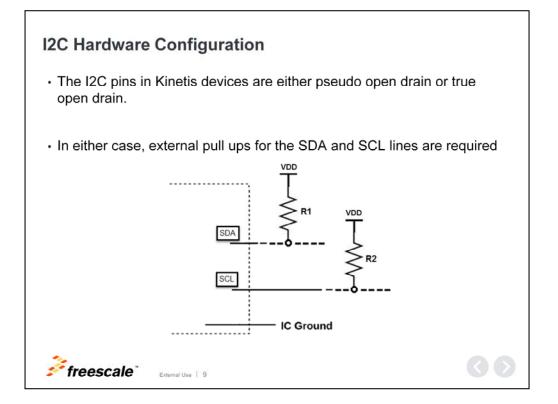
- 1. Enable the desired interrupt triggers in the I2C module, and
- 2. Enable the common interrupt vector in the NVIC module for the corresponding I2C module instance





Now let's examine a basic hardware setup.





I2C Hardware Configuration

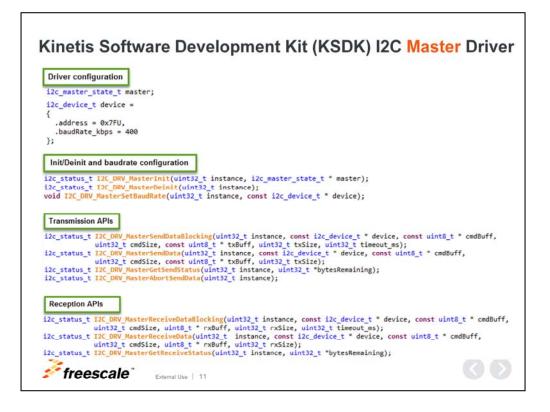
An important hardware component of the I2C bus are the pull-up resistors. There should be one pull-up resistor per I2C line. This is because the I2C specification requires I2C devices to have open drain output stages. Usually the lines of the bus are pulled up to the same voltage level of the MCUs' VDD. If the Kinetis device has true open drain pins, then it is permissible to pull the pins up to 5 volts.





In this section, we will examine the I2C driver provided by the Kinetis Software Development Kit (or KSDK).





Kinetis Software Development Kit (KSDK) I2C Master Driver

The I2C master driver functions require a structure variable of type "i2c_master_state". This should be a persistent structure, so it is recommended to make it global, static or defined in the main function.

A simple structure variable of type "i2c_device" is also needed. This variable should be initialized with the I2C slave address and the desired baud rate.

APIs initialize and de-initialize the driver, as well as set the baud rate.

The transmission APIs are for data transmission. There are blocking and nonblocking calls.

- Blocking calls do not exit the function until the I2C transfer is complete.
- Non-blocking functions simply start the I2C transfer and then exit the function.

Finally there are APIs for data reception, which also have blocking or non-blocking variants.



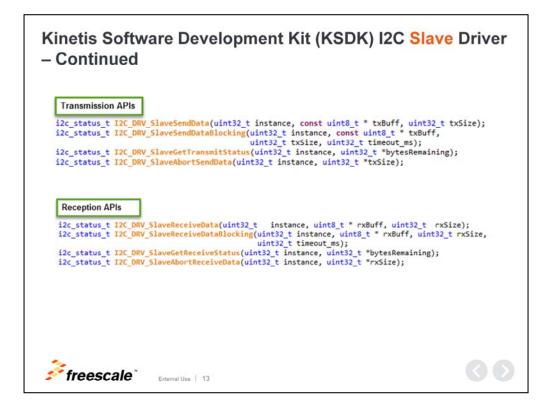


Kinetis Software Development Kit (KSDK) I2C Slave Driver

The slave driver requires a structure variable of type "i2c_slave_state" and a structure of type "i2c_slave_user_config". The "i2c_slave_user_config" variable holds the slave address, slave callback, callback parameter, slave listening mode, and start/stop detection depending on the device.

There are simple APIs for initialization, de-initialization and to retrieve a pointer to the slave's state structure.





Kinetis Software Development Kit (KSDK) I2C Slave Driver – Continued

These are the data transmission APIs.

and APIs for data reception.





Let's take a look at an I2C example available with Kinetis SDK.



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<pre>// Buffer store data to send to slave uint8_t txBuff[DATA_LENGTH] = {0}; // Buffer store data to receive from slave uint8_t rxBuff[DATA_LENGTH] = {0}; bool 12c_compare(uint8_t *txBuff, uint8_t *rxBuff, uint32_t count) { uint32_t i; for (i = 0; i < count ; i++) { if (txBuff[i] != rxBuff[i]) { return false; } return true; } int main(void) { uint32_t i = 0; uint32_t i = 0; uint32_t i = 0; uint32_t i = 0; i2c_mester_state_t master; uint32_t bytesRemaining; i2c_device_t device = { .address = 0x7F, .baudRate_kbps = 400 }; freescale</pre>		#define DATA_LENGTH 64	
<pre>// Buffer store data to receive from slave uint8_t rxBuff[DATA_LENGTH] = {0}; bool i2c_compare(uint8_t *txBuff, uint8_t *rxBuff, uint32_t count) { uint32_t i; for (i = 0; i < count ; i++) { if (txBuff[i] != rxBuff[i]) { return false; } return true; } int main(void) { { uint32_t i = 0; uint32_t i = 0; uint32_t i = 0; i2c_master_state_t master; uint32_t bytesRemaining; i2c_device_t device = { .address = 0x7F, .baudKate_kbps = 400 };</pre>			
<pre>uint8_t rxBuff[DATA_LENGTH] = {0}; bool i2c_compare(uint8_t *txBuff, uint8_t *rxBuff, uint32_t count) { uint32_t i; for (i = 0; i < count ; i++) { if (txBuff[i] != rxBuff[i]) { return false; } } return true; } int main(void) { uint32_t i = 0; izc_master_state_t master; uint32_t bytesRemaining; i2c_device_t device = { .address = 0x7F, .baudKate_kbps = 400 }; </pre>			
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<pre>uint32_t i; for (i = 0; i < count ; i++) { if (txBuff[i] != rxBuff[i]) { return false; } } return true; } int main(void) { uint32_t i = 0; i12c_master_state_t master; uint32_t i = 0; i2c_master_state_t master; uint32_t bytesRemaining; i2c_device_t device = { .address = 0x7F, .baudKate_kbps = 400 };</pre>		<pre>bool i2c_compare(uint8_t *txBuff, uint8_t *rxBuff, uint32_t count)</pre>	
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<pre>{ if (txBuff[i] != rxBuff[i]) { return false; } return true; } int main(void) { uint32_t count = 0; uint32_t i = 0; i2c_master_state_t master; uint32_t bytesRemaining; i2c_device_t device = { .address = 0x7F, .baudKate_kbps = 400 }; </pre>			
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<pre>i2c_master_state_t master; uint32_t bytesRemaining; i2c_device_t device = { .address = 0x7F, .baudRate_kbps = 400 };</pre>		<pre>uint32_t count = 0;</pre>	
<pre>uint32_t bytesRemaining; i2c_device_t device = { .address = 0x7F, .baudRate_kbps = 400 };</pre>			
<pre>i2c_device_t device = { .address = 0x7F, .baudRate_kbps = 400 };</pre>			
<pre>{ .address = 0x7F, .baudRate_kbps = 400 };</pre>		<pre>uint32_t bytesRemaining;</pre>	
<pre>{ .address = 0x7F, .baudRate_kbps = 400 };</pre>		i2c device t device =	
.baudRate_kbps = 400 };			
};		.address = 0x7F,	
freecale		};	
	fro	ascalo"	

Kinetis SDK I2C Example – Master Code

The next three slides are an example of basic master – slave communication. The code in this slide is the I2C master project.

The application consists of continuous iterations of the master sending 1 byte or more to the slave, along with a command byte indicating to the slave how many bytes to expect. Then the master waits for the slave to echo the bytes it received from the master. The communication continues with the master incrementing the number of bytes sent or received within each iteration.



hardware_init();	
OSA_Init();	
<pre>I2C_DRV_MasterInit(BOARD_I2C_COMM_INSTANCE, &master);</pre>	
// Initialize data to send	
<pre>for(i = 0; i < DATA_LENGTH; i++)</pre>	
{	
}	
count = 1;	
// Loop for transfer	
while(1)	
(
// Wait user press any key	
GETCHAR();	
// Master send 1 byte CMD and data to slave	
<pre>I2C_DRV_MasterSendData(BOARD_I2C_COMM_INSTANCE, &device, (const uint8_t*)&count</pre>	, 1, (const
<pre>uint8_t*)txBuff, count);</pre>	
// Wait until finish send	
<pre>while(I2C_DRV_MasterGetSendStatus(BOARD_I2C_COMM_INSTANCE, &bytesRemaining) !</pre>	<pre>= kStatus_I2C_Success){}</pre>
// Delay to wait slave received data	
OSA TimeDelay(25);	
// Clear rxBuff	
for(i = 0; i < count; i++)	
rxBuff[i] = 0;	
}	
External Use 16	

This is the continuation of the I2C master code.



	<pre>// Master receive count byte data from slave IZC_DRV_MasterReceiveData(BOARD_IZC_COMM_INSTANCE, &device, NULL, 0, rxBuff, count); // Wait until finish receive while(IZC_DRV_MasterGetReceiveStatus(BOARD_IZC_COMM_INSTANCE, &bytesRemaining) != kStatu /* Compare to check result */ if(izc_compare((uint8_t*)txBuff, rxBuff, count) != true) { break; } if(++count > DATA_LENGTH) { count = 1; } OSA_TimeDelay(2); 2C_DRV_MasterDeinit(BOARD_IZC_COMM_INSTANCE); eturn 0;</pre>	s_12C_Success){
i free	escale External Use 17	00

... and the final section of the master code.



Γ

#define DATA_LENGTH 64	
<pre>int main(void) { uint32_t i = 0; uint32_t i = 0; uint8_t dataBuff[DATA_LENGTH] = {0}; i2c_slave_state_t slave; i2c_slave_state_t slave; i2c_slave_user_config_t userConfig = { .address = 0x7F, .slaveCallback = NULL, .callbackParam = NULL, .slaveListening = false, #if FSL_FEATURE_I2C_HAS_START_STOP_DETECT .startStopDetect = false, #endif #if FSL_FEATURE_I2C_HAS_STOP_DETECT .stopDetect = false, #endif </pre>	
<pre>hardware_init(); OSA_Init();</pre>	
<pre>I2C_DRV_SlaveInit(BOARD_I2C_COMM_INSTANCE, &userConfig, &slave);</pre>	
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Kinetis SDK I2C Example – Slave Code

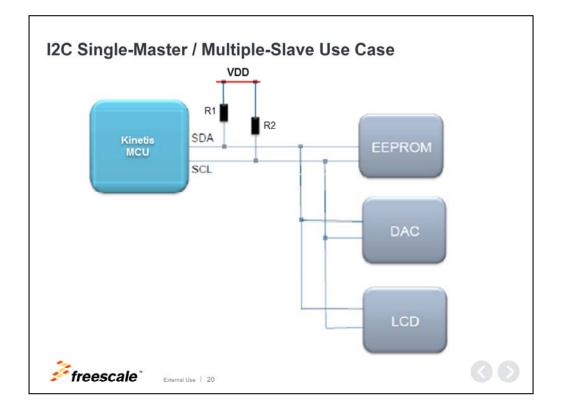
In the next two slides is the code for an I2C slave application. The first byte received by the slave indicates the incoming number of bytes. Then the slave receives the specified number of bytes in a buffer and sends them back to the master. The communication continues by the slave receiving and echoing as many bytes as indicated by the master.



// Loop transfer	
while(1)	
<pre>{ // Slave receive buffer from master I2C_DRV_SlaveReceiveData(BOARD_I2C_COMM_INSTANCE, (uint8_t*)&count, 1);</pre>	
<pre>/* Wait until transfer is succesful */ while(I2C_DRV_SlaveGetReceiveStatus(BOARD_I2C_COMM_INSTANCE, NULL) != kStatus_I2C_Success);</pre>	
<pre>// Clear receive buffer for(i = 0; i < count; i++)</pre>	
<pre>{ dataBuff[i] = 0; }</pre>	
<pre>// Slave receive buffer from master I2C_DRV_SlaveReceiveData(BOARD_I2C_COMM_INSTANCE, dataBuff, count);</pre>	
<pre>/* Wait until transfer is successful */ while(I2C_DRV_SlaveGetReceiveStatus(BOARD_I2C_COMM_INSTANCE, NULL) != kStatus_I2C_Success);</pre>	
<pre>// Slave send buffer received from master I2C_DRV_SlaveSendData(BOARD_I2C_COMM_INSTANCE, dataBuff, count);</pre>	
<pre>/* Wait until transfer is succesful */ while(I2C_DRV_SlaveGetTransmitStatus(BOARD_I2C_COMM_INSTANCE, NULL) != kStatus_I2C_Success);</pre>	
OSA_TimeDelay(1);	
}	
Freescale External Use 19	

And here is the remaining piece of the slave code.





I2C Single-Master / Multiple-Slave Use Case

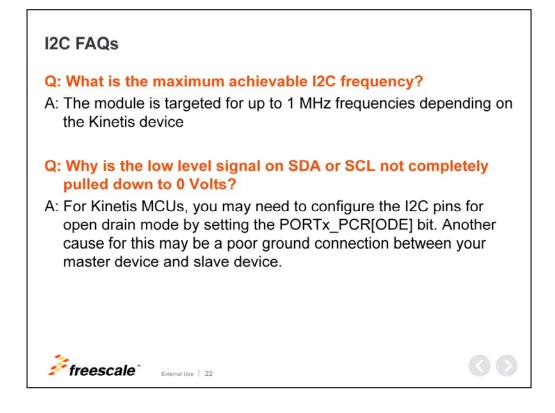
This diagram represents one use case with one I2C master and three I2C slave devices. In this case, the three slaves are an EEPROM memory device, a DAC, and a LCD device. Please note the use of pull-up resistors.





Now, let's review a few FAQs that arise when using the I2C module.





I2C FAQs

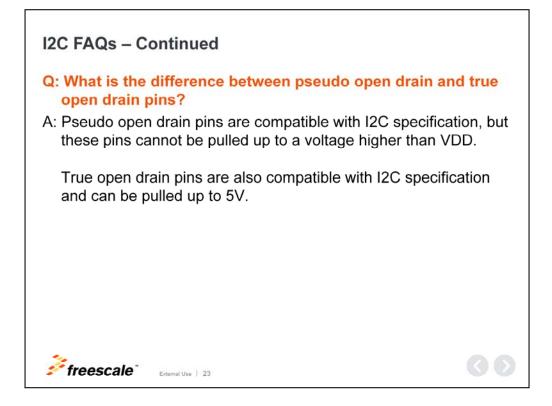
Question: What is the maximum bus frequency of the I2C module?

Answer: The module is targeted for up to 1 MHz frequencies depending on the Kinetis device.

Question: Why is the low level signal on SDA or SCL not completely pulled down to 0 Volts?

Answer: For Kinetis MCUs, you may need to configure the I2C pins for open drain mode by setting the PORTx_PCR [ODE] bit. Another cause for this may be a poor ground connection between your master device and slave device.





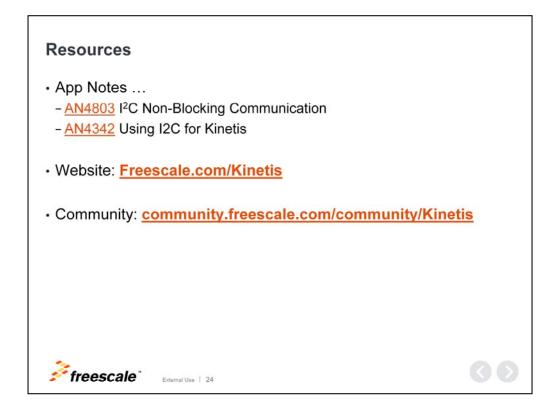
I2C FAQs – Continued

Question: What is the difference between pseudo open drain and true open drain pins?

Answer: Pseudo open drain pins are compatible with I2C specification, but these pins cannot be pulled up to a voltage higher than VDD.

True open drain pins are also compatible with I2C specification and can be pulled up to 5V.





Resources

This concludes our presentation on the I2C module for Kinetis MCUs.

For additional references, please visit the application notes listed here.

We also invite you to visit us on the web at Freescale.com/Kinetis and check out our community page.



