EXCEPTION
PROCESSING
EXCEPTION PROCESSING OVERVIEW

FEATURES:

• SIMPLIFIED EXCEPTION VECTOR TABLE

• REDUCED RELOCATION CAPABILITY OF VECTOR BASE REGISTER (VBR)

• SINGLE EXCEPTION STACK FRAME FOR ALL EXCEPTION TYPES

• SELF-ALIGNED STACK POINTER

• SUPPORT FOR AUTOVECTORED INTERRUPTS

• RESTRICTIVE DEFINITION OF FAULT ON FAULT

• RESTART EXCEPTION MODEL
# SOFTWARE CONTROL DEFINITION

<table>
<thead>
<tr>
<th>Term</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>USER MODE</td>
<td>THE PRIVILEGE LEVEL THAT APPLICATIONS RUN IN.</td>
</tr>
<tr>
<td>SUPERVISOR MODE</td>
<td>THE PRIVILEGE LEVEL THAT OPERATING SYSTEMS RUN IN. ALSO REFERRED TO AS PRIVILEGED MODE.</td>
</tr>
<tr>
<td>NORMAL PROCESSING</td>
<td>NORMAL INSTRUCTION EXECUTION, USER OR SUPERVISOR</td>
</tr>
<tr>
<td>EXCEPTION PROCESSING</td>
<td>WHEN AN EXCEPTION OCCURS, THE PROCESSOR AUTOMATICALLY SAVES THE CURRENT MACHINE CONTEXT BEFORE HANDLING THE EXCEPTION CONDITION.</td>
</tr>
<tr>
<td>EXCEPTION HANDLING</td>
<td>PROCESSOR IS EXECUTING THE NECESSARY INSTRUCTIONS TO HANDLE THE EXCEPTION CONDITION</td>
</tr>
<tr>
<td>STOPPED STATE</td>
<td>CORE EXECUTED STOP INSTRUCTION AND WAITING FOR INTERRUPT TO EXIT</td>
</tr>
<tr>
<td>HALTED STATE</td>
<td>CPU EITHER EXECUTED A HALT INSTRUCTION OR ENCOUNTERED FAULT ON FAULT CONDITION</td>
</tr>
</tbody>
</table>
EXCEPTION PROCESSING

APPLICATIONS

NORMAL

RTE

S = 1

OPERATING SYSTEM

(Exception Handlers)

USER PRIVILEGE LEVEL

SUPERVISOR PRIVILEGE LEVEL

ERRORS, TRAPS, INTERRUPTS

EXCEPTION

CONTEXT SWITCHING

ERRORS, TRAPS, INTERRUPTS

S = 1
# EXTERNAL EXCEPTIONS

<table>
<thead>
<tr>
<th>Reset</th>
<th>Hard Reset</th>
<th>Non-Maskable</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interrupts</td>
<td>External Interrupt Pin</td>
<td>Maskable &amp; Non-Maskable</td>
</tr>
</tbody>
</table>

**Asynchronous input signals**
# INTERNAL EXCEPTIONS

<table>
<thead>
<tr>
<th>TYPE</th>
<th>CAUSE OF EXCEPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADDRESS ERROR</td>
<td>INDEX SIZE AND SCALE FACTOR NOT SUPPORTED</td>
</tr>
<tr>
<td>ILLEGAL INSTRUCTION</td>
<td>ATTEMPT TO EXECUTE $0000 OR $4AFC Opcode</td>
</tr>
<tr>
<td>PRIVILEGE VIOLATION</td>
<td>ATTEMPT TO EXECUTE PRIVILEGED INSTRUCTION OR ACCESS SUPERVISOR RESOURCES</td>
</tr>
<tr>
<td>TRACE</td>
<td>SR T-BIT SET DURING INSTRUCTION EXECUTION</td>
</tr>
<tr>
<td>DIVIDE BY ZERO</td>
<td>DIVISOR = 0</td>
</tr>
<tr>
<td>FORMAT ERROR</td>
<td>STACK FRAME IS CORRUPTED</td>
</tr>
<tr>
<td>HARDWARE BKPT</td>
<td>HARDWARE BKPT TRIGGER (NON-MASKABLE)</td>
</tr>
<tr>
<td>TRAP INSTRUCTION</td>
<td>TRAP 0-15 INSTRUCTIONS</td>
</tr>
<tr>
<td>INTERNAL MODULES IRQ'S</td>
<td>OCCURANCE OF AN EVENT (MASKABLE)</td>
</tr>
</tbody>
</table>
THE VECTOR TABLE IS LOCATED WHEREVER THE VECTOR BASE REGISTER IS POINTING. ON RESET VBR = $000000.

AT INITIALIZATION, O.S. MAY RELOCATE VECTOR TABLE TO RAM. VCT MUST BE LOCATED ON 1M-BYTE BOUNDARY.

VECTOR ADDRESS CALCULATION:

VECTOR ADDRESS = VBR + VECTOR # * 4
The processor detects exception conditions in application programs or by external inputs and transfers control to the appropriate exception service routine via the exception vector table.
RESET EXCEPTION PROCESSING

RESET
IF BKPT Asserted
BDM
PST = $F

VEC_OFFSET
VECTOR TABLE

VEC #
$00
$01
$02
$03

SP
PC

BEGIN INSTRUCTION EXECUTION
NO

ACCESS ERROR

YES

ILLEGAL ADDRESS OR ACCESS ERROR

YES

HALT

FETCH VECTOR NO. 00

ACCESS ERROR

NO

VECTOR 00

NO

VECTOR 01

PC

ILEGAL ADDRESS OR ACCESS ERROR

NO

BEGIN INSTRUCTION EXECUTION

VECTOR TABLE

VEC_OFFSET

000000
000004
000008
00000C

- 

BEGIN INSTRUCTION EXECUTION

COVERED IN DEVELOPMENT MODULE

5307 Exception Processing
Motorola ColdFire®
**Exception Processing Flow**

1. **EXCEPTION** → **SAVE INTERNAL COPY OF SR**
2. **1 → S, 0 → T:** IF IRQ EXCEPTION MASK = IRQ_LVL 0 → M
3. **OBTAIN VECTOR NUMBER**
4. **ACCESS ERROR**
   - **AVEC** NQ VECTOR
   - **SPURIOUS VECTOR $24**
5. **AUTOVEC $25-$31**
6. **COPIED SR AD PC → STACK**
7. **PST = $F**
   - **HALTED STATE**
8. **READ VECTOR CONTENTS INTO PC**
9. **FETCH FIRST INSTRUCTION OF HANDLER**
10. **BEGIN 1ST INSTRUCTION EXECUTION**
11. **END**
## EXCEPTION STACK FRAME

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
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<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### EXCEPTION STACK FRAME

<table>
<thead>
<tr>
<th>BITS[1:0] OF A7 @ TIME OF EXCEPTION</th>
<th>A7 @ 1st INSTRUCTION OF HANDLER</th>
<th>FORMAT FIELD</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0</td>
<td>ORIGINAL A7 - 8</td>
<td>0 1 0 0</td>
</tr>
<tr>
<td>0 1</td>
<td>ORIGINAL A7 - 9</td>
<td>0 1 0 1</td>
</tr>
<tr>
<td>1 0</td>
<td>ORIGINAL A7 - 10</td>
<td>0 1 1 0</td>
</tr>
<tr>
<td>1 1</td>
<td>ORIGINAL A7 - 11</td>
<td>0 1 1 1</td>
</tr>
</tbody>
</table>

### STACK FRAME FORMAT ENCODINGS
## EXCEPTION STACK FRAME (CONT’d)

**FAULT STATUS ENCODINGS**

<table>
<thead>
<tr>
<th>FS [3:0]</th>
<th>DEFINITION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 x x</td>
<td>RESERVED</td>
</tr>
<tr>
<td>0 1 0 0</td>
<td>PHYSICAL BUS ERROR ON INSTRUCTION FETCH</td>
</tr>
<tr>
<td>0 1 0 1</td>
<td>RESERVED</td>
</tr>
<tr>
<td>0 1 1 x</td>
<td>RESERVED</td>
</tr>
<tr>
<td>1 0 0 0</td>
<td>PHYSICAL BUS ERROR ON OPERAND WRITE</td>
</tr>
<tr>
<td>1 0 0 1</td>
<td>ATTEMPTED WRITE TO WRITE PROTECTED SPACE</td>
</tr>
<tr>
<td>1 0 1 x</td>
<td>RESERVED</td>
</tr>
<tr>
<td>1 1 0 0</td>
<td>PHYSICAL BUS ERROR ON OPERAND READ</td>
</tr>
<tr>
<td>1 1 0 1</td>
<td>RESERVED</td>
</tr>
<tr>
<td>1 1 1 x</td>
<td>RESERVED</td>
</tr>
</tbody>
</table>
ACCESS ERROR

ACCESS ERROR EXAMPLES:

- CORE ADDRESS REFERENCES NON-RESIDENT MEMORY OR I/O DEVICE (ADDRESS DOES NOT COMPARE WITH ANY OF THE CHIP SELECTS).
- AN ATTEMPT TO WRITE TO WRITE-PROTECTED MEMORY SPACE.
- ACCESS TO SUPERVISOR MEMORY FROM USER MODE.

NOTE: AN ACCESS ERROR EXCEPTION ON INSTRUCTION FETCH IS DELAYED UNTIL THE INSTRUCTION IS ATTEMPTED.
ILLEGAL ADDRESS ERROR

ADDRESS ERROR EXAMPLES:

*MOVE.L X D3,$3001 LONGWORD ACCESS TO ODD ADDRESS

*MOVE.W X D0,($04,A1) A1 CONTAINS ODD ADDRESS

*MOVE.W X ($50,A5),D2 A5 CONTAINS ODD ADDRESS

*MOVE.L X ($18,A3,D7.L), D0 D7 CONTAINS ODD NUMBER

MOVE.B ($10,A2,D2.W),D2 INDEX SIZE IS A WORD

MOVE.B ($2,A5,D7*8),D5 ONLY SCALE FACTOR 2 AND 4 ALLOWED

* CURRENT IMPLEMENTATIONS ALLOW FOR THESE ACCESSES DUE TO PRESENCE OF MISALIGNMENT MODULE.
ILLEGAL INSTRUCTION EXAMPLE:

- AN ATTEMPT TO EXECUTE $0000 AND $4AFC OPCODE

- THESE OPCODES MAY BE USED AS SOFTWARE BREAKPOINTS

- COLDFIRE CPU WILL GENERATE AN ILLEGAL INSTRUCTION ON ALL UNDEFINED INSTRUCTIONS
### PRIVILEGE VIOLATION

- An attempt to execute a Supervisor mode instruction in the User mode will cause a Privilege Violation Exception.

### PRIVILEGE INSTRUCTIONS:

<table>
<thead>
<tr>
<th>OPCODE</th>
<th>OPERAND SIZE</th>
<th>ADDRESSING MODE</th>
</tr>
</thead>
<tbody>
<tr>
<td>*HALT</td>
<td>UNSIZED</td>
<td>CONFIGURABLE</td>
</tr>
<tr>
<td>MOVE SR</td>
<td>W</td>
<td>Dn</td>
</tr>
<tr>
<td>MOVEC</td>
<td>L</td>
<td>Rn,Rc</td>
</tr>
<tr>
<td>RTE</td>
<td>UNSIZED</td>
<td>-</td>
</tr>
<tr>
<td>STOP</td>
<td>UNSIZED</td>
<td>-</td>
</tr>
<tr>
<td>WDEBUG</td>
<td>L</td>
<td>&lt;EA&gt;</td>
</tr>
<tr>
<td>*PULSE</td>
<td>UNSIZED</td>
<td>-</td>
</tr>
</tbody>
</table>

*Privileged by default*
TRACE EXCEPTION

1 - IF T = 1, TRAP AFTER INSTRUCTION COMPLETES EXECUTION.
2 - EXECUTE TRACE EXCEPTION SERVICE ROUTINE.
3 - RETURN FROM EXCEPTION TO MAIN(RTE).
**INTERRUPTS**

**TWO LEVEL PRIORITY**

1\(^{ST}\) **IRQ 7, 5, 3, & 1. LEVEL 1 IS LOWEST AND LEVEL 7 IS HIGHEST LEVEL 7 IS NON-MASKABLE.**

2\(^{ND}\) **IRQ'S AT SAME HARDWARE LEVEL ARE PROGRAMMABLE TO 1 OF 4 PRIORITIES**
HARDWARE INTERRUPT SEQUENCE

INTERRUPTING DEVICES ASSERTS IRQ SIGNAL

INT.LEVELS > MASK OR NMI?

CONTINUE IN CURRENT PROGRAM

YES

PROCESSOR FINISHES CURRENT INSTRUCTION

NORMAL PROCESSING

EXCEPTION PROCESSING

PROCESSOR Responds WITH IACK AND INTERRUPT LEVEL

AVEC

AUTO VECTOR

SPURIOUS VECTOR

CONTINUATION OF EXCEPTION PROCESSING

TA

USER VECTOR
NOTE: Bus Time Out circuitry and Interrupt Acknowledge circuitry can be derived using on chip resources. (i.e. Bus Monitor and Chip Selects)