

### 1 General description

The PF0300 integrates multiple high performance buck regulators and LDO regulator. It can operate as a stand-alone point-of-load regulator IC, or as a companion chip to a larger PMIC.

Built-in one-time programmable (OTP) memory stores key startup configurations, drastically reducing external components typically used to set output voltage and sequence of regulators. Regulator parameters are adjustable through high-speed I2C after startup, offering flexibility for different system states.

This PF0300 target AEC-Q100 Automotive grade

Note: Electrical characteristics for the PF0300 are maintained in the datasheet.

### 2 Features and benefits

- Three high efficiency buck regulators
- One LDO regulators
- BUCKs and LDO Voltage monitoring
- Current limit protection
- Watchdog monitoring
- External clock synchronization and Frequency spread spectrum
- Standby mode – controlled by dual function Sync/Standby pin
- Reset input monitoring – by dual function INTB\_RSTB pin
- One-time programmable device configuration
- 3.4 MHz I2C communication interface
- 28-pin flip chip QFN package with wettable flank

### 3 Applications

- Infotainment, Domain controllers
- High-end consumer and industrial



## 4 Ordering information

Table 1. Ordering information

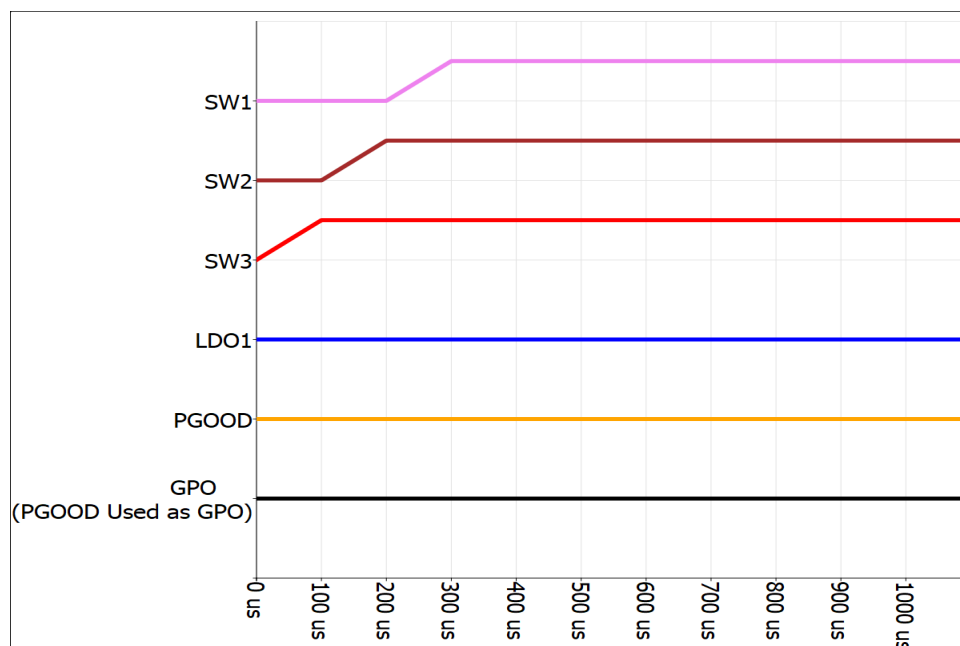
Type number <sup>[1]</sup>	Package		
	Name	Description	Version
MPF0300AMMA5ES <sup>[2][3]</sup>	HWQFN28	HWQFN28, plastic thermal enhanced very thin quad flat pack; no leads, wettable flank, 28 terminals, 0.5 mm pitch, 4.5 mm x 4.5 mm x 0.53 mm body	SOT2089-1(SC)

[1] To order parts in tape and reel, add the R2 suffix to the part number

[2] QM, non-programmed device, Programmed device is PPF0300AMMxxES (xx is capital and numeric number assigned to OTP)

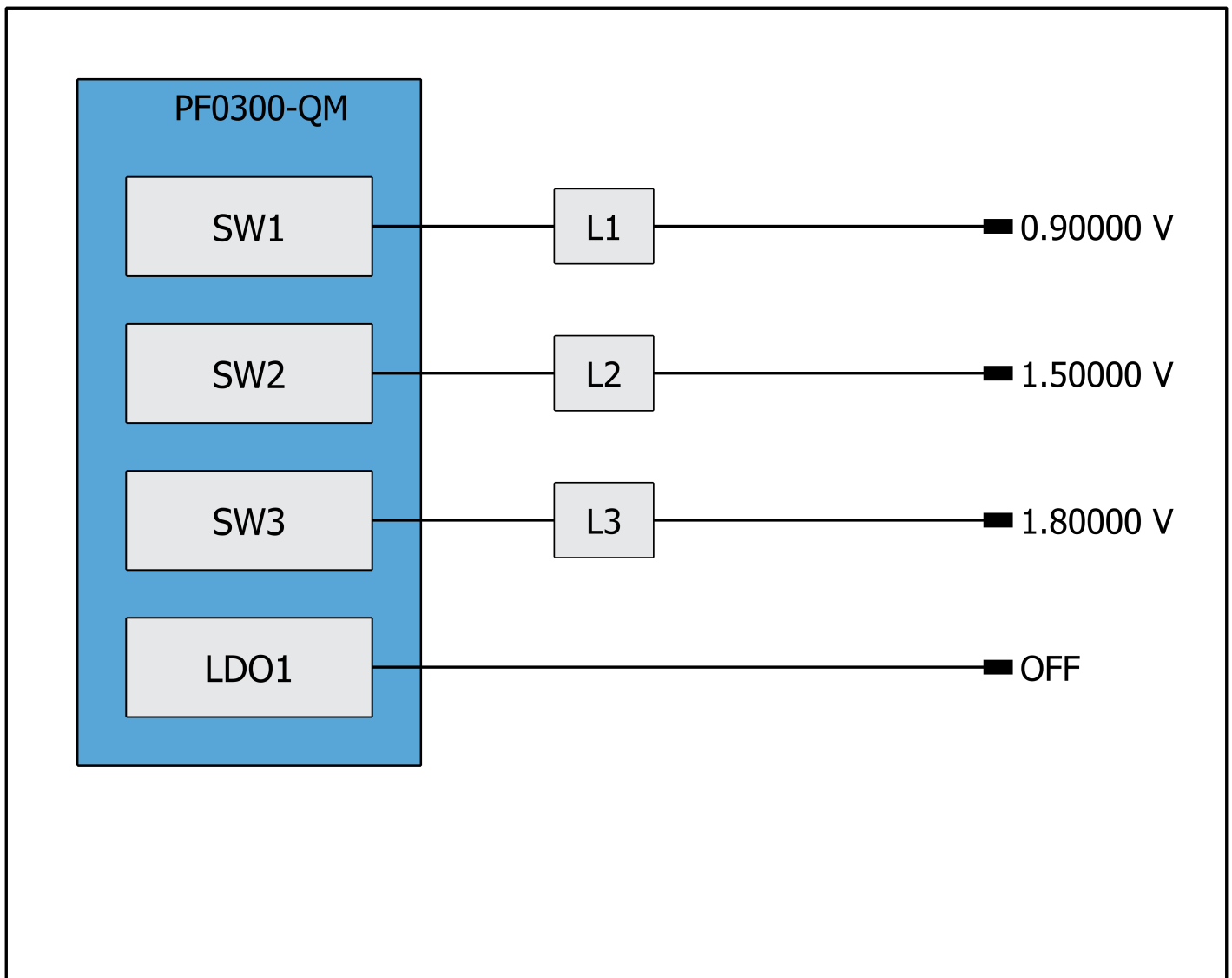
[3] Engineering sample part number

## 5 Power-up sequence summary



The signals depicted above are enable signals for each regulator. They don't represent the actual ramp voltage.

## 6 Hardware configuration diagram



## 7 OTP configuration

See PF0300 datasheet for parametric details. The OTP configuration summary for A5 sequence ID is provided in Tables below.

**Table 2. Device OTP configuration**

Functional block	Feature	OTP selection
System Configuration	I2C Address	0x0A
	I2C CRC	Disabled
	VIN_OVLO Enable	Disabled
	VIN_OVLO Mode	Interruption only on VIN_OVLO
	VIN_OVLO Debounce	10 us
	VIN_OV Threshold	103.25 %
	VIN_UV Threshold	96.75 %
	Maximum Fault Counter	15
	Standby Mode Enable	Standby function Disabled
	Low Power STANDBY	Disabled
I/O Configuration	XFAIL Operation	Disabled
	Standby Polarity	STANDBY Active High
	INTB Dual Function	INTB function enabled
Watchdog Monitoring	WD Timer	WD Disabled
	WD Window Duration	1 ms
	WD Clear Window	Cleared within 100 % timer
	Watchdog Error Maximum Value	8
	WD Standby Mode	Disabled

## Configuration report for PF0300-QM OTP program ID: A5 rev A

Clock Management	Nominal Switching Frequency	18 MHz
	SYNC Mode	SYNC function Enabled
	SW Mode	PWM
	Frequency Spread Spectrum Mode	Disabled
	Spread Spectrum Type	Pseudo-random modulation
	FSYNC Frequency Range	Between 2.2 MHz and 2.8 MHz
	FSS Mode	23.5 kHz
	Clock DIV1	Divider 5 and frequency = 3.60 MHz
	Clock DIV2	Divider 8 and frequency = 2.25 MHz

Table 3. Power Sequencer configuration

Functional block	Feature	OTP selection
Power Up Sequence	Sequence Time Base	100 us
	SW1 Sequence Slot	Slot 2
	SW2 Sequence Slot	Slot 1
	SW3 Sequence Slot	Slot 0
	LDO1 Sequence Slot	OFF
	PGOOD Power Up Sequence	OFF
	GPO Sequence Slot	OFF
Power-Down Sequence	Phase Sequence Delay	No delay

Table 4. SW Regulator configuration

Functional block	Feature	OTP selection
SW1	Output Voltage	0.90000 V

## Configuration report for PF0300-QM OTP program ID: A5 rev A

	UV Detection Threshold	95 %
	OV Detection Threshold	105 %
	ILIM Detection Threshold	6.0 A
	Output Inductor	0.47 uH
	Switching Phase	No phase shift
	SW1 Standby	Disabled
	PGOOD Mode	Enabled
	SW1 Clock	CLK_DIV2
	SW1 OV Bypass	OV Protection Enabled
	SW1 UV Bypass	UV Protection Enabled
	SW1 ILIM Bypass	ILIM Fault bypassed
	SW1 DVS Ramp	1.95 mV/us at fsw = 2.5 MHz
	SW1 Gain Margin	70 uS
	SW1 Compensation Resistor	80 kOhm
	SW1 Compensation Capacitor	100 pF
SW2	Output Voltage	1.50000 V
	UV Detection Threshold	95 %
	OV Detection Threshold	105 %
	ILIM Detection Threshold	5.0 A
	Output Inductor	0.47 uH
	Switching Phase	No phase shift
	SW2 Standby	Disabled
	PGOOD Mode	Enabled

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## Configuration report for PF0300-QM OTP program ID: A5 rev A

	SW2 Clock	CLK_DIV2
	SW2 OV Bypass	OV Protection Enabled
	SW2 UV Bypass	UV Protection Enabled
	SW2 ILIM Bypass	ILIM Fault bypassed
	SW2 DVS Ramp	1.95 mV/us at fsw = 2.5 MHz
	SW2 Gain Margin	53 uS
	SW2 Compensation Resistor	80 kOhm
	SW2 Compensation Capacitor	100 pF
SW3	Output Voltage	1.80000 V
	UV Detection Threshold	95 %
	OV Detection Threshold	105 %
	ILIM Detection Threshold	5.0 A
	Output Inductor	0.47 uH
	Switching Phase	No phase shift
	SW3 Standby	Disabled
	PGOOD Mode	Enabled
	SW3 Clock	CLK_DIV2
	SW3 OV Bypass	OV Protection Enabled
	SW3 UV Bypass	UV Protection Enabled
	SW3 ILIM Bypass	ILIM Fault bypassed
	SW3 DVS Ramp	1.95 mV/us at fsw = 2.5 MHz
	SW3 Gain Margin	53 uS

## Configuration report for PF0300-QM OTP program ID: A5 rev A

	SW3 Compensation Resistor	80 kOhm
	SW3 Compensation Capacitor	100 pF
Multi Phase selection	SW1 Multi-phase Selector	SW1,SW2 and SW3 operate in single phase mode

Table 5. LDO Regulator configuration

Functional block	Feature	OTP selection
LDO1	Output Voltage	1.8 V
	UV Detection Threshold	95 %
	OV Detection Threshold	105 %
	LDO1 STANDBY	Disabled
	PGOOD Mode	Enabled
	LDO1 DVS Ramp	390 us
	LDO1 Regulator Mode	Normal Mode
	LDO1 OV Bypass	OV Protection Enabled
	LDO1 UV Bypass	UV Protection Enabled
	LDO1 ILIM Bypass	ILIM Fault bypassed
	LDOx Out Open	Disabled

Table 6. Program ID

Functional block	Feature	OTP selection
Program ID	Program ID High	A
	Program ID Low	5
	Program ID Rev	A



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