

1 General description

The "PF09 Family" is a power management integrated circuit (PMIC) optimized for high performance i.MX9x based applications. It Integrates multiple high efficiency switch mode and linear voltage regulators to support base system power from a pre-regulated system rail (3.3V or 5.0V). It provides low quiescent current in Standby and low power off modes.

Built-in multiple time programmable configuration stores key startup configurations drastically reducing external components typically used to set output voltage and sequence of external regulators. Regulator parameters are adjustable through high-speed I2C communication after start up offering flexibility for different system states.

The "PF09 Family" is developed in compliance with ISO 26262 standard, including safety features, with Failsafe outputs and integrated self-test mechanisms, becoming part of a safety oriented system partitioning targeting high integrity safety level up to ASIL D and complies with the IEC 61508 industrial safety specification targeting high safety integrity level up to SIL 2.

2 Applications

- Automotive Infotainment
- High-end consumer and industrial
- Connectivity domain controller
- Telematics

3 Ordering information

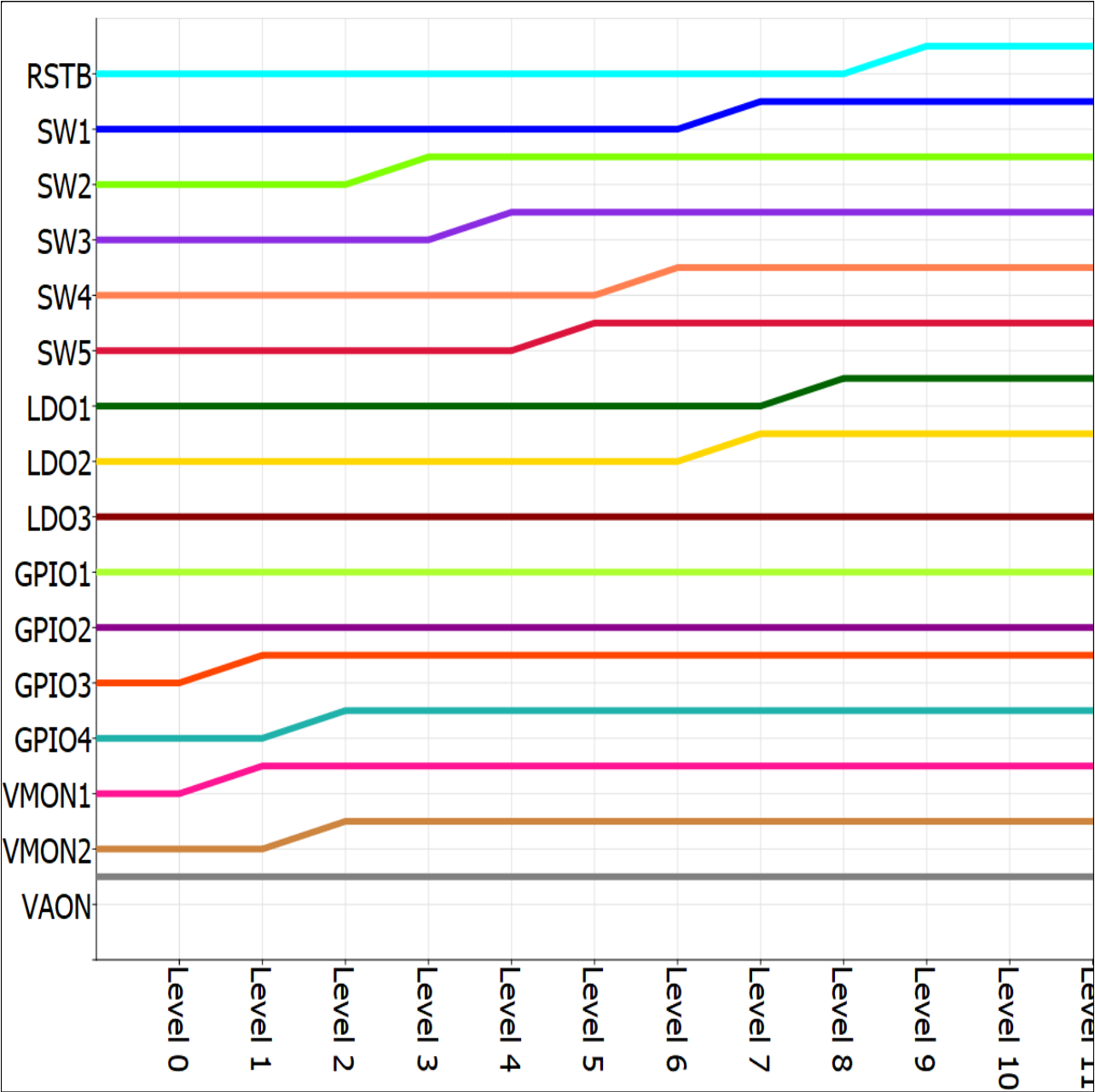
Table 1. Ordering information

Type number ^[1]	Package		
	Name	Description	Version
MPF0900AVSA1ES ^[2]	HVQFN56	HVQFN56, plastic thermal enhanced very thin quad flat pack; no leads, wettable flank, 56 terminals, 0.5 mm pitch, 8 mm x 8 mm x 0.53 mm body	SOT684-32(DD)

[1] To order parts in tape and reel, add the R2 suffix to the part number.

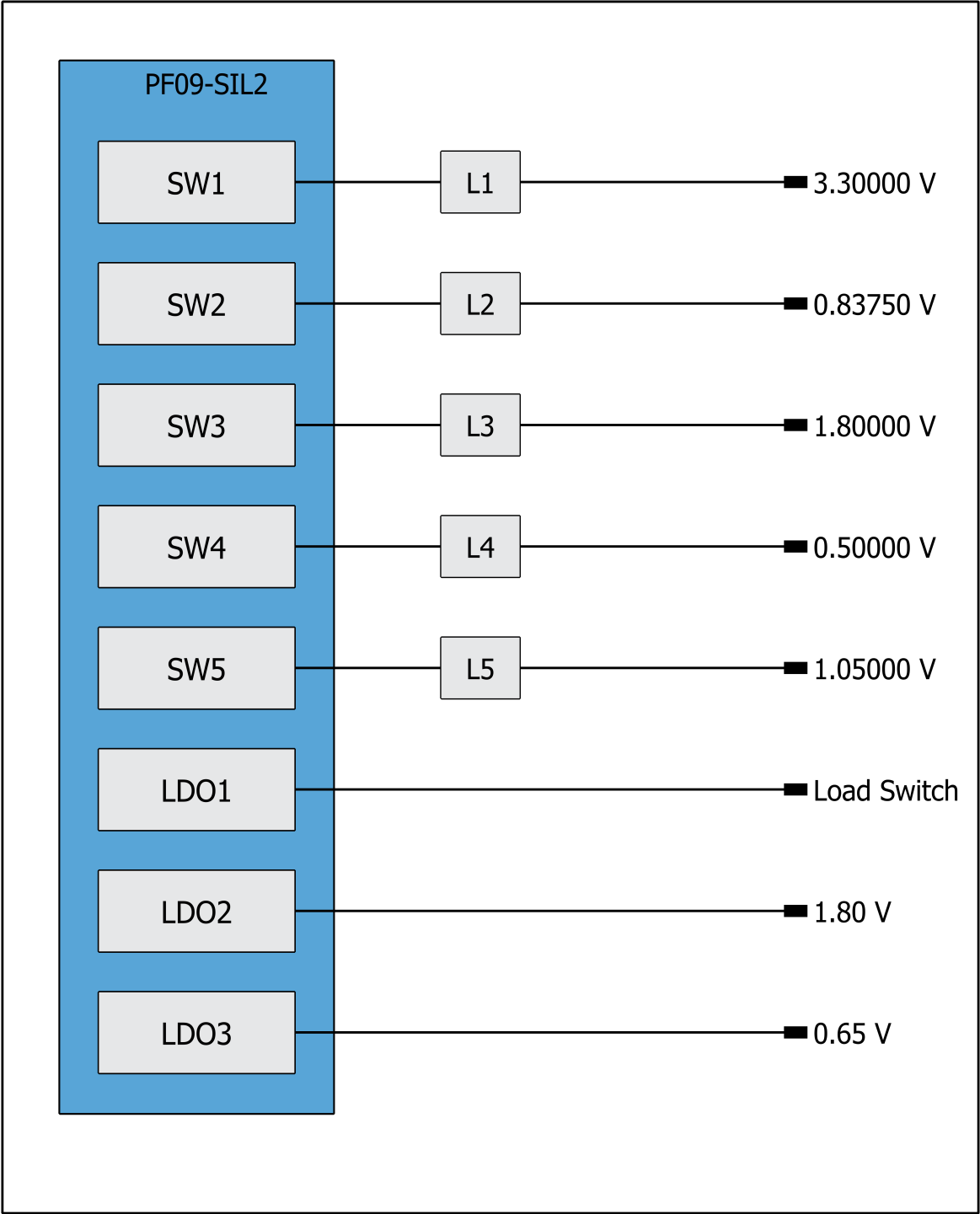


4 Power-up sequence summary



The signals depicted above are enable signals for each regulator. They don't represent the actual ramp voltage.

5 Hardware configuration diagram



Configuration report for PF09-SIL2 OTP program ID: A1 rev A

6 OTP configuration

See PF09 datasheet for parametric details. The OTP configuration summary for A1 sequence ID is provided in Tables below.

Table 2. Device OTP configuration

Functional block	Feature	OTP selection
System Configuration	Max Autoretry Mask Bits	0000
	DFS Autoretry Timer Mode	Infinite Retry
	DFS Autoretry	Autoretry Enabled
	VDIG OV RSTB Debounce	No Assertion
	VDIG OV CUTOFF Debounce	No Power Cutoff
	BGMON RSTB Debounce	No Assertion
	BGMON CUTOFF Debounce	No Power Cutoff
	Safety Handshake RSTB Debounce	No RSTB asserted
	Safety Handshake Power Cutoff	No Power Cutoff
	EWARN Delay Time	100 us
	PWRUP PG Monitoring	No PG check on PWRUP
	STANDBY Request Window	Always Open
	Low Power STANDBY	Low Power Operation
	System VIN Selection	5.0 V System
	Regulator Fault Timer	Disabled
	Max Soft Faults Allowed	Unlimited
	Max Fail-Safe Transitions	DFS Disabled
	Maximum Allowed Reset Events	Unlimited Resets

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FCCU Configuration	FCCU Debounce	12 us
	FCCU0 Operation	FCCU Bi-stable monitoring
	FCCU0 Polarity	Fault on HIGH state
	FCCU1 Operation	XRESET operation
	FCCU1 Polarity	Reset event on falling edge
	XRESET Operation In STANDBY	Enabled
	XRESET Reset Mode	Hard Reset
	XRESET Debounce	10 us
I/O Configuration	STBY Pin Polarity	STBY active high
	XFAIL Functionality	XFAIL enabled
	VAON Reaction On XFAILB	VAON not affected
	VIN OV Reaction	Interrupt only
	VIN OV FS0B Control	Enabled
	VIN OV Debounce Time	100 us
	VIN OV Monitoring	Enabled
	PWRON Push Reset Mode	Turn off Mode
	PWRON Operating Mode	Level Sensitive
	PWRON Debounce	32 ms
	DFS PWRON Wakeup	Wakeup Enabled
	RSTB Pulse On Soft Reset	Assert RSTB for 1000 us
	RSTB Buffer Type	Open Drain
	RSTB Short Detection Timer	500 us
	Dynamic CRC FS0B Control	Disabled

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	DFS FS0B Control	Enabled
	XFAIL FS0B Control	Enabled
	Watchdog FS0B Control	Enabled
	XRESET FS0B Control	Enabled
	Soft Faults FS0B Control	Enabled
	Hard Fault FS0B Control	Enabled
Watchdog Monitoring	Watchdog Timer Duration	32768 ms
	Watchdog Open Window	50 %
	Watchdog Counter	Disabled
	WD NOK Reset Limit	Development Mode
	Fault Counter Reduction	Good WD cannot Clear Faults
Clock Management	Clock Frequency Selection	20.0 MHz
	FSYNC Operating Mode	Clock OUT Mode
	Frequency Spread Spectrum	FSS Disabled
	Spread Spectrum Mode	Triangular modulation
I2C Configuration	I2C 7 Bit Address	0x08
	I2C CRC	Enabled
	I2C Secure Write	Disabled

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GPIO	GPIO1 Mode	VSELECT Input
	GPIO1 State In STANDBY	High
	GPIO2 Mode	LDO1EN Input
	GPIO2 State In STANDBY	High
	GPIO3 Mode	Push-pull Output
	ERRMON Input Polarity	Rising Edge detection
	GPIO3 State In STANDBY	Low
	GPIO4 Mode	Push-pull Output
	GPIO4 State In STANDBY	Low

Table 4. Power Sequencer configuration

Functional block	Feature	OTP selection
Power Sequencing	PWRON Push Reset Time	100 us
	Power-up Sequence Mode	Dynamic Mode
	Dynamic Sequence Settling Time	4000 us
	Power Down Delay	500 ms
	Sequencer Time Base	120 us
Power-Up Sequence	RSTB Power-up Sequence	Slot 29
	SW1 Power-up Sequence	Slot 19
	SW2 Power-up Sequence	Slot 9
	SW3 Power-up Sequence	Slot 11

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	SW4 Power-up Sequence	Slot 18
	SW5 Power-up Sequence	Slot 15
	LDO1 Power-up Sequence	Slot 25
	LDO2 Power-up Sequence	Slot 19
	LDO3 Power-up Sequence	OFF
	GPIO1 Power-up Sequence	OFF
	GPIO2 Power-up Sequence	OFF
	GPIO3 Power-up Sequence	Slot 1
	GPIO4 Power-up Sequence	Slot 5
	VMON1 Power-up Sequence	Slot 1
	VMON2 Power-up Sequence	Slot 5
	VAON Power-up Sequence	Always ON

Table 5. SW Regulators configuration

Functional block	Feature	OTP selection
SW1	SW1 Voltage In RUN State	3.30000 V
	SW1 Voltage In STANDBY State	3.30000 V
	SW1 Operation In Standby	PFM
	SW1 Current Limit	6.0 A
	SW1 DVS Ramp Rate	3.9 mV/us
	SW1 Phase Selection	45°
	SW1 Maximum DVS Range	0.400 V
	SW1 Minimum DVS Range	0.400 V

Configuration report for PF09-SIL2 OTP program ID: A1 rev A

	SW1 UV Threshold	95.0 %
	SW1 OV Threshold	105.0 %
	SW1 Inductor Selection	0.47 uH
	SW1 Hysteresis	Disabled
	SW1 Compensation Loop Capacitor	40 pF (Recommended)
	SW1 Compensation Loop Resistor	80 kOhm (Recommended)
	SW1 Compensation Transconductance	88 us (Recommended)
	SW1 Operating Mode	Buck Mode
	SW1LS Over Current Reaction	Interrupt Only
SW2	SW2 Voltage In RUN State	0.83750 V
	SW2 Voltage In STANDBY State	0.80000 V
	SW2 Operation In STANDBY	PFM
	SW2 Current Limit	4.5 A
	SW2 DVS Ramp Rate	3.9 mV/us
	SW2 Phase Selection	90°
	SW2 Maximum DVS Range	0.400 V
	SW2 Minimum DVS Range	0.400 V
	SW2 UV Threshold	95.0 %
	SW2 OV Threshold	105.0 %
	SW2 Inductor Selection	0.47 uH
	SW2 Hysteresis	Disabled

Configuration report for PF09-SIL2 OTP program ID: A1 rev A

	SW2 Compensation Loop Capacitor	40 pF (Recommended)
	SW2 Compensation Loop Resistor	80 kOhm (Recommended)
	SW2 Compensation Transconductance	88 us (Recommended)
SW3	SW3 Voltage In RUN State	1.80000 V
	SW3 Voltage In STANDBY State	1.80000 V
	SW3 Operation In STANDBY	PFM
	SW3 Current Limit	4.5 A
	SW3 DVS Ramp Rate	3.9 mV/us
	SW3 Phase Selection	135°
	SW3 Maximum DVS Range	0.400 V
	SW3 Minimum DVS Range	0.400 V
	SW3 UV Threshold	95.0 %
	SW3 OV Threshold	105.0 %
	SW3 Inductor Selection	0.47 uH
	SW3 Hysteresis	Disabled
	SW3 Compensation Loop Capacitor	40 pF (Recommended)
	SW3 Compensation Loop Resistor	80 kOhm (Recommended)
	SW3 Compensation Transconductance	88 us (Recommended)
SW4	SW4 Voltage In RUN State	0.50000 V
	SW4 Voltage In STANDBY State	0.50000 V
	SW4 Operation In STANDBY	PFM
	SW4 Current Limit	4.5 A
	SW4 DVS Ramp Rate	3.9 mV/us

Configuration report for PF09-SIL2 OTP program ID: A1 rev A

	SW4 Phase Selection	180°
	SW4 Maximum DVS Range	0.400 V
	SW4 Minimum DVS Range	0.400 V
	SW4 UV Threshold	95.0 %
	SW4 OV Threshold	105.0 %
	SW4 Inductor Selection	0.47 uH
	SW4 Hysteresis	Disabled
	SW4 Compensation Loop Capacitor	40 pF (Recommended)
	SW4 Compensation Loop Resistor	80 kOhm (Recommended)
	SW4 Compensation Transconductance	88 us (Recommended)
SW5	SW5 Voltage In RUN State	1.05000 V
	SW5 Voltage In STANDBY State	1.05000 V
	SW5 Operation In STANDBY	PFM
	SW5 Current Limit	4.5 A
	SW5 DVS Ramp Rate	3.9 mV/us
	SW5 Phase Selection	225°
	SW5 Maximum DVS Range	0.400 V
	SW5 Minimum DVS Range	0.400 V
	SW5 UV Threshold	95.0 %
	SW5 OV Threshold	105.0 %
	SW5 Inductor Selection	0.47 uH
	SW5 Hysteresis	Disabled
	SW5 Compensation Loop Capacitor	40 pF (Recommended)

Configuration report for PF09-SIL2 OTP program ID: A1 rev A

	SW5 Compensation Loop Resistor	80 kOhm (Recommended)
	SW5 Compensation Transconductance	88 us (Recommended)
Multi-Phase selection	SW2/3 Configuration	Single Phase Mode
	SW4/5 Configuration	Single Phase Mode

Table 6. LDO Regulators configuration

Functional block	Feature	OTP selection
LDO1	LDO1 Voltage In RUN State	3.30 V
	LDO1 Voltage In STANDBY	3.30 V
	LDO1 Enabled In STANDBY	Enabled
	LDO1 UV Threshold	95.0 %
	LDO1 OV Threshold	105.0 %
	LDO1 Operating Mode	Load Switch Mode
	LDO1 Soft Start	Slow Ramp
LDO2	LDO2 Voltage In RUN State	1.80 V
	LDO2 Voltage In STANDBY	1.80 V
	LDO2 Enabled In STANDBY	Enabled
	LDO2 UV Threshold	95.0 %
	LDO2 OV Threshold	105.0 %
	LDO2 Operating Mode	LDO Mode
	LDO2 Soft Start	Slow Ramp
	VLDO2MON Blanking Time	250 us
	VLDO2MON Masking Time	500 us

Configuration report for PF09-SIL2 OTP program ID: A1 rev A

LDO3	LDO3 Voltage In RUN State	0.65 V
	LDO3 Voltage In STANDBY	0.65 V
	LDO3 Enabled In STANDBY	Enabled
	LDO3 UV Threshold	95.0 %
	LDO3 OV Threshold	105.0 %
	LDO3 Operating Mode	LDO Mode
	LDO3 Soft Start	Slow Ramp
	VLDO3MON Blanking Time	250 us
	VLDO3MON Masking Time	500 us

Table 7. VMON and VAON

Functional block	Feature	OTP selection
VMON1	VMON1 Monitoring Voltage	0.9000 V
	VMON1 Standby Monitoring Voltage	0.9000 V
	VMON1 UV Threshold	95.0 %
	VMON1 OV Threshold	105.0 %
	VMON1 Settling Period	1000 us
	VMON1 Masking Time	5000 us
VMON2	VMON2 Monitoring Voltage	0.9000 V
	VMON2 Standby Monitoring Voltage	0.9000 V
	VMON2 UV Threshold	95.0 %
	VMON2 OV Threshold	105.0 %

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	VMON2 Settling Period	1000 us
	VMON2 Masking Time	5000 us
VAON	VAON Voltage Selection	1.8 V
	VAON UV Threshold	95 %
	VAON OV Threshold	105.0 %
	VAON Fault Mode	Standard Mode
	VAON Fault Time	100 ms

Table 8. Program ID

Functional block	Feature	OTP selection
OTP ID	Program ID High Bits	A
	Program ID Low Bits	1

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