

### 1 General description

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The PF5103 integrates multiple high performance buck regulators, and LDO regulators. It can operate as a stand-alone point-of-load regulator IC, or as a companion chip to a larger PMIC.

Built-in one-time programmable (OTP) memory stores key startup configurations drastically reducing external components typically used to set output voltage and sequence of regulators. Regulator parameters are adjustable through high-speed I2C after startup offering flexibility for different system states.

Functional safety features, developed according to ISO26262 specifications, enables the device to reach up to ASIL B safety level.

Note: Electrical characteristics for the PF5103 are maintained in the datasheet.

### 2 Features and benefits

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- Three high efficiency buck regulators
- Two LDO regulators
- Functional safety circuits to fit up to ASIL B safety level
  - Voltage monitoring with independent reference
  - Watchdog monitor – Simple
  - Independent Clock monitor
  - Overvoltage monitoring of V1P6 internal regulators
  - ABIST on monitoring circuits at startup
- External clock synchronization and Frequency spread spectrum
- Standby mode – controlled by dual function Sync/Standby pin
- One-time programmable device configuration
- 3.4 MHz I2C communication interface
- 28-pin flip chip QFN package with wettable flank

### 3 Applications

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- Automotive – RADAR, Infotainment, Domain controllers
- High-end consumer and industrial



## 4 Ordering information

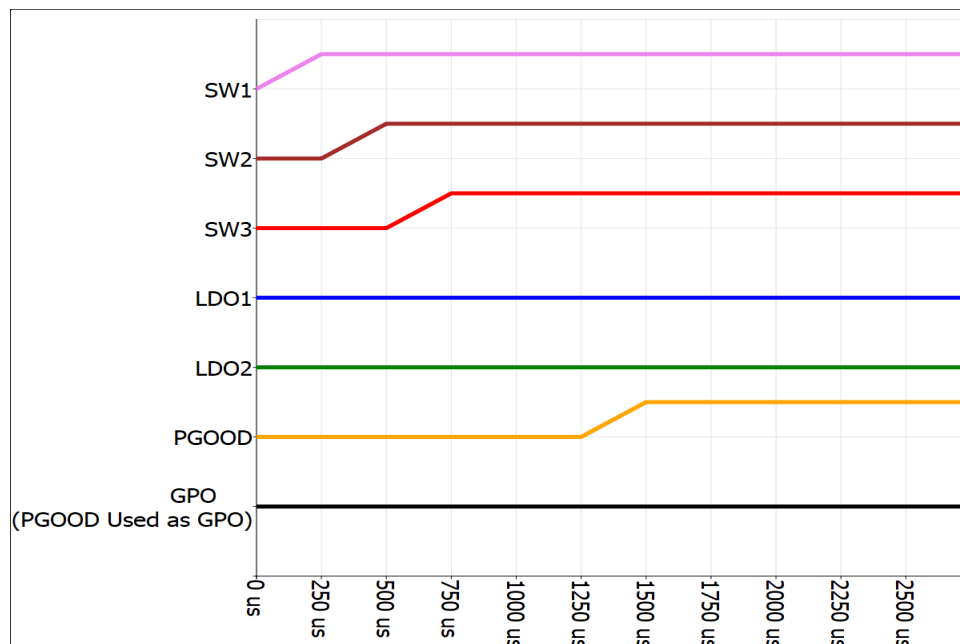
Table 1. Ordering information

Type number <sup>[1]</sup>	Package		
	Name	Description	Version
MPF5103AMBAHES <sup>[2]</sup>	QFN28	QFN28, plastic thermal enhanced very thin quad flat pack; no leads, wettable flank, 28 terminals, 0.5 mm pitch, 4.5 mm x 4.5 mm x 0.53 mm body	SOT2089-1(SC)

[1] To order parts in tape and reel, add the R2 suffix to the part number.

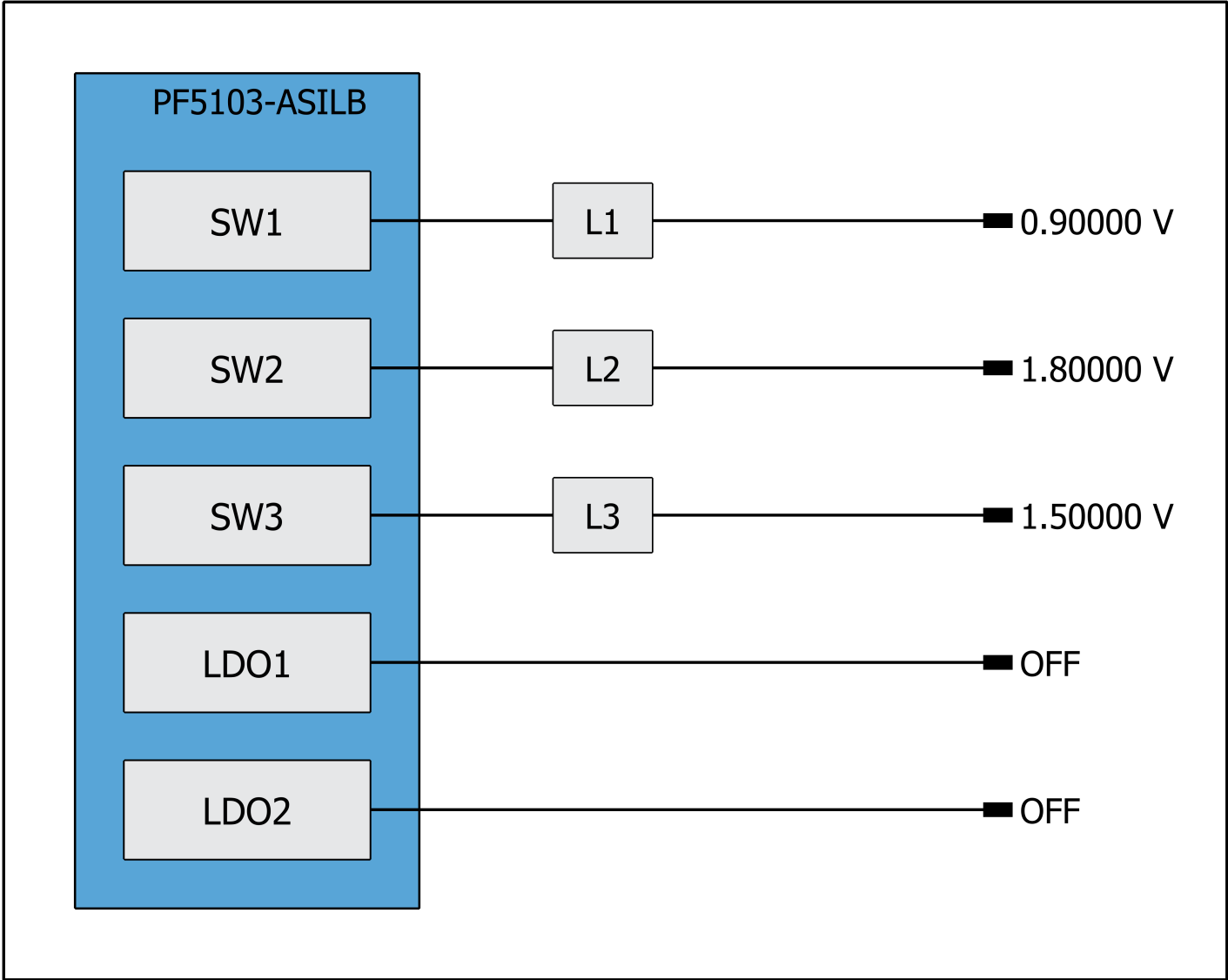
[2] Safety grade: PF5103-ASILB, non-programmed device.

## 5 Power-up sequence summary



The signals depicted above are enable signals for each regulator. They don't represent the actual ramp voltage.

6 Hardware configuration diagram



## Configuration report for PF5103-ASILB OTP program ID: AH rev A

## 7 OTP configuration

See PF5103 datasheet for parametric details. The OTP configuration summary for AH sequence ID is provided in Tables below.

**Table 2. Device OTP configuration**

Functional block	Feature	OTP selection
System Configuration	I2C Address	0x08 (Default)
	I2C CRC	Disabled
	I2C Secure Write	Disabled
	FCCU Monitoring Enable	FCCU monitoring Disabled
	WD Fault Recovery	Disabled
	VIN_OVLO Enable	Disabled
	VIN_OVLO Mode	Interruption only on VIN_OVLO
	VIN_OVLO Debounce	10 us
	VIN_OV Threshold	103.25 %
	VIN_UV Threshold	96.75 %
	Maximum Fault Counter	1
	Fail Safe State	Enabled
	Fail Safe Count	Number of transitions allowed will be configured to 15
	Bandgap Comparator	Enabled (Interruption Only)
	BGMON Selection	Bandgap Monitoring
	Standby Mode Enable	Standby function Disabled
	Low Power STANDBY	Disabled

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I/O Configuration	XFAIL Operation	Disabled
	Standby Polarity	STANDBY Active High
	INTB Dual Function	INTB function enabled
Watchdog Monitoring	WD Timer	WD Disabled
	WD Window Duration	1 ms
	WD Clear Window	Cleared within 100 % timer
	Watchdog Error Maximum Value	8
	Watchdog Selection	Simple type
	WD Standby Mode	Disabled
Clock Management	Nominal Switching Frequency	20 MHz
	SYNC Mode	SYNC function Enabled
	SW Mode	PWM
	Frequency Spread Spectrum Mode	Disabled
	Spread Spectrum Type	Triangular modulation
	FSYNC Frequency Range	Between 17.55 MHz and 22.46 MHz
	FSS Mode	23.5 kHz
	Clock DIV1	Divider 5 and frequency 4.00 MHz
	Clock DIV2	Divider 7 and frequency = 2.86 MHz

Table 3. Power Sequencer configuration

Functional block	Feature	OTP selection
Power-Up Sequence	Sequence Time Base	250 us
	SW1 Sequence Slot	Slot 0

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	SW2 Sequence Slot	Slot 1
	SW3 Sequence Slot	Slot 2
	LDO1 Sequence Slot	OFF
	LDO2 Sequence Slot	OFF
	PGOOD Power Up Sequence	Slot 5
	GPO Sequence Slot	OFF
Power-Down Sequence	Phase Sequence Delay	No delay

Table 4. SW Regulator configuration

Functional block	Feature	OTP selection
SW1	Output Voltage	0.90000 V
	UV Detection Threshold	95 %
	OV Detection Threshold	105 %
	ILIM Detection Threshold	4.0 A
	Output Inductor	0.47 uH
	Switching Phase	No phase shift
	SW1 Standby	Disabled
	PGOOD Mode	Enabled
	SW1 Clock	CLK_DIV1
	SW1 OV Bypass	OV Fault bypassed
	SW1 UV Bypass	UV Fault bypassed
	SW1 ILIM Bypass	ILIM Protection Enabled

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	SW1 DVS Ramp	1.95 mV/us at fsw = 2.5 MHz
	SW1 Gain Margin	35 uS
	SW1 Compensation Resistor	80 kOhm
	SW1 Compensation Capacitor	100 pF
SW2	Output Voltage	1.80000 V
	UV Detection Threshold	95 %
	OV Detection Threshold	105 %
	ILIM Detection Threshold	6.0 A
	Output Inductor	0.47 uH
	Switching Phase	No phase shift
	SW2 Standby	Disabled
	PGOOD Mode	Enabled
	SW2 Clock	CLK_DIV1
	SW2 OV Bypass	OV Fault bypassed
	SW2 UV Bypass	UV Fault bypassed
	SW2 ILIM Bypass	ILIM Protection Enabled
	SW2 DVS Ramp	1.95 mV/us at fsw = 2.5 MHz
	SW2 Gain Margin	70 uS
	SW2 Compensation Resistor	80 kOhm
	SW2 Compensation Capacitor	100 pF
SW3	Output Voltage	1.50000 V
	UV Detection Threshold	95 %
	OV Detection Threshold	105 %

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	ILIM Detection Threshold	6.0 A
	Output Inductor	0.47 uH
	Switching Phase	No phase shift
	SW3 Standby	Disabled
	PGOOD Mode	Enabled
	SW3 Clock	CLK_DIV1
	SW3 OV Bypass	OV Fault bypassed
	SW3 UV Bypass	UV Fault bypassed
	SW3 ILIM Bypass	ILIM Protection Enabled
	SW3 DVS Ramp	1.95 mV/us at fsw = 2.5 MHz
	SW3 Gain Margin	70 uS
	SW3 Compensation Resistor	80 kOhm
	SW3 Compensation Capacitor	100 pF
Multi Phase selection	SW1 Multi-phase Selector	SW1,SW2 and SW3 operate in single phase mode

Table 5. LDO Regulator configuration

Functional block	Feature	OTP selection
LDO1	Output Voltage	0.75 V
	UV Detection Threshold	96.5 %
	OV Detection Threshold	103.5 %
	LDO1 STANDBY	Disabled
	PGOOD Mode	Disabled
	LDO1 DVS Ramp	180 us



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	LDO1 Regulator Mode	Normal Mode
	LDO1 OV Bypass	OV Fault bypassed
	LDO1 UV Bypass	UV Fault bypassed
	LDO1 ILIM Bypass	ILIM Protection Enabled
LDO2	Output Voltage	0.75 V
	UV Detection Threshold	96.5 %
	OV Detection Threshold	103.5 %
	LDO2 STANDBY	Disabled
	PGOOD Mode	Disabled
	LDO2 DVS Ramp	180 us
	LDO2 Regulator Mode	Normal Mode
	LDO2 OV Bypass	OV Fault bypassed
	LDO2 UV Bypass	UV Fault bypassed
	LDO2 ILIM Bypass	ILIM Protection Enabled
LDO Common	LDOx Out Open	Disabled

Table 6. Program ID

Functional block	Feature	OTP selection
Program ID	Program ID High	A
	Program ID Low	H
	Program ID Rev	A

## Configuration report for PF5103-ASILB OTP program ID: AH rev A

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