MSC8156EVM Reference Manual

MSC8156 Evaluation Module

MSC8156EVMRM
Rev 0, October 2010

freescale™
semiconductor

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
+1-800-521-6274 or
+1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064
Japan
0120 191014 or
+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 010 5879 8000
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor
Literature Distribution Center
+1-800 441-2447 or
+1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor
@hibbertgroup.com

MSC8156EVMRM
Rev. 0
10/2009

Contents

1 General Information

The MSC8156 evaluation module system (MSC8156EVM) is a complete debugging environment intended for engineers developing applications for the MSC8156 family of Freescale digital signal processors (DSPs). The MSC8156 DSP family devices are highly integrated DSP processors that contain one to six StarCore SC3850 DSP subsystems (up to 48 GMACS with six cores at 1 GHz). The MSC8156EVM supports the following members of the DSP family:

- MSC8151 which has one SC3850 core with baseband processing (MAPLE-B) support
- MSC8152 which has two SC3850 cores with baseband processing (MAPLE-B) support
- MSC8154 which has four SC3850 cores with baseband processing (MAPLE-B) support
- MSC8156 which has six SC3850 cores with baseband processing (MAPLE-B) support
- MSC8251 which has one SC3850 core
- MSC8252 which has two SC3850 cores
- MSC8254 which has four SC3850 cores
- MSC8256 which has six SC3850 cores

The MSC8156EVM includes an MSC8156 DSP that can be configured to emulate any of the DSPs in the family.

Each SC3850 subsystem includes:

- SC3850 DSP core
- 32 KB DCache
- 32 KB ICache
- 512 KB unified L2 cache/M2 shared memory
- Memory management unit (MMU)
- Write queue
- Dual timers
- Extended programmable interrupt controller (EPIC) that supports 256 interrupts
- Real-time debug support and a profiling unit (DPU)

In addition, the MSC8156 family devices each contain:

- 1 MB of M3 shared memory
- Two DDR2/DDR3 memory controllers with a 64-bit data rate up to 800 MHz
- High speed serial interface (HSSI) with two 4-channel SerDes port that multiplex:
  - Two serial RapidIO x1/x4 interface at 1.25/2.5/3.125 GBaud over SerDes[1–2] ports.
  - PCI express x1/x2/x4 at 2.5 GBaud over the SerDes2 port
  - Two SGMII interfaces
- Dual RISC QUICC Engine subsystem that supports
  - 2 RGMII Ethernet ports with direct PHYs or 2 SGMII ports through the HSSI
  - SPI
- Four 1024-channel 400 Mbps time-division multiplexing (TDM) interfaces
- UART
- I^2C
- Multi-Protocol Baseband Accelerator (MAPLE-B)
- Optional Security Engine (Version 3.1) in the MSC8156E device.

The MSC8156 DSP family targets high-bandwidth highly computational DSP applications and is optimized for 3GPP, TD-SCDMA, 3G-LTE, and WiMAX applications. The MSC8156EVM is intended to serve as a platform for software and hardware development in the MSC8156 DSP family environment. On-board resources and the associated debugger enable developers to perform a variety of tasks, including:

- Download and run code
- Set breakpoints
- Display memory and registers
- Connect proprietary hardware via an expansion connector

The board (shown in **Figure 1-1**) can function in a stand-alone configuration or as a PCI Express board

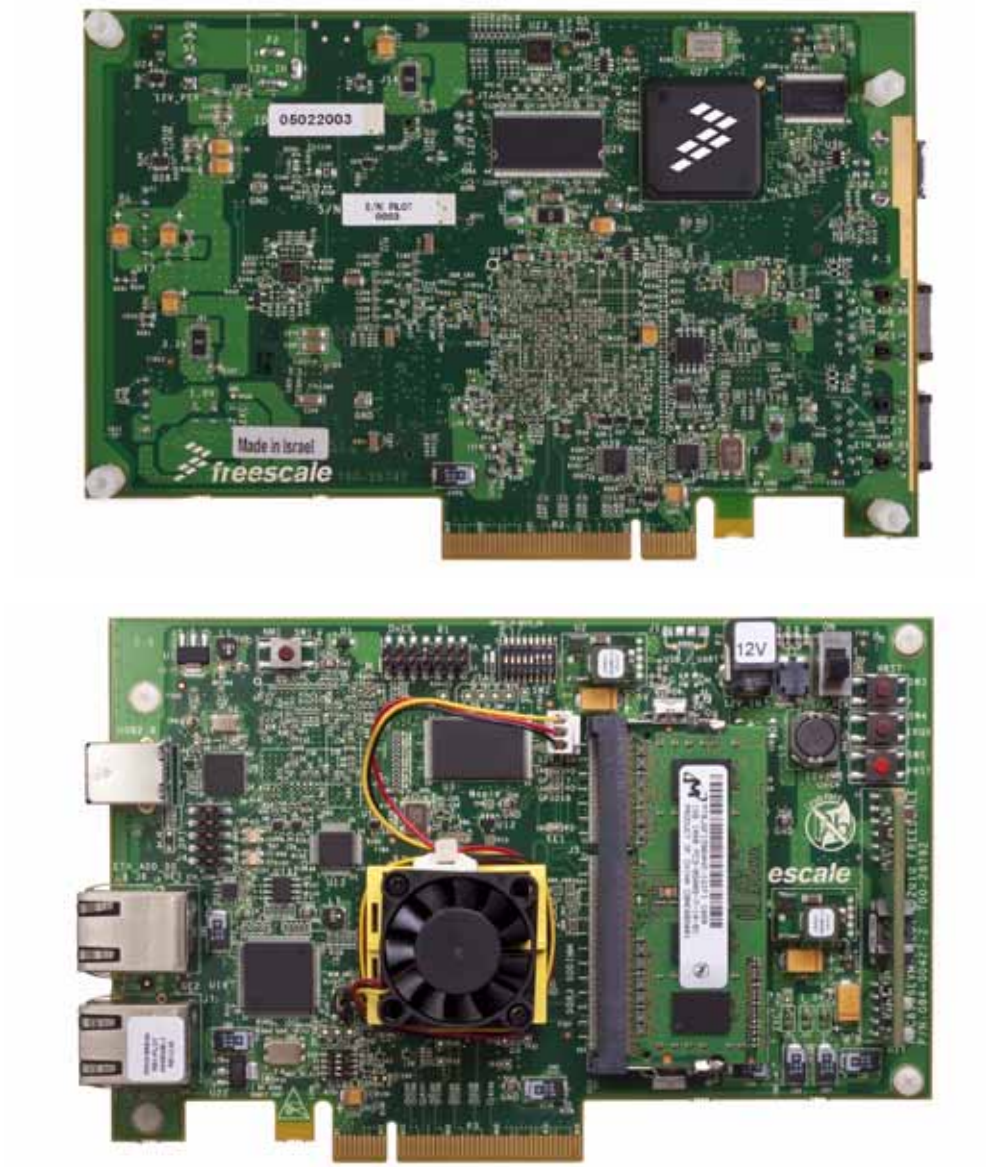

Figure 1-1. MSC8156EVM PCI Express Form Factor Board

1.1 Working Configurations

The MSC8156EVM supports two working configuration:

- *Stand-Alone Mode*. The MSC8156EVM can run in a stand-alone mode like other application development systems, with direct connections to debuggers, power supply, and other external connections.
- *PCI Express Mode*. The MSC8156EVM is inserted in a standard PCI Express slot that allows testing of the high-speed PCI Express port with other platforms.

1.2 MSC8156EVM Feature List

The EVM is based on a MSC8156 DSP family single chip.

- Supports the MSC8156 DSP family devices running at up to 1000 MHz with core voltages of 1 V.
- The DDR controller (DDRC2) is configured in DDR3 mode and connected to a 204-pin SODIMM populated with 1 GB of 64-bit wide memory operating at an 800 MHz data rate.
- The DSP RGMII (at ports GE1 and GE2) connects to one dual Marvell 88E1121 GETH PHYs for regular board configuration.
- The DSP configuration and boot support includes the following:
  - Reset Configuration Reset Source three bits set by appropriate DIP-switches.
  - Serial configuration and boot from a large (64 KB) I^2C EEPROM.
  - Boot from communications port: from Ethernet RGMII port.
- Two available debug interfaces:
  - On-board USB TAP controller (eUTAP)
  - OnCE 14-pin header for any external TAP controller
- 100 MHz clock oscillator for MSC8156 CLKIN.
- The MSC8156 clock output signal may be measured on CLKOUT test point (TP15).
- Can function in various main supply configurations:
  - Stand-alone mode with an external power 12 VDC @ 3A
  - As a PCI Express card in the PCI Express system.
- Onboard power system comprises two regulator steps:
  - Primary power system is 1.0 V POL regulator for MSC8156 loads: cores, MAPLE-B, and M3;
  - 2.5 V for I/O; and 3.3 V for onboard peripherals.
  - DDR switching power supplies for DDRC2 port.
  - LDOs, for onboard peripherals, are fed from 2.5 V
  - Voltage supervisor monitors the EVM power supply. Power Good (PG) signal and dedicated LED LD1 indicate power system status. Any failure causes to nPRST signal be low continuously.
- Push Buttons
  - Main Power-On-Reset $\overline{\text{PORESET}}$ (SW5)
  - Hard Reset $\overline{\text{HRESET}}$ (SW3)
  - $\overline{\text{IRQ0}}$ (SW4)
  - $\overline{\text{NMI}}$ (SW1)

1.3 MSC8156EVM Block Diagram

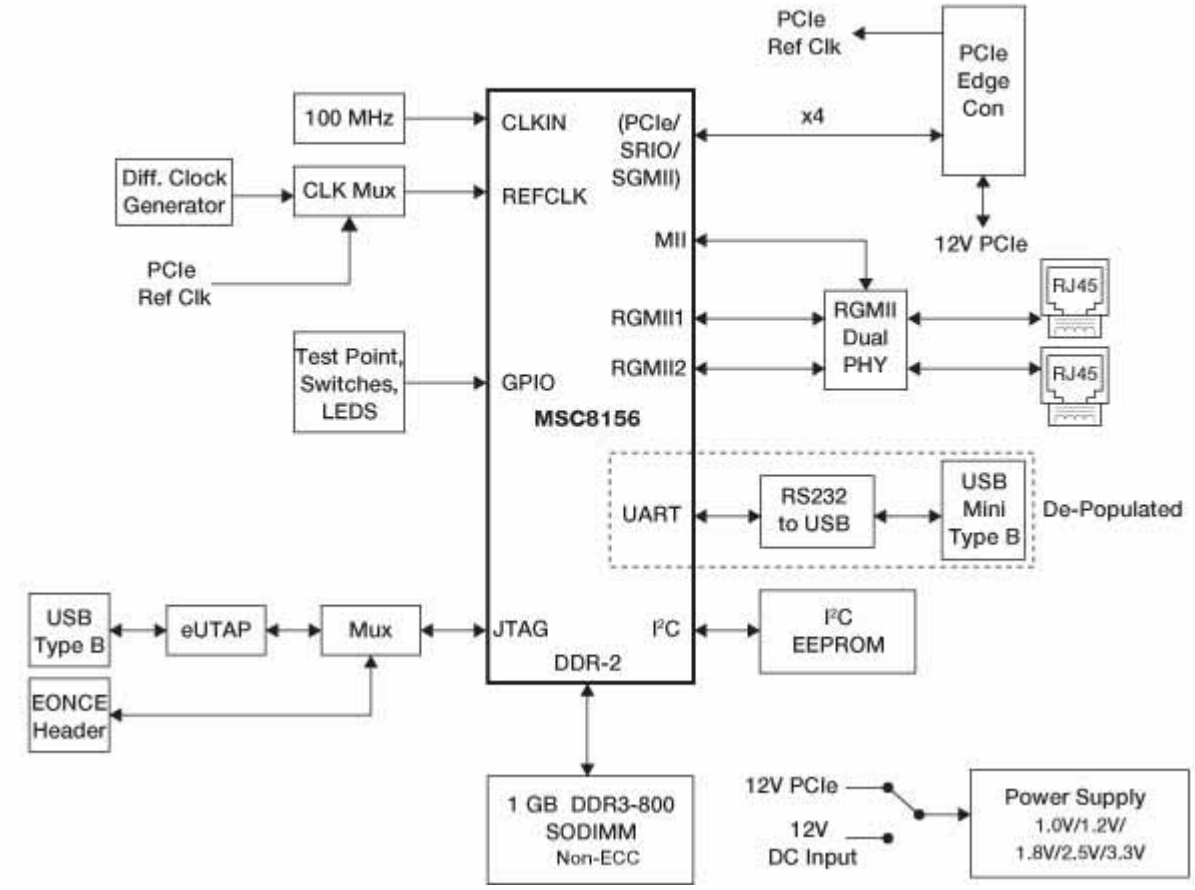

Figure 1-2. EVM Block Diagram

1.4 Definitions, Acronyms, and Abbreviations

EVM	Evaluation Module
BSP	Board Support Package
CS	Chip Select
DDR3	Double Data Rate, or Double Data Rate SDRAM Type 3
DDR-1, DDR-2	The MSC8156 DDR Controller 1 and DDR Controller 2
DIP	Dual-In-Line Package.
DMA	Direct Memory Access
EEPROM	Electrical Erasable Programmable Memory
eUTAP	Embedded USB TAP Controller, populated on the EVM
GETH	Giga-bit Ethernet
I^2C	Inter-IC bus
ISP	In-Circuit Programming
JTAG	Joint Test Access Group
LED	Light Emitting Diode
lsb	least significant bit
MI/MII	Ethernet Management Interface
msb	most significant bit
OnCE	On-Chip Emulation Port
PC	IBM-compatible Personal Computer
PCI Express	Express Peripheral Components Interconnect
PHY	Physical Layer
POL	Point-of-Load DC-DC converter
PS, PSU	Power Supply Unit
RGMII	Reduced Gigabit Media Independent Interface
RCW(L,H)	Reset Configuration Word (Low/High)
SerDes	Serializer/Deserializer
SODIMM	Small outline dual inline memory module
SPD	Serial Present Detect

1.5 Related Documentation

Freescale provides the following documentation with this kit:

- DSP Technical Data Sheet (MSC8156, MSC8156E, MSC8154, MSC8154E)
- DSP Reference Manual (MSC8156, MSC8156E, MSC8154, MSC8154E)
- MSC8156EVM Hardware Getting Started Guide
- MSC8156EVM Reference Manual
- MSC8156EVM Using Code Warrior™ and MSC8156EVM Kit Configuration Guide

1.6 Specifications

The MSC8156EVM specifications are given in **1-1**.

Table 1-1. MSC8156EVM Specifications

CHARACTERISTICS		SPECIFICATIONS
DSP		MSC8156, MSC8156E, MSC8154, or MSC8154E **Note:** See **Figure 2-11** for details on configuring the board for the MSC8156/MSC8156E versus the MSC8154/MSC8154E DSPs.
Power requirements		12 V @3 A (min.) external DC power supply for stand alone mode.
Ambient temperature		0°C to 70°C
Storage temperature		–25°C to 85°C
Relative humidity		5% to 90% (non-condensing)
Dimensions according to Double-width AMC form factor (except the high):		Length: 148 mm Width: 181 mm Height: 27 mm with socket or 17.5 mm with soldered chip PCB Thickness: 1.6 mm
Operating frequency		Cores run up to 1.0 GHz @ 1V
Memory:	Internal: M2, M3, ICache, DCache	—
	DDR3 Module on DDR-2 port	1 GB space 64-bit wide Memory Module in SODIMM204 form factor. Clock 400 MHz, Data rate 800 MHz
	Serial: I^2C EEPROM	64 kB serial EEPROM.
COM ports	Gigabit Ethernet	Two Gbps Ethernet Ports for RGMII interface.
	I^2C	Compliant with standard. Running up to 400 Kbps
	SerDes port 2	x1/x4 serial RapidIO endpoint operates at 1.25, 2.5, or 3.125 Gbaud and complies with Specification 1.2. x1/x2/x4 PCI Express endpoint operates at 2.5 Gbaud and complies with Specification 1.0.

2 Functional Description

This chapter describes the functional blocks of the MSC8156EVM and indicates how to configure the features of each block.

2.1 SerDes Configuration

SerDes1 and SerDes2 of the MSC8156 family high speed serial interface (HSSI) are independent, configurable, multiprotocol four-lane serial ports. SerDes1 supports Serial RapidIO and SGMII ports; SerDes2 supports Serial RapidIO, SGMII, and PCI Express ports in different modes. The EVM supports only SerDes2 configurations, SerDes1 is not connected.

The EVM links the MSC8156 family SerDes port 2 to the PCI Express edge connector, as shown on **Figure 2-1**.

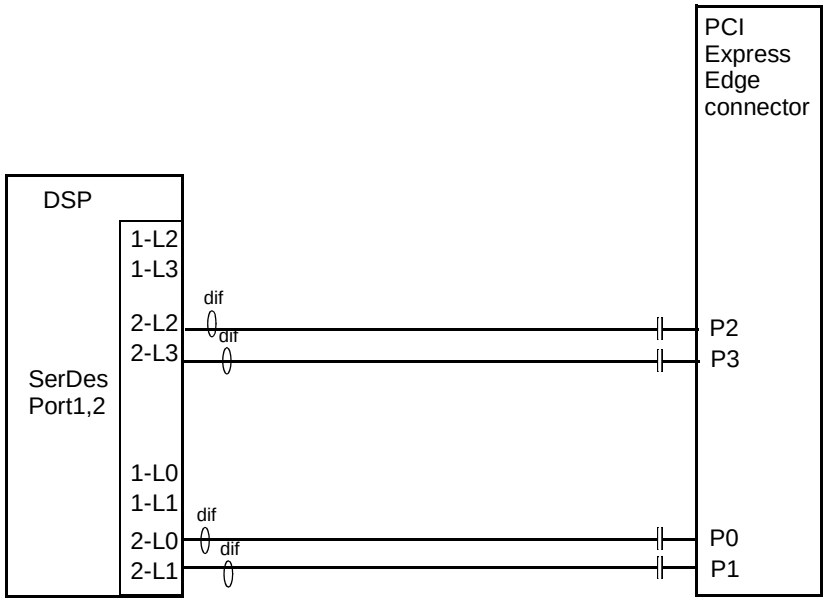

Figure 2-1. SerDes Connection Scheme

2.2 Gigabit Ethernet Ports (RGMII ETH PHY)

The MSC8156 has two gigabit Ethernet controllers (GE1 and GE2) that can be configured independently for RGMII or SGMII interface mode, The ETH PHY in the MSC8156EVM only supports RGMII mode.

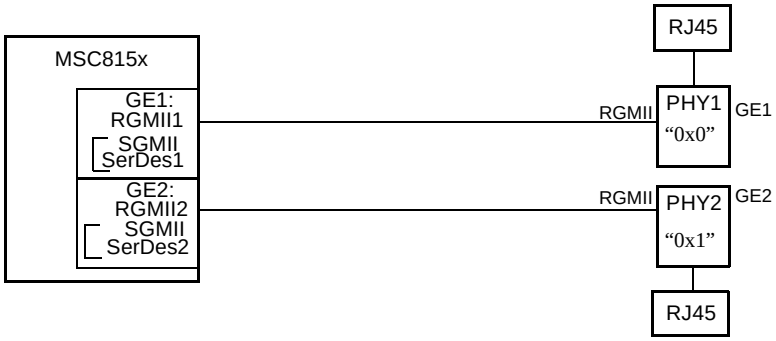

Figure 2-2. EVM Gigabit Ethernet Links

Two Marvell 88E1121 dual GETH PHYs serve the MSC8156 RGMII ports. The PHYs connect the RGMII signals to 1000Base-T interfaces. The PHY for GE Port1 has MII bus address "0x0"; The GE Port2 uses address "0x1". The PHY is from the Alaska family which is compliant to the 10/100/1000 Base-T standard. It features:

- RGMII support
- Virtual Cable Tester
- Automatic MDI/MDIX crossover
- Low power

The PHY is hardware configured and is automatically configured upon Power on Reset to operate in GETH mode.

The Management Interface bus accesses the PHY and allow the MSC8156 to read and write the PHY registers in order to change the initial default settings.

2.3 Boot Over Ethernet

Boot over Ethernet can execute only through GE1. Boot is set up in the Reset Configuration Word. **Figure 2-3** shows the boot configuration.

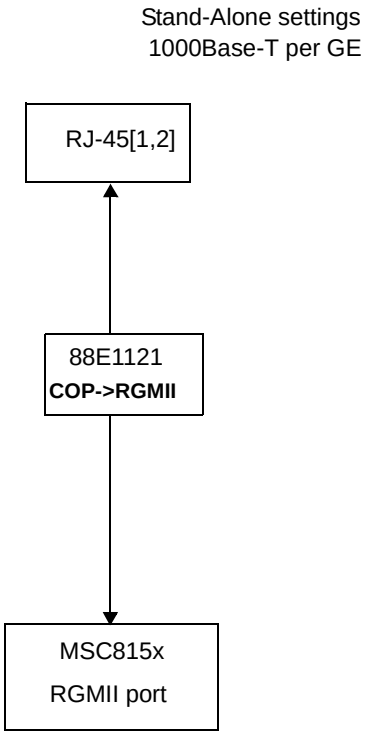

Figure 2-3. Boot-over-ETH configuration

2.4 DDR3 Module

The DDR3 Module is an MT8JSF12864H(I)Y-1G1 by Micron inserted in SODIMM204 socket. It has 1GB accessed via a 64-bit Data Bus. The socket is 78193-3012 produced by Molex. The module has an I^2C SPD EEPROM at address 0x52.

2.5 I²C Bus

Figure 2-4 shows the I²C bus diagram.

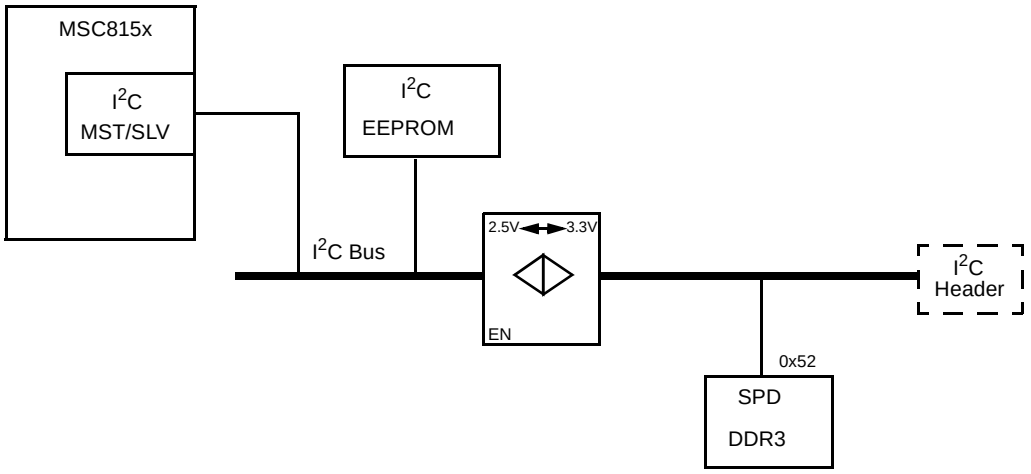

Figure 2-4. I²C Bus Peripherals

The only Master on the I²C bus: is the MSC8156 I²C controller. The on-board master can access all the I²C slaves on the bus. The SPD EEPROM on the DDR Module contains configuration data needed to program the DDR controller.

The MSC8156 can load the configuration word from one-byte (short) and two-byte (long) addressing I²C EEPROM parts. The RCW source part has device address 0x50. See **Figure 2-5** for connection details.

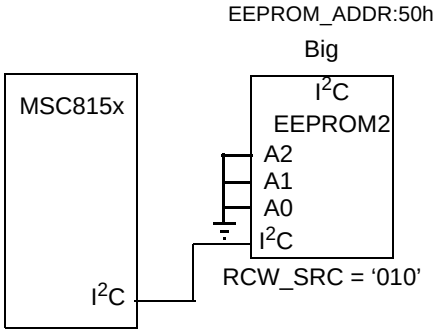

Figure 2-5. I²C EEPROM Select

2.6 JTAG Debug Interface

The EVM JTAG interconnection scheme is shown in **Figure 2-6** below:

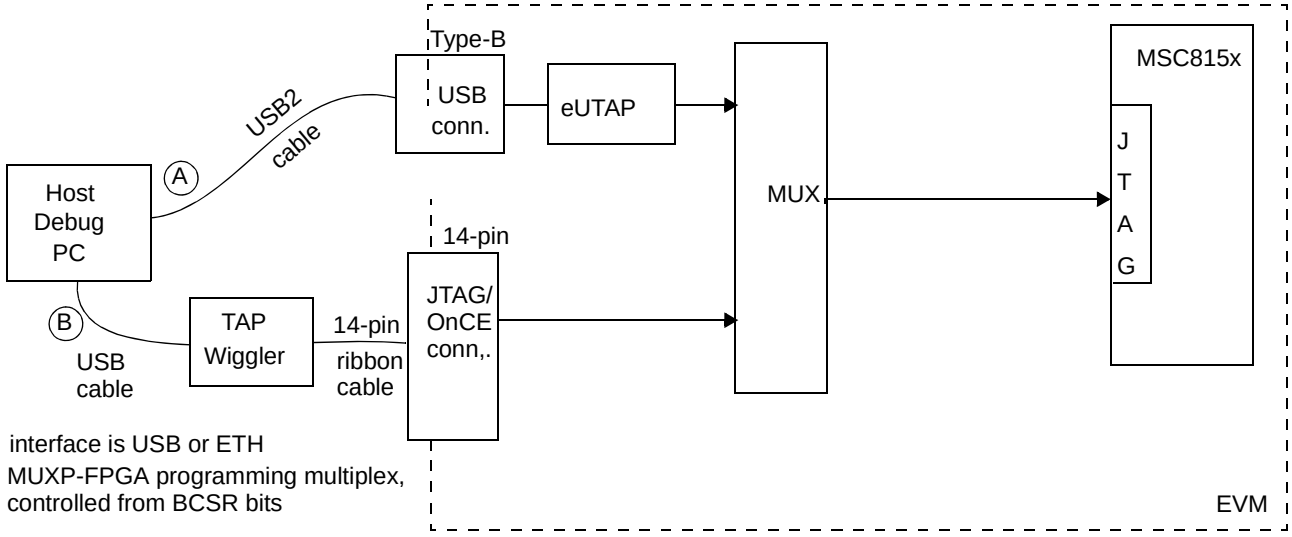

Figure 2-6. EVM JTAG Multiplexer

The MSC8156 Debug Port (JTAG) can interface to the Host Debug PC over USB port (“A” path) or through standard 14-pin JTAG/OnCE header (“B” path). The “B” configuration requires an external device, such as a USB TAP, to transform the Host interface to JTAG signals.

The default “A” interconnection uses only USB cable. On the EVM, the embedded USB-to-TAP drives JTAG signals to the FPGA multiplex. Selection of the JTAG source direction is done logically by USB Vbus sensing. When the USB cable is disconnected, the MSC8156 Debug Port is linked to the 14-pin OnCE header.

2.7 Reset Operation and Configuration

2.7.1 Reset Connectivity

Figure 2-7 shows the reset connectivity scheme to the MSC815x device

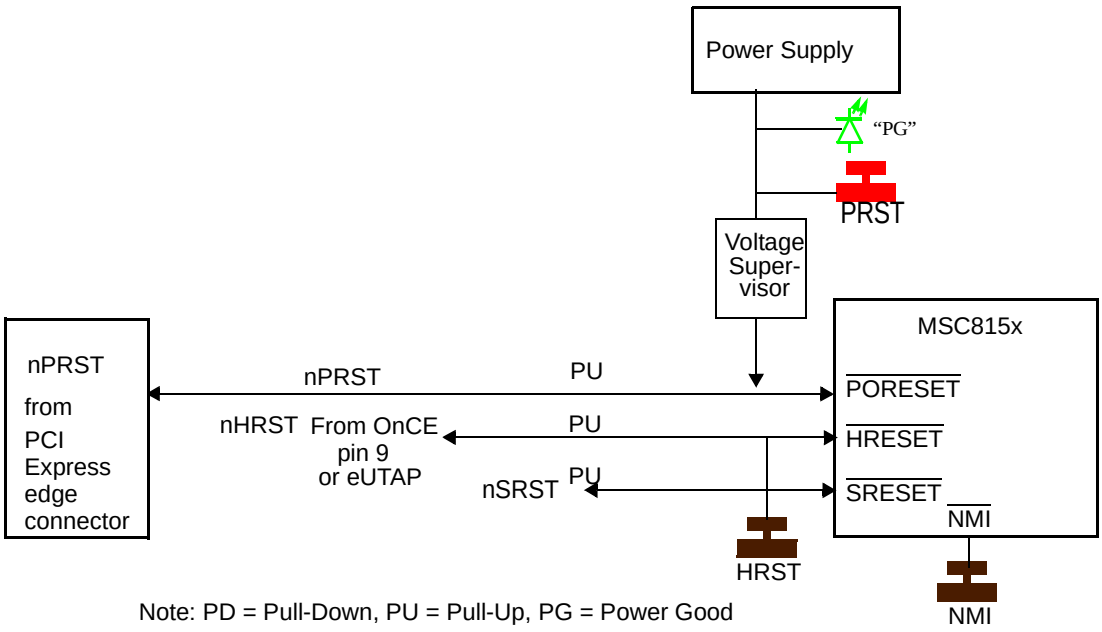

Figure 2-7. EVM Reset Scheme

The MSC8156EVM has two sources for power-on reset signal:

- In stand-alone mode, the voltage supervisor generates Power-On-Reset as long as the power supply voltages are not stable and when the push button is asserted.
- In PCI Express mode, a power-on-reset signal comes from the PCI Express Edge connector and connects to the nPRST signal on the MSC8156EVM board. In PCI Express mode, the power is provided from the Edge connector and the voltage supervisor is also active and can generate reset signal.

2.7.2 MSC815x Hardware Configuration

The MSC8156EVM uses the following configuration options for the hardware configuration:

- When the nPRST signal is asserted, the MSC8156 samples the RCW source bits.
- There are two reset configuration sources. Jumper JP1 chooses the selected option.
  - If there is no jumper attached or when the jumper is in the 2-3 position, the default is a 1 KΩ resistor between pins 1 and 2 that selects the I^2C EEPROM as the source.
  - When the Jumper is in the 1-2 position, the reset configuration word source is a hard coded external reduced 22 bit reset configuration word (see the **Reset** chapter in the device specific reference manual for details).
- The user can change the BOOT PORT SELECT field (BPRT) in the hard-coded Reset Configuration Word High, that defines the boot port interface configuration (default is 000 which selects I^2C).

Table 2-1. MSC8156 Configuration Modes

RCW_SRC[0:2]	JP1 Connections	Source Type	Description
010	None or pins 2-3	I^2C EEPROM	The EEPROM applies address 0x50 to provide configuration data. Configuration DIP-switches don't care.
011	pins 1-2	External 22-bits (reduced) Configuration Word	The MSC8156 samples 22 appropriate RC bits value

Figure 2-8 shows the reset configuration signal connection details.

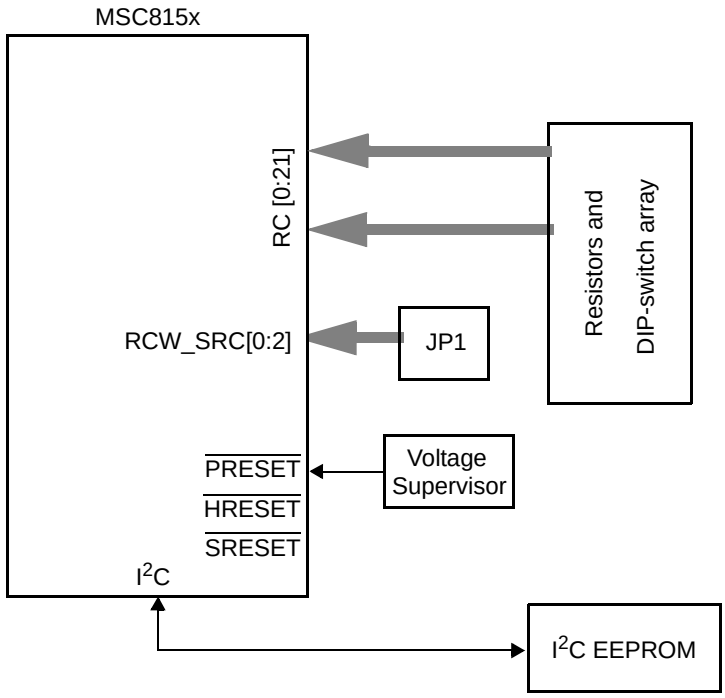

Figure 2-8. General Configuration Connection Scheme

2.7.3 Boot Port

The EVM supports the following boot ports defined by the hard-coded RCWH[BPRT] field (configured by a 0 plus the RC[7–9] inputs—see the Reset Configuration Word High Register in the device reference manual **Reset** chapter).

Table 2-2. Boot Modes

BPRT[03] Value	MSC815x Boot Mode	Source
0000	I^2C	I^2C EEPROM 512 KB
0001	RGMII1	RJ-45-1 over RGMII PHY
0010	RGMII1 + I^2C	

2.8 Clock Options

The main clock source is a 100 MHz, 100 PPM 3.3 V clock oscillator. The 2.5 V buffer transforms the 3.3 V clock signal to the 2.5-V level required for MSC8156 CLKIN input. The clock circuits generate the clocks for the cores, the internal CLASS buses, the QUICC Engine module, the RapidIO/PCI Express controllers, and other device peripherals. The clock generation components and clock scheme are shown **Figure 2-9**.

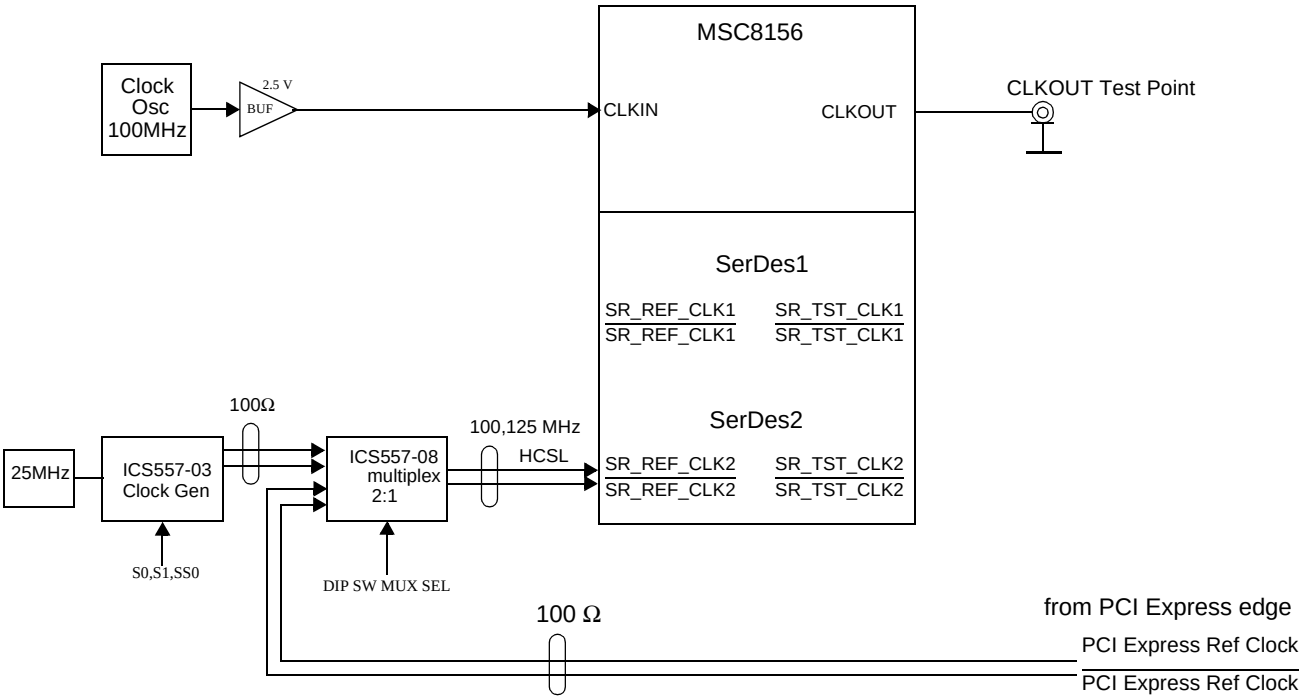

Figure 2-9. MSC8156 Clock Scheme

The SerDes Clock Generator is an ICS557-03 part by IDT that provides the SerDes2 reference clock from a 25 MHz crystal with the spread spectrum feature. The device has two differential (HCSL) outputs. The spread type and amount are configured via a select pin. The ICS557-08 2:1 multiplexer device allows selection of the SerDes2 clock reference. The on-board SerDes clock reference is used for the EVM standalone configuration. The PCI Express backplane mode requires a reference clock from an external PCI Express Root Complex. The DIP-switch SW6[4] selects the source for REF_CLK2. When SW6[4] is in “ON” position, this provides a logic “0” that indicates that the REF_CLK2 comes from the PCI Express Backplane. When SW6(4) is in “OFF” position, it applies a logic “1” that indicates that REF_CLK2 is coming from the ICS557-3 On board Clock generator.

SW6[3] and SW6[2] select an output frequency of 100 or 125 MHz.as listed in **Table 2-3**.

Table 2-3. SerDes Clock Frequency Selection

SW6[3]	SW6[2]	Frequency
1	0	100 MHz
0	1	125 MHz

SW6[1]enables the Spread Spectrum mode for ICS557-03 generator. When SW6[1] is in the “ON” position, spread spectrum mode is not selected.

Table 2-4. SerDes Clock Frequency Selection

SW6[1]	Spread Spectrum
0	No spread
1	Down –0.5

2.9 Power Supply System

This section describes the power supply system and how it operates.

2.9.1 Primary Power Supply

There are two possible sources of power, depending on the working mode:

- Stand-alone Mode—external 12VDC @ 3A Power Supply with Power Switch S1 is “ON”.
- PCI Express Mode—12V from PCI Express backplane when Power Switch S1 is “OFF”.

The External 12V Power Supply is a standard power supply. Its parameters are:

- Vin = 100 V–240 V AC @ 50–60 Hz
- Vout = 12 VDC ± 5% @ 3.0 A

2.9.2 Power Supply Operation

The secondary power system is built from several of DC to DC power supplies:

- 16 A DC to DC convertor (iAD12016A008V from TDK) set to 1 V: supplies the core voltage.
- 3 A DC to DC convertor (LDO03C from Emerson) set to 3.3 V supplies power for several devices on the board
- 3 A DC to DC convertor (LDO03C from Emerson) set to 2.5 V supplies power for MSC8156 I/O and the GETH PHY
- 4 A special DDR power supply:MC34716EP from Freescale set to 1.5 V for DDR3

MSC8156 Power-UP sequence is determine by power sequencer:ISL6125IRZA from Intersil.

Figure 2-10 shows power distribution.

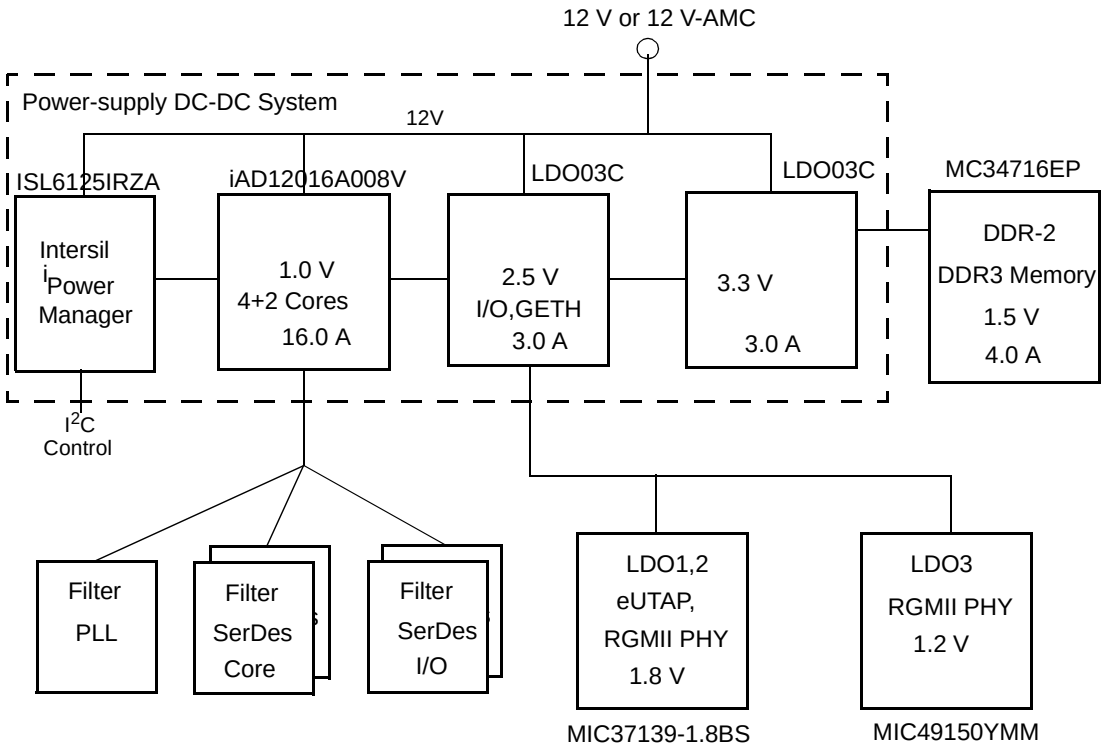

Figure 2-10. Power Distribution Scheme

The iAD12016A008V that provides the core voltage for the MSC8156 DSP has jumpers on the 1.0 V power rail to isolate two of the six cores for better power saving. The DDR-2 port power supply is configured for a DDR3 module that requires a 1.5 V power supply and VTT and VREF voltages are set accordingly.

Note: Supporting the DSPs with less than 6 cores requires that JS1 power jumper be tied to TP28: GND instead of to the 1 V as shown in **Figure 2-11**.

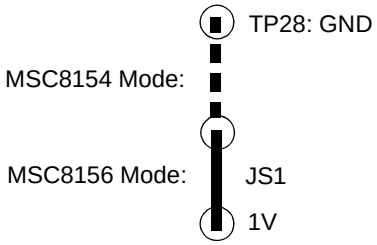

Figure 2-11. Power Rails Disconnect Scheme

2.9.3 Power-Up Sequence

MSC8156 family DSPs require the following power-up sequence:

- 1.0 V supplies should rise before any other supplies in any sequence: VCORE,VPLL,VMAPLE, VM3,VSXP, VSXC.
- After the 1.0 V supplies rise to 90% of their nominal value, the other DSP 2.5 V I/O supply rises.

The Intersil ISL6125IRZA device provides the required power-up sequence. The 3.3 V is powered directly from the 12V input without any control.

2.10 Separate LEDs

MSC8156EVM LEDs are described in **Table 2-5**.

Table 2-5. LED Descriptions

Ref.	Name	Color	LED On	LED Blinking	LED Off[a]
LEDs in J6	LINK	Green	RGMII phy -1 has Link at 1Gbps	Activity	No link on Port1
	ACT	Orange	RGMII phy -1 has Activity		
LEDs in J7	LINK	Green	RGMII phy -2 has Link at 1Gbps	Activity	No link on Port2
	ACT	Orange	RGMII phy -2 has Activity		
LD6	HOST	Multicolor	eUTAP mode indication[b].	—	—
LD7	TARGET	Multicolor	eUTAP mode indication[c].	—	—
LD1	PG	Green	Power Good	—	Internal power supply fail(*)
LD2	GPIO17	Orange	USER DEFINE.	USER DEFINE.	USER DEFINE.
LD4	GPIO18	Green	USER DEFINE.	USER DEFINE.	USER DEFINE.
LD5	EE1	Green	MSC8156 in Debug mode	—	MSC8156 not in Debug mode
LD3	12 V	Green	Indicates external power is ON(*) or PCI Express 12 V Power	—	The EVM is power off
(*) Critical indicator					

a. The LED does not illuminate.
b. Operates in the same way as the Transmit/Receive indicator on a USB TAP device:
The LED LD6 flashes **red** when the eUTAP is powered but has not been configured
The LED LD6 flashes **green** when the eUTAP is properly configured
The LED LD6 flashes **orange** when data is being transferred.
c. Operates in the same way as the Run/Pause Indicator indicator on a USB TAP device:
The LED LD7 is **green** when the target is running.
The LED LD7 is **red** when the target is paused.
The LED LD7 is **orange** when the target is in mixed mode.
The LED LD7 is initially unlit and remains so until the debugger is connected to the eUTAP.

2.11 Push-Buttons

Table 2-6 below describes the push-button functionality.

Table 2-6. The MSC8156EVM Push Buttons

Name and Description	Depiction	Function
SW3 Hard Reset	 HRESET	Pressing button SW3 results in a Hard Reset for the MSC8156.
SW5 Power-on-Reset	 PRESET	Pressing button SW5 results in Power-On-Reset for ***all components*** on the MSC8156EVM.
SW1 NMI (Abort)	 NMI	Pressing button SW1 results in aborting program execution by issuing a level 0 interrupt to the MSC8156. Sets pin EE0 to high.
SW4 IRQ0	 IRQ0	Pressing button SW4 results in enabling Interrupt request ‘0’ procedure

2.12 Jumpers

MSC8156EVM jumper settings are described in **Table 2-7**.

Table 2-7. Jumpers

Jumper	Name	Description
JP1	RCW SOURCE	RCW SOURCE: • When **CLOSED ON 1-2.** RCW is loaded from a reduced hard coded word (22 bit). • When **CLOSED ON 2-3**.RCW is loaded from I2C EEPROM Default setting: **CLOSED ON 2-3**

2.13 Switches

S1 is the power switch that selects the external power supply input (ON) or the PCI Express power (OFF).