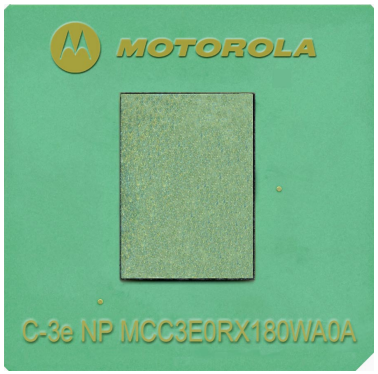
Introducing Motorola's New Network Processing Solutions



Solving the Design Challenges of Access Applications

RJG, April 2002
Motorola General Business Information, Rev 01

MOTOROLA intelligence everywhere

digital dna

Motorola's C-Port Network Processor Family

Solid Foundation of Silicon and Software

- **First generation C-5 Network Processor well established with 90+ design wins**
  - Including publicly disclosed wins at: Alcatel, Lucent, Extreme Networks, LGE, Tektronix, Atoga Systems, Empirix, Raonet, ….
- **Enhanced 5Gbps network processing solutions**
  - C-5e Network Processor
    - Most integrated, flexible, and functionally rich 5Gbps NPU for intelligent edge / access network services
  - Q-5 Traffic Management Coprocessor
    - Most comprehensive fine-grained Quality-of-Service capabilities for packet and/or cell based networks
- **Strong next generation 10G roadmap**
  - C-10 NP and Q-10 TMC for advanced high-layer applications
- **Best-in-class C-Ware Tools and Applications**

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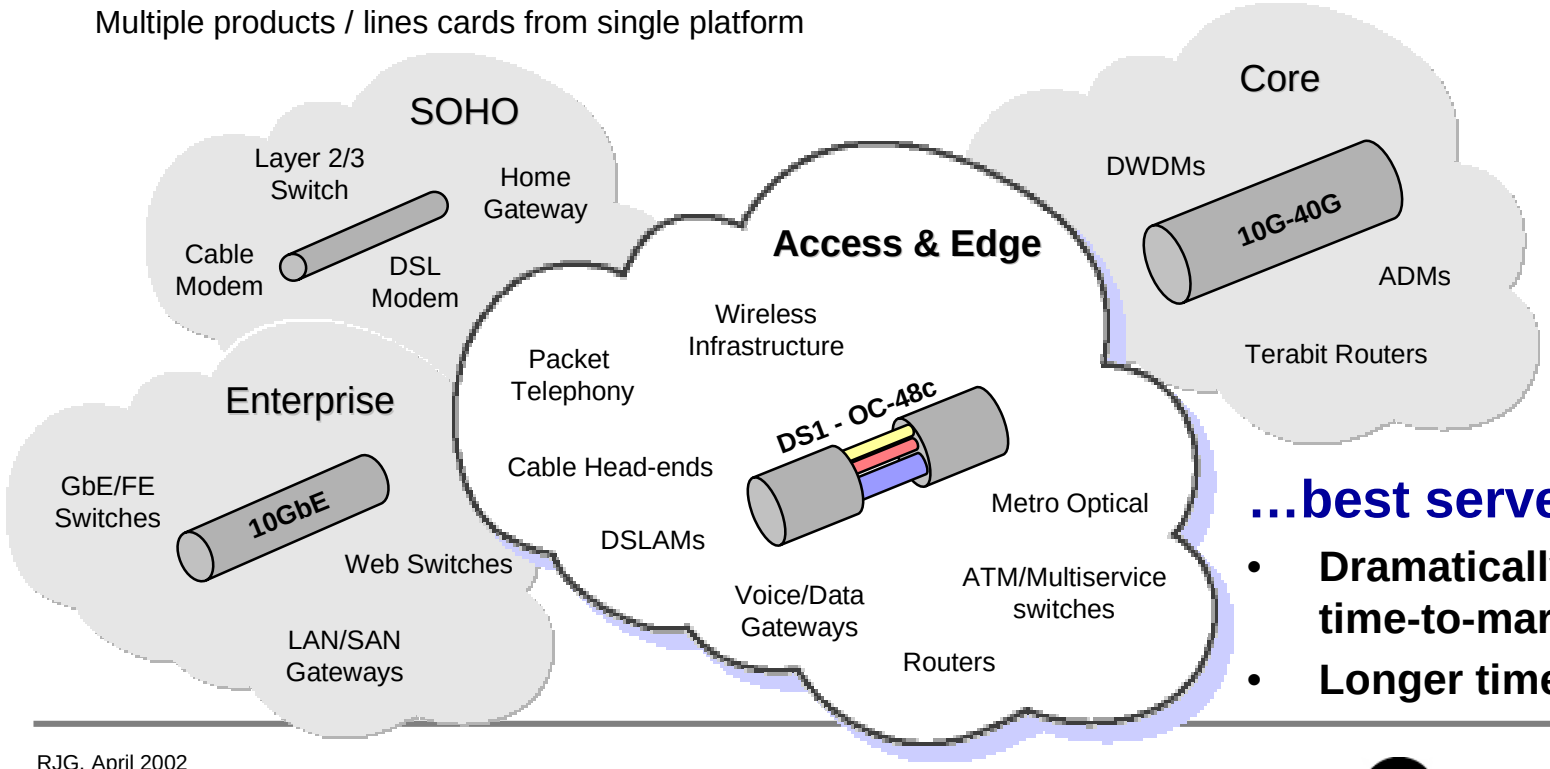
C-Port Family Network Processing Focus

Access & Edge systems differentiated by services...

- **Interfaces ranging from multi-T1 through OC-48c**
  GbE, 10/100 Ethernet, FC, OC-3c, OC-12, OC-12c, OC-48, OC-48c, T/E-x, ….etc
- **Technology discontinuity, protocol diversity**
  Advanced QoS, protocol interworking, encapsulation, tunneling, standards uncertainty, etc.
- **Delivering a "platform" for time-to-market**
  Multiple products / lines cards from single platform



…best served by NPUs

- **Dramatically improved time-to-market**
- **Longer time-in-market**

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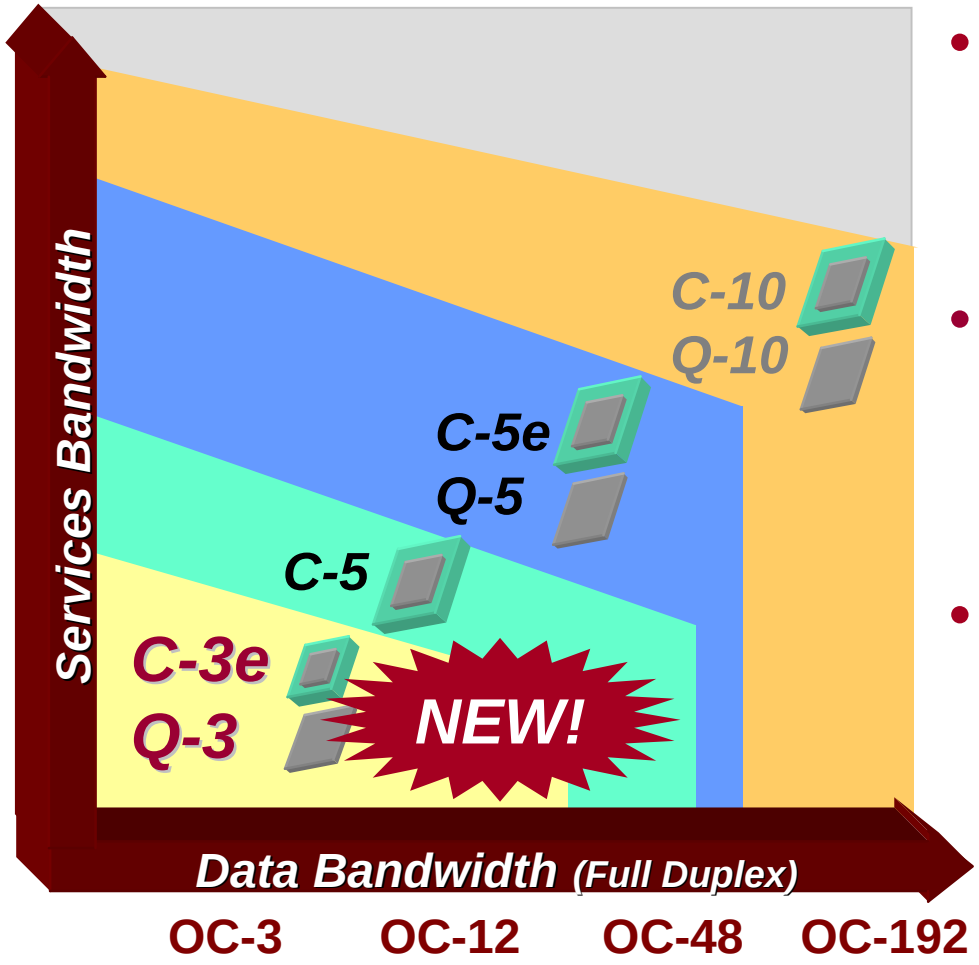
Motorola Network Processing News



- **C-3e Network Processor**
  - Most flexible, highest performance NPU aimed at access applications
- **Q-3 Traffic Management Coprocessor**
  - Extends best-in-class traffic management for IP and ATM
- **TDM Channel Adapters**
  - Extending NPU flexibility to high-density TDM applications

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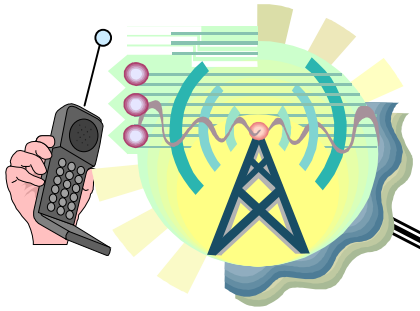
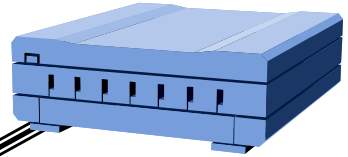
Focus on Key Access Markets



Broadband CMTS/DSLAM

Interfaces: DOCSIS, Customized Ethernet, TDM, Customized serial

Protocols: IP, Diffserv, MPLS, ATM AAL-5/AAL-2, …..



Wireless Infrastructure

Interfaces: TDM interfaces, SONET, ...

Protocols: AAL-2, AAL-2 SSSAR, AAL-5 MPE, IMA, IP, UDP, RTP, PoS, PPP, ML-PPP, …

Internet

Media Gateways

Interfaces: TDM through GbE

Protocols: IP, VoIP/RTP, ATM AAL-2/AAL-5, PoS, Proprietary, …

Multiservice Access Platforms

Interfaces: TDM, SONET, Ethernet, ...

Protocols: ATM, Frame Relay, IP, MPLS, DiffServ, PoS, …

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Access Equipment Design Challenges

System Design Requirements

- Diverse/evolving/converging interfaces and protocols
  - IP, ATM, SONET, TDM, ….
- Increasing performance
  - Demands of broadband access
- Differentiation through new services
  - SLAs, subscriber management, etc.
- Time-to- and time-in-market
  - Time-to-Market: 9 months to field trials
  - Time-in-Market: continuous enhancements
  - Design reuse and scaling
- System environment
  - Cost per bps (T1/E1/DS3/OC-X/STM-X)
  - Increasing port density per rack
  - Low power, Industrial temperature range

NPU Architecture Requirements

- Multi-protocol, multi-interface flexibility
  - Mix and match interfaces and protocols
- Scalability to ~3Gbps throughput
  - 2xOC-12c PoS, AAL-5 SARing, IP
  - High-performance AAL-2 <-> VoIP
- Application flexibility
  - True Layer 2-7 programmability
- Development productivity
  - Programmable in C/C++ with robust APIs
  - Complete software and hardware tools
  - Robust reference applications
- Cost / power efficiency
  - Advanced process technology
  - Minimal sub-system footprint

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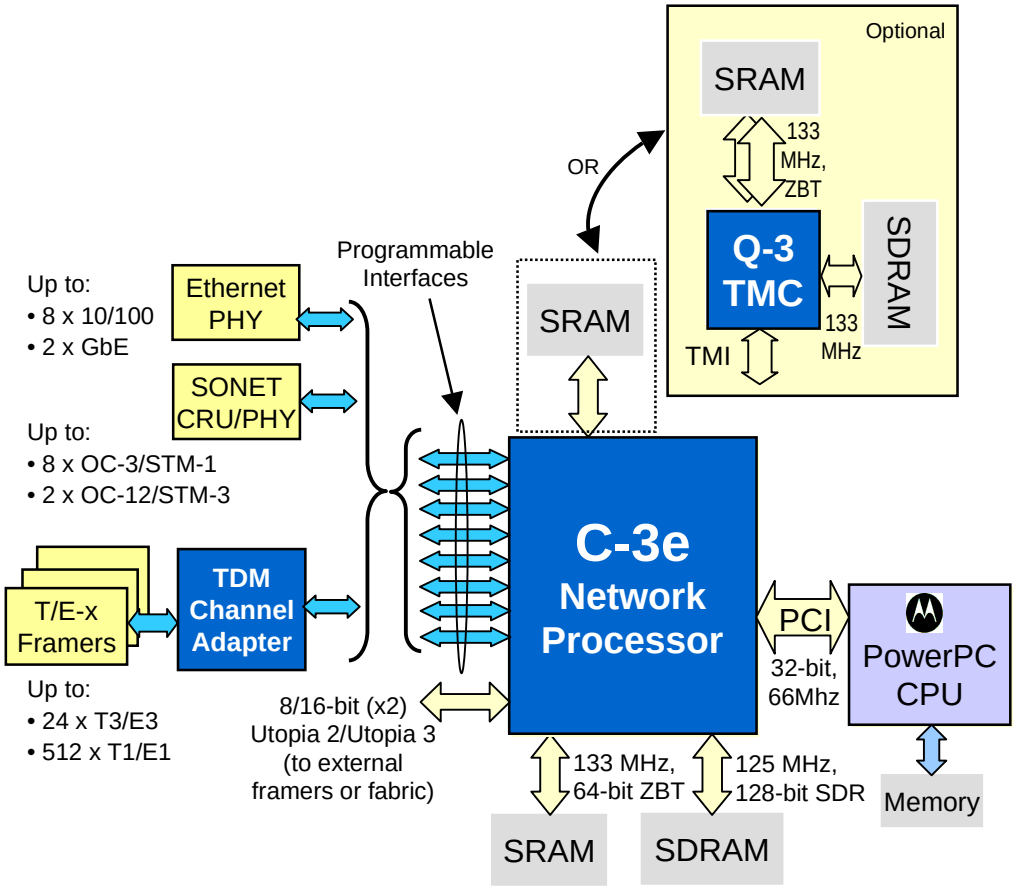
C-Port C-3e Network Processor



- **Fully programmable 3Gbps NPU**
  - **Programmable line interfaces**
  - **Integrated Ethernet MACs (10/100/1000) and SONET/SDH Framers (155/622Mbps)**
- **Complete protocol flexibility**
  - **Virtually any packet and/or ATM protocols and advanced interworking support**
- **Easy to program using C language**
  - **Fully compatible with C-5, C-5e NPs**
- **Integrated coprocessors for classification & traffic management**
  - **Example: > 46M IPv4 lookups/sec**
- **Optional Q-3 Traffic Management Coprocessor for up to 64k queues**
  - **Multi-level scheduling hierarchy**
- **Low cost & power**
  - **5.5W (typ) at 180MHz**
  - **Industrial temp range (Tj: -40C - 125C)**
  - **728 pin HiTCE CBGA package**
  - **0.15u technology**
- **Sampling Q3 '02**

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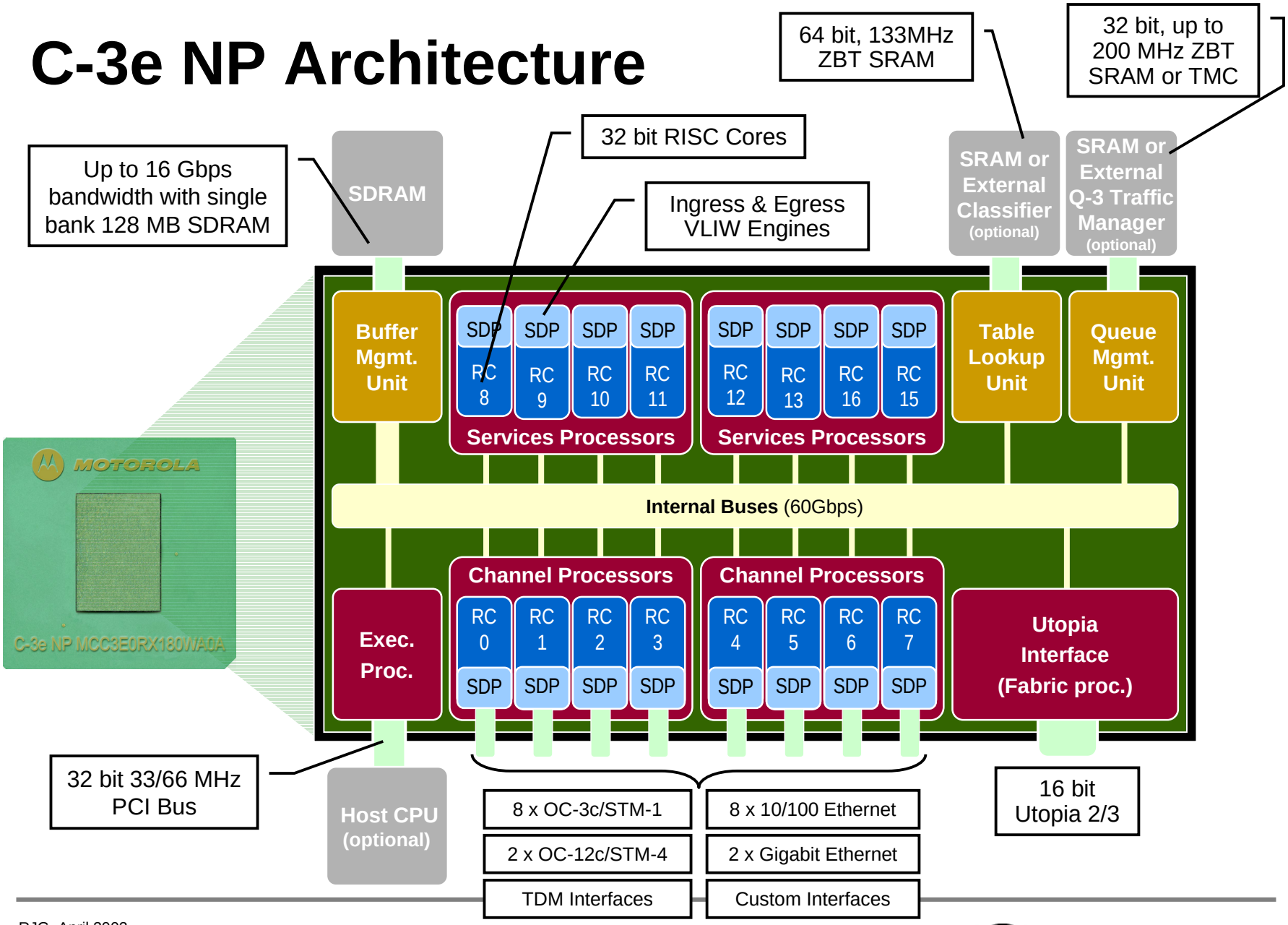
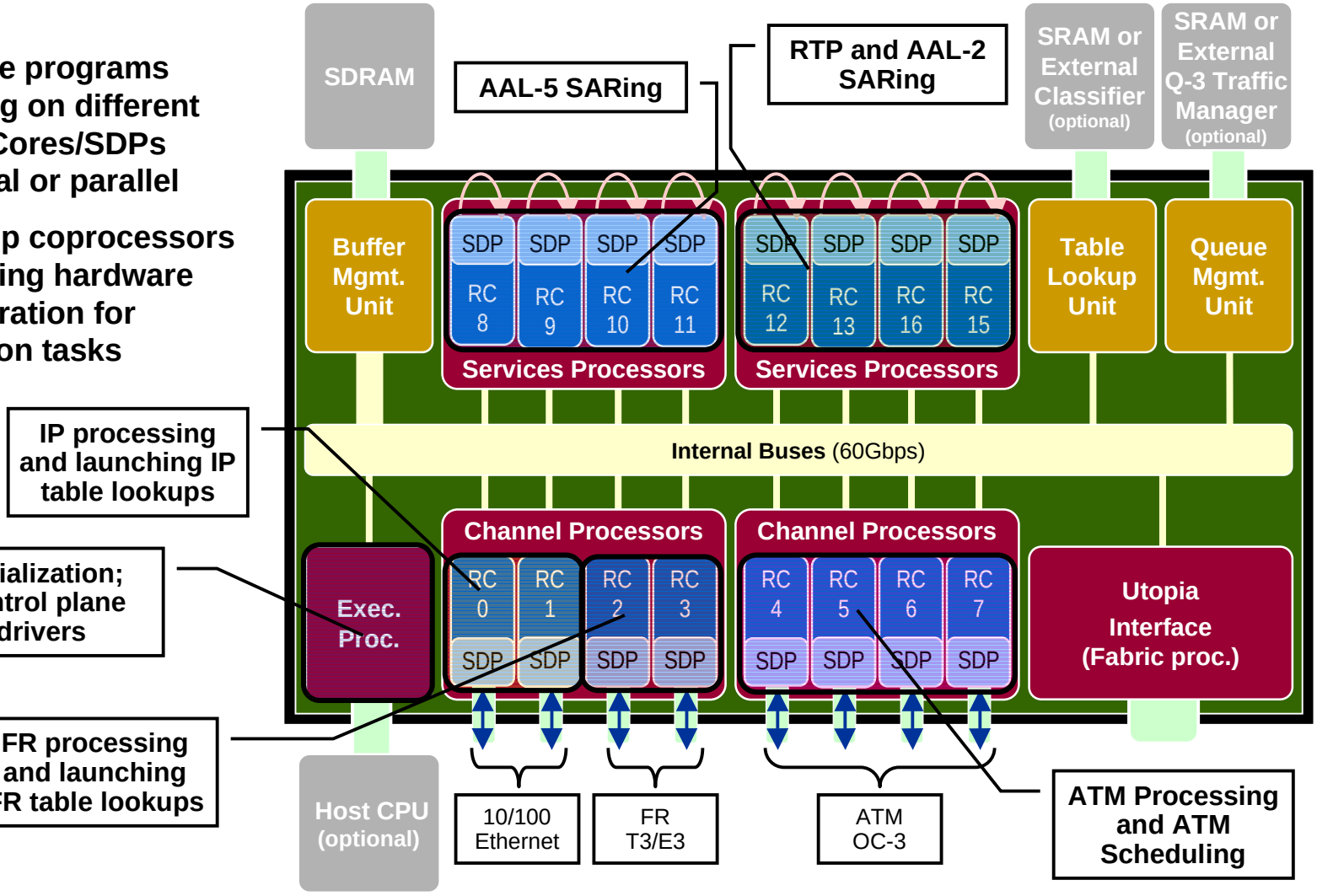
C-3e NP Architecture



Application Mapping Example

Multiservice Access Platform Line Card

- Diverse programs running on different RISC Cores/SDPs in serial or parallel
- On-chip coprocessors providing hardware acceleration for common tasks



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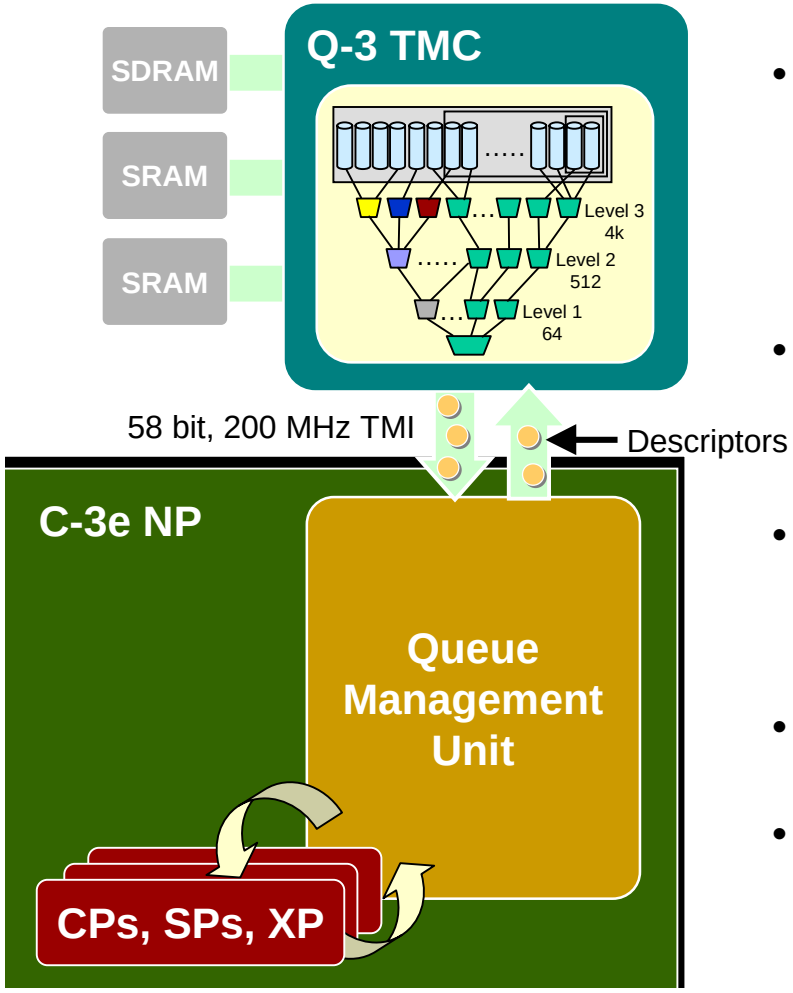
Q-3 Traffic Management Coprocessor

For Advanced, Comprehensive Quality of Service Management



- **Acceleration of advanced QoS functions**
  - Up to 64k truly independent queues with per queue policing & shaping for micro-flow QoS
  - Configurable scheduling hierarchy
  - Flexible Active Queue Management with per-queue, class, or interface congestion control
- **Scheduling for up to 4096 virtual channels**
  - Independent traffic management for individual T1/E1/Fractional interfaces, and/or subchannels on higher-speed interfaces
- **Protocol-independent performance**
  - >8M Queuing operations / sec
  - ATM and/or packet-oriented scheduling algorithms enable complex interworking services
- **Fully compatible with Q-5 TMC**
  - APIs and algorithms
- **Low power, cost effective design**
  - < 4W (typ), industrial temp range (Tj: -40C - 125C)
  - 0.13u HiP7 technology

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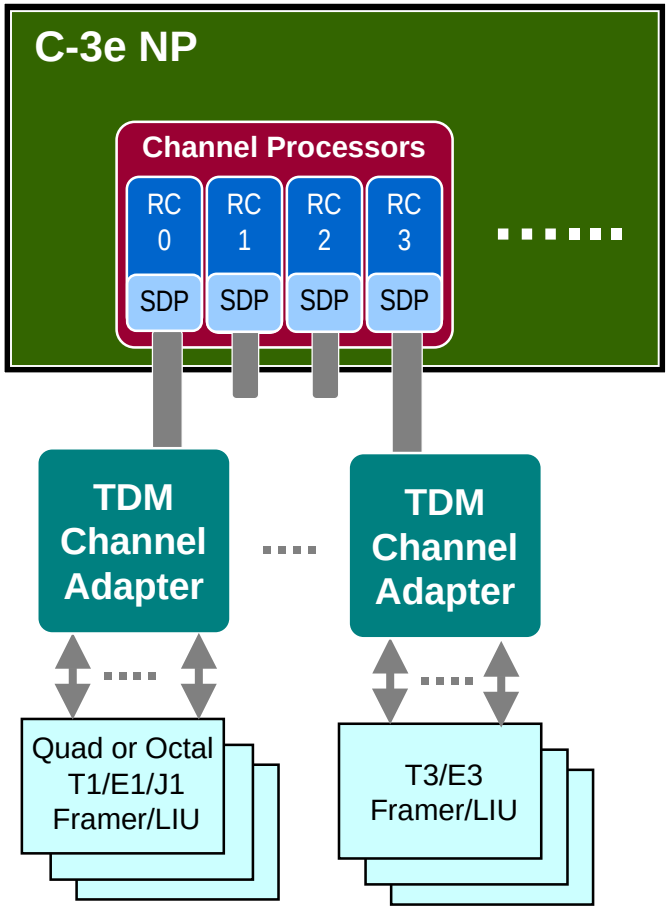
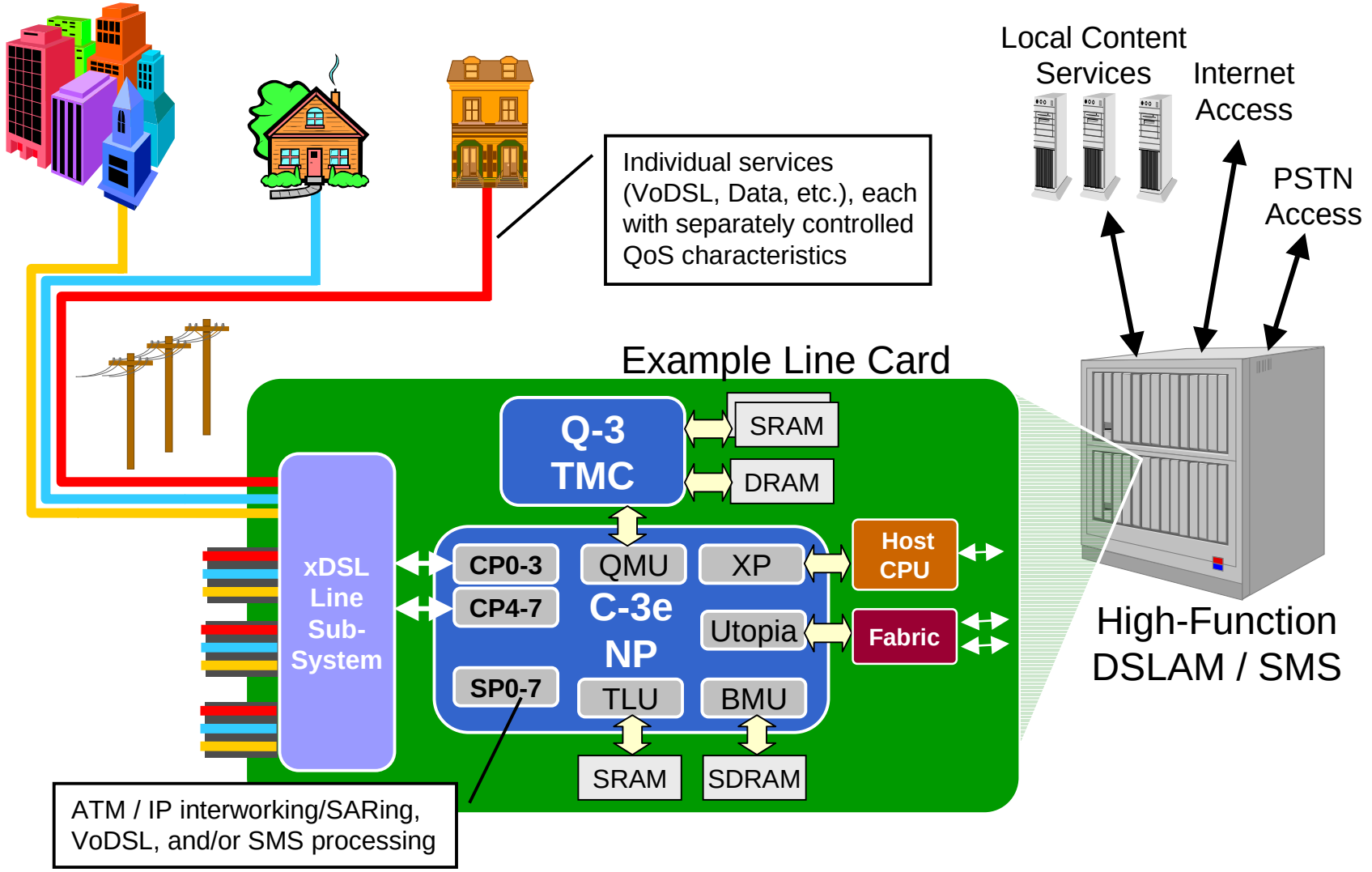
TDM Channel Adapter Technology



- Extends C-3e/C-5e interface flexibility to high-density T1/E1/T3/E3 applications
- Up to 16 x 8.192Mbps TDM or serial interfaces
  - Channelized, unchannelized, or fractional support for T1/E1/J1
  - Logical channels from 64Kbps to 2048Kbps
- Supports large number of independent HDLC and/or ATM logical channels per C-3e / C-5e Channel Processor
- Flexible interconnect options
  - Seamless interface to popular framers / LIUs
  - Direct TDM highway (MVIP / H.100) up to 128Mbps
- Low power / cost / footprint

Example: Solving xDSL Design Challenges



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Providing “Programmability Insurance” for the Network System Designer

“Motorola continues to simplify the arduous job of designing the modern network. By providing programmable devices…network designers can create systems today with no fear of what tomorrow brings. This ‘programmability insurance’ provides an extended time-in-market that allows for better infrastructure ROI in these financially thrifty times.”

-Eric Mantion, Senior Analyst,
Networking Technology for In-Stat/MDR

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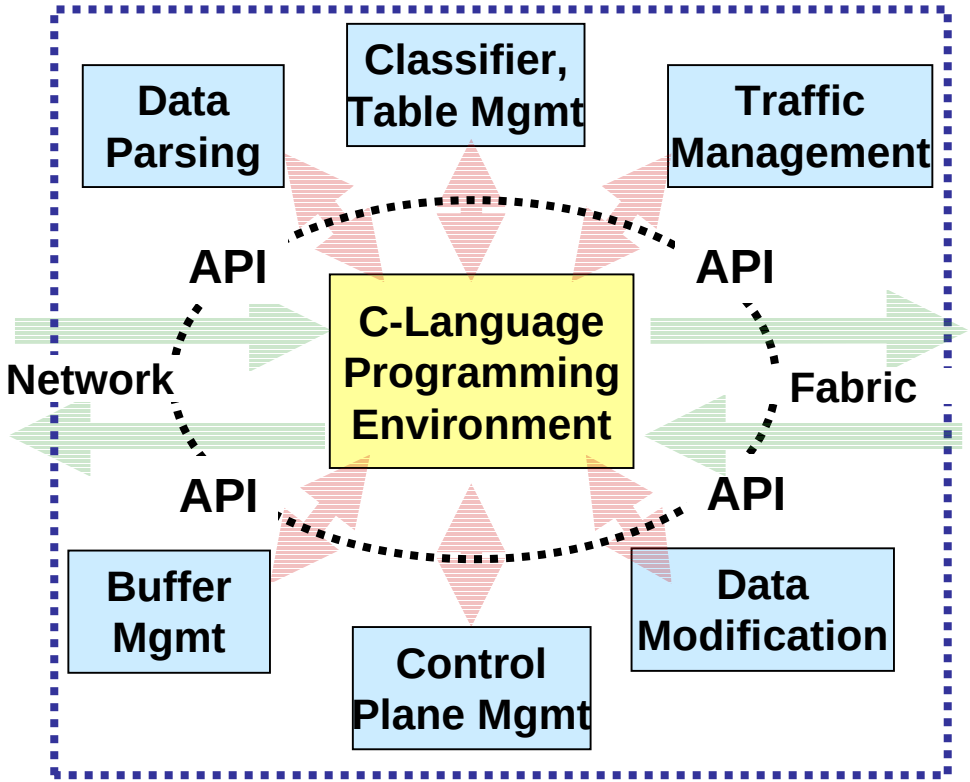
Fundamental C-Port NP Principles

Fully integrated programming model with stable API abstractions



- **Unified programming model**
  - Complete services flexibility
  - Avoids serious restrictions of flow-through pipelines
- **Stable API abstractions**
  - Ultimate in *application* scalability
  - Enables dedicated, generic coprocessing functions
  - Yields dramatically higher "programming potency"

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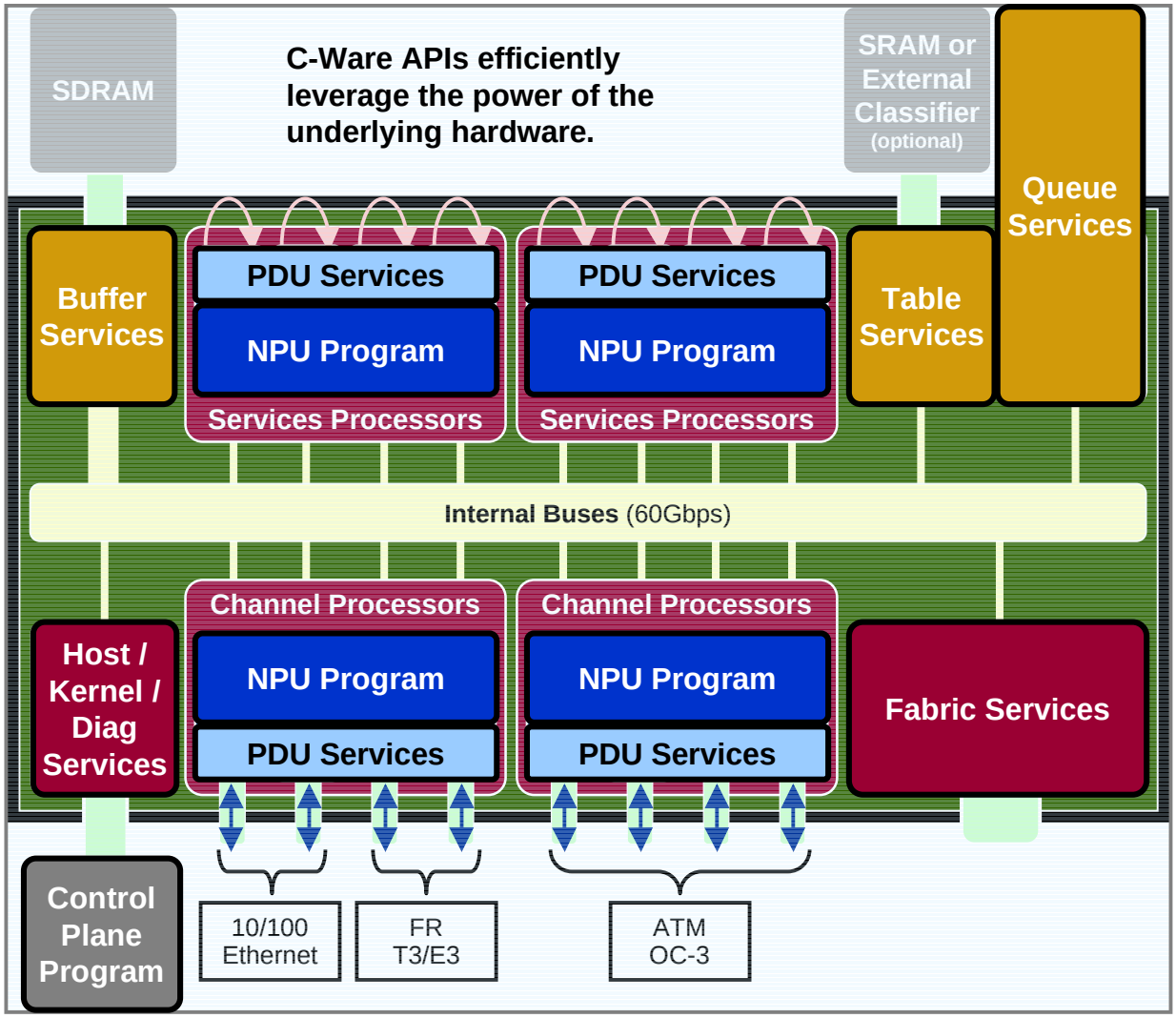
Programming a C-3e NP Application

Reference Applications and Robust APIs

C-Port Application Library:

Protocols:
- IEEE 802.1 (p, Q, etc.)
- IPv4 / IPv6
- Packet on SONET
- SONET/SDH overhead
- DiffServ; MPLS
- Frame Relay
- ATM Switching; AAL-5 SAR; AAL-2 Switching; Packet to AAL-2 SAR
- VoIP / RTP
- PPP/ML-PPP

Interfaces:
- SONET/SDH (PoS/ATM)
- 10/100 Ethernet
- GbE (optical)
- 10/100/1000BaseT
- DS-3 (serial channel)
- FibreChannel
- OC-3c / STM-1
- OC-12c / STM-4
- Utopia 2 and 3
- TDM w/adapter



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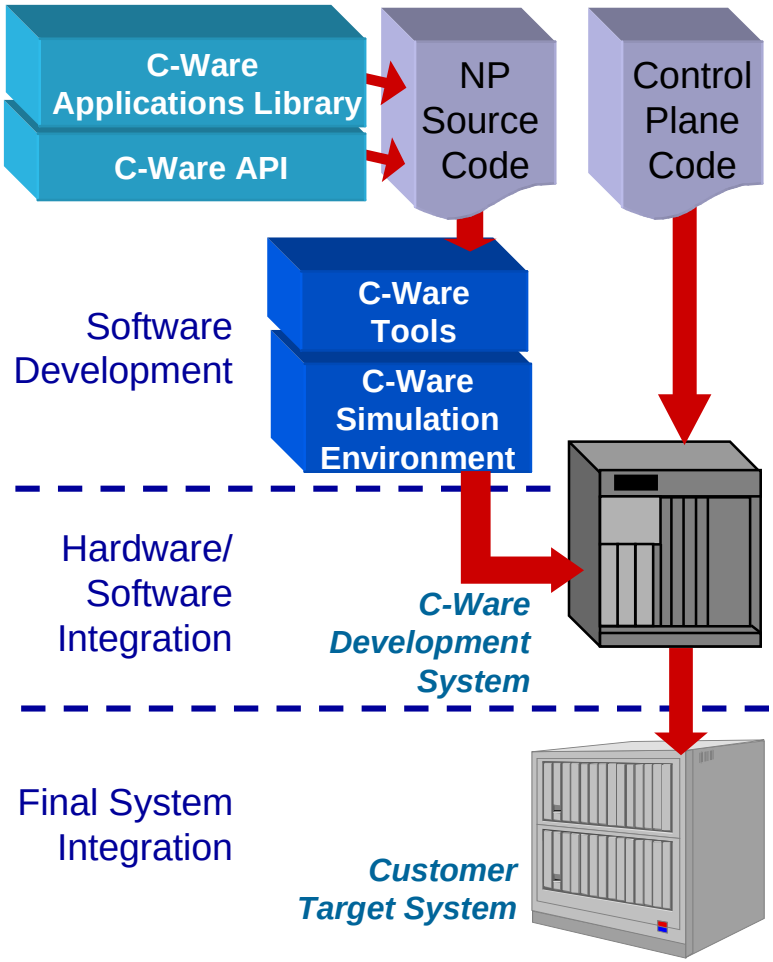
Development Environment

Powerful Toolset and Development System



- **C-Ware Simulation Environment**
  - Fast, performance-accurate simulation of all aspects of C-Port NPs, TMCs, and adapters
  - Open interfaces for system simulation creation (host, fabric, coprocessors, etc.)
- **C-Ware iPerformance Analyzer**
  - Advanced, integrated GUI, with per CP, per thread monitoring
  - Graphical C-language level debugging
- **Enhanced Compiler & Debugger**
  - Mature, GNU-based, with performance and code size optimizations
- **C-Ware APIs (forwarding & control plane)**
  - Assures source code compatibility
- **C-Ware Development System**
  - For early system integration and test
  - Includes hardware reference designs

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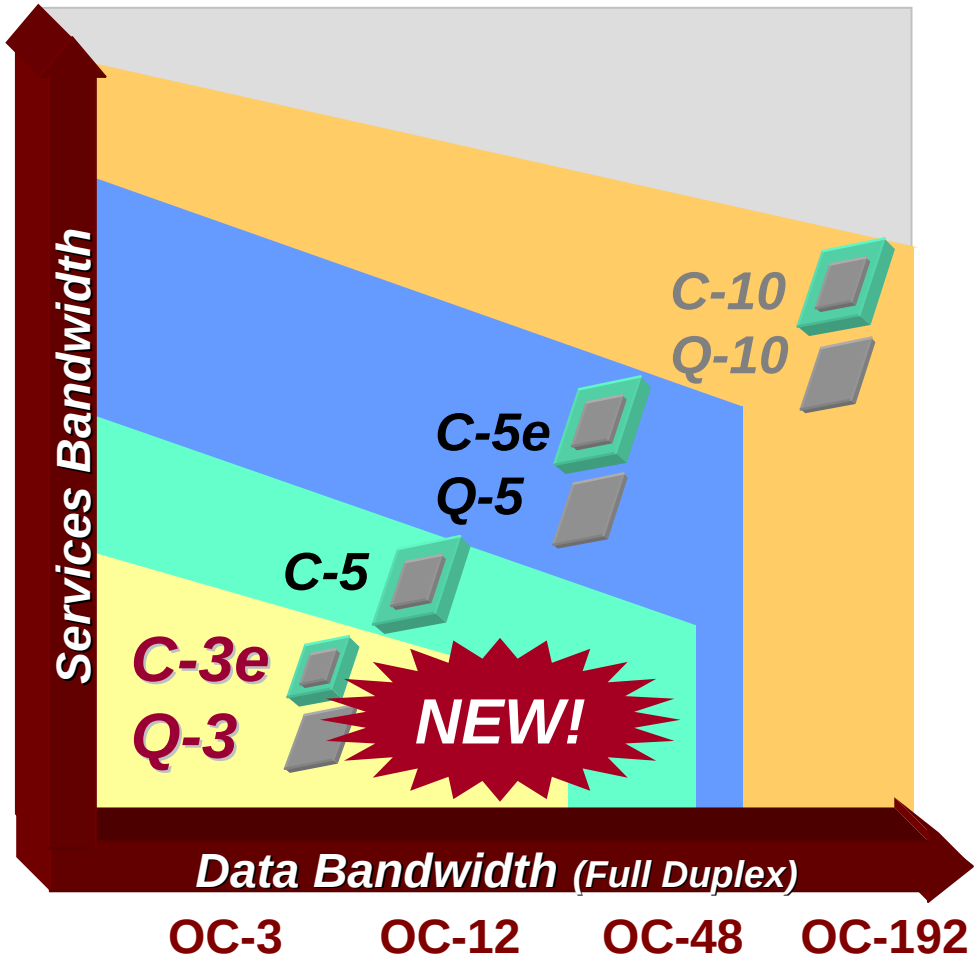
Motorola Network Processing Solutions

Enabling Intelligent Access and Edge Applications



- **C-3e Network Processor**
  - Advanced services for access and wireless infrastructure
- **C-5 / C-5e Network Processor**
  - Flexible, high-function OC-48c NP for next-generation services
- **Q-5 / Q-3 Traffic Management Coprocessors**
  - Best-in-class fine-grained QoS
- **C-10 / Q-10 Roadmap for 10G**
  - NP/TMC for true next-generation services at 10GbE and OC-192c
- **C-Ware Development Tools**
  - Optimized development productivity

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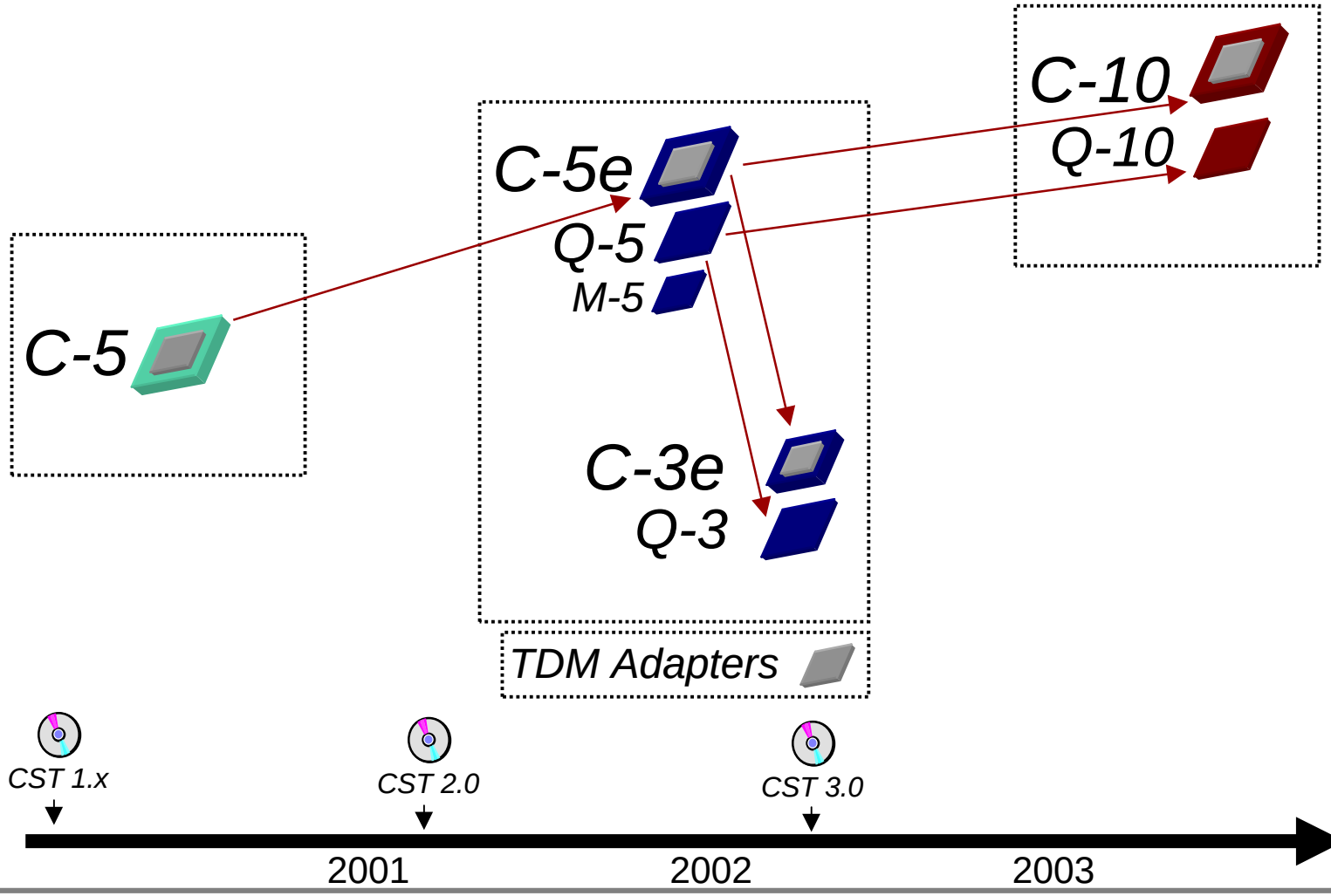
C-Port Family Silicon Roadmap



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