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Designing Wide Instantaneous Bandwidth Doherty PAs for Cellular

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The 3.5 GHz band is emerging as prime 4G and 5G spectral real estate around the globe. Radio interfaces are evolving through LTE-Advanced and LTE-Advanced Pro, raising the bar on base station power amplifier (PA) capability and performance. Instantaneous signal bandwidth is the key to a suitable solution. This article outlines the fundamentals of PA design for a symmetrical, wideband Doherty using load-pull and introduces concepts such as "Doherty friendliness" and "digital predistortion (DPD) compatibility." The design example of a wideband Doherty PA (DPA) demonstrates a solution suitable for 3.5 GHz LTE-Advanced: a two-stage LDMOS DPA delivering 6.61 W average (35 W peak) at 37 percent efficiency, with 24.5 dB gain and over 300 MHz instantaneous signal bandwidth.

The RF carrier is the virtual packhorse of the cellular network. Today's 4G LTE-Advanced network operates with the concept that a team of packhorses, in aggregate, carry a heavier burden. With LTE-Advanced Pro, the next evolutionary step in cellular network technology, multiple packhorses are tied together: some we own, some we borrow when needed. The beasts we borrow come from a shared pool, such as the Citizen's Broadband Radio Service (CBRS) spectrum.

The U.S. CBRS spectrum—3550 to 3700 MHz—is open to the public and administered via a central server for "dynamic shared use," either within a building or outdoors via small cells. Mobile network operators in the U.S. are thrilled about this new cost-effective option for LTE-Advanced network capacity expansion. In China and other leading 5G nations, the 3.5 GHz band—3400 to 3800 MHz—will become primary licensed spectral real estate for 5G.

LTE-Advanced Pro was introduced with 3GPP Release 13 and builds on LTE-Advanced from 3GPP Release 10. LTE-Advanced accommodates five simultaneous carriers, aggregating 100 MHz bandwidth. With LTE-Advance Pro, the capacity jumps to 32 simultaneous carriers, mixing licensed and shared spectrum with higher-order modulation and higher-order MIMO, using up to 640 MHz aggregate bandwidth. These capabilities push the requirement for instantaneous signal bandwidth (ISBW), the maximum modulated signal bandwidth, ever higher in the radio interface, which is particularly challenging for the RF PA (RFPA) design.

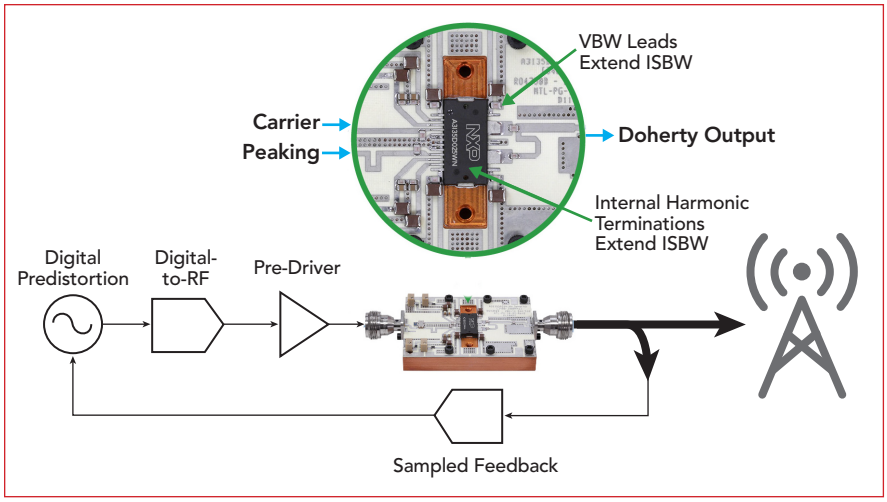

Fig. 1 **Wideband Doherty PA with DPD.**

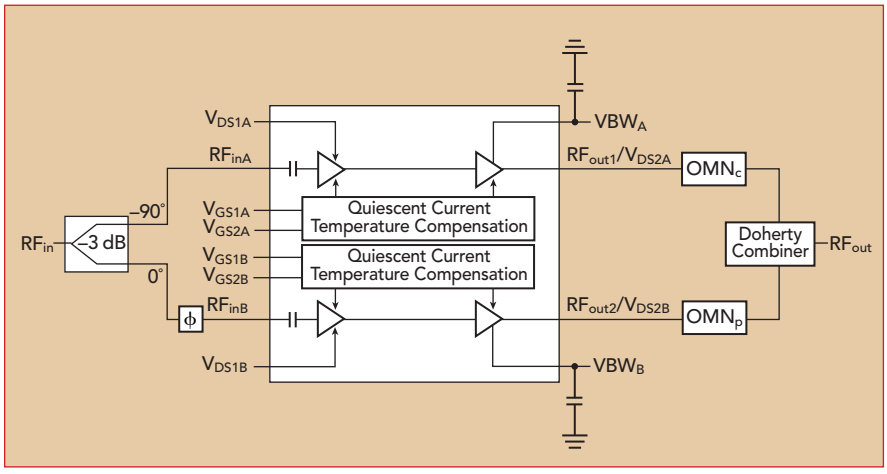

Fig. 2 **Functional block diagram of the NXP A3I35D025WN Doherty PA.**

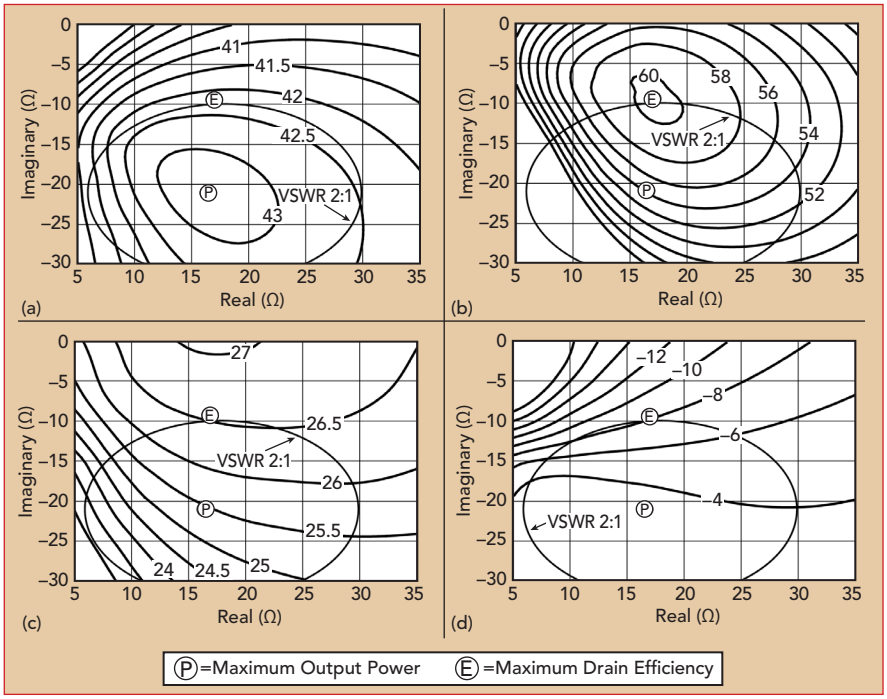

Fig. 3 **3600 MHz load-pull contours: output power (a), drain efficiency (b), gain (c) and AM/PM at 3 dB compression (d).**

RFPA technology, on its own, is unable to address the linearity requirements of LTE-Advanced over wide bandwidths. Using adaptive numerical methods, DPD provides the necessary bridge to the performance required of higher-order modulation and wider signal bandwidth. The RFPA is engineered to dovetail with the DPD system, a task that would be quite difficult if the RFPA and DPD were not designed for compatibility—a quality RFPA designers call "DPD compatibility." More on this in a bit.

The following discussion will demonstrate the fundamentals of DPA design based on a device uniquely suited for LTE-Advanced applications, a solution using NXP's A3I35D025WN, a two-stage LDMOS DPA that delivers 3.4 W average (45.2 W peak) with 34 percent efficiency, 24.5 dB gain and greater than 300 MHz instantaneous signal bandwidth (see ***Figure 1***).

DPA DESIGN

The DPA is the current topology of choice for efficient, high power RF amplifiers (see ***Figure 2***). The "trick" of the Doherty configuration is: At lower signal power, the peaking drain is in an off state and the carrier path is providing the full power gain, as efficiently as possible based on the bias. As the signal level increases, the peaking transistor turns on, changing the impedance it presents to the Doherty combining node. At full power, the carrier's performance is pulled from optimal efficiency to maximum power. However, the magic is that none of the energy used to pull the carrier drain is wasted.

The designer selects the load impedance targets for the carrier and peaking amplifiers for the two modes of Doherty operation: full power and the peaking path off. Z_{opt} reflects the full power mode, corresponding to the maximum output power, and Z_{mod} reflects the peaking off mode, corresponding to optimal efficiency. Z_{opt} is the target drain impedance at the carrier and peaking drains in full power mode. In this mode, the carrier and peaking paths combine constructively at the Doherty combining node, and the peaking output is actively load-pulling the carrier output

TABLE 1

CARRIER AND PEAKING LOAD IMPEDANCE TUNING TARGETS (GAMMA = 0.3333 < 67.7˚ BETWEEN Z_{opt} AND Z_{mod})

f (MHz)	Z_{opt} (Ω)	Z_{mod} (Ω)
3500	17.1 - j22.3	20.7 - j9.3
3600	15.0 - j21.3	15.7 - j11.0
3700	13.8 - j20.6	12.7 - j11.6

TABLE 2

RECOMMENDED A3I35D025WN DPA BIAS

Single Path	V_{dd} (V)	Stage 1		Stage 2	
		Gate Voltage (V)	Drain Quiescent Current (mA)	Gate Voltage (V)	Drain Quiescent Current (mA)
Carrier: Class AB	28	3.41	32	3.30	111
Peaking: Class C	28	2.79	0	2.52	0

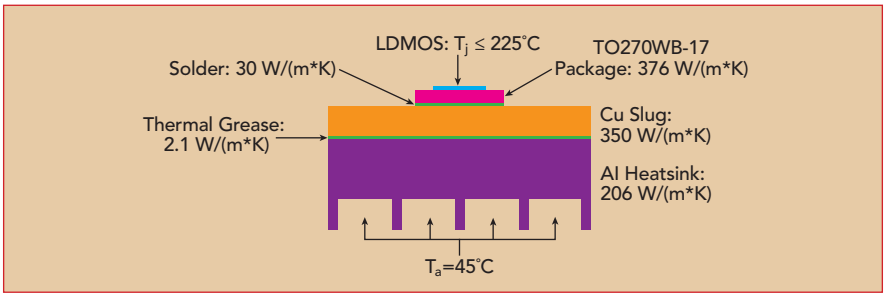

Fig. 4 **Assembly stack for thermal modeling.**

toward maximal output power. Z_{mod} is the target drain impedance at the carrier drain in the peaking off mode. In this mode, the peaking path is in its off state and should not be loading the Doherty combination node significantly.

These impedances are selected from the load-pull contours at the predefined bias settings at the band-center and band-edge frequencies (see ***Figure 3*** and ***Table 1***). Note the gamma spacing between the Z_{opt} and Z_{mod} points: |gamma| = 0.3333 or 2:1 VSWR. This spacing corresponds nicely with the 2:1 VSWR load modulation of the carrier drain with a symmetrical Doherty—the first characteristic which indicates the Doherty friendliness of the device. Also note any significant gradient in output power, efficiency, gain and AM-to-PM vs. load impedance in and around the Z_{opt} and Z_{mod} points, i.e., within 2:1 VSWR. There should be no significant gradient in load-pull contours across frequency; the lack of any significant pitch also reflects Doherty friendliness for wideband applications.

The best starting point for the optimal device bias is at or near class AB, as defined in the product datasheet (see ***Table 2***). As noted, in the Doherty configuration, the carrier amplifier will be operated in class AB and the peaking path in or near class C. Thermal tracking circuits on the A3I35D025WN DPA regulate the quiescent current over wide temperature variation, and the datasheet specifies the quiescent current accuracy over temperature, gain variation over temperature and output power variation over temperature. Consider using an off-chip temperature monitor if the datasheet specification for variation over temperature is not sufficiently precise for the target application.

ICs specifically configured to bias LDMOS Doherty circuits are available, such as TI's AMC7834 or ADI's AD7294. In addition to setting the bias, they monitor temperature, current and voltage. The key parameters to monitor and control are the carrier amplifier quiescent current, maximum channel or junction temperature and accommodating part-to-part variation in the transistor pinch-off voltage.

DPA Tuning

To optimize the performance of the DPA, the design needs to be tuned, paying attention to the following:

- The peaking leg in the off state may load the carrier output through the Doherty combiner, shifting it from the Z_{mod} target impedance. The designer needs to adjust the line length of the peaking output to present a high impedance at the combining node.
- It is much easier to tune the Doherty if the test fixture design includes provisions for separately tuning the carrier and peaking outputs to each of the target impedances.
- On combination of the carrier and peaking paths, adjust the phasing between the two paths to align constructive combination.
- Tuning requires at least a couple of iterations of fine adjustments of the output matching network, input matching network, phase alignment and the bias for optimal performance.
- If the solution falls short of expectations after several iterations of fine tuning, revisit the Doherty combiner design to see if that is limiting the performance.

ISBW

The large-ISBW of a PA is usually limited by either the video bandwidth (VBW) or the RF bandwidth of the DPA circuit. VBW is usually dominated by the drain capacitance (C_{ds}), bond wires, leadframe inductance and package parasitics, which the designer should minimize. To extend ISBW, the A3I35D025WN has special purpose pins labelled "VBW" that provide access to an internal RF "cold node" on the drain of each final stage transistor. A high-quality chip capacitor on each VBW pin provides an alternate path to RF

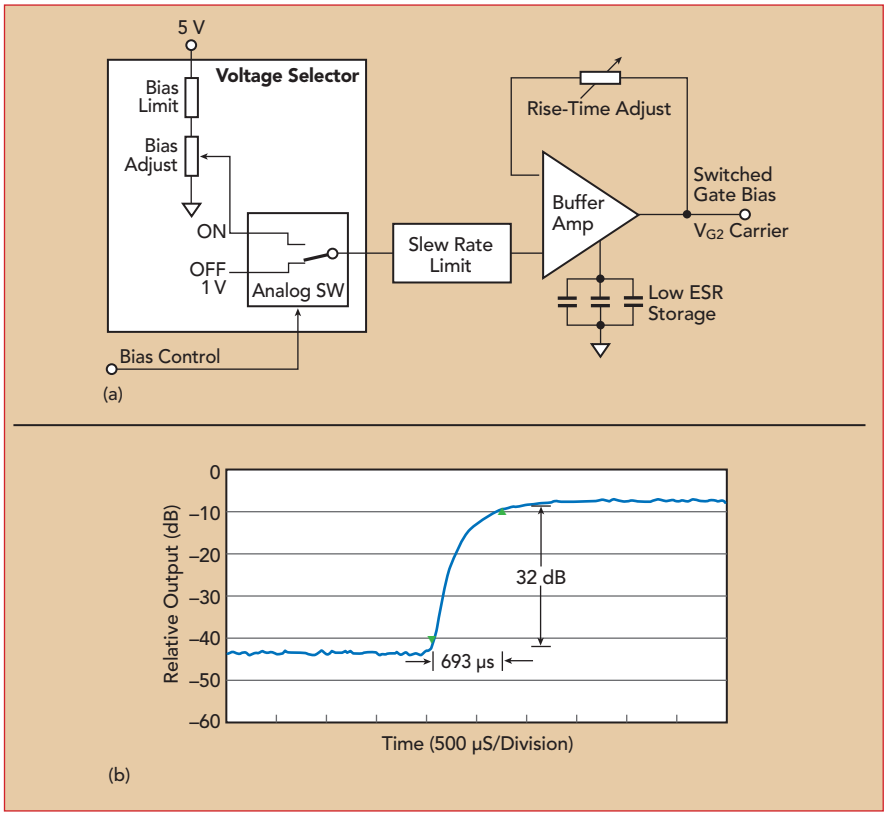

Fig. 5 Gate switching circuit (a) and output power response (b) for TDD operation.

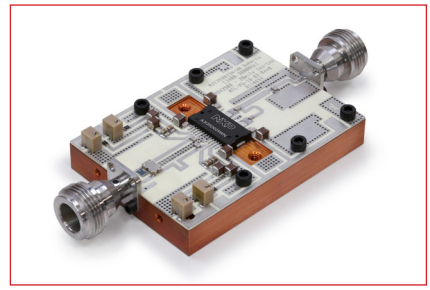

Fig. 6 A3I35D025WN PA test fixture.

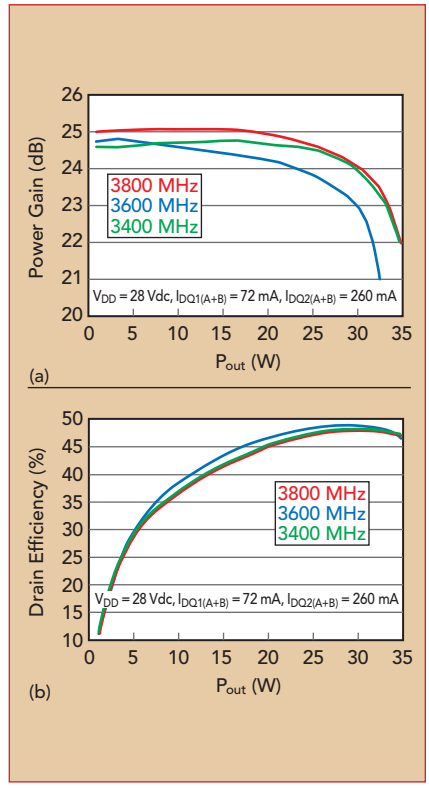

Fig. 7 Output power vs. power gain (a) and drain efficiency (b) at 3400, 3600 and 3800 MHz.

ground for the baseband currents, avoiding inductance in the prematch network or on the drain bias feed lines and pushing the drain impedance resonances beyond the baseband frequencies. For multi-stage PAs, such as the A3I35D025WN, the interstage matching networks should not limit RF bandwidth, efficiency or gain.

A topic beyond the scope of this article, but worth mentioning, is another difficulty with wideband PA design: higher-order intermodulation distortion (IMD) can produce products which fall in-band. Designs such as the A3I35D025WN mitigate IMD products with on-chip harmonic terminations.

Thermal Design

The integrity of the Doherty design should be confirmed by checking the thermal integrity and stability. The maximum operating channel or junction temperature must be comfortably below the datasheet maximum rating of 225°C, as operation at or beyond the maximum rating will degrade the mean-time-to-failure. A stack-up of thermal resistances, beginning with the DPA thermal resistance from junction to case, provides a quick check of thermal design integrity (see ***Figure 4***). The most effective means of heat conduction from the device is soldering the package bottom directly to a copper slug through a cutout in the PCB, which is at RF ground potential.

Accommodating TDD

For fastest time-division duplex (TDD) switching, the gate capacitance should be minimized to below 1 nF, adding a series resistance (~50 Ω) on the gate bias feed to dampen any overshoot on the transitions (see ***Figure 5***). On RF envelope peaks nearing transistor saturation, Schottky diode current on the gate can momentarily surge to 100 mA, so some charge storage is needed on the gate.

DESIGN VALIDATION: CBRS PA

Using the dual-stage A3I35D025WB in a symmetrical Doherty configuration, a PA was designed for TDD operation in the CBRS band (see ***Figure 6***). DPA performance with a CW input signal and without DPD is shown in ***Figure 7*** and summarized in ***Table 3***. Figure 7a shows the gain compression at 3400, 3600 and 3800 MHz, and Figure 7b shows the drain efficiency vs. output power at the same three frequencies.

Driven by two carriers, the linearity performance of the DPA at 3600 MHz, with and without DPD, is shown in ***Figure 8***. At 3600 MHz, with two, 20 MHz LTE carriers separated by 200 MHz and 7 dB peak-to-average ratio, the DPA achieves 6.61 W average power with 37.1 percent efficiency and 24.5 dB power gain. The adjacent channel leakage power is −56.8 dBc at ±20 MHz offset from the carrier, −58.6 dBc at ±40 MHz offset and −59.3 dBc at ±60 MHz offset.

The ISBW of this DPA is greater than 300 MHz, which enables it to

TABLE 3
WIDEBAND DPA PERFORMANCE W/O DPD

Frequency (MHz)	Linear Gain (dB)	Output Power at 3 dB Gain Compression (W)	Efficiency at 6 W Pout (%)	ISBW (MHz)	Supply Voltage (V)
3400	25.1	35.5	33.9	> 300	28
3600	25.4	35.5	33.5		
3800	24.7	35.5	31.8		

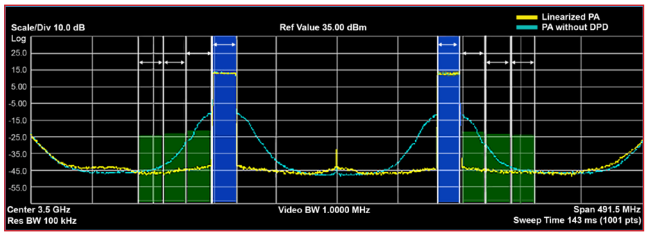

Fig. 8 **PA linearity with and without DPD.**

use DPD linearization over the full CBRS band. Depending on the DPD friendliness of the DPA, the DPD may require the output ISBW to be as much as 3 to 5× the baseband frequency to adequately sense the amplifier's dominant intermodulation products. The ISBW requirement for DPD can be relaxed somewhat if the DPA has other favorable aspects of DPD compatibility. The DPD system may be sensitive to the symmetry of the IMD products, variation in gain compression characteristics (AM-to-AM and AM-to-PM) across the tuned band and memory effects.

SUMMARY

This article discussed the design of a symmetrical, wideband DPA for the CBRS band, reviewing the fundamental theory of DPAs and covering the design approach to optimize the performance of the carrier and peaking amplifiers and the overall DPA. The importance of ISBW for wideband operation with DPD was discussed, including design approaches to maximize the ISBW and the compatibility of the device technology to DPD. Using a commercial, two-stage LDMOS MMIC from NXP, the DPA delivered 6.61 W average output power with 37 percent efficiency, 24.5 dB gain, adjacent channel leakage of −56.8 dBc at ±20 MHz offset and greater than 300 MHz instantaneous signal bandwidth—suitable for covering the full 3550 to 3700 CBRS band.■