COOPERATIVE RESEARCH PROJECTS

NXP Semiconductors Romania is engaged in the following cooperative research projects at European and National level.

- IPCEI ME/CT: SENTHICOM
- Chips JU: TRISTAN
- Chips JU: ISOLDE
- Chips JU: RIGOLETTO
- Chips JU: SHIFT2SDV

Details about these projects and collaborations can be found in the next pages. For more details, please contact respective project responsible.

Finanțat de Uniunea Europeană NextGenerationEU

Planul Național de Redresare și Reziliență

SENTHICOM – SENse, THInk and COMmunicate

IPCEI Microelectronics and Communication Technologies (IPCEI ME/CT)
State aid decision: SA.101192
Project starting date and duration: 1 April 2023, until 31-Dec-2028
NXP Romania project director: Bogdan Costinescu (bogdan.costinescu@nxp.com)
Details: https://competition-cases.ec.europa.eu/cases/SA.101192
Webpage: https://ipcei-me-ct.eu/
National contract: 3/RUE Nr.3/C9/I4 PNRR

Project Description: The scope of the SENTHICOM project is to develop breakthrough NXP products (mainly focused on SoC and associated software) in the area of Radar (aligned with WS Sense), Automotive (aligned with WS Think), and 5G/B5G/6G (aligned with WS Communicate). For each product, NXP Romania team will research, develop and innovate, together with the HW design teams in other NXP sites or with partner R&D teams, the design of the domain-specific HW accelerators and the associated firmware, drivers and middleware such that customers can focus their efforts on creating value based on their own domain expertise. The domain-specific HW accelerators allow to reduce the power consumption of the final SoC while delivering the functionality and performance required in each of the respective domains, thus being an important part of advanced silicon design.

Estimated Results: The innovative contributions expected from Romanian researchers in NXP teams and partners span (1) usage of programmable accelerators based on RISC-V cores, including novel programming approaches for these accelerators, (2) finding the right mix of hardware-supported processing with integration of already in-use middleware and applications, and (3) definition of new algorithms and methods to cope with the increased complexity of next generation radar, 5G/6G wireless communication, evolution of vehicle electronics architecture, embedded AI, safety and security

Dissemination: This section will be updated after the annual report scheduled for Feb-2025.

TRISTAN - Together for RISc-V Technology and ApplicatioNs

Horizon Europe, HORIZON-JU-IA, Project number: 101095947
Call: HORIZON-KDT-JU-2021-1-IA, Topic: HORIZON-KDT-JU-1-IA-Focus-Topic-1
Project starting date and duration: 1 December 2022, 36 months
NXP Romania project director: Bogdan Costinescu (bogdan.costinescu@nxp.com)
Details: https://cordis.europa.eu/project/id/101095947
Webpage: https://tristan-project.eu/
National contract: PN-IV-P8-8.1-PME-2024-0026

Project Description: The TRISTAN consortium aims to expand, mature and industrialize the European RISC-V ecosystem to compete with existing commercial/proprietary alternatives. This will be achieved by leveraging the Open-Source community to gain in productivity and quality. This goal will be achieved by defining a European strategy for RISC-V-based designs, including the creation of a repository of industrial quality building blocks to be used for SoC designs in different application domains (e.g. automotive, industrial, etc.). The TRISTAN approach is holistic, covering electronic design automation tools (EDA) and the full software stack. The broad 46 partner consortium will expose many engineers to RISC-V technology, further strengthening adoption. This ecosystem will ensure a European sovereign alternative to existing commercial/proprietary players. The consortium, which includes the largest EU companies and globally operating semiconductor IDMs, is convinced that once solutions using RISC-V building blocks are well verified, the industry will feel sufficiently confident to make the investments necessary for tape-outs.

Estimated Results: TRISTAN'S overarching aim is to expand, mature and industrialize the European RISC-V ecosystem to compete with existing commercial alternatives. Building blocks developed in TRISTAN will be demonstrated in the business domains of Automotive, Industrial, Aerospace, Mobile, Wearables and Health. The objective is to reach TRL-5 for the TRISTAN building blocks enabling further industrial adaptation into commercial applications.

Dissemination:

1. "*RISC-V Extension Enablement*", Simona Costinescu, presentation during TRISTAN Technical Conference, 11-Sep-2024 (link).
2. "*ADL Tools to generate LLVM target description files and tests*", ADL-Tools project in GitHub, documentation and codebase available at https://github.com/nxp-auto-tools/tools_adl
3. "*TRISTAN & ISOLDE Chips-JU RISC -V Projects*", by Catalin Bogdan Ciobanu, Holger Schmidt, Wolfgang Ecker, Rob Wullems, Patrick Pype, Tiberio Fanti, Dominik Baumann, Alexandru Puscasu, Mihai Gologanu, Razvan Stancu, Octavian Buiu, Sven Mehlhop, Joerg Walter, Gianvito Urgese, Michelangelo Barocci, Tommaso Terzano, Guido Masera, Maurizio Martina, George Suciu, Mari-Anais Sachian, Nicoleta Capbun, Alexandru Sneapota, Calin Zamfir, Anca Burlacu-Zane, Simona Costinescu, Ambily Suresh, Diego Gigena-Ivanovich, Honorius Galmeanu, Mihai Munteanu, Alexandru Drambarean, Darshak Sheladiya, Jan Reinhard, Florian Krebs, David Engraf, Holger Blasum, Mattia Paladino, Daniele Gregori, Federico Proverbio, Jan

Kastil, Pavel Zaykov, Alexander Schober, Rainer Buchty, Mladen Berekovic, Amrit Sharma Poudel, Lukas Groth, Saleh Mulhem, Emanuele Valpreda, Andrea Zunino, Luigi Feola, Samuel Matea, Cosmin Moisa, Andrei Stan, Alexandru-Tudor Popovici, George Iulian Uleru, Cristian-Tiberius Axinte, Cosmin-Andrei Popovici, Daniel Gracia Pérez, Sylvain Girbal, Jerome Quévremont, André Sintzoff, Angelo Garofalo, Alessandro Nadalini, Fatma Jebali, Aaliph Andriamisaina, Florian Egert, Maurizio Capra, Alessandro Aimar, Valerio Venceslai, Francesco De Maldé, Maria Elena D'Agostino, Gabriele Magnani, Davide Baroffio, Andrea Galimberti, Carlo Brandolese, Giancarlo Storti Gajani, Costin-Emanuel Vasile, Vlad Gabriel Serbu, Alexandra-Mihaela Enescu, Radu Hobincu, Calin Bira, Elijah Seth Cishugi and Marco Ottavi; Presented during International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS) 2025 conference, Jun-28-2025 - 3-Jul-2025

4. RISC-V Technology Challenges for Tools – by Ana Maria Staicu, Razvan Ionescu, Mihai-Dan Apostu, Calin Zamfir - presentation to Transilvania University of Brasov - Electronics and Computers Department (Faculty of Electrical Engineering and Computer Science) - Master class – Brasov 12th of May 2025

5. RISC-V Technology Challenges for Tools – by Ana Maria Staicu, Aida Dinca, Razvan Ionescu, Adrian-Sebastian Grigoroiu, Alexandru Sneapota, Calin Zamfir - presentation to University Politehnica Bucharest - Computer Science and Engineering Department (Faculty of Automatic Control and Computers) - Year 3 Course – 10th of November 2025

6. RISC-V Technology Challenges for Tools – by Ana Maria Staicu, Aida Dinca, Razvan Ionescu, Adrian-Sebastian Grigoroiu, Calin Zamfir - presentation to University Politehnica Bucharest - Automatic Control and Systems Engineering Department (Faculty of Automatic Control and Computers) - Year 3 Course – 12th of November 2025

7. TRISTAN Consortium meeting - RISC-V ecosystem – WP6 progress status presentations - RISC-V Debugger support enablement and Semihosting demonstrated on FPGA and Instruction Set Simulator – Ana Maria Staicu - Istanbul 18&19 November 2025

ISOLDE - High Performance, Safe, Secure, Open-Source Leveraged RISC-V Domain-Specific Ecosystems

Horizon Europe, HORIZON-JU-IA, Project number: 101112274
Call: HORIZON-KDT-JU-2022-1-IA, Topic: HORIZON-KDT-JU-2022-1-IA-Focus-Topic-3
Project starting date and duration: 1 May 2023, 36 months
NXP Romania project director: Bogdan Costinescu (bogdan.costinescu@nxp.com)
Details: https://cordis.europa.eu/project/id/101112274
Webpage: https://www.isolde-project.eu/
National contract: PN-IV-P8-8.1-PME-2024-0025

Project Description: The ISOLDE project aims to significantly support the digital transformation of all economic and societal sectors, to speed up the transition towards a green, climate neutral and digital Europe, to strengthen the design capacity and to achieving digital autonomy EU wide. By the end of our project, we will have high performance RISC-V processing systems and platforms at least at TRL 7 for the vast majority of building blocks, demonstrated for key European application domains such as automotive, space and IoT with the expectation that two years after completion ISOLDE's high performance components will be used in industrial quality products. To achieve such an ambitious goal, an industrial-grade open-source support for development, verification, and maintenance will be provided. The customizable IPs will be hosted on physically located European servers to address the European digital sovereignty requirement that the ISOLDE project will support. This way, ISOLDE will have delivered a major contribution to the unification and focus of the full-fledged – industry-supported – eco-system for RISC-V open-source architecture, especially in the area of embedded high-performance computing, and thus to the creation of a breakthrough design capacity across the EU microelectronics industry.

Estimated Results: ISOLDE'S overarching aim is to expand, mature, industrialize and make available the European high-performance RISC-V ecosystem so that it is able to compete with existing commercial/ proprietary alternatives.
This will be achieved by exploring and implementing advanced architectures and in addition by providing novel accelerators as well as IPs to complete the high-performance compute infrastructure based on inputs of partners that cover the entire value chain.
Further, this goal will be supported by following and contributing to specifications from suitable industrial bodies and to Europe's long term strategy for RISC-V based ecosystem including the creation of a repository of industrial quality building blocks to be used for SoC designs in different application domains (e.g. automotive, industrial, etc.).
The ISOLDE approach is holistic, includes all players along the value chain covering also electronic design automation tools (EDA) and the full software stack. The broad industrial guided consortium will expose a large number of engineers to RISC-V technology, which will further strengthen adoption. This ecosystem will ensure a European sovereign alternative to existing commercial/proprietary players.

Dissemination:

1. "*RISC-V Accelerators, Enablement and Applications for Automotive and Smart Home in the ISOLDE Project*", Cătălin Bogdan Ciobanu, Honorius Gâlmeanu, Alexandru Puscas, Mihai Gologanu, Octavian Buiu, Mihai Antonescu, Vlad-Gabriel Serbu, et al., presented during International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS) 2024 conference, 3-Jul-2024 (link).
2. ISOLDE Project Meeting in Bucharest, Simona Costinescu, 17-18-Jul-2024 (link).
3. "*Contributions of Romanian ISOLDE Cluster: RISC-V Accelerators, Enablement and Applications for Automotive and Smart Home*", Bogdan Costinescu, Cătălin Ciobanu, presented during workshop organized by the STMS Commission of the Academy in collaboration with the Romanian Section of IEEE on 1-Oct-2024.
4. "*Efficient OpenMP Target Offloading for Bare-Metal Embedded System*", article abstract submitted to Embedded World 2025.
5. "*Using reconfigurable hardware in the ISOLDE RISC-V CHIPS-JU project*", by Catalin Ciobanu IMT, RO, & others; presented at RAW 2025, 03-04 Jun 2025 Milano, Italy

RIGOLETTO - RISC-V GENERATION OF HIGH PERFORMANCE AUTOMOTIVE PROCESSORS AND COMPUTING PLATFORMS

Horizon Europe, HORIZON-JU-IA, Project number: 101194371
Call: HORIZON-KDT-JU-2024-1-IA, Topic: HORIZON-JU-Chips-2024-1-IA-T2
Project starting date and duration: July 2025, 36 months
NXP Romania project director: Bogdan Costinescu (bogdan.costinescu@nxp.com)
Details: https://cordis.europa.eu/project/id/101194371
Webpage: -
National contract: PN4-P8-1106/31.10.2025

Project Description: Electrification, autonomy, and digital technologies are driving rapid innovation in electric vehicles, but today's decentralized ECU architecture cannot keep pace with growing complexity. The EU-funded Rigoletto project will pioneer a next-generation automotive hardware platform based on the RISC-V ISA, supporting Europe's move toward centralized E/E architectures and the consolidation of ECUs into DCUs and ZCUs.

Estimated Results: RIGOLETTO focuses on creating a next-generation automotive hardware platform based on the open RISC-V instruction set architecture. The project develops scalable 32- and 64-bit automotive control processors with strong safety, security, and real-time capabilities. It also delivers high-performance application processors featuring out-of-order execution, hypervisor support, memory encryption, and post-quantum cryptography accelerators. A major goal is to design diverse AI/ML accelerators, including heterogeneous architectures, neuromorphic solutions, and systolic arrays. These components will be integrated into a unified automotive computing platform to support centralized E/E architectures. RIGOLETTO provides a comprehensive toolchain for EDA, compilers, deployment, AI/ML code generation, benchmarking, and safety/security evaluation. The project involves leading European IDMs, Tier 1 suppliers, academia, and research institutes, ensuring strong collaboration and standardization. By leveraging the flexibility of RISC-V, RIGOLETTO strengthens Europe's position in software-defined vehicles and automotive electronics. It aligns with EU Chips Joint Undertaking and the Vehicle of the Future initiative to promote digital sovereignty. Ultimately, RIGOLETTO lays the foundation for electrified, automated, and connected vehicles through innovative hardware and software ecosystems.

Shift2SDV - a common Software development framework and hardware independent microservice-oriented middleware architecture for the stepwise migration to the Software Defined Vehicle of the Future

Horizon Europe, HORIZON-JU-IA, Project number: 101194245
Call: HORIZON-JU-Chips-2024-1-IA, Topic: HORIZON-JU-Chips-2024-1-IA-T3
Project starting date and duration: July 2025, 36 months
NXP Romania project director: Bogdan Costinescu (bogdan.costinescu@nxp.com)
Details: https://cordis.europa.eu/project/id/101194245
Webpage: -
National contract: PN4-P8-1107/31.10.2025

Project Description: Middleware services connect applications, enabling seamless communication and data exchange, both of which are vital for the European automotive sector. The EU-funded Shift2SDV project will create a Software Defined Vehicle (SDV) ecosystem using a middleware and API framework to enhance collaboration in the automotive sector. By developing a modular framework with microservices, the project will address the limitations of current systems, ensuring compatibility with both in-vehicle and cloud technologies. Key goals include establishing a secure architecture, simplifying application development, and integrating edge computing. Through effective communication and collaboration, the project seeks to bolster European leadership in SDVs and drive innovation in the automotive industry.

Estimated Results: The Shift2SDV project aims to revolutionize the European automotive domain by creating an SDV ecosystem around middleware & API framework enabling collaboration across the automotive value chain. This ambitious endeavor envisions a comprehensive shift towards a modular framework that transcends the limitations of current monolithic systems, fostering agility and innovation through the development of complementary middleware services and software development solutions.

Central to Shift2SDV is the development of a cutting-edge middleware framework that provides micro-services to build automotive applications upon, abstracting from underlying hardware components – supporting stepwise migration, open source and proprietary components, in-vehicle safety critical and off-vehicle cloud functionality. It is specifically designed to streamline software development and integration while ensuring compatibility and flexibility with existing and emerging technologies.

Key technical objectives include the development of a modern, flexible micro-services-based architecture, middleware framework that simplifies the brand-specific application development, and establishment of a safe and secure system architecture compliant with functional safety standards. Additionally, the project aims to develop an orchestration for efficient resource management, integrate edge and cloud computing, and demonstrate the practical viability of the developed middleware through concrete use cases.

To maximize impact, Shift2SDV prioritizes active communication, dissemination, and exploitation of project outcomes, fostering collaboration among stakeholders and existing projects and initiatives aligning technological advancements with market demands. Through these concerted efforts, Shift2SDV seeks to propel European leadership in Software Defined Vehicles, driving innovation and economic growth in the automotive industry.