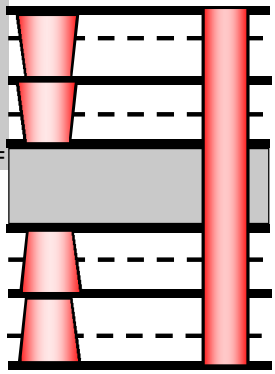
Build Up HDI

HDI 06 — **6 - Layers**

WE-Articel No.: — **2 + 2 + 2**

Customer: **Artemis** NXH3770 SDK

layer description		configuration	Raw-Material	CU	PREPREG	Dielectric constant	Final Thickness	Customer requirements
Customer	WE					[εr]	[µm]	[µm]
	TOP/VS	S1 S2	Foil	12 µm	1)		12	
					1 X 1080	3.5	68	
	2	GND	Foil	12 µm			30	
					1 X 2116	3.8	100	
	3	SIG REF		35 µm			33	
			0.930 mm			5.1	930	
	4	PWR		35 µm			33	
					1 X 2116	3.8	108	
	5	GND	Foil	12 µm			30	
					1 X 1080	3.5	68	
	BOT/RS	S	Foil	12 µm	1)		12	



Material: lowCTE Tg.150° hf

1) copper thickness outer layers: appr. 50 µm

Impedance Calculation:

S1 Zo 50 Ohm @ 109 µm Track Width

S1 Zdiff 90 Ohm @ 100 / 132 / 100 µm

OR **S1 Zdiff 90 Ohm @ 120 / 228 / 120 µm**

S2 Zo 50 Ohm @ 373 µm Track Width

S2 Zo Coplanar 50 Ohm @ 248 µm track width
120 µm Distance to Gnd

OR **S2 Zo Coplanar 50 Ohm @ 282 µm track width**
150 µm Distance to Gnd

total material thickness: 1424

Note: Lamination thickness for Prepregs depending on layout characteristics.

final lamination thickness:	**1,42**	+/-	**0,14**	mm			Date:	Engineer:
thickness with electro plated Cu:	1,50	+/-	**0,15**	mm			**07.12.2016**	**Muniyappa**
total thickness with soldermask	1,56	+/-	**0,16**	mm				
customer requirement	**1,60**	+/-		mm	point:			

prepared: on	by	checked: on	by	approved: on	by	revision		page:	
		07.12.2016	P. Reeb			00			