P1020-WLAN

Hardware User Guide

P1020-WLANUG
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Federal Communications Commission Radio Frequency Interference Statement

This device complies with Part 15 of the FCC rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference and

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—Reorient or relocate the receiving antenna.

—Increase the separation between the equipment and receiver.

—Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

—Consult the dealer or an experienced radio/TV technician for help.

Reminding

1. The installed antennas must not be located in a manner that allows exposure of the general population at a distance of less than 23cm.
2. Mount the antennas in a manner that prevents any personnel from entering the area within 23cm from the central position of the antenna.

This device has been designed to operate with the attached antennas, and having a maximum gain of 2.5dBi. Antennas not identical as that or having a gain greater than 2.5dBi are strictly prohibited for use with this device. The required antenna impedance is 50 ohms.
To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that permitted for successful communication.

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About This Book

This document describes the system architecture, board-level functions, external connections, and software features for the P1020-WLAN board. It provides guidance for operating this product, making it easy for the user to connect with the outside world. The first half of this book explains board and functions while the latter part of the book focuses on mechanical aspects.

Audience

The audience of this manual are the end users who want to know the architecture of the platform and detailed hardware configuration, or the engineer who want to acquire more design reference from the system. It is assumed that the reader understands operating systems, microprocessor system design, and the basic principles of RISC processing.

Organization

This book is divided into the following chapters:

- Chapter 1, Introduction - provides a high-level description of features and block diagram of the P1020-WLAN board.
- Chapter 2, P1020-WLAN Board - describes the board in terms of its hardware: board-level functions, connectors, configurations, and board mechanical data.
- Chapter 3, Board Bootup - describes the board settings and physical connections needed to boot the P1020-WLAN board.
- Chapter 4, P1020-WLAN Software - describes the main software features of P1020-WLAN board
- Chapter 5, Unit Assembly - provides an instruction for enclosure and peripherals assembly.

Suggested Reading

This section lists additional reading that provides background for the information in this manual as well as general information about the architecture.

The following are the reference used to produce this book:

- *P1020 QorIQ™ Integrated Processor Hardware Specifications*
- *P1020 QorIQ™ Integrated Processor Reference Manual*

Acronyms and Abbreviations

Table i contains acronyms and abbreviations used in this document.

Table i. Acronyms and Abbreviated Terms

Term	Meaning
NAS	Network-Attached Storage
RAID	Redundant Array of Inexpensive Disks
CPU	Central Processing Unit

Table i. Acronyms and Abbreviated Terms (continued)

Term	Meaning
PoE	Power over Ethernet
DDR2 SDRAM	Double-Data-Rate Two Synchronous Dynamic Random Access Memory
NOR Flash	Nor Gare Flash
eTSEC	Enhanced Three-Speed Ethernet Controller
RGMII	Reduced Gigabit Media Independent Interface
WAN	Wide Area Network
LAN	Local Area Network
USB	Univeral Serial Bus
ULPI	USB Low-Pin Count Interface
SATA	Serial Advanced Technology Attachment (Computer Bus)
PCI	Peripheral Component Interconnect (Computer Bus)
PCI-E	Peripheral Component Interconnect Express (Computer Bus)
SDHC	Secure Digital High Capacity (SD 2.0 Memory Card)
I^2C	Inter-Integrated Circuit (Computer Bus)
EEPROM	Electrically Erasable Programmable Read-Only Memory
JTAG	Joint Test Action Group
UART	Universal asynchronous receiver/transmitter
DHCP	Dynamic Host Configuration Protocol
DNS	Domain Name System
VLAN	Virtual Local Area Networks
NAT	Network Address Translation
PAT	Port Address Translation
RIP	Routing Information Protocol
VRRP	Virtual Router Redundancy Protocol
PPPoE	Point-to-Point Protocol over Ethernet
IGMP	Internet Group Management Protocol
UPnP	Universal Plug and Play (Computer Protocol)
GPIO	General-purpose I/O
SNMP	Simple Network Management Protocol
QoS	Quality of Service
IPsec	Internet Protocol Security
PPTP	Point-to-Point Tunneling Protocol

Table i. Acronyms and Abbreviated Terms (continued)

Term	Meaning
L2TP	Layer 2 Tunneling Protocol
RGMII	Reduced gigabit media independent interface

Chapter 1
Introduction

This chapter describes the features and block diagram for the P1020-WLAN board.

This chapter has following sections:

- Section 1.1, "Overview " - This section gives a brief introduction of P1020-WLAN board.
- Section 1.2, "Features " - This section describes the main features of P1020-WLAN board.

1.1 Overview

The P1020-WLAN is a reference design based on the QorIQ™ P1020 integrated processor. It supports the application of Wi-Fi Router. The documentation for manufacturing the P1020-WLAN—including schematic, Gerber files, reference software, Bill Of Material (BOM) — is in the product USB Storage. With the help of this documentation, the original equipment manufacturers (OEMs) and the original design manufacturers (ODMs) can accelerate the development process and speed time-to-market for their real product.

1.2 Features

This section describes the features, specification, and block diagram of the P1020-WLAN board. The features are listed below:

- CPU
  - Dual Power Architecture™ e500v2 cores up to 800 MHz
- Power
  - PoE power solution based on UNION MICROSYSTEMS™ MQ7800T120R up to 12W
  - 12V DC input used as the alternative power source when PoE is not available
- Memory subsystem
  - On-board 1-GByte DDR3 unbuffered SDRAM
  - 64-MByte NOR Flash
  - 256-MByte NAND Flash
- eTSECs
  - 10/100/1000 BaseT Ethernet ports
    - eTSEC1: RGMII interface, WAN, 1 x 10/100/1000 BaseT with RJ-45 interface, using VITESSE™ VSC8641 single port 10/100/1000 BaseT PHY
    - eTSEC2: No connection
    - eTSEC3: RGMII interface, LAN, 1 x 10/100/1000 BaseT with RJ-45 interface, using VITESSE™ VSC8641 single port 10/100/1000 BaseT PHY

- USB 2.0 Host
  - ULPI interface: using SMSC™ USB3300 Hi-Speed USB PHY and Genesys Logic's GL850A USB 2.0 HUB Controller with 4 downstream ports
  - 2x USB2.0 Type A Receptacle interface
  - 1x USB2.0 signal to mini PCI express slot
- PCI Express
  - PCI-E lane 0: mini PCI Express connector with USB2.0 signal
  - PCI-E lane 1: mini PCI Express connector without USB2.0 signal
  - Both mini PCI Express connectors support half size mini-PCI-e card
- eSDHC
  - One SDHC Card Connector
- I^2C
  - I^2C1 connected to ST M24256 Serial EEPROM
  - I^2C1 connected to RTC device DS1339U
  - I^2C2 connected to mini PCI express connectors
  - I^2C2 connected to ATMEL AT24C01B Serial EEPROM
  - I^2C2 connected to DC-DC device ZL2006
- Serial Port
  - UART0: RJ45 connector
  - UART1: internal 2x5 header
- Board Connectors
  - One DC power jack
  - JTAG / COP for debugging
  - One Reset Switch
- Form factor
  - Mini ITX form factor (170 mm x 170 mm, or 6693 mils x 6693 mils)
- 6-layer PCB (4 layers signals and separate power and ground layers)
- Certification
- CE/FCC
- Lead-Free (RoHS)

Figure 1-1 shows the P1020-WLAN board block diagram.

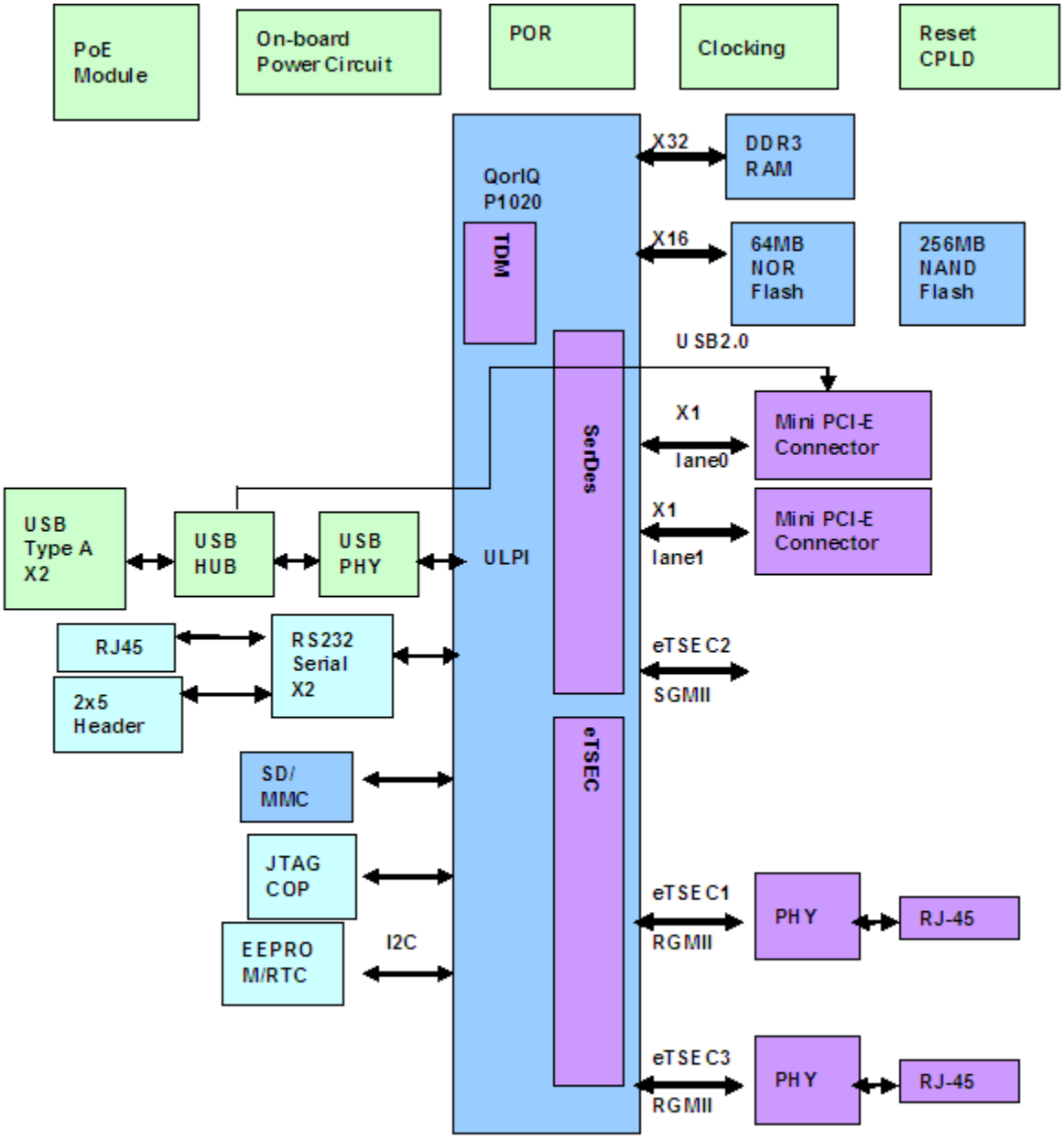

Figure 1-1. P1020-WLAN Board Block Diagram

Chapter 2
P1020-WLAN Board

This chapter describes the board-level functions, specifications, and mechanical data for the P1020-WLAN board.

This chapter includes following sections:

- Section 2.1, "Board-Level Functions " - This section includes reset, interrupts, clock distribution, and interface specification description.
- Section 2.2, "P1020-WLAN Assembly " - This section shows top and bottom view of P1020-WLAN board.
- Section 2.3, "Connectors " - describes pin assignment of all connectors on the board.
- Section 2.4, "LEDs ", shows LED indicators on the front panel.
- Section 2.5, "P1020-WLAN Board Configuration " - describes the operational mode and configuration options of the P1020-WLAN board.
- Section 2.6, "Electric Characteristics " - lists the electric characteristics of the P1020-WLAN board.
- Section 2.7, "Mechanical Data " - shows P1020-WLAN board dimensions.

2.1 Board-Level Functions

The board-level functions discussed in this section are reset, interrupts, clock distribution, and interface specification.

2.1.1 PoE

When 12V DC adapter input is not available, PoE - Power over Ethernet is an alternative power source for P1020-WLAN. This avoids a separate power cord. P1020-WLAN uses UNION MICROSYSTEMS's MQ7800T120R module to implement PoE PD (Powered Device) management, fully compliant to IEEE 802.3af.

The PoE application in P1020-WLAN board supports nominal voltage input 48V and output 12V, currents up to 1A. It also supports two methods of sending PoE on the Ethernet cable, on pairs 4-5 and 7-8 or pairs 1-2 and 3-6.

2.1.2 Reset and Reset Configurations

The P1020-WLAN board uses Lattice CPLD LCMXO256C to reset the P1020 and other peripherals on the board are reset by GPIOs of P1020. The reset unit provides power-on reset, hard reset, and soft reset signals in compliance with the P1020 hardware specification.

Figure 2-1 shows the reset circuitry.

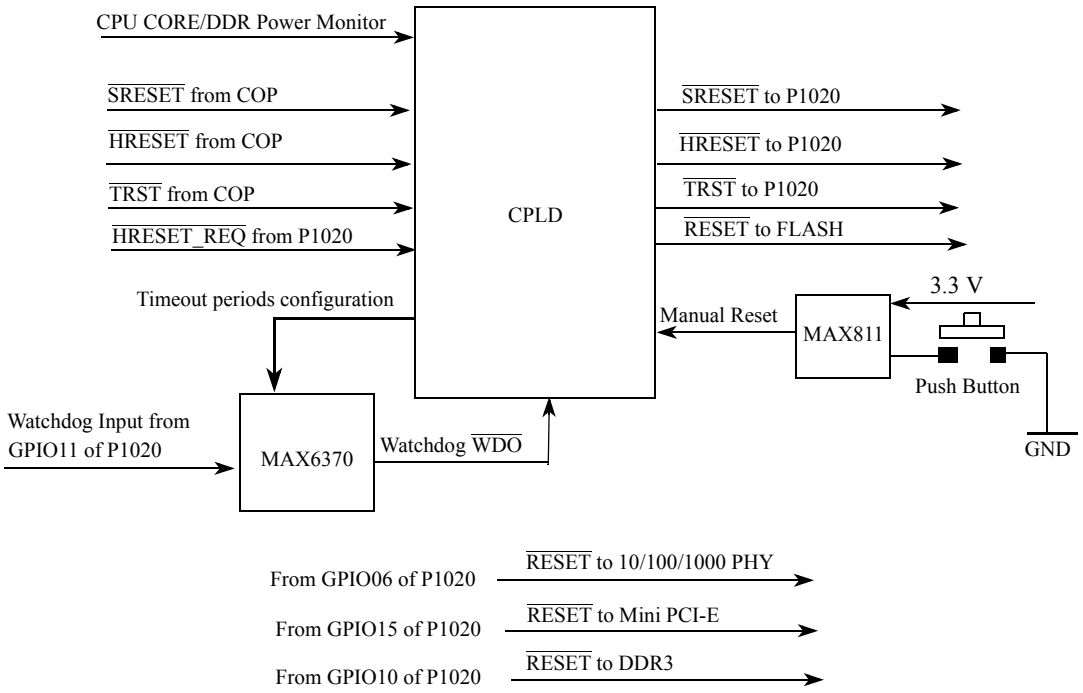

Figure 2-1. Reset Circuitry of the P1020-WLAN Board

- CPLD generates power-on reset for P1020 and flash when it detects that the CPU CORE/DDR Power is ready.
- The COP/JTAG port or HRESET_REQ signal from P1020 generates the signal for hard reset.
- The COP/JTAG port reset provides convenient hard-reset capability for a COP/JTAG controller. The HRESET line is available at the COP/JTAG port connector. The COP/JTAG controller can directly generate the hard-reset signal by asserting this line low.
- The COP/JTAG port also generates the soft reset for the system. Assertion of SRESET causes the P1020 to abort all current internal and external transactions and set most registers to their default values.
- CPLD will generate hard-reset if the system software is dead. Maxim MAX6370 watchdog device detects the system status. GPIO11 of P1020 provides watchdog input to MAX6370. CPLD configures MAX6370 watchdog timeout periods from 1ms to 60s or disable.
- CPLD monitors the time period of Push Button pressed. When it is pressed for a short duration (less than 3 seconds), CPLD will reset the system; when it is pressed for a long time (more than 6 seconds), CPLD will generate LOAD_DEFAULT signal to P1020 to load default configuration settings.

2.1.3 External Interrupts

Figure 2-2 shows the external interrupt circuitry to the P1020.

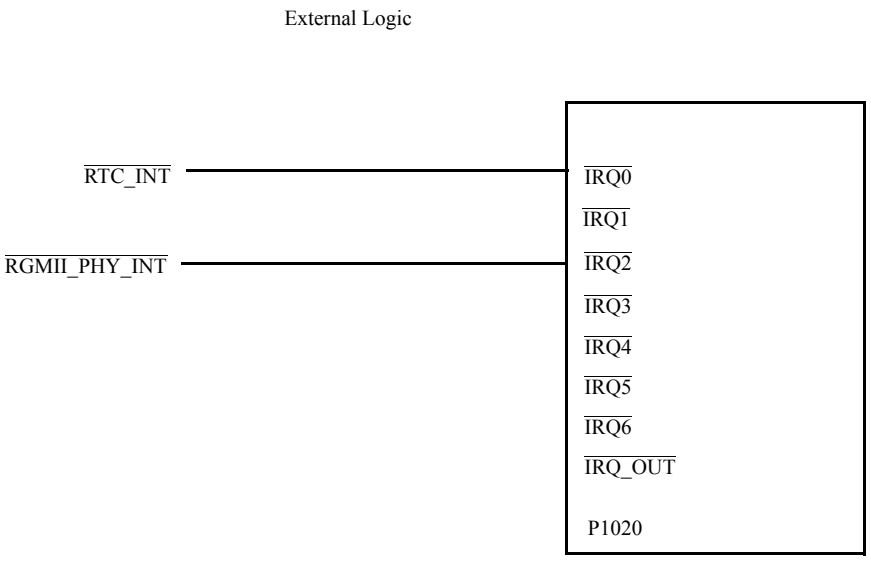

Figure 2-2. P1020 Interrupt Circuitry

The following items describe the interrupt signals shown in Figure 2-2:

- PHY interrupt (RGMII_PHY_INT). Two VSC8641 GBE PHY interrupts are connected to IRQ2 of P1020. The system software can detect the status of the Ethernet link and the PHY internal status.
- RTC interrupt (RTC_INT). RTC device DS1339U interrupt drives IRQ0 of P1020.

2.1.4 Clock Distribution

Figure 2-3 shows the clock distribution on the P1020-WLAN board.

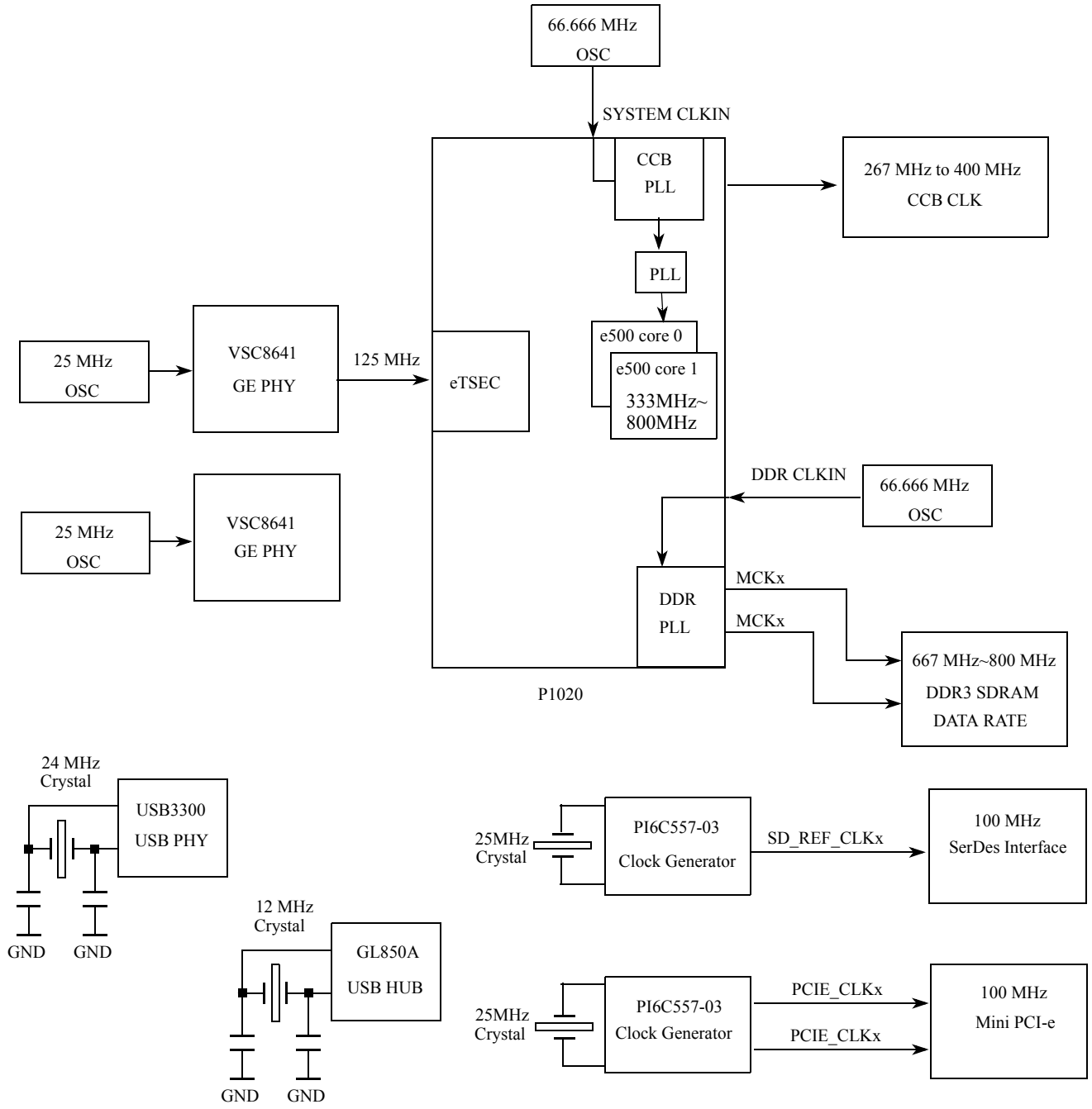

Figure 2-3. P1020-WLAN Clock Distribution Diagram

Table 2-1 shows the clock distribution on the P1020-WLAN board.

Table 2-1. Clock Distribution

Clock Frequency	Module	Generated by	Description
66.666 MHz	SYSTEM CLKIN	66.666 MHz oscillator	The P1020 uses SYSTEM CLKIN to generates the CCB clock (the platform clock), which is also fed to the e500 core PLL for generating the e500 core clock.
66.666 MHz	DDR CLKIN	66.666 MHz oscillator	The P1020 uses DDR CLKIN to drive the DDR SDRAM data rate.
125 MHz	P1020 eTSEC	VSC8641	The gigabit Ethernet PHY (VSC8641) provides a 125-MHZ clock for eTSEC operation.)
800 MHz	e500 CORE CLOCK	P1020	e500 core PLL is configured to use 2:1 (e500 core:CCB CLOCK) mode to get 800MHz core clock.
800 MHz	DDR3 SDRAM DATA RATE	P1020	The DDR memory controller is configured to use the 12:1 (DDR controller : DDR CLKIN) mode for the DDR interface.
400 MHz	PLATFORM CLOCK	P1020	The local bus controller uses 6:1 (CCB clock:SYSTEM CLKIN) PLL configuration to get 400MHz platform clock.
25 MHz	GBE PHY (VSC6841)	25 MHz oscillator	The 25 MHz oscillator generates the clock for VSC8641.
24 MHz	USB PHY (USB3300)	24 MHz crystal	
12 MHz	USB HUB Controller (GL850A)	12 MHz crystal	
100 MHz	SerDes Interface	25 MHz crystal and PI6C557-03 clock generator	The SerDes reference clock uses 100 MHz.
100 MHz	Mini PCI-e interface	25 MHz crystal and PI6C557-03 clock generator	

2.1.5 DDR3 SDRAM Controller

P1020-WLAN board uses DDR3 SDRAM as the system memory. The DDR3 interface uses 1.5 V power supply. Vref 1.5V/2 is also needed in the DDR3 interface.

Figure 2-4 shows the DDR3 SDRAM controller connection.

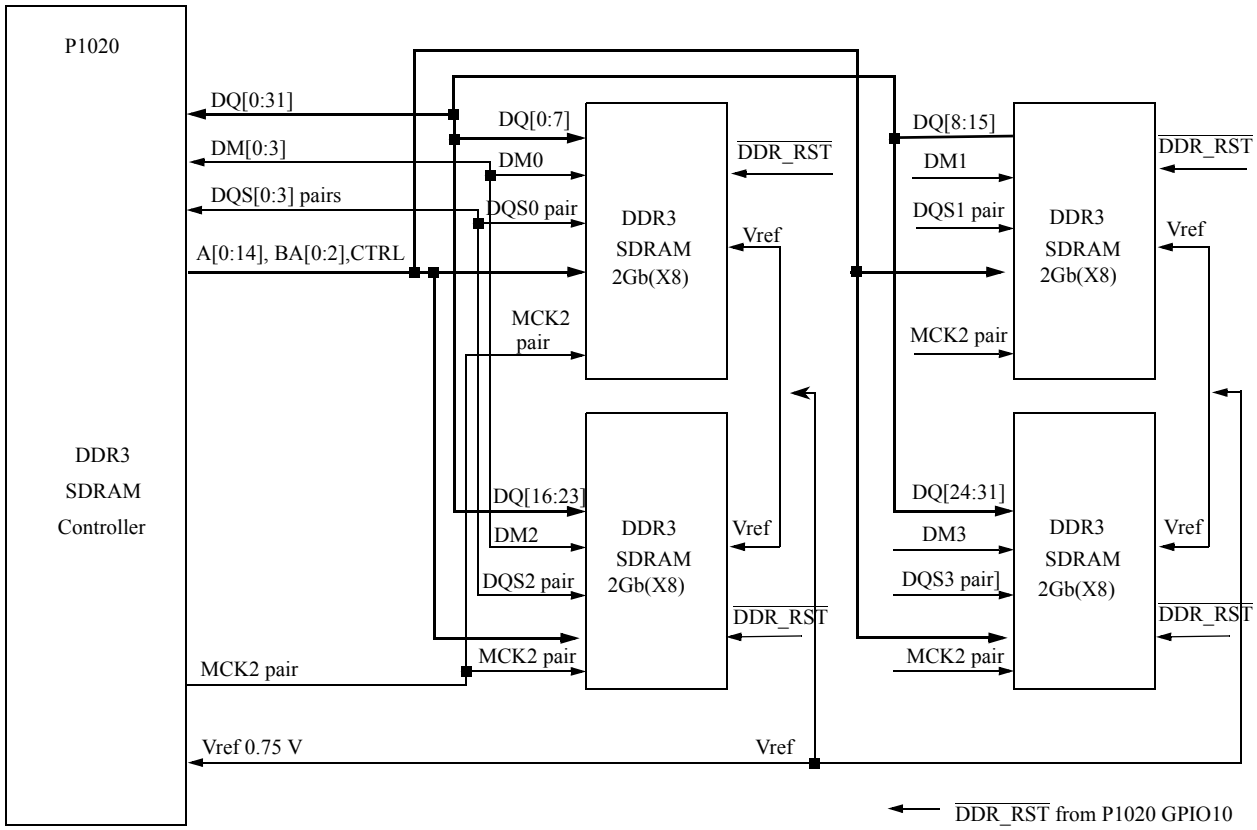

Figure 2-4. DDR3 SDRAM Connection

2.1.6 Local Bus Controller

The P1020 local bus controller has a 32-bit LAD[0–31] address that consists of data multiplex bus and control signals. The local bus speed is up to 50 MHz. To interface with the standard memory device, an address latch must provide the address signals. The LALE is used as the latching signal. To reduce the load of the high speed 32-bit local bus interface, there is a data buffer for all low-speed devices attached to the memory controller. The local bus drives the 64MB NOR Flash and 256MHz NAND Flash on the board, meanwhile, local bus is also interfaced with CPLD for some registers control and setting.

Figure 2-5 shows the block diagram and connections for the local bus.

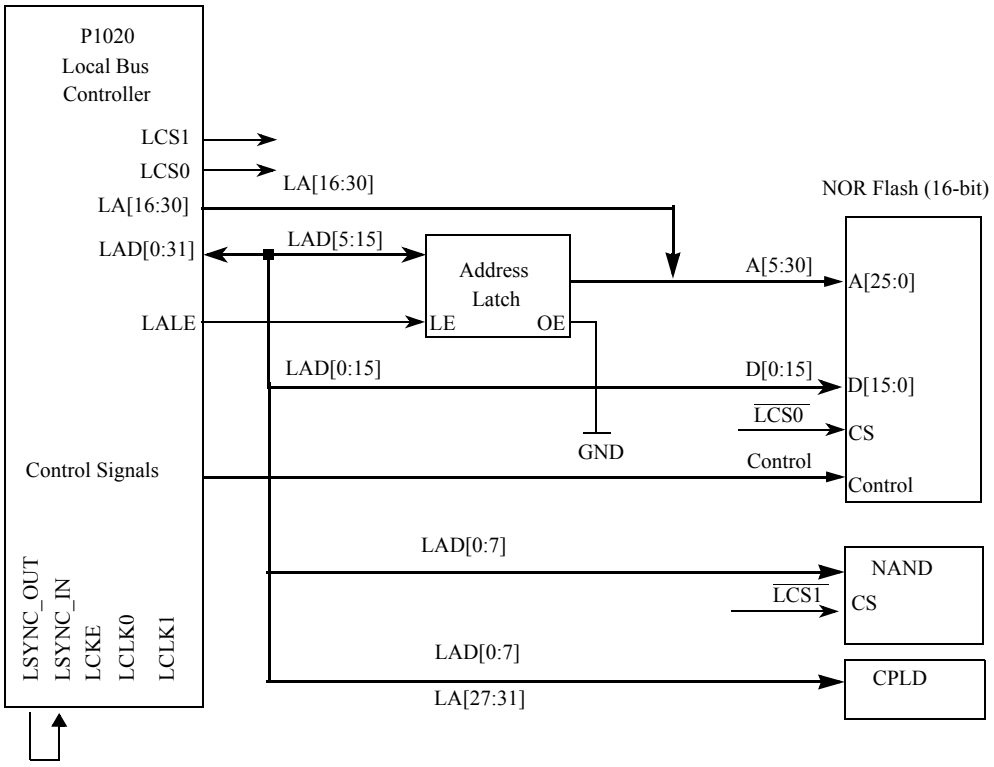

Figure 2-5. Local Bus Connections

2.1.7 Flash Memory

P1020-WLAN provides 64Mbytes NOR Flash memory using general-purpose chip-select machine (GPCM). The NOR Flash memory is 16-bit port size in the system. It is selected as the boot Flash by default, connected to CS0.

P1020-WLAN also support 256MB NAND flash. It is a 8-bit, SLC NAND flash with 2K large page size. The NAND flash is connected to CS1 as extended flash memory. CS0 and CS1 is swappable between NOR and NAND flash by J6, that is, NAND flash can be assigned as boot flash and NOR flash acts as extended flash memory.

2.1.8 I^2C

The P1020 silicon has two I^2C interfaces. On the P1020-WLAN board, the P1020 serves as I^2C master for both I^2C buses (I2C1 and I2C2). I2C1 is connected to the following:

- Serial EEPROM M24256 at address 0x50
- External RTC controller DS1339 at address 0x68

I2C2 is connected to the following:

- Two Mini PCI-E sockets

- Board EEPROM AT24C01 at address 0x52
- CPU power regulator ZL2006 at address 0x11

The M24256 serial EEPROM can store the reset configuration word of the P1020, as well as store the configuration registers values if the boot sequencer of P1020 is enabled. The I^2C address of the M24256 EEPROM on I2C1 bus is 0x50.

External RTC controller DS1339 is powered by on board battery. It can be accessed by IIC interface for RTC functions, and generate interrupt to CPU if an alarm occurs.

Board EEPROM AT24C01 can be used by customer to store board information such as board name, revision and so on.

ZL2006 is a switching power regulator to generate CPU core voltage. It can be accessed by IIC interface to set internal registers for control and debug purpose.

2.1.9 PCI Express Interface (Mini PCI-E)

P1020 supports two PCI Express (PCI-E) x1 interfaces. They are connected to two mini PCI-E slots as shown in Figure 2-6. Two Atheros 802.11n WiFi cards will be plugged in the slots to provide wireless connection. It requires a 100-MHz input clock, which is provided by the clock generator.

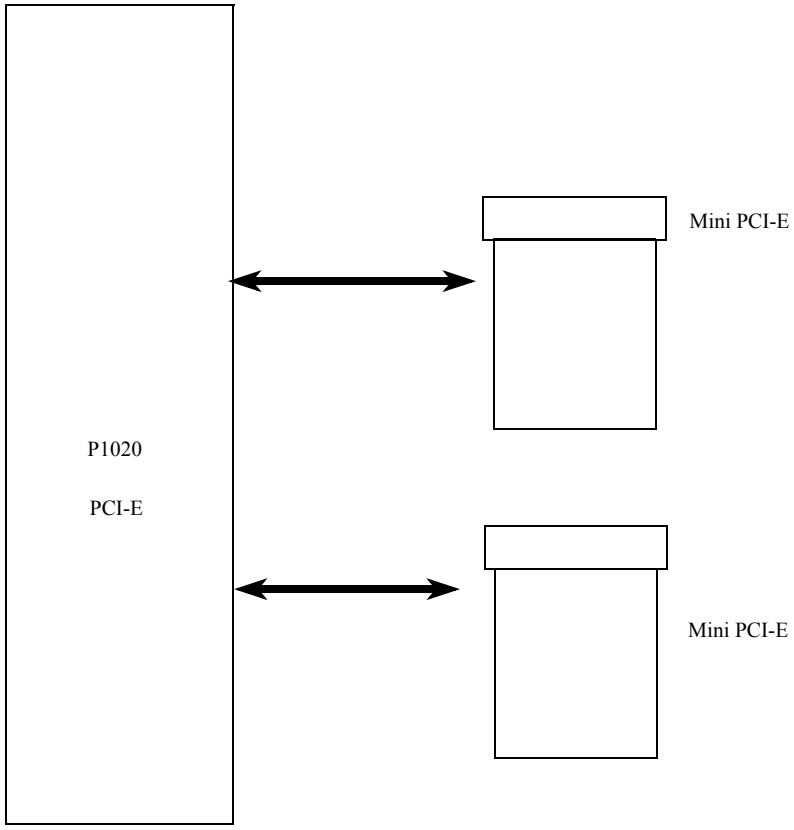

Figure 2-6. PCI-E Connections

2.1.10 10/100/1000 BaseT Interface

P1020 supports 3 configurable eTSEC interfaces. On the P1020-WLAN board, eTSEC1 and eTSEC3 are used as RGMII mode while eTSEC2 is not used. The eTSEC1 and eTSEC3 drive two on-board 10/100/1000 PHYs (VSC8641) respectively. The I/O voltage is set to 2.5V RGMII for VSC8641. The RGMII (1000 BaseT) is a source synchronous bus. For a transmit bus connection, it is synchronous to GTX_CLK from the TSEC module. The receive bus connection is synchronous to RX_CLK generated from the PHY device. The P1020-WLAN MII management interface also connects to the VSC8641 for

configuration settings. Figure 2-7 shows the connection between the P1020 eTSEC1 and eTSEC3 to the VSC8641.

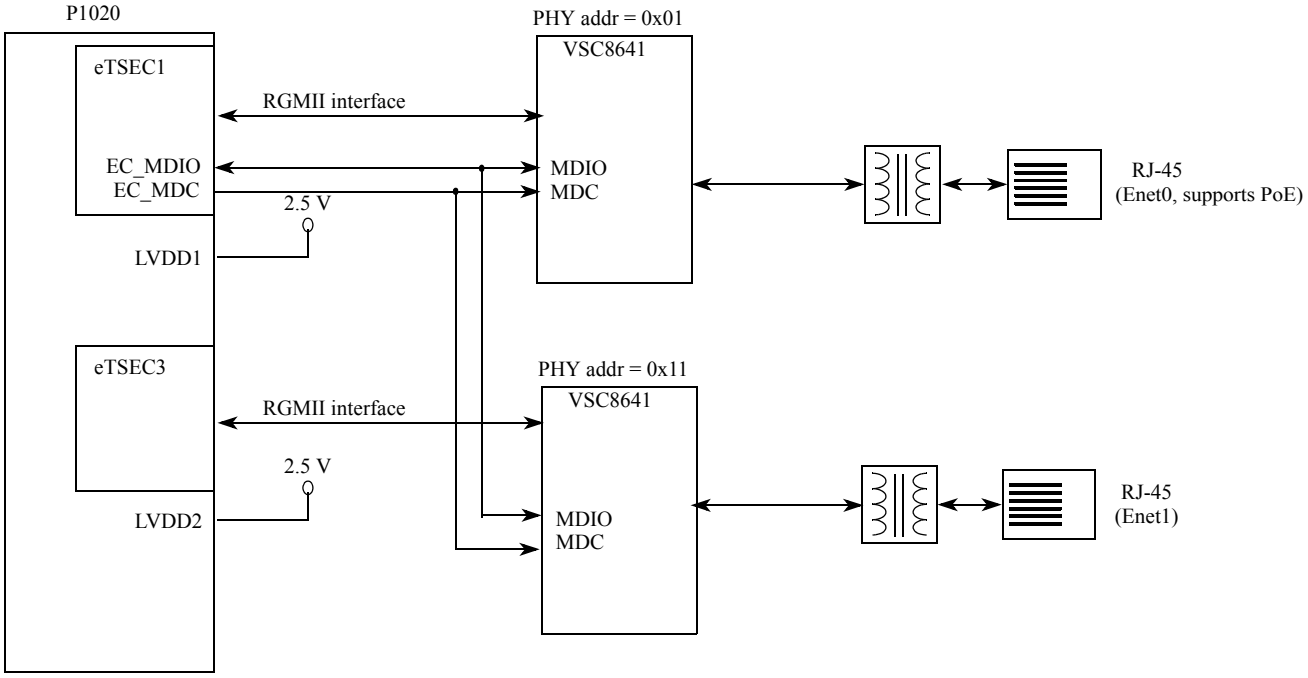

Figure 2-7. RGMII Interface Connection for 10/100/1000 BaseT Ethernet

2.1.11 RS-232 Port

P1020-WLAN supports two UART interfaces. One is connected to external RJ45 connector on enclosure while the other is connected to on board 2x5 header for 2nd console when running at dual core mode.

Figure 2-8 illustrates the serial port connection using a SP3232 3.3 V RS-232 driver to interface with the 2 x 5 Header and RJ45 connector. The serial connections run at up to 115.2 Kbps.

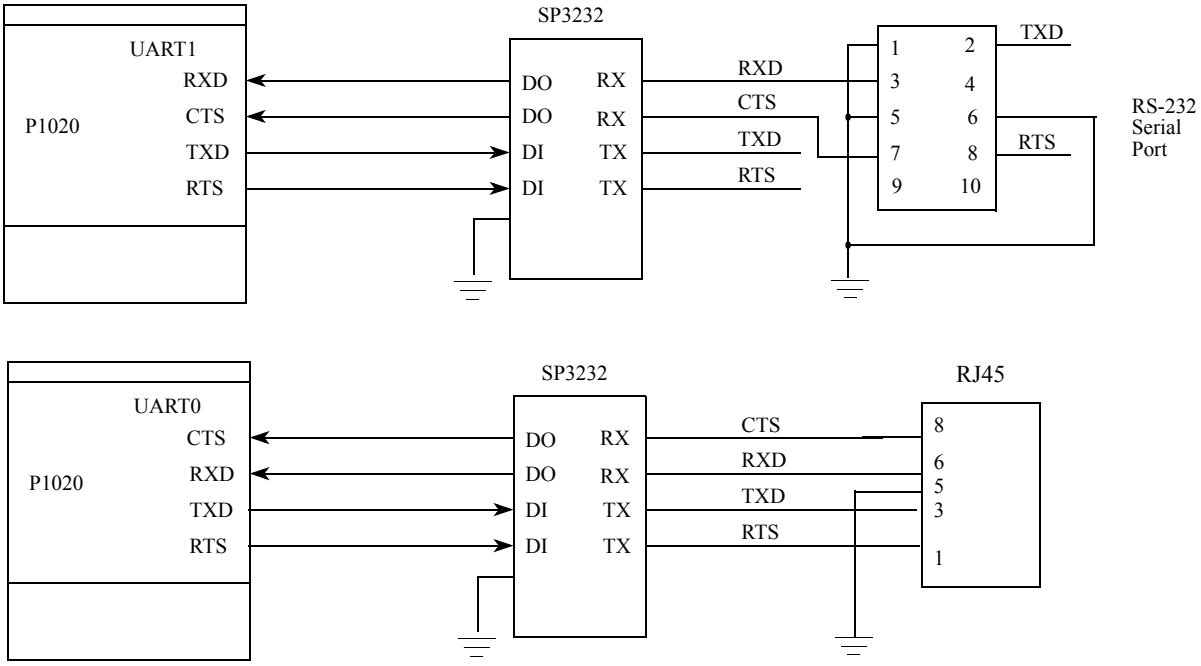

Figure 2-8. UART Debug Port Connection

2.1.12 USB 2.0 Interface

The P1020 has 2 integrated USB DR modules with ULPI interface. On the P1020-WLAN board, 1st USB DR module is used (2nd one is muxed with eLBC bus so it is not used). It connects to the USB PHY (USB3300) through the 8-bit UTMI low-pin-count interface (ULPI). The USB3300 connects to one USB 2.0 HUB Controller GL850A with 4 downstream ports. Port 3 and 4 of the USB HUB serve as USB host

interfaces with USB Type A Receptacle. Port 2 is connected to one of the Mini PCI Express slot. Figure 2-9 shows the connection of USB.

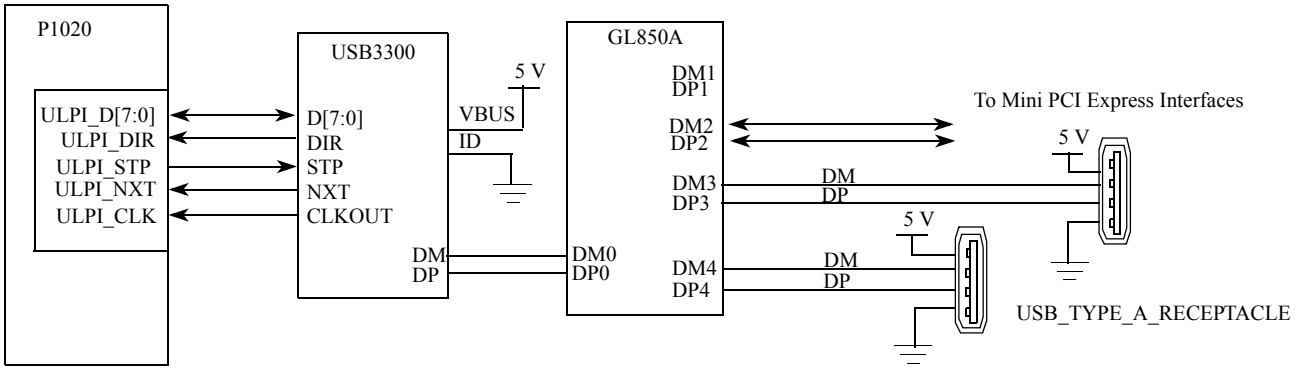

Figure 2-9. USB Port Connections

2.1.13 SDHC

P1020-WLAN has on board SDHC/MMC slots which supports following modes,

- SD 1-bit mode
- SD 4-bit mode
- MMC 1-bit mode
- MMC 4-bit mode
- MMC 8-bit mode
- SD full speed mode up to 25MHz
- SD high speed mode up to 50MHz
- MMC full speed mode up to 20MHz
- MMC high speed mode up to 52MHz

2.1.14 COP/JTAG Port

The common on-chip processor (COP) is part of the P1020 JTAG module and is implemented as a set of additional instructions and logic. This port can connect to a dedicated emulator for extensive system debugging. Several third-party emulators in the market can connect to the host computer through the

Ethernet port, USB port, parallel port, RS-232, etc. Figure 2-10 shows a typical setup using a USB port emulator.

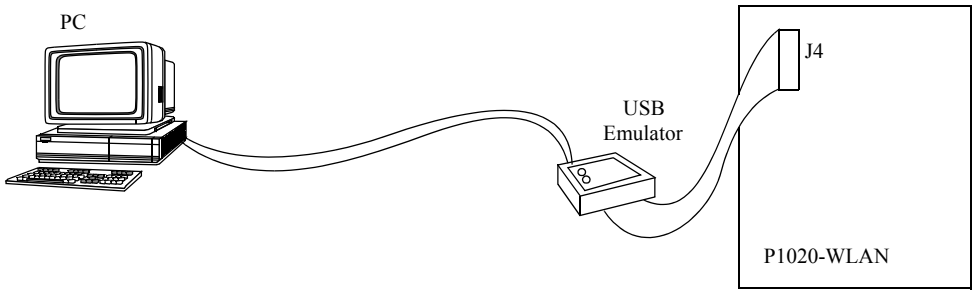

Figure 2-10. Connecting the P1020-WLAN Board to a USB Emulator

The 16-pin generic header connector carries the COP/JTAG signals and the additional signals for system debugging. Figure 2-11 shows the connector pinout.

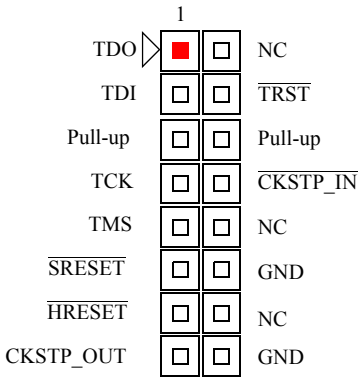

Figure 2-11. P1020-WLAN Board COP Connector

2.2 P1020-WLAN Assembly

Figure 2-12 shows the P1020-WLAN board top view.

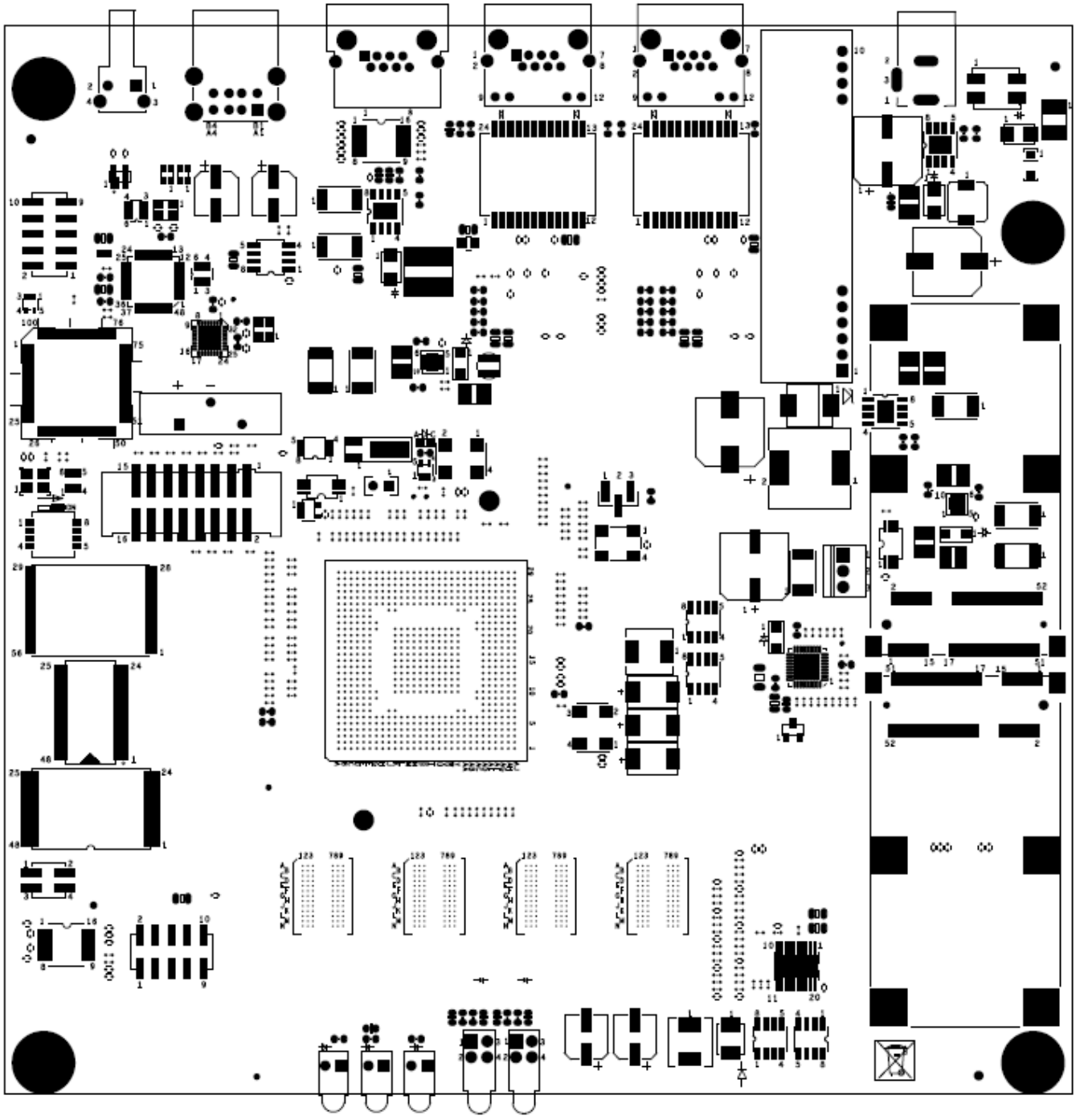

Figure 2-12. P1020-WLAN Top View

Figure 2-13 shows the P1020-WLAN board bottom view.

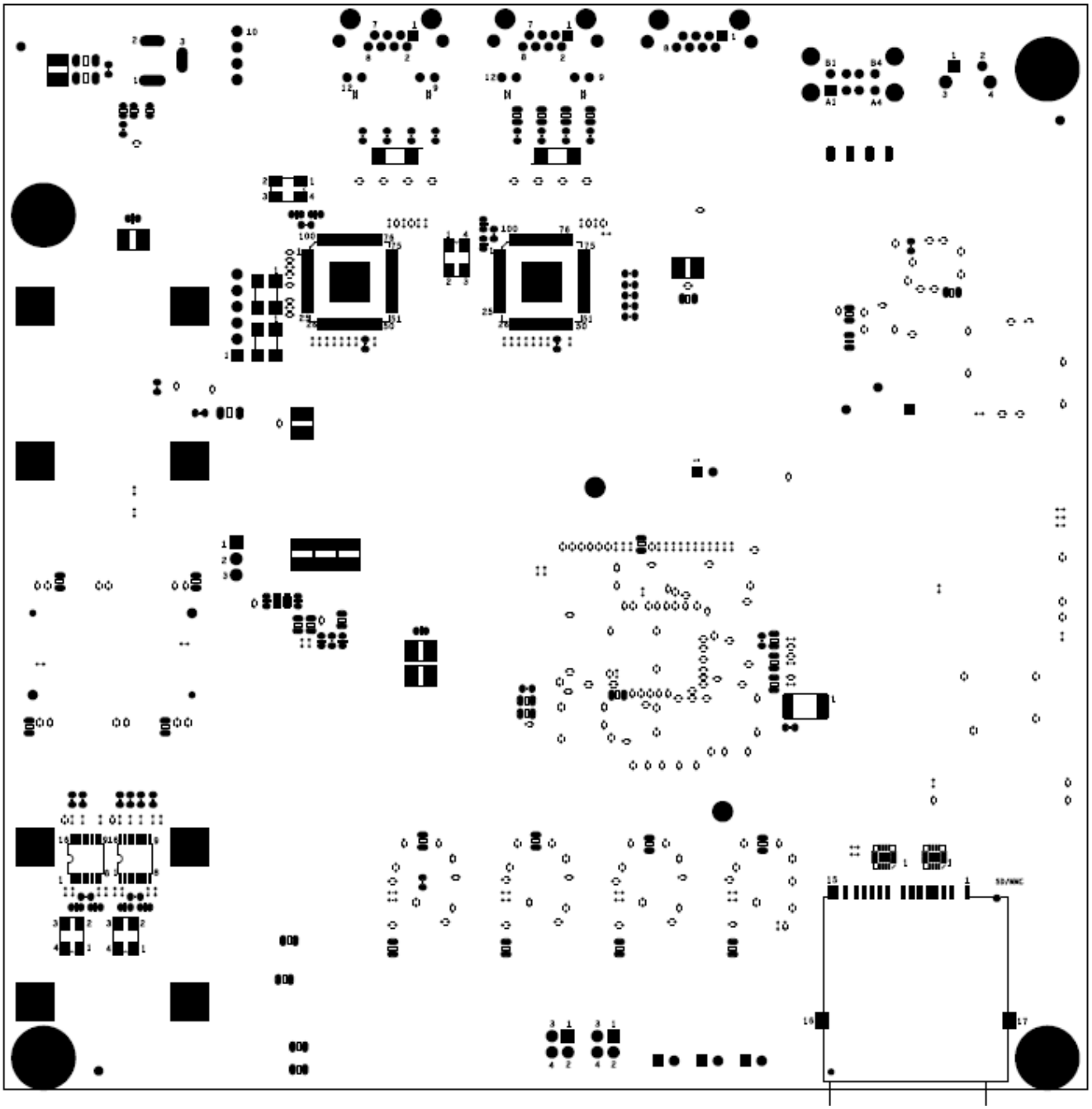

Figure 2-13. P1020-WLAN Bottom View

Table 2-2 shows references and descriptions of LEDs, jumpers, headers, and switches.

Table 2-2. Lists of Connectors, Jumpers, Switches, and LEDs

Reference	Description
Connectors	
J4	16-pin COP/JTAG connector
P4, P5	Mini PCIe connector
J1	Dual USB Type A receptacles (for USB high-speed external device)
J2	12 V DC power jack (external power adapter input)
P1	RJ45 connector for UART0 access
J9	2x5 header for UART1 access
P2	RJ-45 connector Eth0 (GBit Ethernet port that connects to Ethernet Switch). Eth0 is the WAN connector and supports PoE.
P3	RJ-45 connector Eth1 (GBit Ethernet port that connects to external device). Eth1 is the LAN connector.
J8	SD/MMC Card socket
Jumpers	
J11	Isolate IRQ0 to RTC interrupt, default is on
J6	selection of boot flash from NOR flash or NAND flash 1-3,2-4: Boot from NOR flash, NAND flash is extended flash memory (**default**) 1-2,3-4: Boot from NAND flash, NOR flash is extended flash memory.
Switches	
SW1	System reset button. When pressed for 1~ 3seconds the system is reset and when pressed for more than 10 seconds the system loads default configuration settings.
SW2	System configuration switch. Switch 1 on: P1020 is working in dual core mode (**default**) off: P1020 is working in single core mode, that is P1011. Switch 2 on: P1020 is working at 800MHz (**default**) off: P1020 is working at 533MHz. Switch 3 on: DDR3 is working at 800M data rate (**default**) off: DDR3 is working at 667M data rate.
LEDs (See also Section 2.4, "LEDs ")	
D7	Indicator for CPU state
D16	WiFi LED indicator
D11,D12	Act/Link LED for Eth0 and Eth1
D14	Status LED
D13	Power LED

2.3 Connectors

This section describes the P1020-WLAN connectors and their pin assignments.

2.3.1 COP Connector

The COP connector (J4) allows the user to connect a COP/JTAG-based debugger to the P1020-WLAN board for debugging. Table 2-3 lists the pin assignments of the COP connector.

Table 2-3. COP Connector Pin Assignments

Pin	Signal	Pin	Signal
1	TDO	2	NC
3	TDI	4	$\overline{\text{TRST}}$
5	NC	6	VDD_SENSE
7	TCK	8	$\overline{\text{CHKSTOP\_IN}}$
9	TMS	10	NC
11	$\overline{\text{SRESET}}$	12	GND
13	$\overline{\text{HRESET}}$	14	NC
15	$\overline{\text{CHKSTOP\_OUT}}$	16	GND

2.3.2 RS-232C Connectors

Serial interface UART1 is available at connector (J9) with pin assignments as shown in Table 2-4. UART0 is available on the RJ45 connector, the pin assignment follows standard RS232-RJ45 connection.

Table 2-4. UART1 Connector Pins

Pin	Signal
1	NC
2	TXD
3	RXD
4	NC
5	GND
6	NC
7	CTS
8	RTS
9	NC
10	NC

2.3.3 Mini PCIe Connector

The board has two mini-PCIe connectors (P4, P5) for plugging in mini PCIe cards. The pin assignment follows standard specification.

2.3.4 Ethernet RJ45 connector

The board has two Ethernet RJ45 connectors (P2, P3) for Giga bit Ethernet connection. The pin assignment follows standard specification.

2.3.5 Power Connector

J2 is a DC jack for a 12 V power supply to the P1020-WLAN board.

2.4 LEDs

Figure 2-14 shows fiveLED indicators on the front panel of P1020-WLAN.

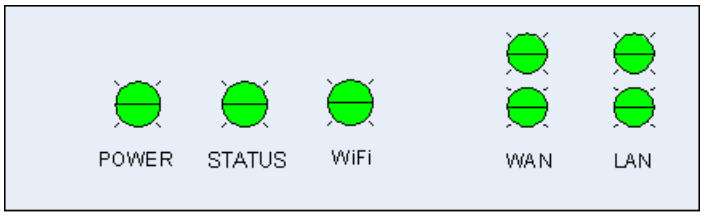

Figure 2-14. LED Indicators on the Front Panel of P1020-WLAN

2.4.1 Power-on LED

Green Power LED (D13): indicates the system is power-on if lit.

2.4.2 RDS Programmable LEDs

Green WiFi LED (D16) indicates whether the WiFi Card is inserted and activated. GPIO5 controls this LED. Writing 0 turns on the LED, and writing 1 turns off the LED.

Yellow Status LED (D14) indicates the status of diagnostics for P1020-WLAN board. The LED is flashing when system is going through the diagnostics. It is on if the system finds some problems during the diagnostics. And it is off if the system passes the diagnostics (SW not implemented yet). CPLD controls this LED. Writing 0 turns on the LED, and writing 1 turns off the LED.

2.4.3 Ethernet LEDs

D11 indicates the activity and link status for WAN.

D12 indiciates the activity and link status for LAN.

2.5 P1020-WLAN Board Configuration

This section describes the operational mode and configuration of the P1020-WLAN board.

2.5.1 POR settings

P1020-WLAN board has resistors and switch (SW2) for POR settings. In this way, some POR settings are fixed and some are configurable. Below Table2-5 shows the configurable settings.

Table 2-5. POR settings

Functional Signals	Name	Description	
LA[29:31]	cfg_sys_pll[0:2]	CCB Clock : SYSCLK Ratio	
		000	**4:1**
		001	5:1
		010	**6:1**
		011	8:1
		100	10:1
		101	12:1
TSEC_1588_CLK_OUT, TSEC_1588_PULSE_OUT1, TSEC_1588_PULSE_OUT2	cfg_ddr_pll[0:2]	DDR Complex : DDRCLK Ratio	
		000	3:1
		001	4:1
		010	6:1
		011	8:1
		100	**10:1**
		101	**12:1**
		110	14:1
TEST_SEL		1	Dual core
		0	Single core

2.5.2 Power Supply

The P1020-WLAN requires a 12 V power supply from the DC power jack or 48V PoE supply for normal operation. The 48 V PoE power supply is regulated to 12 V by on board PoE module. Low voltage 5 V, 3.3 V, 2.5 V, 1.5 V, 1.2V and 0.95 V are all generated from 12 V by switching regulators. The 0.95 V power is for a CPU core. The 2.5 V and 1.2 V powers are for two GE PHYs. The 1.5 V power is for the DDR circuitry. The 5 V power is for USB interfaces and 3.3V is for most IO.

2.5.3 Chip-Select Assignments and Memory Map

Table 2-6 shows an example memory map on the P1020-WLAN that is used for u-boot in the Flash memory.

Table 2-6. Example Memory Map, Local Access Window, and Chip-Select Assignments

Start Address (HEX)	End Address (HEX)	Size (Byte)	Devices	Access
0_0000_0000	0_3FFF_FFFF	1G	DDR3	Read/write
0_8000_0000	0_9FFF_FFFF	512M	PCI Express slot 1 Memory	Read/write
0_A000_0000	0_BFFF_FFFF	512M	PCI Express slot 2 Memory	Read/write
0_D000_0000	0_DFFF_FFFF	256M	NAND FLASH	Read/write
0_EE00_0000	0_EFFF_FFFF	32M	NOR FLASH	Read/write
0_FF00_0000	0_FF9F_FFFF		Reserved	NO
0_FFA0_0000	0_FFA1_FFFF	128K	CPLD	Read/write
0_FFC0_0000	0_FFC0_FFFF	64K	PCI Express slot 1 IO	Read/write
0_FFC1_0000	0_FFC1_FFFF	64K	PCI Express slot 2 IO	Read/write
0_FFE0_0000	0_FFEF_FFFF	1M	CCSR	Read/write
0_FFFF_0000	0_FFFF_FFFF	64K	L2 Cache (used as SDRAM)	Read/write

2.6 Electric Characteristics

Table 2-7 lists the electric characteristics of the P1020-WLAN board.

Table 2-7. P1020-WLAN Board Characteristics

Characteristics	Specifications
Power input	12.0 V DC4.0 A
Communication processor	P1020 running @ up to 800 MHz
Addressing: Total address range Flash memory (local bus) DDR SDRAM	36-bit addressing 64 Mbyte NOR Flash 256Mbyte NAND flash 1Gbyte DDR3 SDRAM at DDR800
Operating temperature	0°C to 70°C (room temperature)
Storage temperature	–25°C to 85°C
Relative humidity	5% to 90% (noncondensing)
PCB dimensions: Length Width Thickness	 6693 mil 6693 mil 67 mil

2.7 Mechanical Data

Figure 2-15 shows the P1020-WLAN dimensions (in mil). The board dimensions are 170 mm × 170 mm (6693 mils × 6693 mils) for integration in a mini ITX chassis with a small footprint.

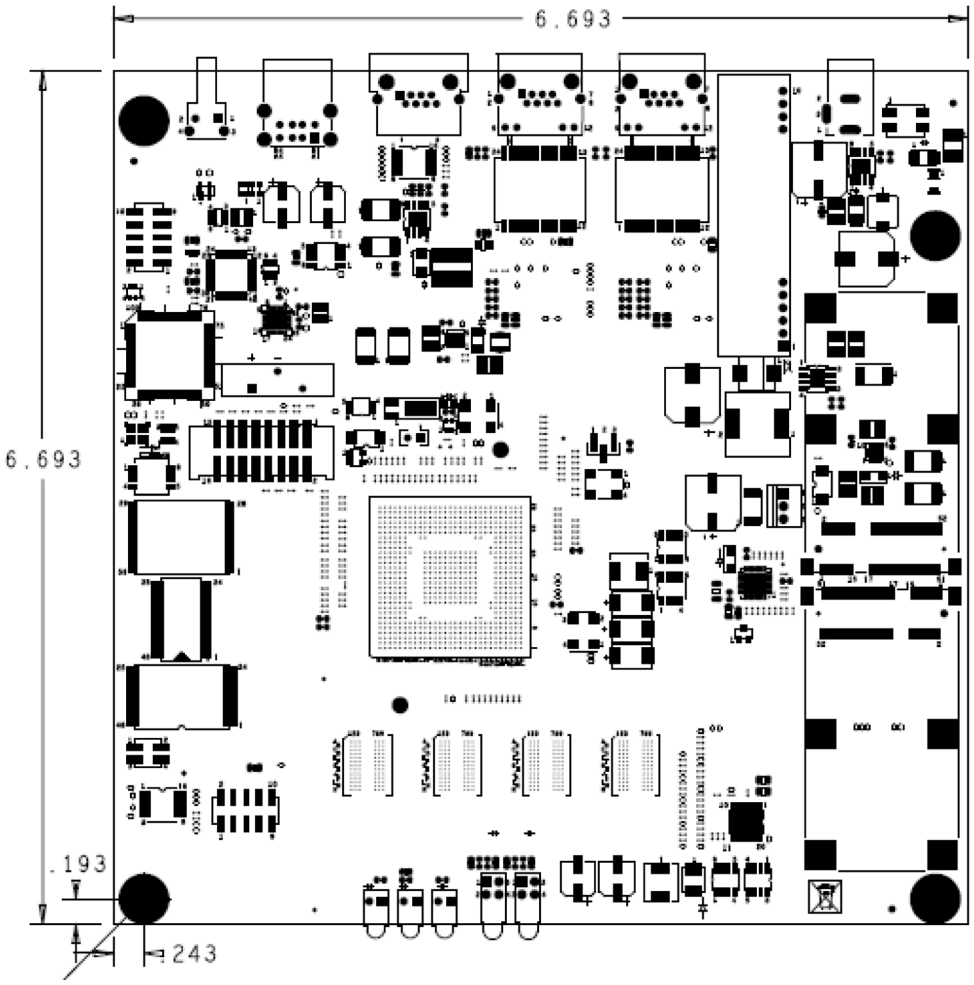

Figure 2-15. Dimensions of the P1020-WLAN Board

Chapter 3
Board Bootup

This chapter describes how to boot up the P1020-WLAN board. The on-board Flash memory comes preloaded with Flash image. Before powering up the board, set the on-board jumpers according to the settings listed in Section 3.1, "Board Jumper Settings ".

This chapter has following sections:

- Section 3.1, "Board Jumper Settings " - This section describes default jumper settings for board bootup.
- Section 3.2, "External Connections " - This section illustrates all available external connections of the P1020-WLAN board.

CAUTION

Avoid touching areas of circuitry and connectors; static discharge can damage circuits.

3.1 Board Jumper And Switch Settings

Figure 3-1 shows jumpers and switch on top of the P1020-WLAN with red outlines at jumper designators J6, SW2.

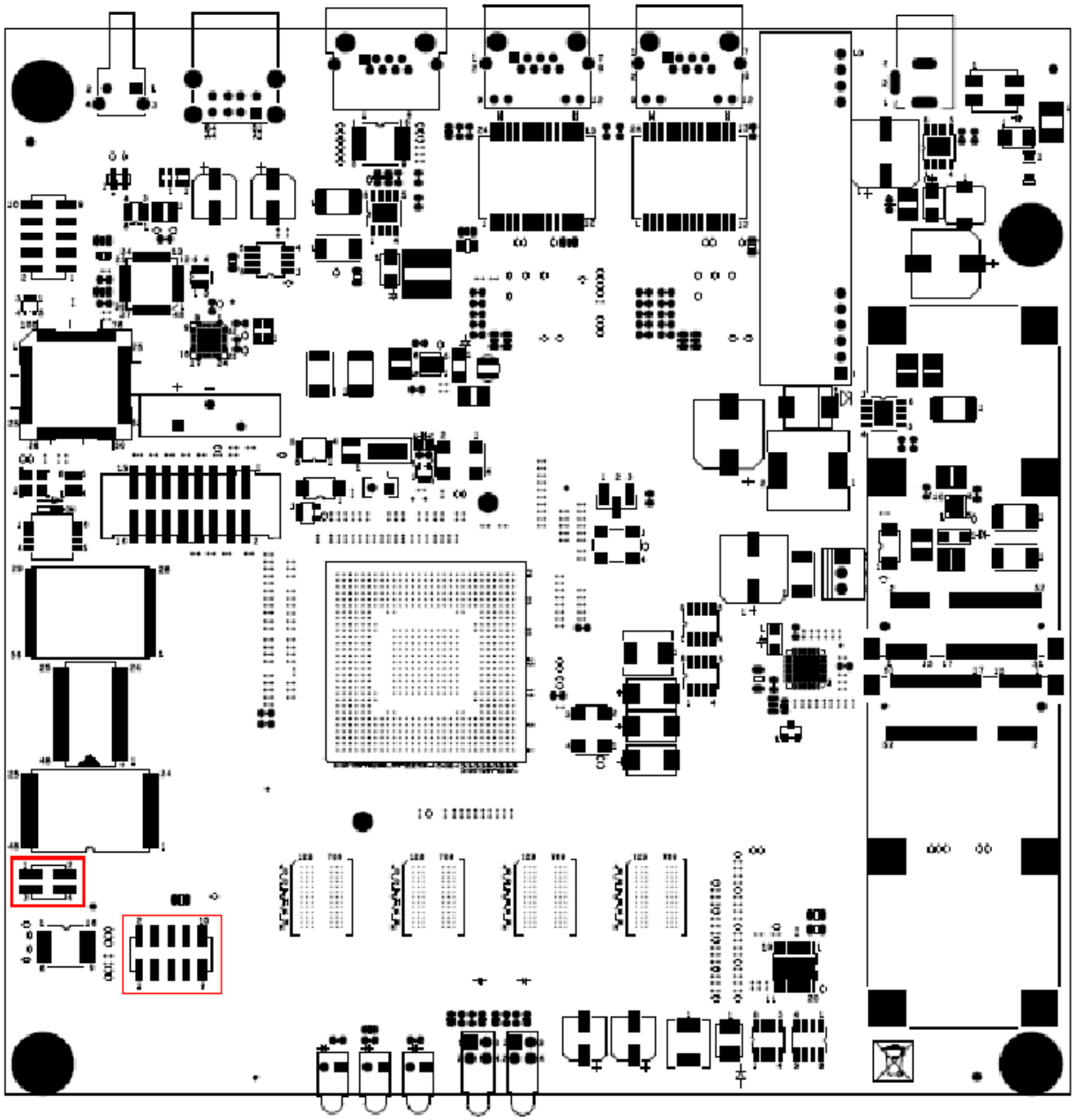

Figure 3-1. Jumper and switch on P1020-WLAN Top View

Table 3-1 shows the default jumper settings.

Table 3-1. Default Jumper and switch Settings

Reference	Setting	Description
J6	1-3,2-4 (default)	NOR: connect to CS0, boot flash NAND: connecto to CS1
	1-2,3-4	NOR: connect to CS1 NAND: connect to CS0, boot flash
SW2	switch 1 switch 2 switch 3	System configuration switch. Switch 1 on: P1020 is working in dual core mode (**default**) off: P1020 is working in single core mode, that is P1011. Switch 2 on: P1020 is working at 800MHz (**default**) off: P1020 is working at 533MHz. Switch 3 on: DDR3 is working at 800M data rate (**default**) off: DDR3 is working at 667M data rate.

3.2 External Connections

Figure 3-2 shows the external connections.

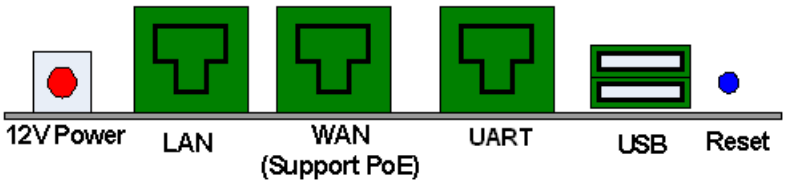

Figure 3-2. External Connections

NOTE

Strong electromagnetic interference might disturb the normal function of the product. Reset the product to resume normal operation by following the steps given in the software user guide. If normal function does not return, please move the product to another location.

Chapter 4
P1020-WLAN Software

The P1020-WLAN comes with a pre-installed reference design software package. This package consists of a bootloader (u-boot), a generic PPC Linux-based system, and a suite of Wi-Fi router applications. The software resides in the on-board Flash memory. Upon powerup, the Linux system and the applications run on the P1020-WLAN.

The P1020-WLAN reference software takes advantage of a tool called OpenWRT, a Linux platform for embedded devices. Instead of trying to create a single, static firmware, OpenWrt provides a fully writable file system with package management. This allows you to customize the device through the use of packages to suit any application.

This chapter has following sections:

- Section 4.1, "Application Features for P1020-WLAN reference software " - This section lists software features for the application of the Wi-Fi router.
- Section 4.2, "Application Connections " - This section shows an application connections for P1020-WLAN board.

4.1 Application Features for P1020-WLAN reference software

The pre-installed reference design software supports the application of the Wi-Fi router, including the following:

- 802.11 a/b/g/n
- IPv4
- DHCP
- DNS
- VLAN
- NAT and PAT
- Static routing
- VRRP
- PPPoE
- IGMP
- UPnP
- SNMP

Network Vedio Record(NVR)

- IP camera video monitor

- Virtual camera display
- Video stream record
- Video file replay

Network Access Storage(NAS)

- USB-Disk/CF support
- Raid disk manage
- Volume management
- Snapshot managment
- Samba/NFS/FTP/ file share
- Rsync backup
- Network access control

Wireless Security:

- Pre-Shared Key (PSK)
- Wi-Fi Protected Access 2 (WPA2)
- 802.11i AES-CCMP
- Wired Equivalent Privacy (WEP), 128/256-bit
- 802.11i EAP authentication with RADIUS

Network Security:

- Access control
- Stateful packet inspection firewall
- Intrusion detection
- Content filtering

Virtual Private Network (VPN):

- IPSec
- PPTP
- L2TP

4.2 Application Connections

Figure 4-1 shows application connections for P1020-WLAN board.

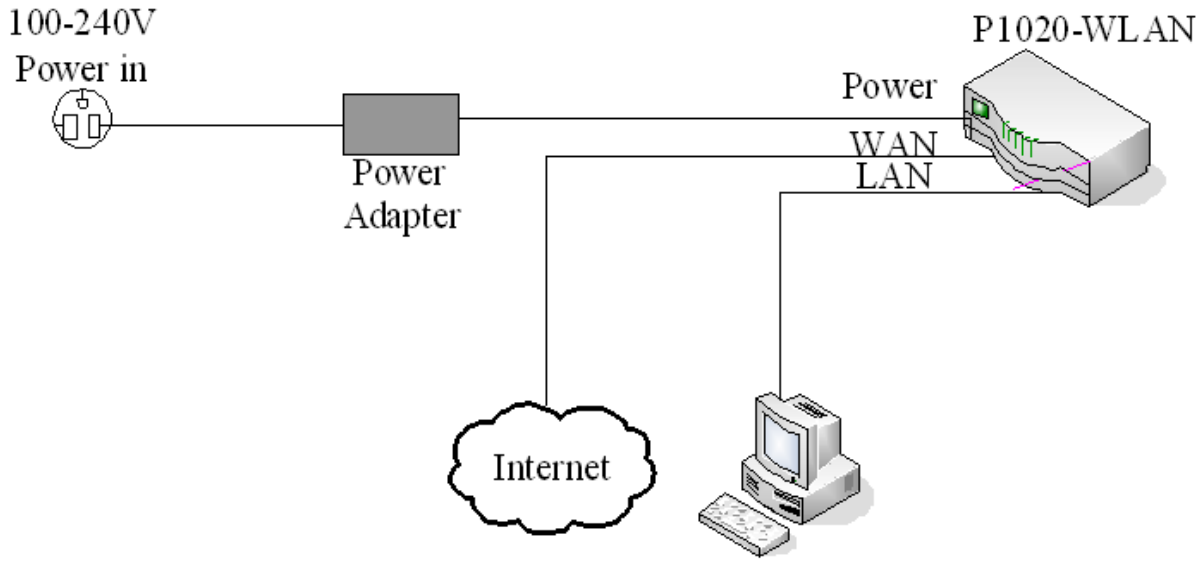

Figure 4-1. P1020-WLAN Application Connections

Configure the P1020-WLAN board by using a web browser. Connect your PC to the LAN port of the board (either directly or through a hub), then use a web browser to configure. TCP/IP settings must be correct. The TCP/IP setting should be on the IP subnet of the P1020-WLAN.

Set up the IP Address automatically.

- P1020-WLAN incorporates a DHCP server. The easiest method is to set your PC to get its IP address automatically and correctly obtain the correct IP address, gateway, and DNS.

Set up the IP Address manually.

- The default IP address of P1020-WLAN reference board is `192.168.1.1`. Set the IP address of the PC as `192.168.1.xxx`, where xxx can be any number between 2 and 254, and the set the default gateway to `192.168.1.1`.
- After setting the IP address, open a web browser and type address http://192.168.1.1.
- At the login window, type `admin` for both User name and Password. The P1020-WLAN main page will appear.
- Now, you can review and modify the configuration as needed. For more information, refer to the software user guide.

Besides acting as one Wi-Fi router, P1020-WLAN platform can also support other utilities and applications. For details of different applications for P1020-WLAN, contact your local Freescale sales office.

Chapter 5
Unit Assembly

The assembled unit is composed of the board assembly, an enclosure, screws, and other parts. This chapter describes instructions for assembling or reassembling the product or adding the peripherals.

This chapter has following sections:

- Section 5.1, "Assembling the Enclosure and Board Assembly " - This section describes how to assemble the board into the enclosure.
- Section 5.2, "Attaching a Wi-Fi Card to the Product " - This section describes how to attach a Wi-Fi card to the product.

5.1 Assembling the Enclosure and Board Assembly

Assembling the board into the enclosure requires screwing the board onto the base, then screwing the top, base, front panel and rear panel together.

1. Place the base on a flat surface.
2. Set the board assembly in the base so the board's mounting holes align with the base's mating holes.
3. With four screws and washers, screw the board to the base.
4. Assemble front panel and rear panel to the base.
5. Align the top with the base.
6. Screw the parts together from the bottom side of the base using screws.

5.2 Attaching a Wi-Fi Card to the Product

Attaching the Wi-Fi card to the product requires separating the top of the enclosure from the unit, plugging a Wi-Fi card into a mini PCIe slot, installing the antenna cable into the Wi-Fi card, then reassembling the the product.

1. From the left and right side of the assembled unit, remove the eight screws.
2. Turn the unit lid up, plug in the Wi-Fi card, then latch it.
3. Install the antenna cable into the Wi-Fi card connector, then select the proper holes on the panel (4 on rear panel and 2 on front panel) to position the antenna.
4. Re-assemble using Steps 5 and 6 of Section 5.1, "Assembling the Enclosure and Board Assembly ".

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