Layerscape Overview: QorIQ with ARM

Webseminar

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External Use

Agenda

- Layerscape overview
  - Introduction / Roadmap / Positioning
  - Feature overview: LS1021
  - Specific features:
    - Networking
    - Security
    - Virtualization
  - Analog companion chips
    - PMIC, Battery Charger.
  - Enablement Tools
    - Linux SDK
    - CodeWarrior
  - Application Examples

Introducing QorIQ LS1020A, LS1021A and LS1022A

ARM-powered networking has arrived!

Leveraging over 20 years of networking expertise, the ARM-based QorIQ LS1 family is optimized to offer unprecedented efficiency and security, together with the broadest array of high-speed interconnects and features ever offered in a sub-3W networking processor.

Comprehensive Portfolio of Embedded Processors Based on ARM® Technology

Kinetis Microcontrollers

Design Potential. Realized

Industry's most scalable ultra-low-power, mixed-signal MCU solutions based on the ARM® Cortex™-M and Cortex™-M0+ architectures.

- Consumer
- Industrial

Vybrid Controller Solutions

Rich Apps in Real Time.

Real-time, highly integrated solutions with best-in-class 2D graphics to enable your system to control, interface, connect, secure and scale.

- Consumer
- Industrial
- Automotive

i.MX Application Processors

Your Interface to the World.

Industry's most versatile solutions for multimedia and display applications, with multi-core scalability and market-leading power, performance & integration.

- Consumer
- Industrial
- Automotive

QorIQ Processors built on Layerscape Architecture

Accelerating the Network's IQ

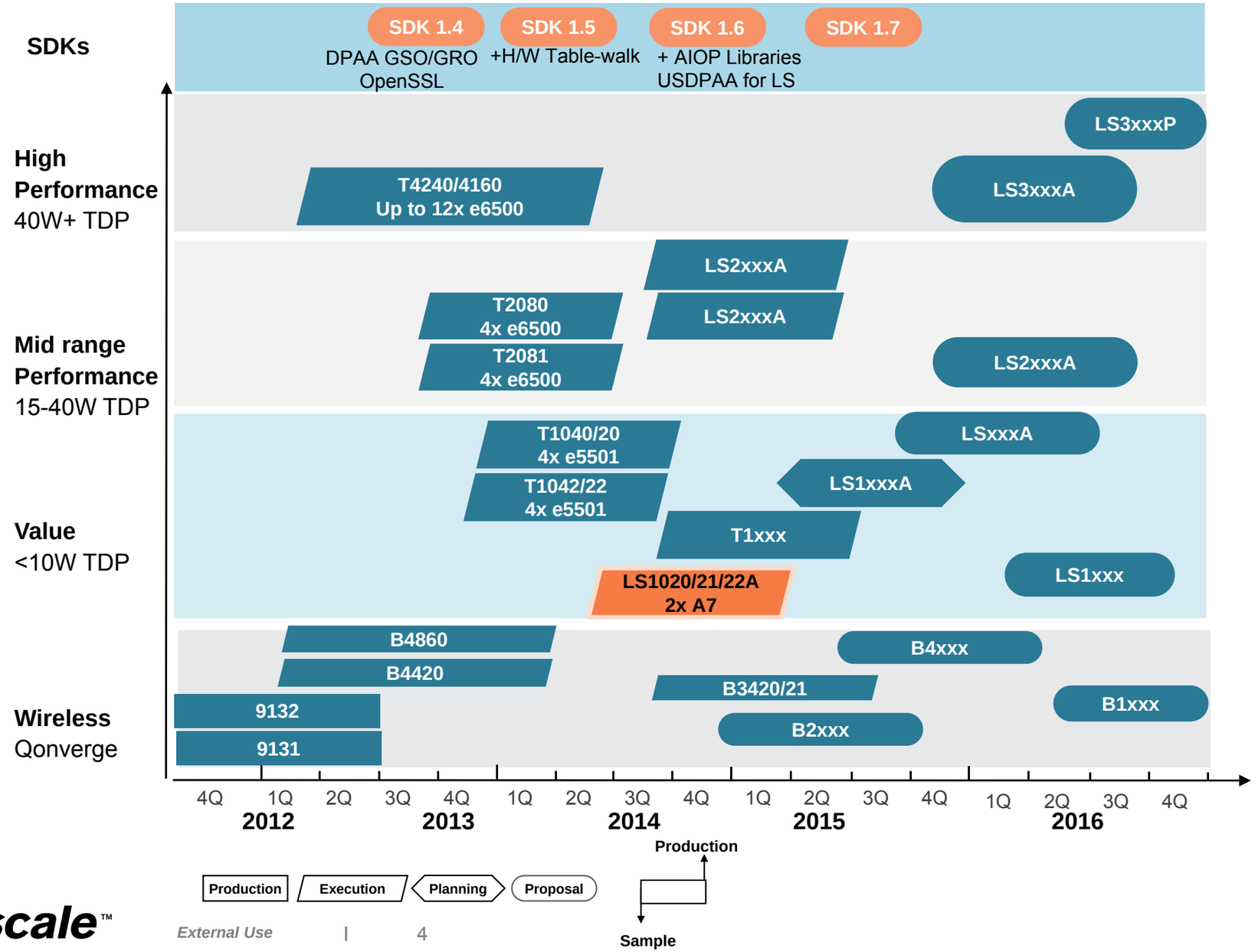
Industry's first software-aware, core-agnostic networking system architecture for the smarter, more capable networks of tomorrow–end to end.

- Consumer
- Industrial
- Networking

Freescale has the industry's broadest range of solutions built on ARM® technology for automotive, industrial, consumer and networking applications.

Find your ideal solution at the price, performance and power level you desire, and leverage the extensive software and tool bundles available to speed and ease your design process.

QorIQ Communications Multicore Roadmap



LS1 Family Overview

Extending our customer reach

ECC | **Virtualization** | **Efficiency** | **Integration**

Highly Efficient	• Delivers 6,000 CoreMark® in under 3 W (Typ) • QUICC Engine for protocol offload
High Reliability	• ECC protection on L1/L2 and all SRAM • Multicore for redundancy
Unmatched Integration	•DDR4, LCD controller, USB 3.0 w/PHY, SD/MMC, CAN and SATA 3

CPU Core *Dual Arm A7 Cores*	**High Reliability** *ECC protection*	**Ease of Use** *Services, Arm and CW tools*	**Robust Ecosystem** *Linux SDK, 5 EBS form factors, 3rd party SW for TTM*

LS1 Family Differentiated Features Overview

Performance starts with the core

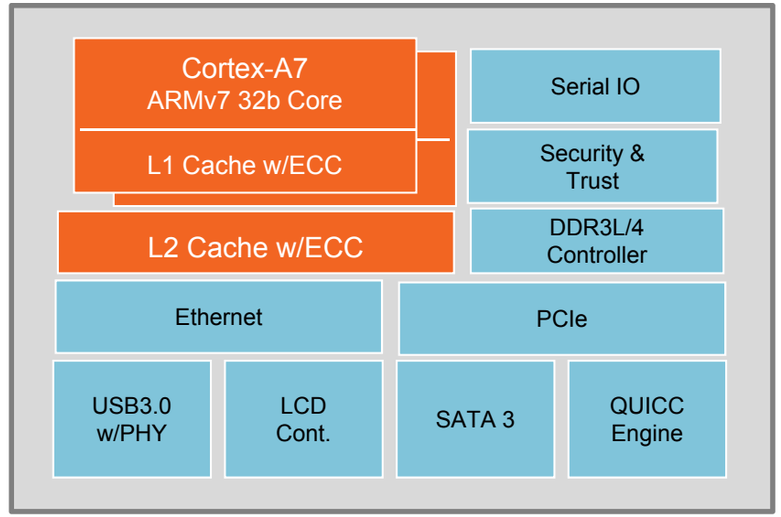
- Dual ARM Cortex-A7 cores delivering **over 5,000 CoreMark®** of performance at **under 3W (typical)** for improved performance without increased power utilization

Defense-in-depth security protection

- **Secure boot**, ARM **TrustZone** and manufacturing protection

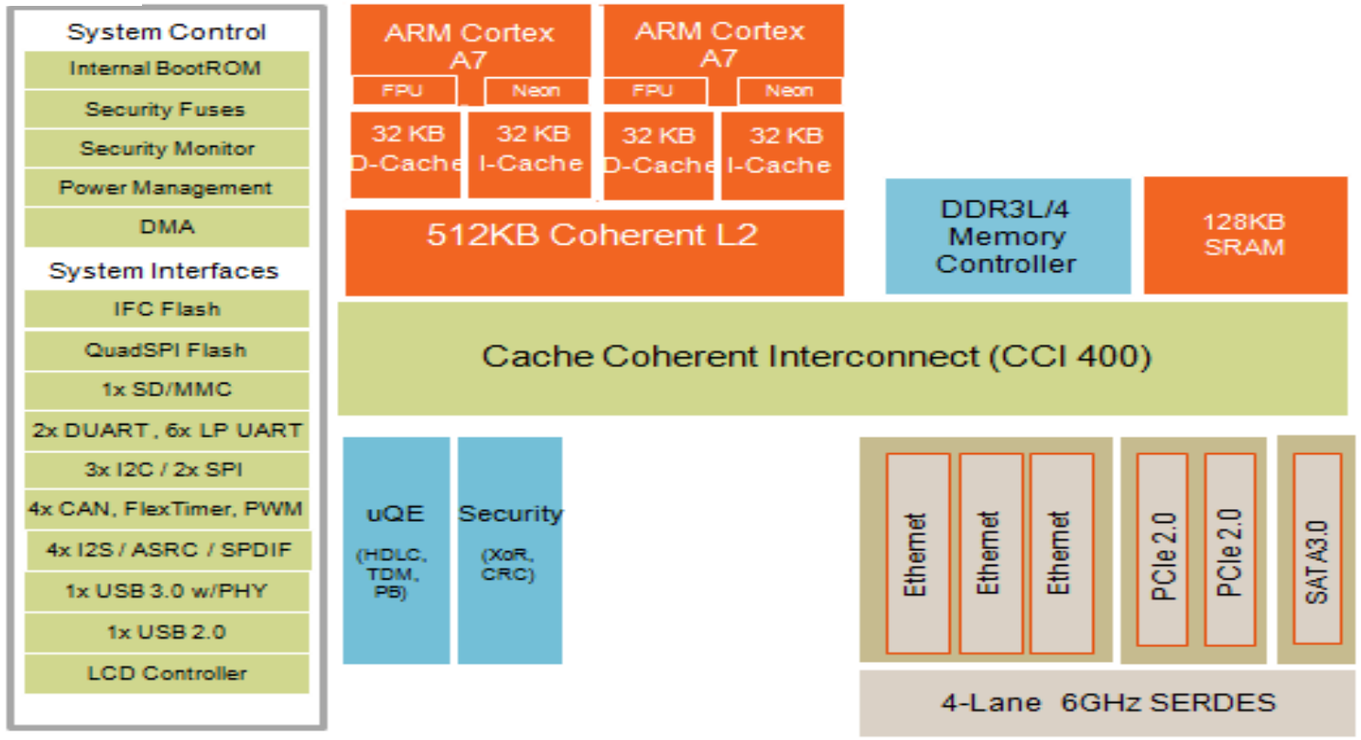
Broadest range of peripheral and I/O features in its class

- Only product in its class to offer **ECC protection** for both **L1/L2 caches,** meeting networking requirements for **high reliability**
- **Virtualization support** enables partitioning of CPU resources on low-power parts for increased system productivity
- **First in its class** to offer support for **DDR4** memory ensuring continued **performance efficiency**
- Only communications processor to combine **LCD controller, USB 3.0 with integrated PHY, SD /MMC and SATA3 on a single SoC** to enable lower system-level costs
- **QUICC Engine** provides **proven support** for protocols required in industrial, building and factory automation applications



LS1 Target Applications
Management processor
Multi-service IOT gateways
802.11ac AP routers
Carrier line cards
Printing & Imaging
Networked attached storage
Industrial Automation & control
M2M
Robotics

QorIQ LS1021A



- **Dual ARM Cortex-A7 cores up to 1.0 GHz**
  - ECC protected L1/L2 caches
  - DDR3L/4 up to 1.6GHz
- **Over 5,000 Coremark at under 3.7W (TDP power)**
- **Industry best Coremark / mW ratio**
- **Outstanding security and IP forwarding**
- **High integration reduces BOM costs** for targeted applications:
  - Industrial gateways
  - Industrial Automation
  - Printing & Imaging
  - HMI
  - M2M, Smart “X”

Key Architectural Features:

- ARM AMBA4 MPCore™ Virtualization
- DDR3L/4 32-bit with ECC support
- 3-port GigE with IEEE 1588
- 2x PCI Express Gen2
- Multi-protocol 4-Lane SerDes
  - PCIe-2, SATA3, SGMII
- QUICC Engine – HDLC/TDM/ProfiBUS
- EnergyStar support with fast wakeup
- 2Gbps IP forwarding

Key System Integration Features:

- Low-cost NAND/NOR flash systems
- Low-cost DRAM systems
- USB3 SuperSpeed
- Audio networking and motor control
- QorIQ Trust Architecture and ARM TrustZone support
- Alignment with Kinetis/Vybrid portfolio

Package & Board:

Package:	525-pin, 19x19mm, 0.8mm ball pitch
Power:	~2.8W @1.0GHz Typical
Temp:	-40C (TA) to 105C (Tj)
Boards:	Tower low-cost board Freescale Linux BSPs

LS102x Product Family Snapshot

	LS1021A	LS1020A	LS1022A
Core Type	ARM Cortex™-A7 MPCore™ + NEON		
Cores/Threads	2 / 2		
Frequency	Up to 1GHz		Up to 600MHz
L1 I/D	32kB / 32kB with ECC		
L2 (Unified)	512kB Shared with ECC		
SRAM	128kB with ECC		
DDR	1x(16/32B +ECC) DDR3L/4 up to 1.6GT/s		DDR3L (8/16B) up to 1.0GT/s
SerDes	4x up to 6.0GHz		1x up to 5GHz
Ethernet	3 x 1GE		2 x 1GE
PCIe	2 x Gen 2.0 (up to 5.0GT/s)		1x Gen 2.0
SATA 3.0	1 up to 6.0GHz		No
USB	1 x USB 3.0 and 1 x USB 2.0		1 x USB 2.0
CAN	Up to 4		Up to 4
TDM/HDLC	2		No
UART/I²C/SPI	Up to 8 / 3 / 2		
I²S	Up to 4		
LCD	1 x Controller	No	
Acceleration	SEC,QE		SEC
	Trusted architecture		
	Pin Compatible 19x19mm, 0.8mm pitch		

LS1020 Family:
All feature Dual Cortex A7 Cores

freescale ™ LS1020	freescale ™ LS1021	freescale ™ LS1022
Networking	**Industrial Printing**	**Entry Consumer & Industrial**
• Up to 1GHz • 2.1W Typ.	• Up to 1GHz • 2.2W Typ. • Adds LCDC • Adds CAN	• Up to 600MHz • 1.6W Typ.

ECC and Trust on Board
Pin & Software Compatibility

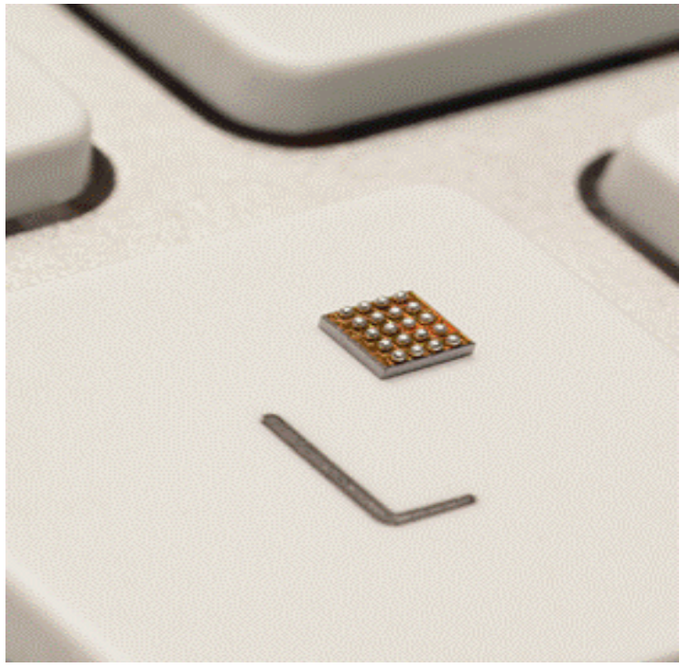
LS102xA Performance Strategy

Key design objective of LS1 family is to deliver the highest level of performance and integration within a sub-4W total design power (TDP) envelope

- Theoretical peak DDR bandwidth: 6.4GByte/s (32-bit * 1.6GHz data rate)
- Theoretical internal bus bandwidth: 4.8GByte/s (128-bit * 300MHz)
- IPfwd: 2Gbps at IMIX packet size
- IPSec: 1Gbps at IMIX packet size
  (up to 2Gbps at large packet size)

- *NOTE: All performance targets for LS102x are pending actual benchmarking in silicon, these numbers are preliminary and subject to change*

LS1 Family Customer Enablement Boards



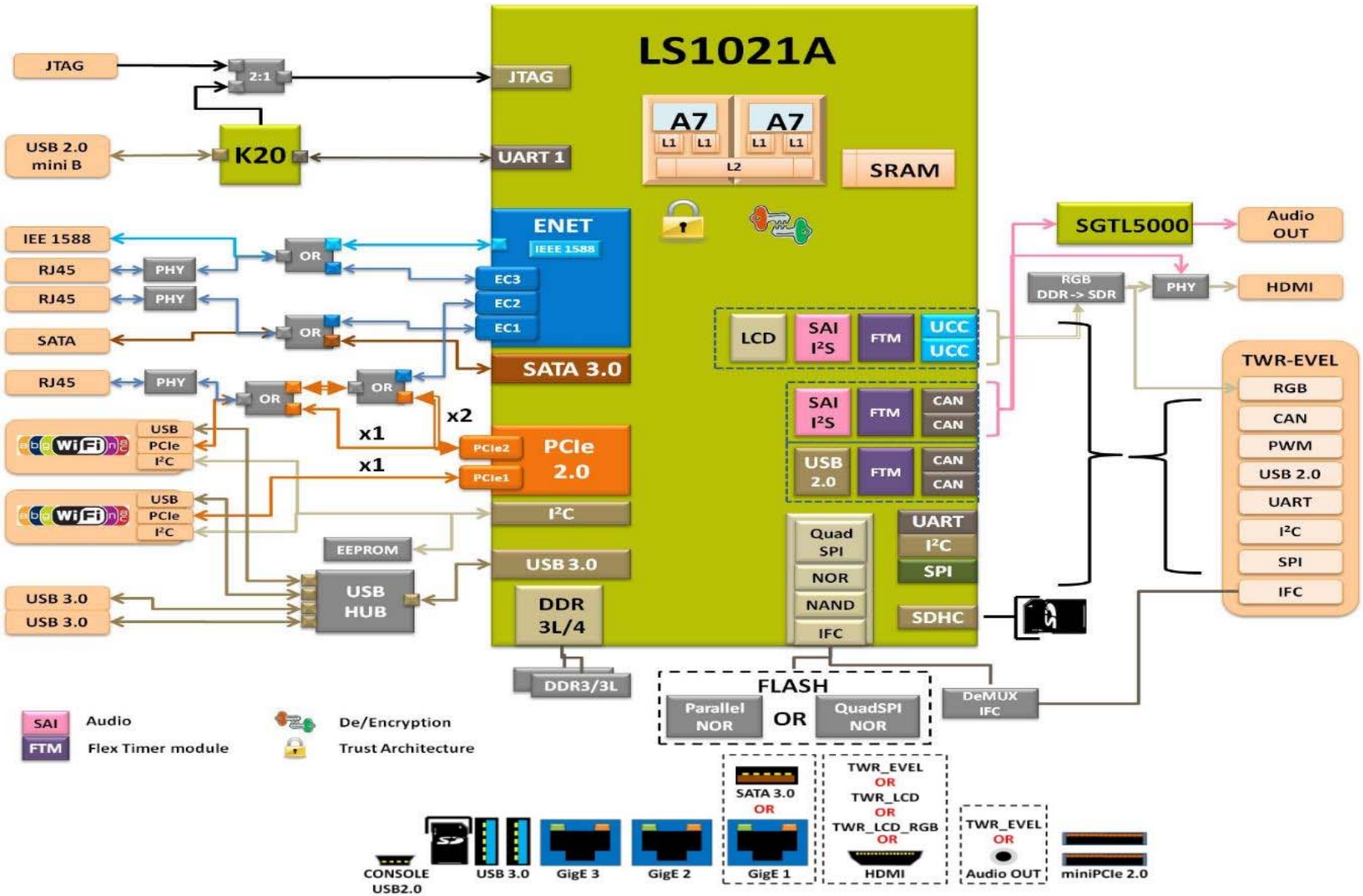
Tower-based Evaluation Platform

- **Rapid prototyping platform** for Industrial applications
- **Modular design** supports a range of connectivity options
- **Cost-effective**, open source development platform
- Designed to **simplify product evaluation**

IoT Gateway Reference Design

- **Multi-protocol support** for IoT devices
- **High speed WAN / LAN** for Cloud connectivity
- **Cost-effective**, open source development platform
- Designed to **accelerate time to market**

TWR-LS1021A Development System



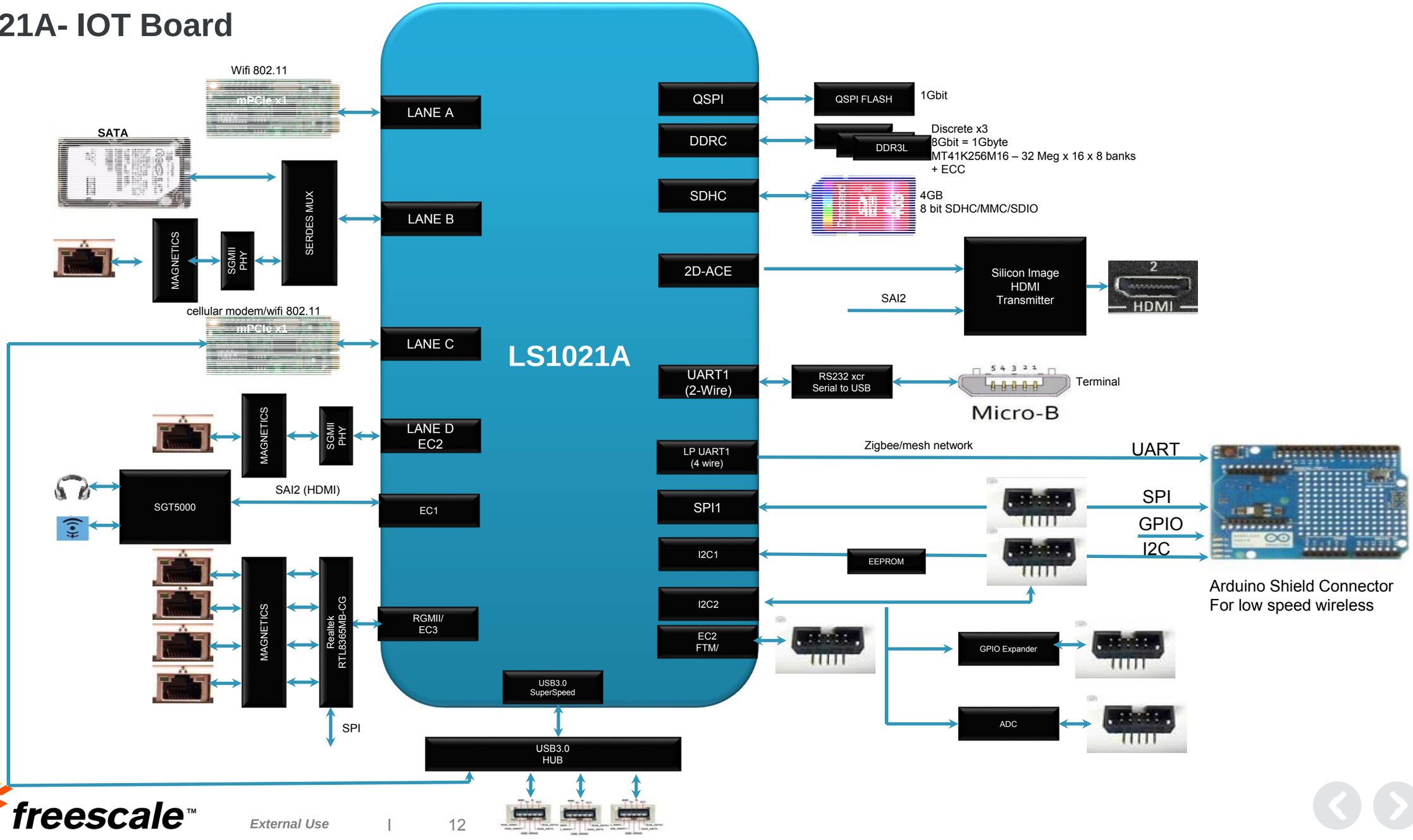
Generic Connectivity Availability

Features

- **Memory**
  - DDR3 1GB
  - Parallel NOR Flash 128MB
    or
    QuadSPI NOR Flash 16MB
- **Connectivity**
  - Up to 3 x RJ45 GigE
  - Up to 1 SATA
  - 2 x USB 3.0
  - 2 x mini PCIe 2.0 (x1 + x1) or (x1 + x2)
  - Display via HDMI or TWR-LCD or TWR-LCD-RGB
  - Audio OUT via HDMI or Jack plug or TWR_EVEL
  - Console port/JTAG via USB 2.0

- **Tower Boards supported via TWR-EVEL**
  - TWR-IND-IO
    2 x CAN, RS485, RS232
    up to 2 boards supported
  - TWR-LCD
  - TWR-LCD-RGB
  - TWR-ETHERCAT-SLV

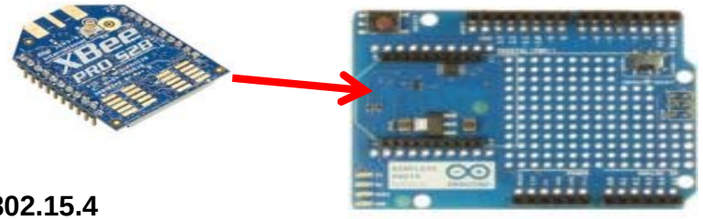
LS1021A- IOT Board



Illustrative Arduino Modules

Arduino Wireless Proto Shield

XBee® Module



XBee® ZB
XBee-PRO 802.15.4
XBee Wi-Fi
XBee® DigiMesh® 2.4

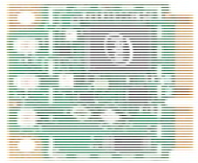
Arduino GSM Shield

Arduino Proto Shield

Mini PCIe modules

Cellular Modem

Wifi (half size module)



Wifi (Full size module)

LS1021 Networking

Virtualized Enhanced Triple-Speed Ethernet Controller

Additional hashing logic to aid in packet distribution

Code compatible with PQ-III TSEC

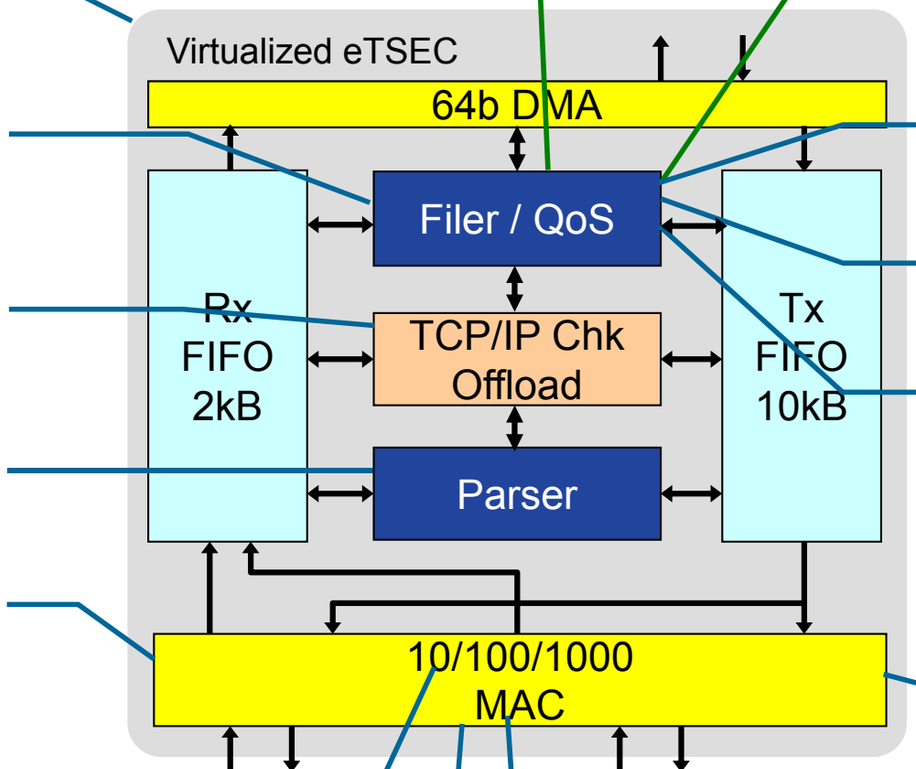
Support for weighted round robin and strict priority queueing

TCP/IP checksum offload for RX and TX

IPv6 and Magic Packet support

FIFO I/F to ASICs - 8/16-bits @ OC-48 rates and above

RMII Interface Support added



SGMII Interface Support

IEEE1588 Hardware Support

QoS support for 8 Rx and 8 Tx H/W queues, with queues individually assigned to any core

Programmable IP header alignment

Customizable per-packet rejection

Customizable per-packet filtering/filing to 64 logical receive queues.
Examples: 802.1p, IP TOS, Diffserv classification, TCP/UDP ports, etc.

Layer 2 features:
- VLAN insertion and deletion per frame
- 16 exact-match MAC addresses
- Increased hash table address matching

VeTSEC Benefits

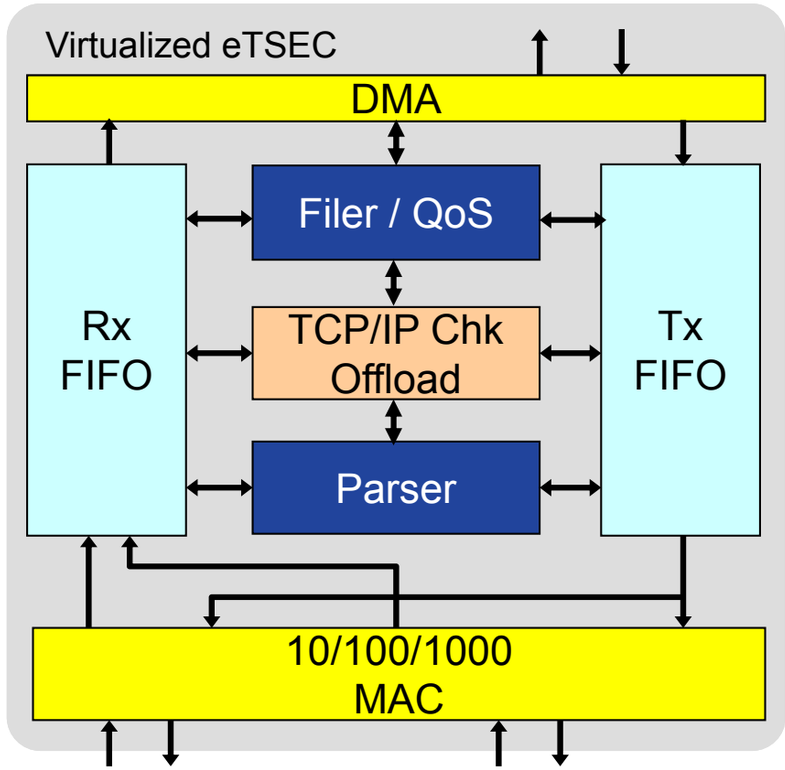
Summary:

- VeTSEC as per Freescale QorIQ P10xx products.
- 3 Ethernet MACs, supporting RGMII (3), SGMII (2) and MII (2) interfaces

- Programmable Protocol classification (5-tupple) for protocols such as IPv4, IPv6 and TCP/UDP
- Offload Checksum operations to accelerate TCP/IP stack performance
- Bandwidth Scheduling - Modified Weighted Round Robin (MWRR) to manage bandwidth allocation for multiple transmit queues
- Programmable quality of service rules per Ethernet port to support differentiated services
- Programmable firewall strategies based on high-level protocol identification
- Virtualization of Interrupts - Interrupts can be steered to any CPU core reducing software overhead and improving performance
- Advanced Hashing logic - Enables load balancing of traffic across CPU cores for improved performance
- Queues can be individually assigned to any CPU core – reduces software and CPU overhead for improved performance
- IEEE1588 hardware support

Packet Classification

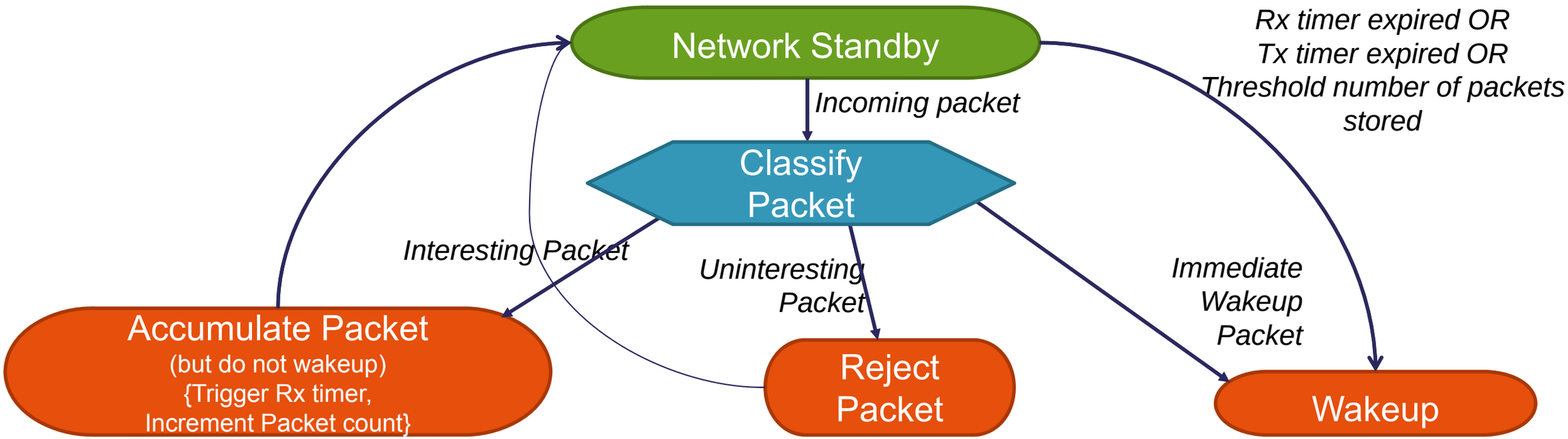
- Network Controller with Receive Filer
  - Inspect and classify incoming packets
  - Drop packets that don't need to be processed
    - Packets destined for other IP addresses
    - Safely ignorable packets
      - E.g. router multi-cast traffic
  - Accept packets that need processing
    - E.g. ARP packet for correct address
    - Write packet to DDR and wake system.



Virtualized Enhanced Triple Speed Ethernet Controller (VeTSEC) on Freescale LS1020A

Packet Accumulation

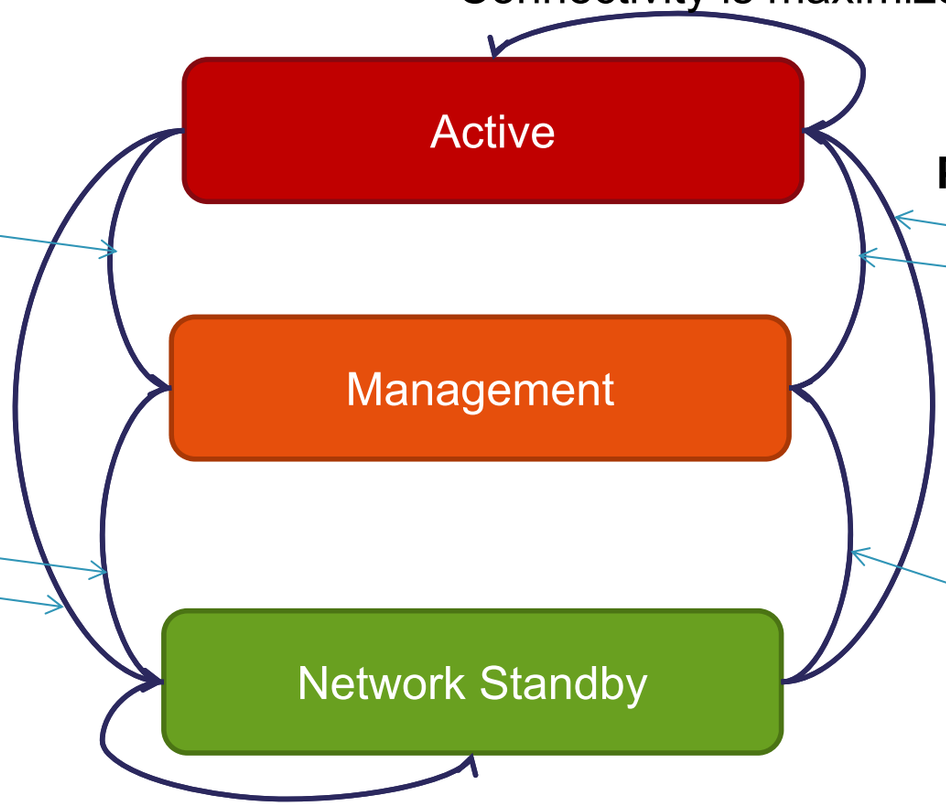
- Extension of Packet Classification, plus:
- Minimize frequency of wakeup events
  - Software may take seconds to re-initialize
  - Therefore solution is to process multiple packets per wakeup



Network Standby with LS102xA

Primary Application Running
· Performance is maximized
· Connectivity is maximized

Management Request
·Decrease CPU freq.
· Disable some I/O



Primary Application Request
· Restore state
· Restore power
· Increase CPU frequency

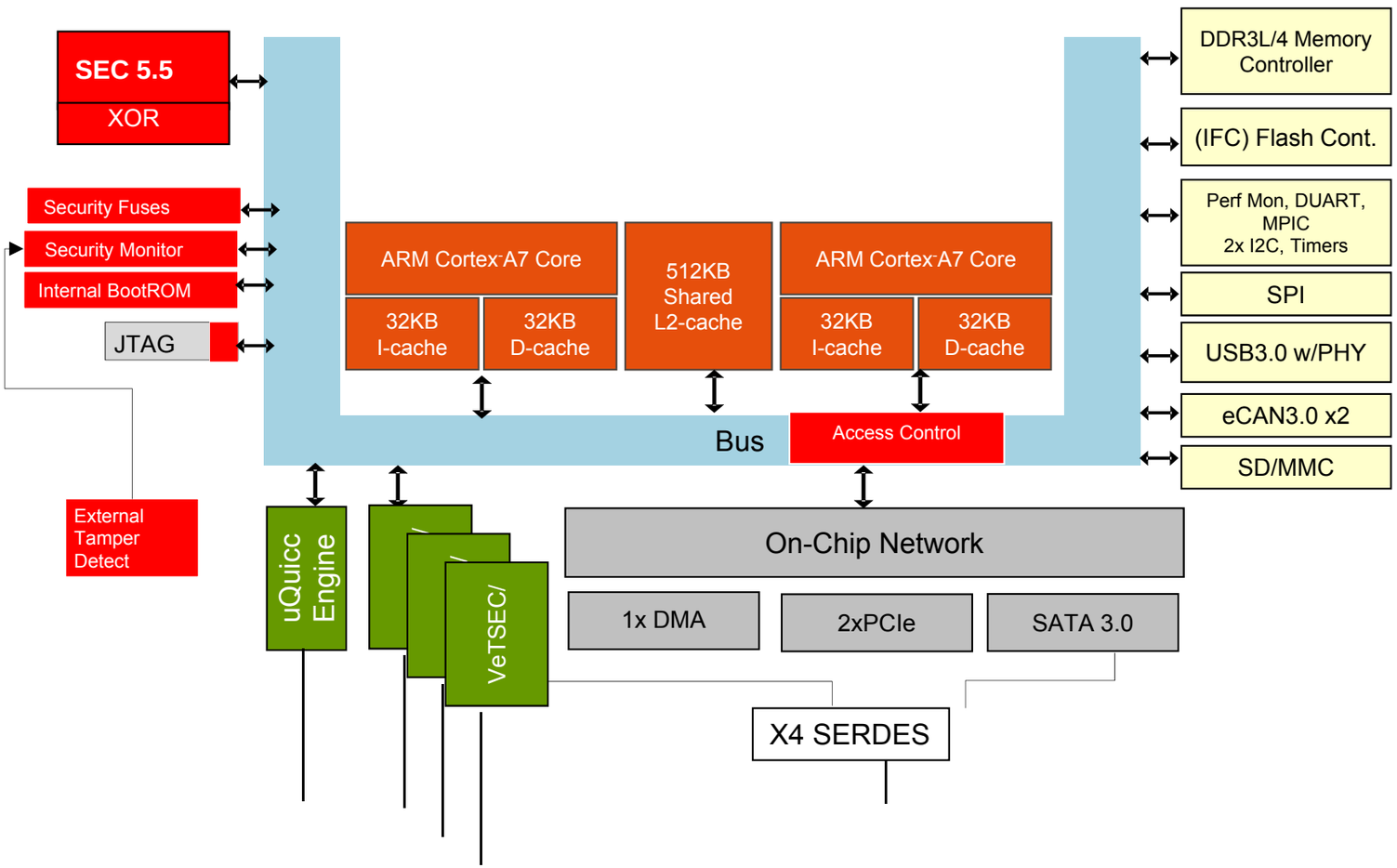
No more work
· Save system state.
· Remove power to non-essential components.

Management Request
· Restore power as needed

No useful work
· Performance is zero
· Connectivity is maintained

Security

Layerscape™ LS1020A Trust Architecture



Layerscape devices with ARM CPUs offer:

- Secure Boot
- Secure Debug
- Tamper Detection
- Memory Access Control
- Peripheral Access Control
- Cryptographic Blobs

  +

- ARM TrustZone ‘Secure World’
- Manufacturing Protection

LS102xA Security Engine Overview (SEC 5.5)

(1) Public Key Hardware Accelerator (PKHA)
- RSA and Diffie-Hellman (to 4096b)
- Elliptic curve cryptography (1024b)
- Supports Run Time Equalization

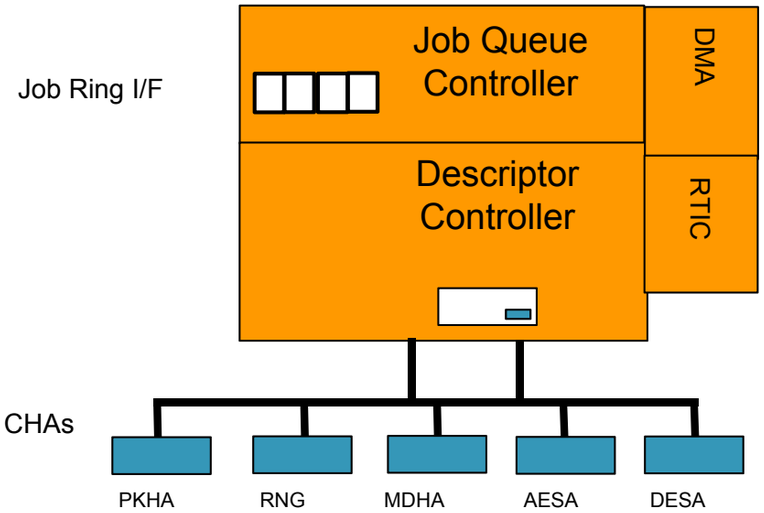
(1) Random Number Generator (RNG)
- NIST Certified
- RNG supports key generation algorithm

(1) Message Digest Hardware Accelerators (MDHA)
- SHA-1, SHA-2 256,384,512-bit digests
- MD5 128-bit digest
- HMAC with all algorithms

(1) Advanced Encryption Standard Accelerators (AESA)
- Key lengths of 128-, 192-, and 256-bit
- ECB, CBC, CTR, CCM, GCM, CMAC, OFB, CFB, and XTS

(1) Data Encryption Standard Accelerators (DESA)
- DES, 3DES (2K, 3K)
- ECB, CBC, OFB modes

(1) CRC Unit
- CRC32, CRC32C, 802.16e OFDMA CRC



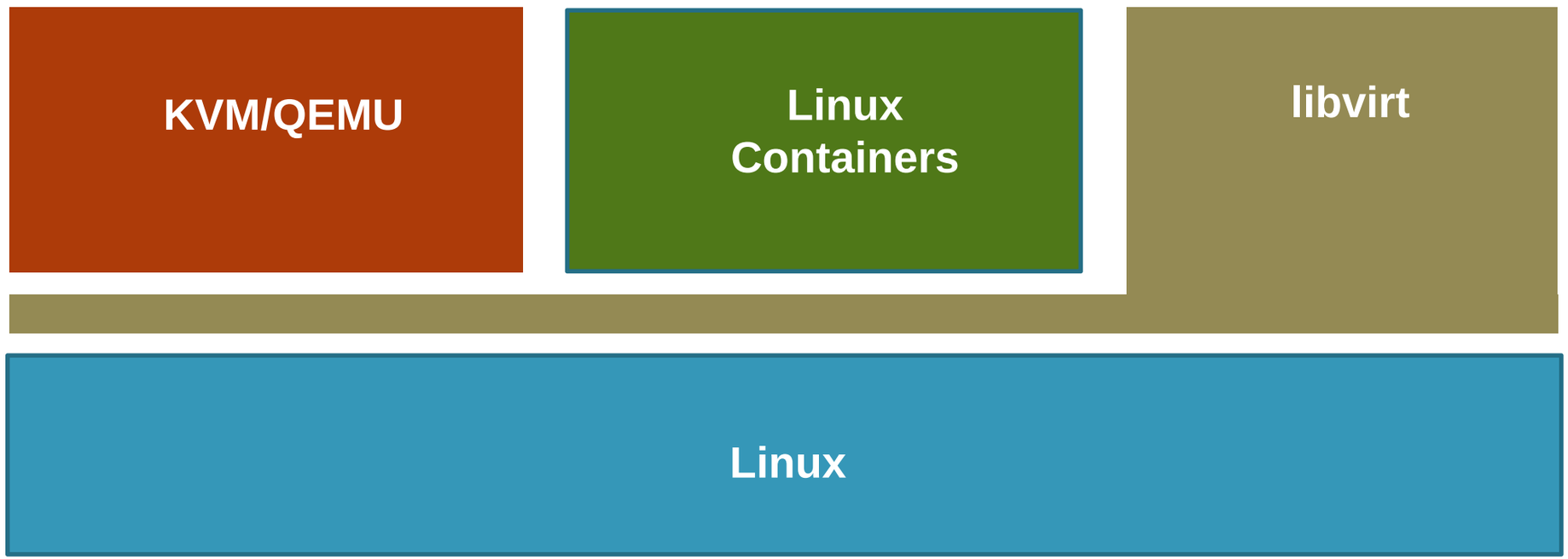
Header & Trailer off-load for the following Security Protocols:
- IPSec
- SSL/TLS
- 3G RLC
- PDCP
- SRTP
- 802.11i
- 802.16e
- 802.1ae

IPsec throughput performance:
- 64B: 0.5Gbps
- 390B: 1.6Gbps
- 1456B: 2.1Gbps

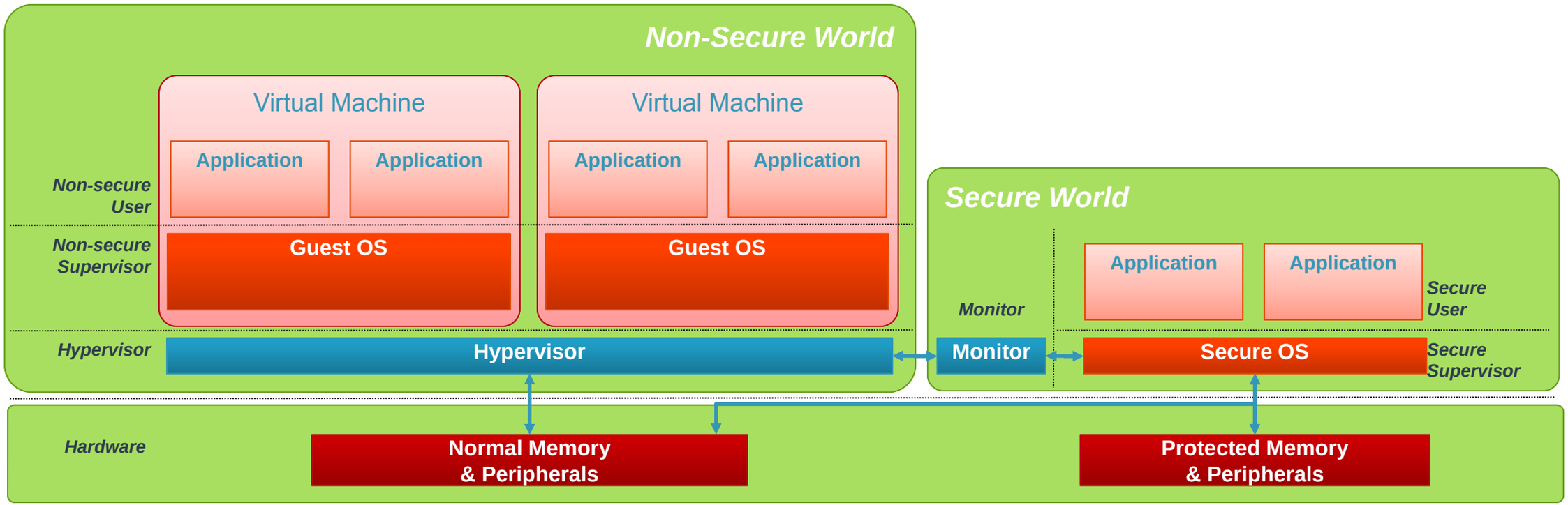
Virtualization

Freescale – Software Virtualization Technologies

Freescale strategy is to enable and offer standard Linux-based virtualization technologies across Power and ARM based SoCs – with superior I/O capabilities



Virtualization – CPU modes

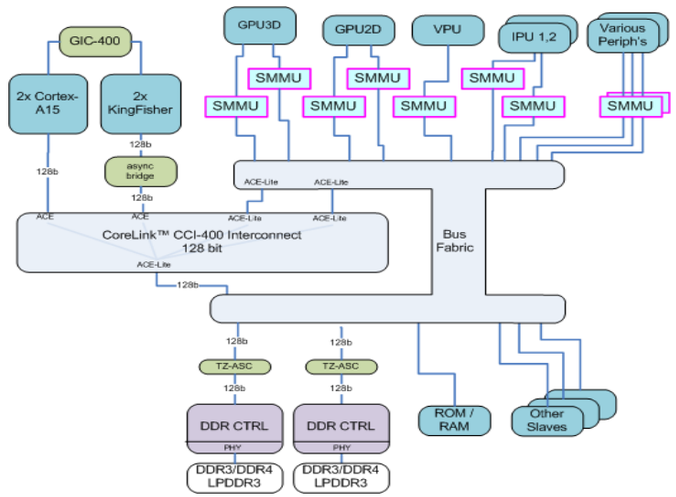


Virtualization Support by S-MMU

- System-MMU for 2nd stage translation of Intermediate Physical Address (IPA) to Physical Address (PA) addresses
- Analagous concept to PAMU on QorIQ P3/P4/P5

- Benefits of using System MMU's for virtualizations are:
  - Full HW Virtualization support (a.k.a. "IO Virtualization")
  - Better performance than SW virtualization ("Para-Virtualization")
  - Simpler (thus faster) porting of the Virtualized ("guest") OS
  - Support for >4GB address space, for 32-bit bus masters

- S-MMU features:
  - Up to 64 TLB entries in TLB cache
  - Address translation in HW, for best performance
  - TLB size configurable, to best suite each master needs

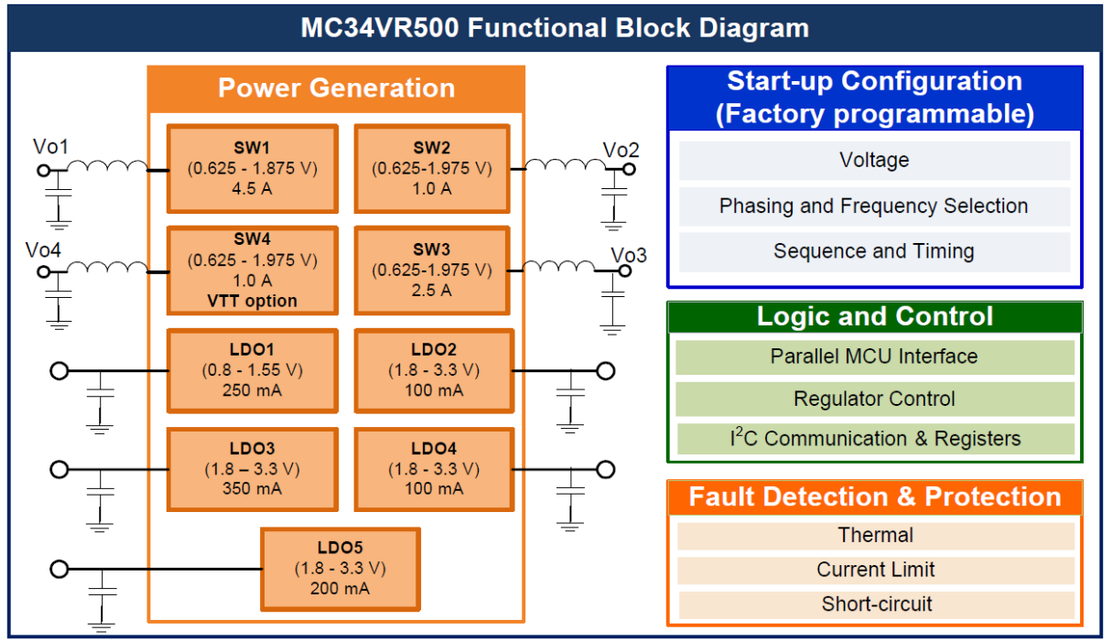


34VR500 Power Management

MC34VR500: Power Solution for Network Processor Systems

Differentiating Points

- Optimized to work with LS1, T1 network processor systems,
- High full load efficiency with 91% peak
- Pre-programmed output voltages, sequencing, and timing available
- Dynamic regulator control via I2C
  - Voltage, Current Limit, Frequency
- Power control logic with processor interface and event detection
- I2C interface
- **TA: - 40 to 105°C, TJ: - 40 to 125°C**
- **Qualified AEC Q100 grade 2**

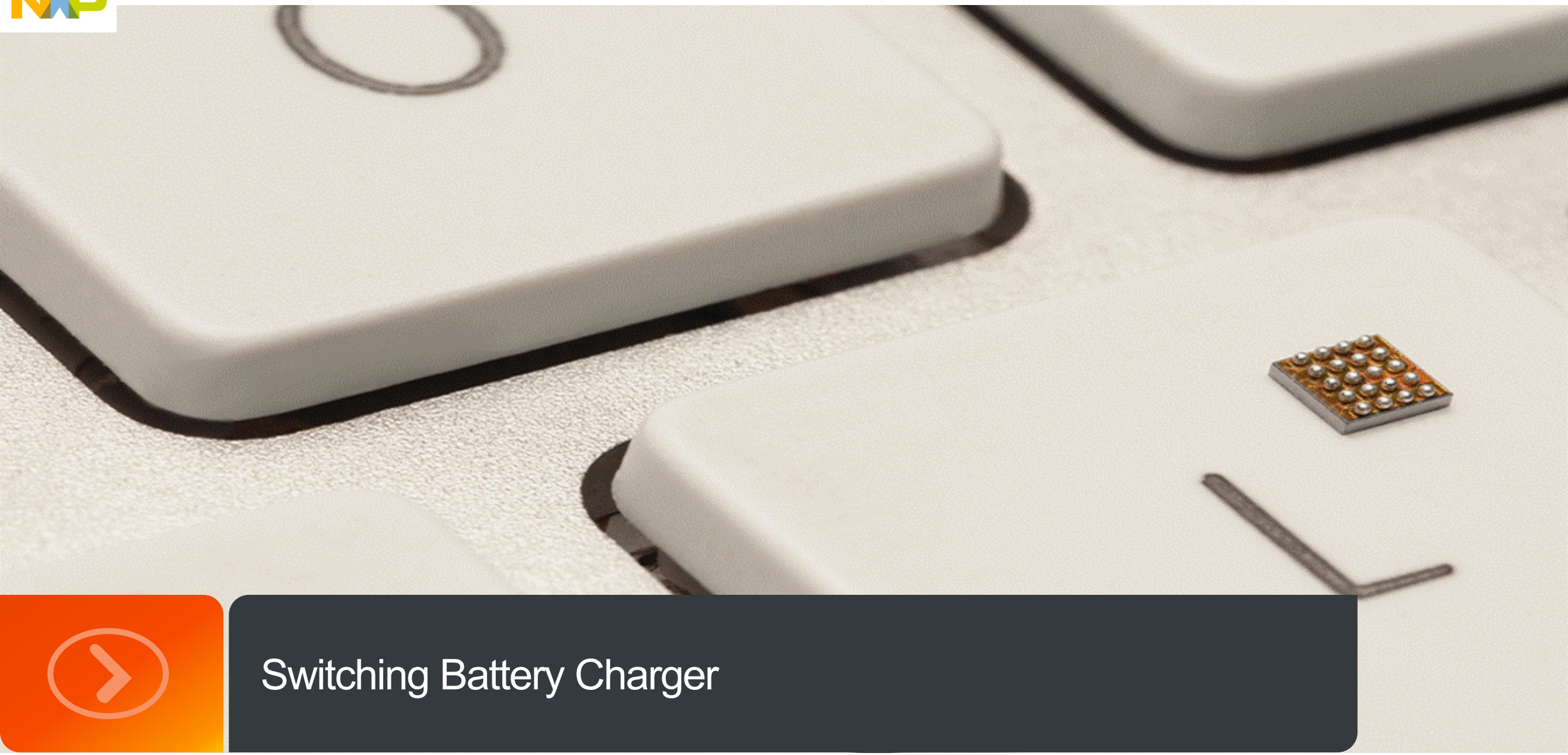


Product Features

- Vin = 3.7Vbus Supply (2.8V to 4.5V)
- Four independent buck converters
- Five user programmable LDOs
- DDR reference LDO
- Forced PWM/PFM or APS operation
- High power 8x8 mm QFN wettable flank package

Applications

- IoT Gateway
- Mobile Wireless Router
- MFP Printer
- Network Attached Storage
- Automatic Teller Machine
- Industrial computing



Switching Battery Charger

MC32BC3770: 2A Switch Mode Dual-Path Li-Ion Battery Charger

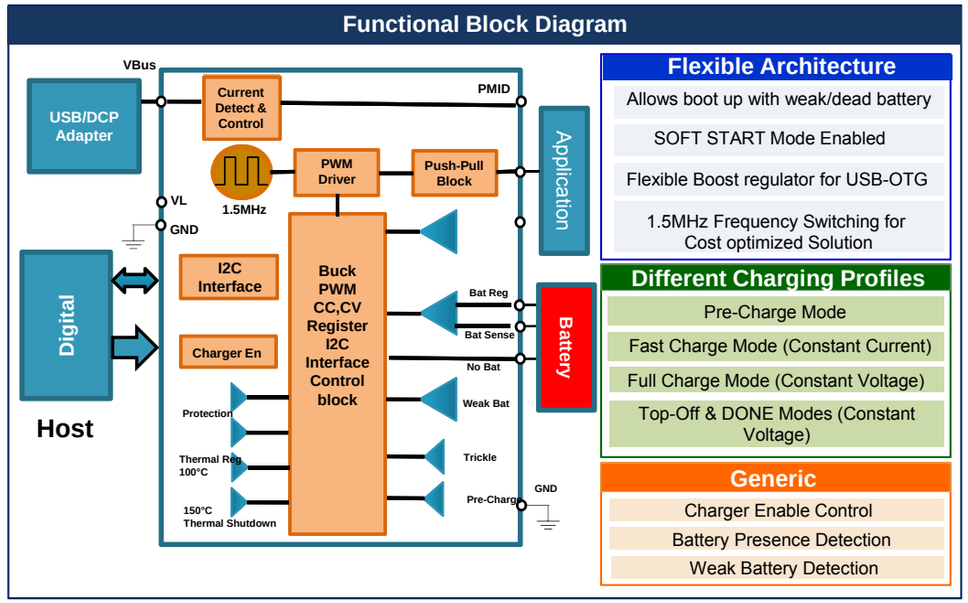
Single input, 20 V tolerant high efficiency 1.5 MHz synchronous switch-mode charger with programmable charge parameters, fast charge capability, and USB-OTG operation

Differentiating Points

- Dual-Path outputs with 30mΩ switch for powering system while charging battery
- 2A maximum charging current
- 20V tolerant single input USB/DCP adapter
- Small footprint with 1.5MHz switching
- Four charging modes, including fast charge

Product Features

- Boost mode for USB OTG: 5.0 – 5.2 V, programmable @900 mA
- High speed USB2.0 compliant
- 4.1- 4.475 V ±0.5V battery voltage programmable in 25mV steps
- Programmable through I^2C interface
- Operating Temp: -40degC to +85degC
- 25-pin 2.27 x 2.17 mm WLCSP Package, 0.4 mm pitch



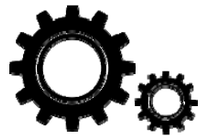
Applications

- IoT Products
- Handheld consumer devices
- Wearable
- mPoS Terminals
- Medical portable equipment
- Consumer Tablets

Software tools for LS1021

Networking Software and Services Group

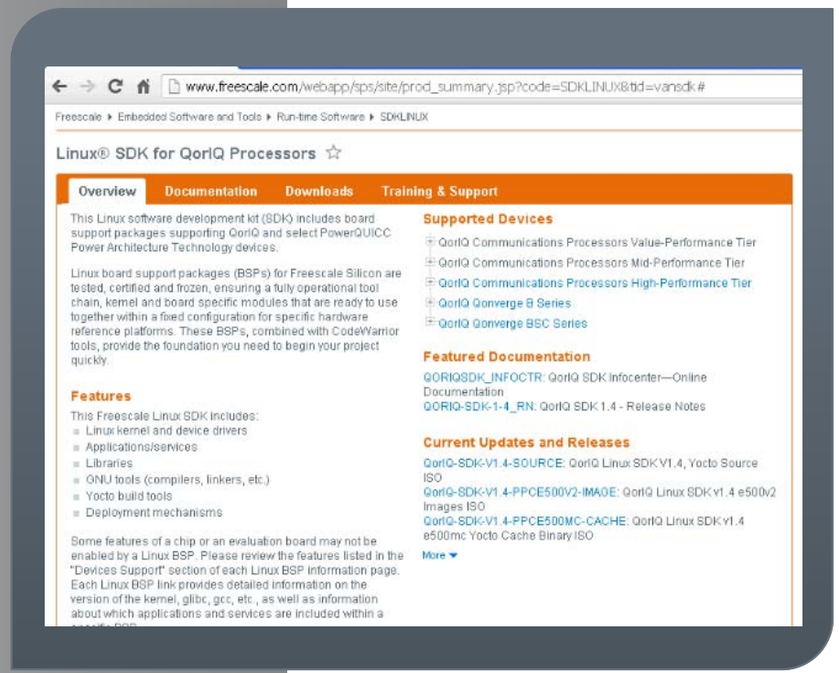
Software Products and Custom Services

Development Tools	Runtime Products	Solutions Reference	Linux® Services	Integration Services
• CodeWarrior – IDE – Debug – Compiler – Trace • QorIQ Optimization Suite – Scenarios Tools – DDrV	• Vortiqa Software Products – Application Identification Software (AIS) – Open Networking Switching Framework – Mobile Transport	• Storage Controller • SDN Switch • Wireless LAN • Data Concentrator • Smart Converged Gateway • Digital Signage	• Commercial Support • Frozen Branch • Application Specific Hardening • Feature Acceleration	• Systems Consulting • Design Services • Porting • Migration
CodeWarrior QorIQ	VortiQa			

Linux SDK

Freescale Networking Linux SDK

- Linux Software Development Kit (SDK) for Power Architecture®
  - Optimized Linux software
    - Complete range of QorIQ and PowerQUICC platforms
    - Hardware accelerated
  - Rigorous testing
    - Multiple configurations, Host OSes
    - Performance tuned
  - Flexible AMP/SMP support
  - Yocto-based
  - Bi-annual update
  - No-cost download
- http://freescale.com/sdk

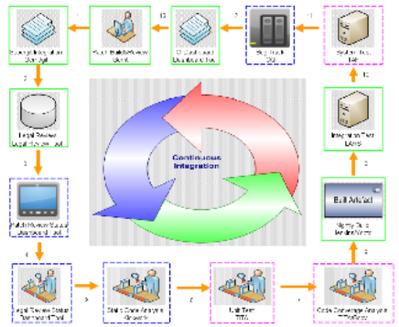


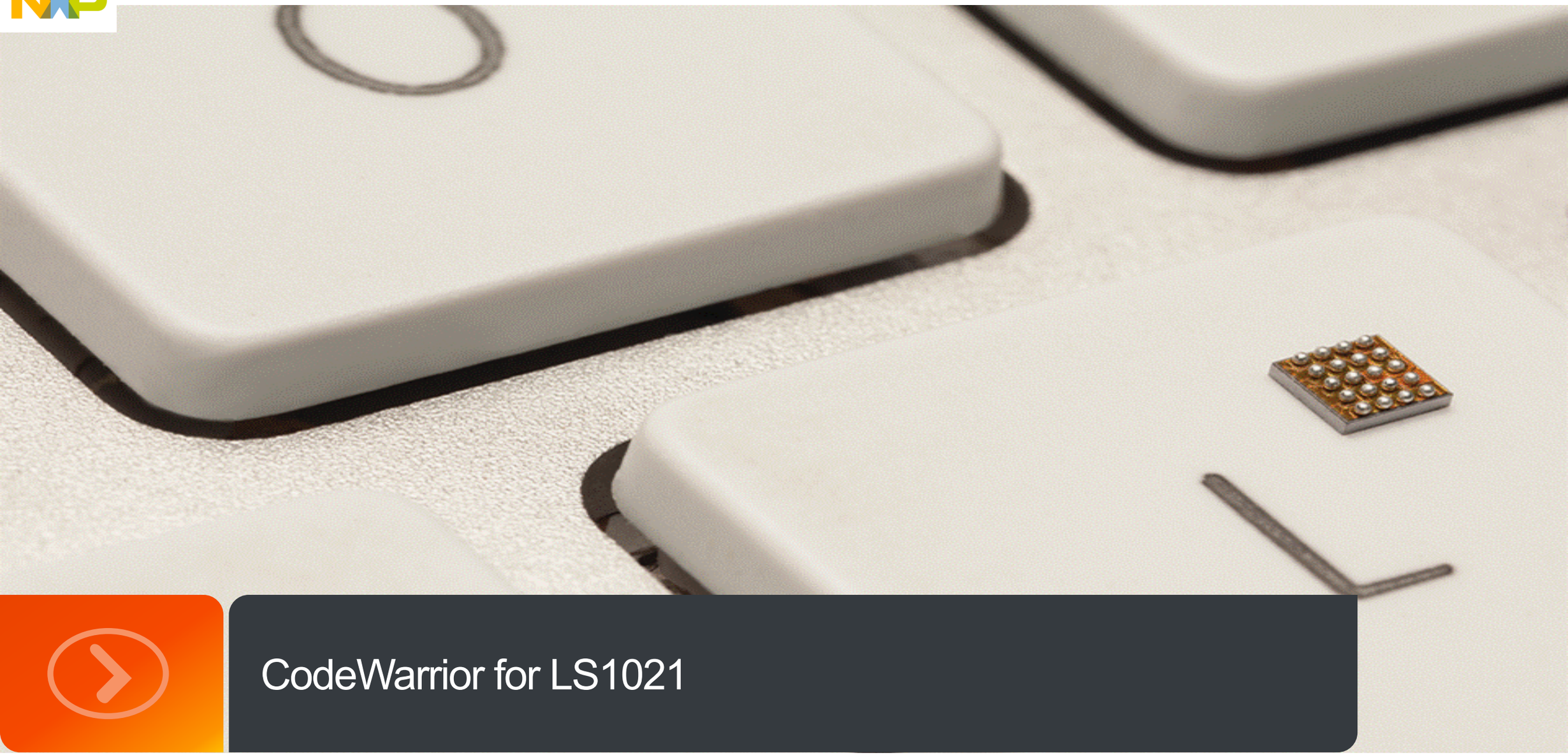
Freescale SDK Support Offerings

- Freescale SDK is provided “as is” with the comprehensive support plan
  - SDK includes source code for easy debug
  - Linux has vibrant/active open source community
    - Freescale engineers respond to community inquiries
  - Freescale communities (community.freescale.com)
  - World-class ecosystem—Freescale Connect Program (freescale.com/partners)
  - Technical service requests (freescale.com/support)
  - Global Field Applications Engineering

Freescale SDK Highlights

- Freescale Linux Investment
  - Hundreds of man-years per year
  - Global Board Farms
  - Top 15 Company Contributor to `kernel.org`
  - Systems Designed, Tightly Integrated with Freescale SOC
  - Systems Validated - Tightly aligned with Freescale NPI
- Quality
  - ISO-9000 Quality Processes – Externally Audited
  - On-going Maintenance, regular kernel updates (LTSi)
  - Open Source Compatible – Upstreamed, Dedicated Team
    - Standards based – Yocto
- Ease of Use
  - Combined P, T and Layerscape support in unified SDK
  - Common Kernel Across support platforms





CodeWarrior for LS1021

CodeWarrior Development Suites for Networked Applications

Developer Level

- QorIQ LS Series for ARMv7
- QorIQ LS Series for ARMv8
- Packet Processing Development
- CPU only Performance Analysis
- StarCore DSP
- Power Architecture

Specialist Level

- Board Bring up Specialist Tools
- SoC Performance Analysis
- LS1 ARM Core Trace

Architect Level

- Trace
- Ethernet Communication Analysis

Architect Level offers no additional value for LS1 customers

- Trace for LS1 is included in the specialist level
- No Ethernet Communication Analysis Tools are available for LS1

CodeWarrior Development Studio

A Complete Development Environment Under Eclipse

- **Eclipse IDE**
  - Configuration Wizards
  - Plug-In Architecture
  - 3rd party community

- **Build Tools**
  - C/C++ Compiler

- **Initialization Tools**
  - SOC platform initialization and configuration

- **Run Control**
  - CW-TAP

- **Debugger**
  - Multicore aware
  - Cross-triggering
    - Run/Stop of targets simultaneously
  - Access to all on-chip resources
  - Linux awareness

- **Software Analysis - Trace & Profile**
  - Leverages chip capabilities
    - Profiling Unit
    - In system trace buffering
  - Trace / Code / Performance Viewer
  - Offline trace visibility

CodeWarrior Development Suites for Networked Applications
JTAG Probe Options

- CMSIS-DAP*
  - TWR-LS1021A kit feature support at no additional cost
  - full CodeWarrior run control support
  - basic JTAG download speed
- CodeWarrior TAP
  - full CSS JTAG debug and CodeWarrior run control support
  - premium JTAG download speed
  - serial port pass through
  - operate locally over USB
  - operate remotely over Ethernet
  - buy separately (below $500)
- Reminder : no USB-TAP support !

***CMSIS-DAP Cortex Microcontroller Software Interface Standard – Debug Access Port**


CodeWarrior for ARMv7
Configure
Build
Debug
Trace and Analysis

QCVS: Dissecting the Acronym

- Configuration of QorIQ processors is increasing in complexity
  - **Q**orIQ - All QorIQ SoCs, including Qonverge and LS
  - **C**onfiguration - Tools for *manually* defining a configuration for key SoC HW and SW features
  - **V**alidation - Tools for verifying and/or optimizing a configuration
  - **S**uite - All these tools under one app, in one framework (Eclipse + Processor Expert)

- How is QCVS different than QCS? **It isn't.**
  - QCVS = QCS + DDR Validation Tool
  - One release; one distribution; one installation. Simplicity is king.
  - 4.0 was first QCVS release. Previous was QCS 3.0.5 and DDR Validation Tool 2.0.2
  - Now bundled with CodeWarrior

QorIQ Configuration and Validation Suite

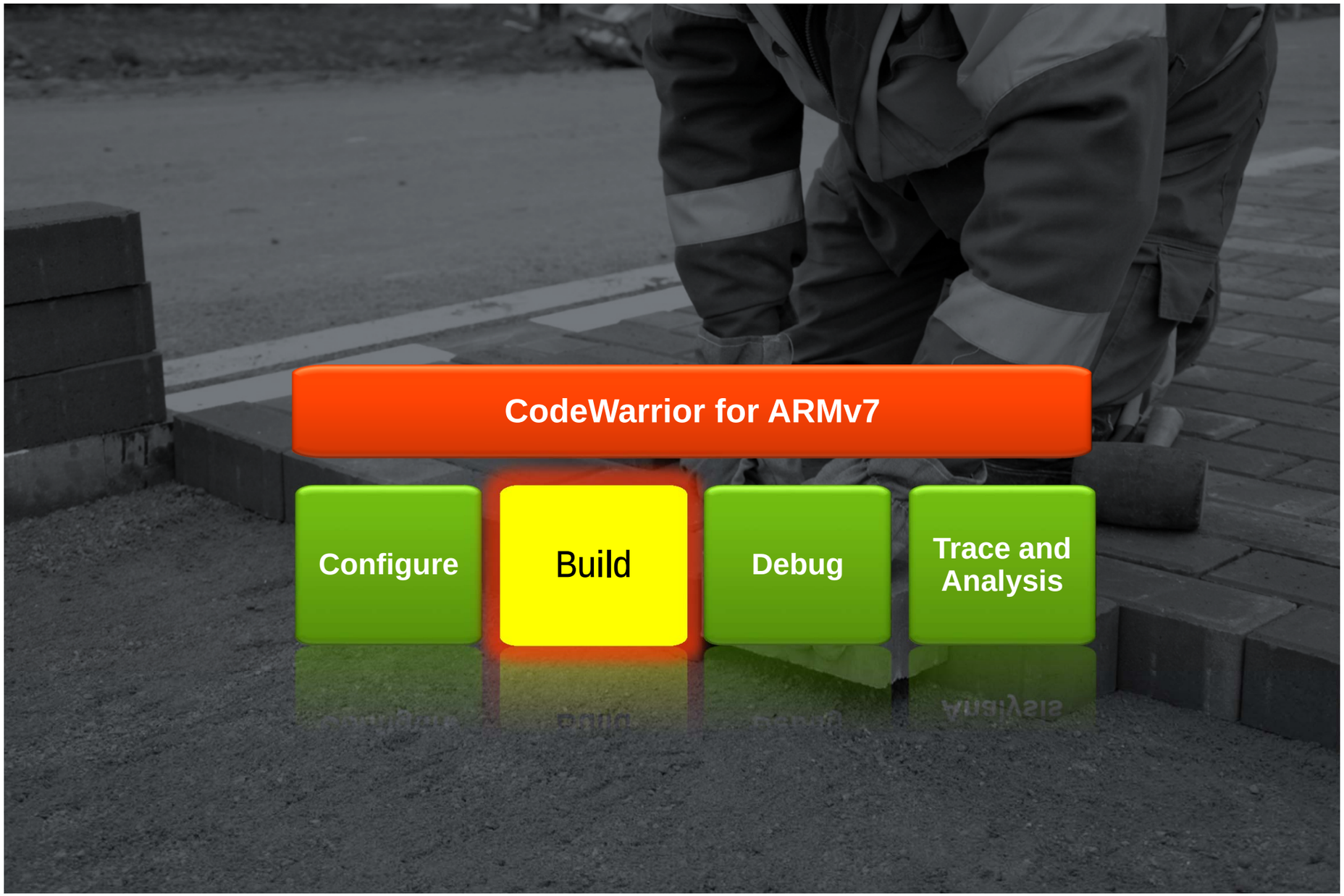
The configuration tools help you configure key HW and SW features in QorIQ designs

- **Pre-boot loader / RCW configuration**
  Configures RCW and PBI
- **DDR Configuration Tool**
  Configures the DDR controllers
- **Boot ROM Tool**
  Configures pin strapping and BootROM process in P1/P2 devices
- **Device Tree Editor**
  Supports visual editing of device trees
- **SerDes configuration (coming soon)**
  Configures lane protocols and speed
- **DPAA1 PCD configuration (coming soon, Not Applicable to LS1)**
  Configures PCD using a wizard

QorIQ Configuration and Validation Suite

The validation tools allow you to validate and optimize SoC HW features

- **DDR Validation Tool**
  Shmoo controller properties to find optimal values and determine magins
- **SerDes Validation Tool (coming soon)**
  Run BIST and built-in Jitter Scope to evaluate and optimize SerDes configuration


CodeWarrior for ARMv7
Configure
Build
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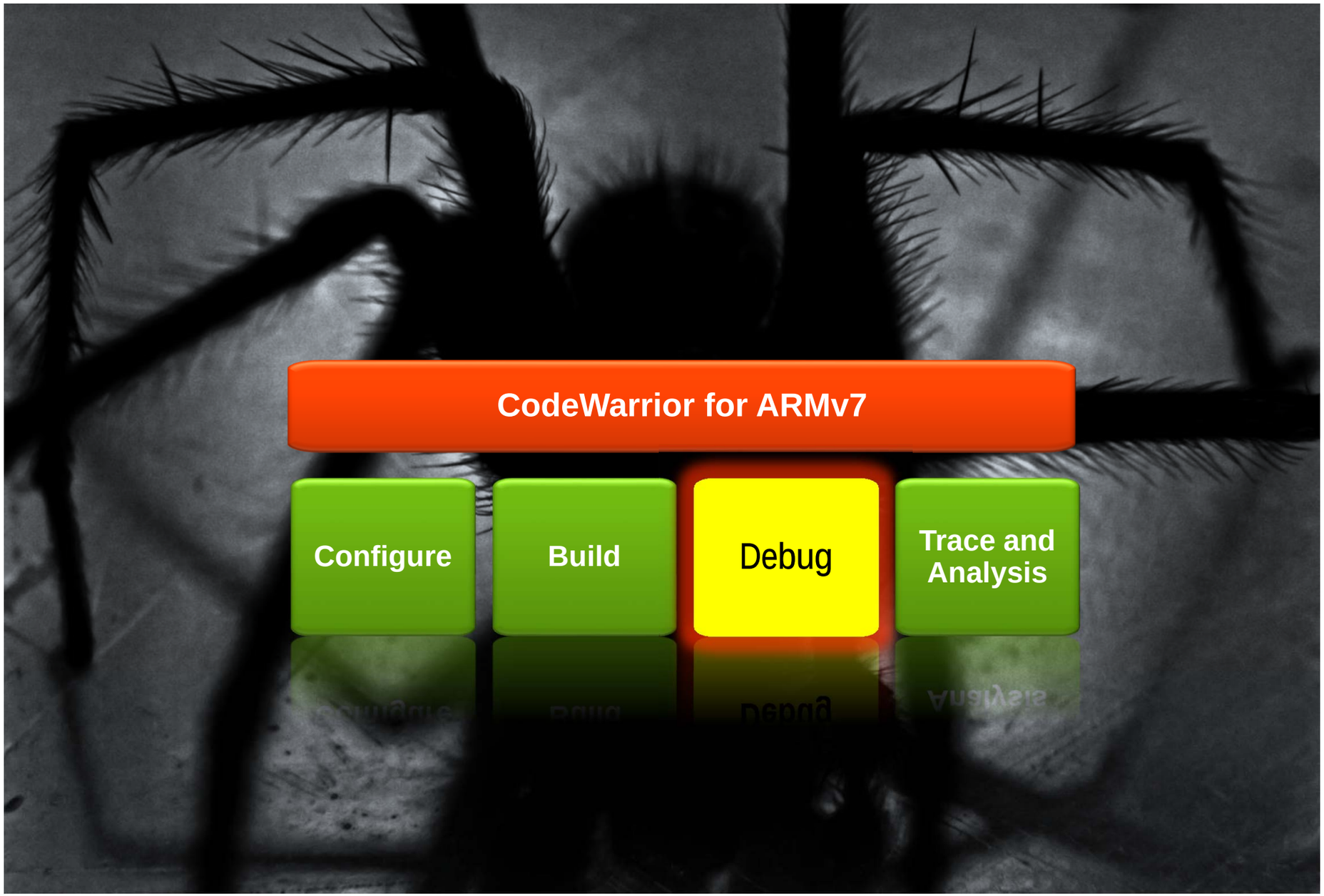
Trace and Analysis

Build Tools

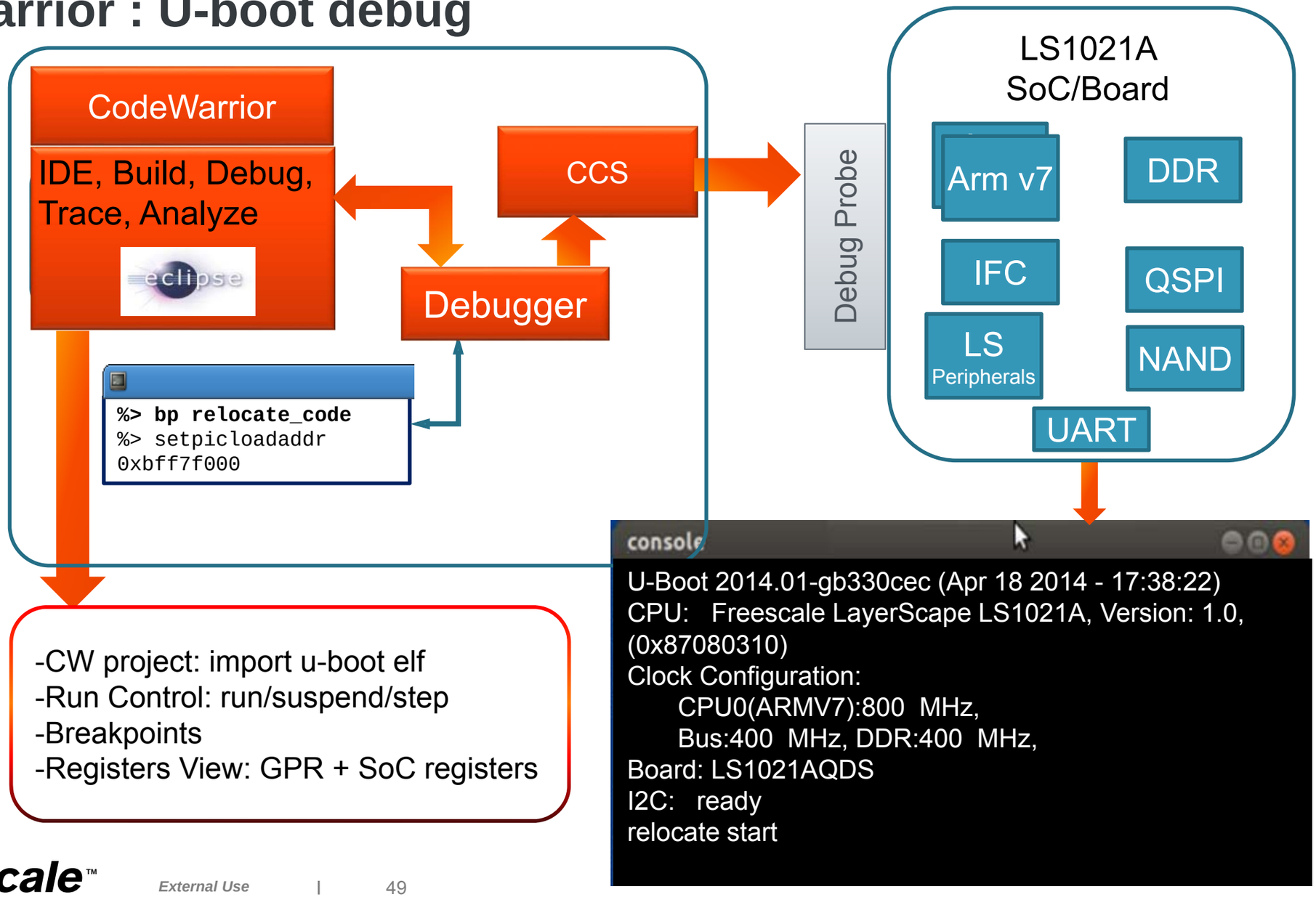
- Compiler and Linker
  - GCC is the compiler of choice
    - Bare-metal ARM GCC compiler sourced from Linaro
    - Newlib for bare-metal
    - eglibc for run-time
  - Bundled with CodeWarrior
    - Project build system or makefile
  - Bundled with SDK for Linux builds


CodeWarrior for ARMv7
Configure
Build
Debug
Trace and Analysis

Debug Tools

- CodeWarrior usage scenarios:
  - SoC and board bring-up
    - Single- and multi-core (AMP) bare-metal debugger
    - Device introspection: core and SoC registers, memory
    - Bare-metal utilities: Flash Programmer
  - Linux oriented development
    - SMP aware kernel debug
    - Device driver development and debug
    - Linux application debug
    - Linux target information: System Browser
    - Aligned with Freescale SDK: Linaro GNU toolchain, integrated target debug agent

CodeWarrior : U-boot debug



CodeWarrior : U-boot debug

- U-boot bring-up and debugging
  - Import u-boot ELF with symbol information
  - Debug from first u-boot instruction (in flash)
  - Debug after u-boot relocation in ram / relocate symbols
  - Debug to console prompt
  - Debug to kernel hand-off

- Registers View: GPR + SoC registers

- Debugging features:
  - Run control run/suspend/step
  - Breakpoints, in any ARMv7 EL mode
  - Disassembly, Memory view, Variable View, Expressions

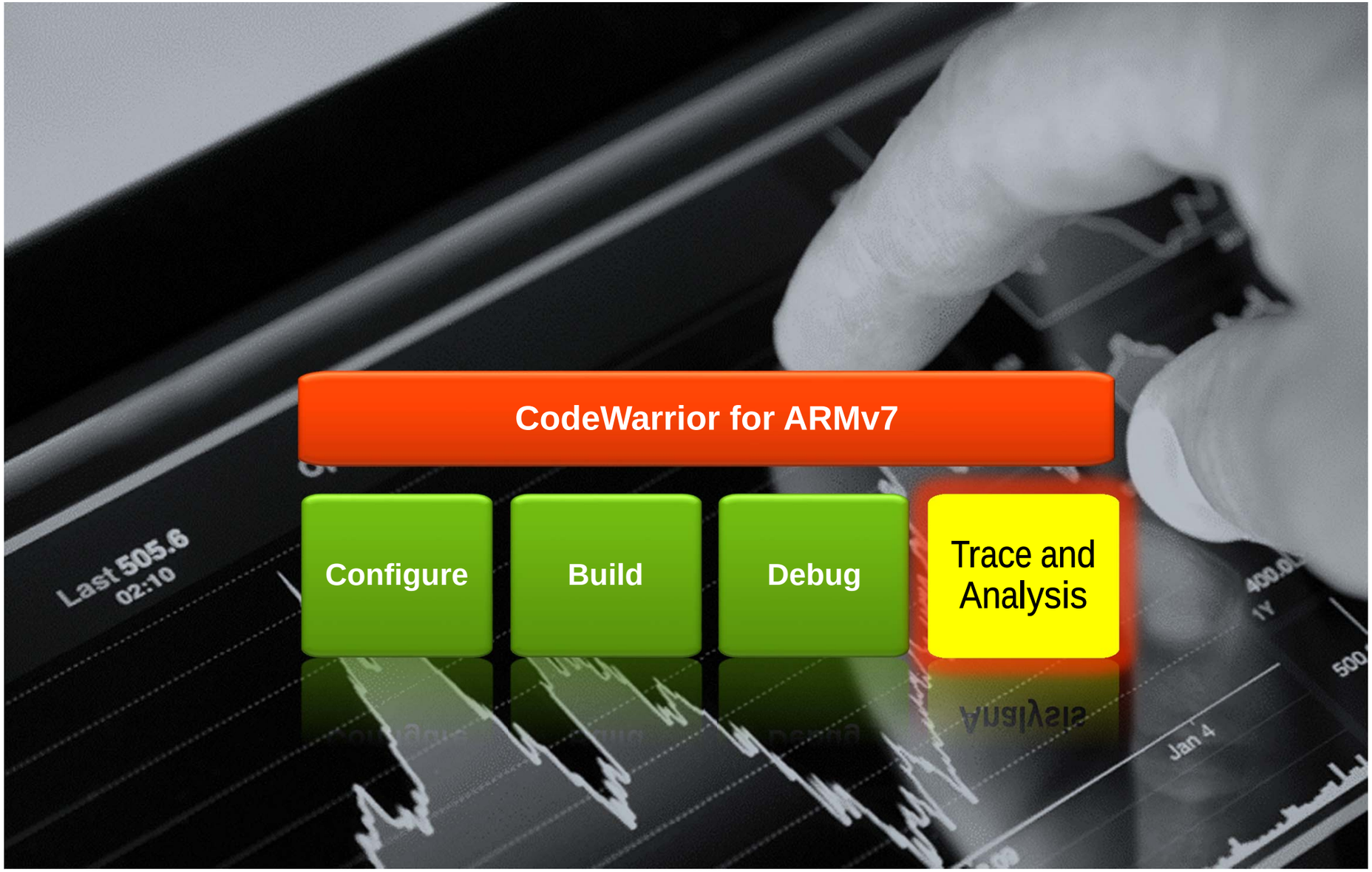
- Prerequisite
  - U-boot image (optionally with symbolic information, useful for source level debug)

Linux kernel debug – Capabilities

- **Full Linux debugger**
  - View program's source code (C/C++ or disassembly), memory, registers, stack frames, variables, etc.
  - Breakpoints, run control
- **No** kernel **changes** required
- **Multicore** debugging
- **MMU awareness** (HW page tables & Linux's page tables)
- **System information** display (kernel info, per core threads list, kernel modules list)
- Loadable **kernel modules debug**
- **Scenarios** supported
  - **Attach** to a running Linux kernel
  - **Attach** to u-boot & start Linux from u-boot

Linux application debug – Capabilities

- **AppTRK** – Debug agent
  - User-space application
  - Uses **ptrace**
- Debug **scenarios** supported
  - **Download**, start & debug application from main
  - **Attach** to a running process
- Features
  - Read/write memory, registers, variables
  - **Fork detection**
  - **Threads creation/death detection**
  - Shared libraries awareness
  - Configurable signal policies
  - I/O redirection
- **System Browser**
- CodeWarrior – AppTRK interaction
  - Ethernet connection
  - Serial connection


CodeWarrior for ARMv7
Configure
Build
Debug
Trace and Analysis

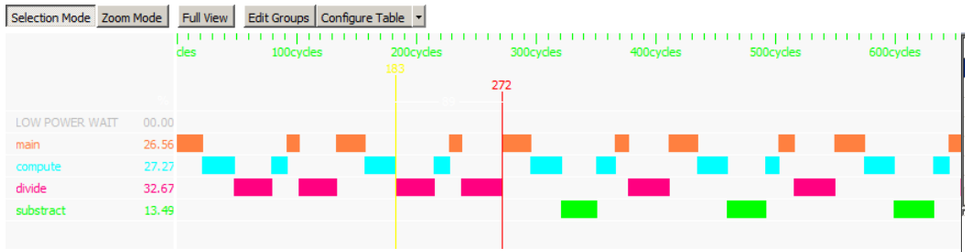
System Analysis

- Trace
  - ARM Core Program Flow Trace
    - ETM trace data stored in DDR
  - Profiling: Built from the ARM core Trace

- Performance Analysis
  - Scenarios Tool: Performance analysis for SOC resources
    - Makes use of EPU
  - Perf: Performance analysis for ARM core

- Problem Analysis
  - Valgrind

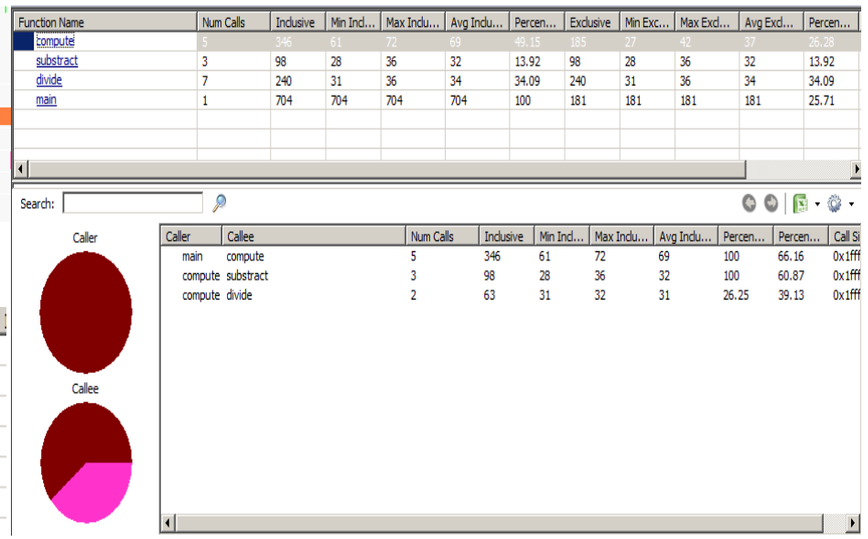
Profiling



Timeline

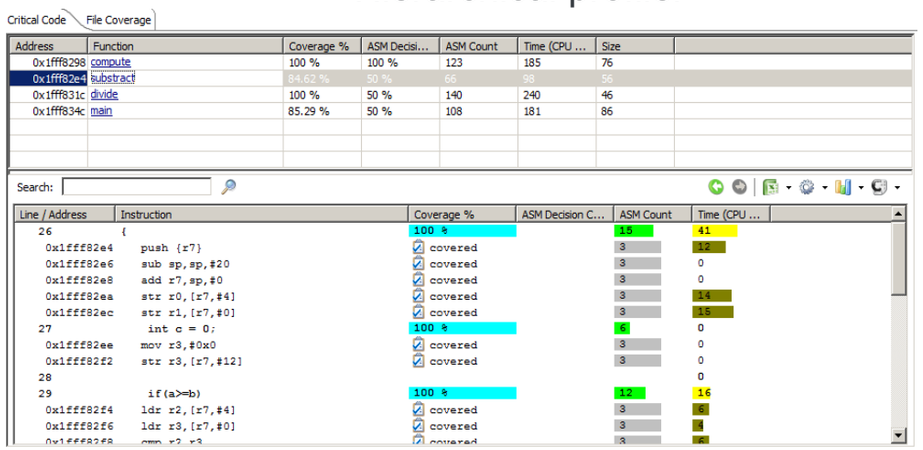
Function Name	Num Calls	% Total calls of parent	% Total times it was called
<START>			
main	1	100.00	100.00
compute	5	50.00	100.00
substract	3	60.00	100.00
divide	2	40.00	28.57
divide	5	50.00	71.43

Call Tree & Stack analysis



Hierarchical profiler

- Statistics based on non-intrusive collected trace
  - Code coverage (asm and C level)
  - Optimize application using Hierarchical profiler
  - Spot bottlenecks using Critical Code
  - Visually identify out-of-order execution using Timeline
  - Identify critical call chain using Call Tree
  - Critical stack usage (simulator based)



Critical Code & Code Coverage

Linux user space trace

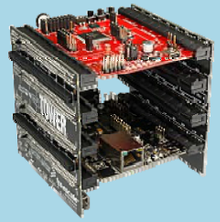
Start the application using satrace

Snapshot of libraries and their load address is created automatically.

Start trace – configure trace module to generate program trace only for a specific context ID.

Run user application.

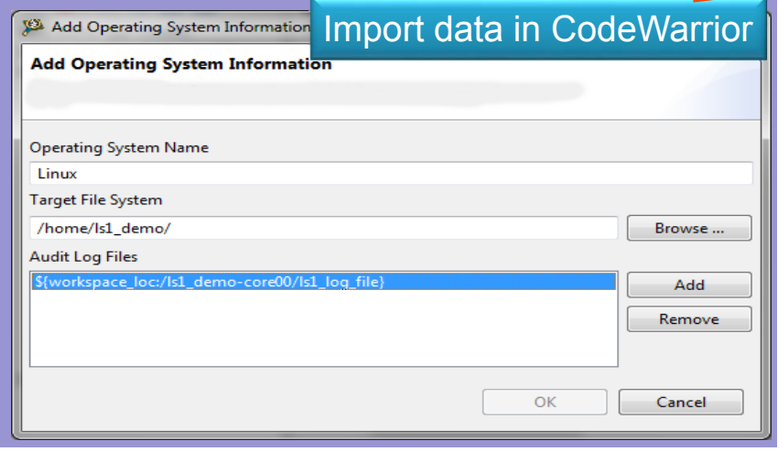
Save raw trace data.



On target

On host

Import data in CodeWarrior



Performance Analysis: Scenarios Tool

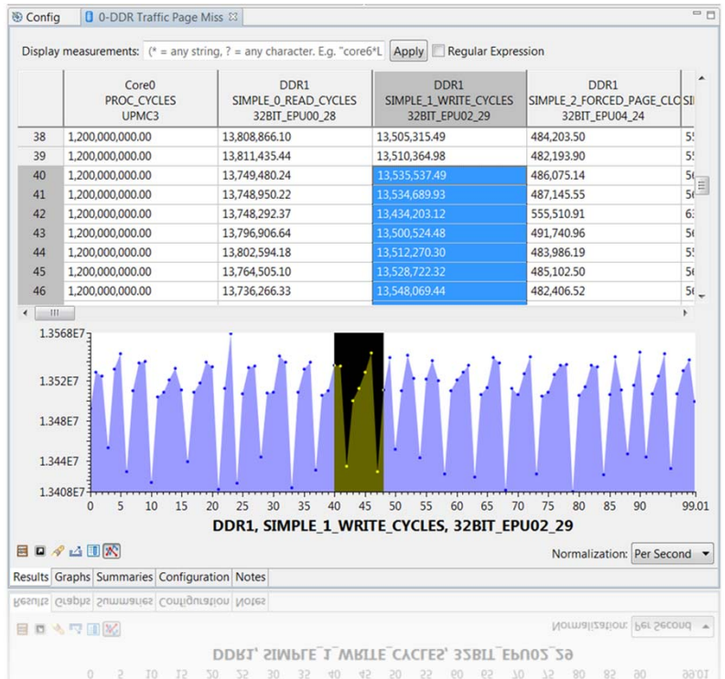
Optimized workflow for efficiently narrowing down performance issues anywhere on the system

Customer Benefits

- System Optimization for Cores and SoC
- Complexity Abstraction
- Delivers FSL expertise to users .
- Ease of Use
- Probe-less, field based usage.
- Streamlined to solve several performance issues

Key Features

- Stand alone – *no CodeWarrior Needed*
- Performance Analysis including visualization
- Connection auto discovery
- “Canned” measurement scenarios
- 100+ scenarios covering Core and SoC blocks
- User defined measurement scenarios
- Compare pairs of runs
- Graphically visualize all measurements
- “Live” view of events and metrics
- Supports “bare metal” or Linux applications
- Python scripting support

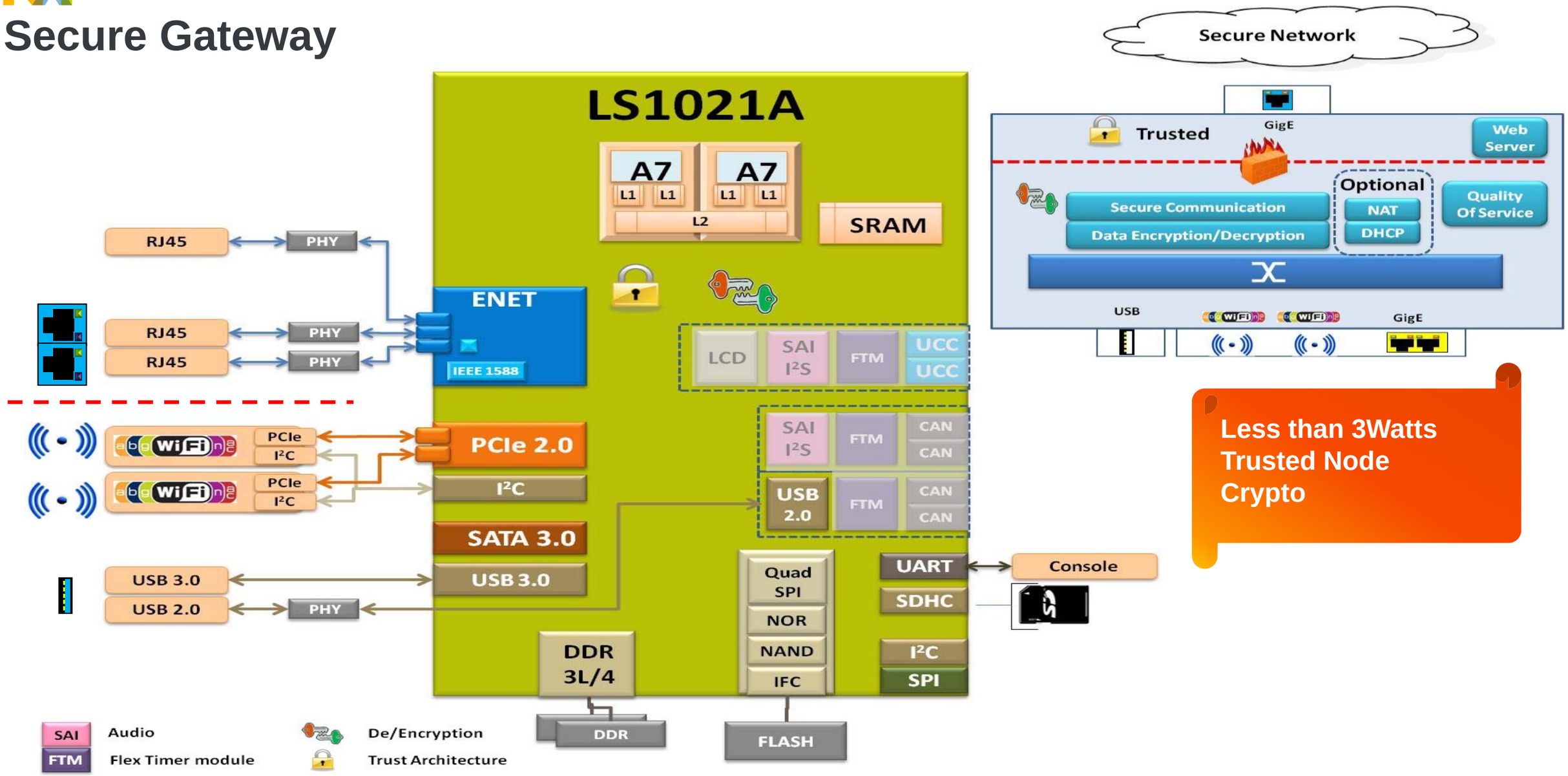


Devices supported

- P2040, P3041, P5020x P5040, P4080 (Revs 1,2)
- T1040,T2080
- T4240 (Rev1, 2)
- B4860 (Rev 2, 2.1)
- LS1020A, LS1021A, LS1022A.

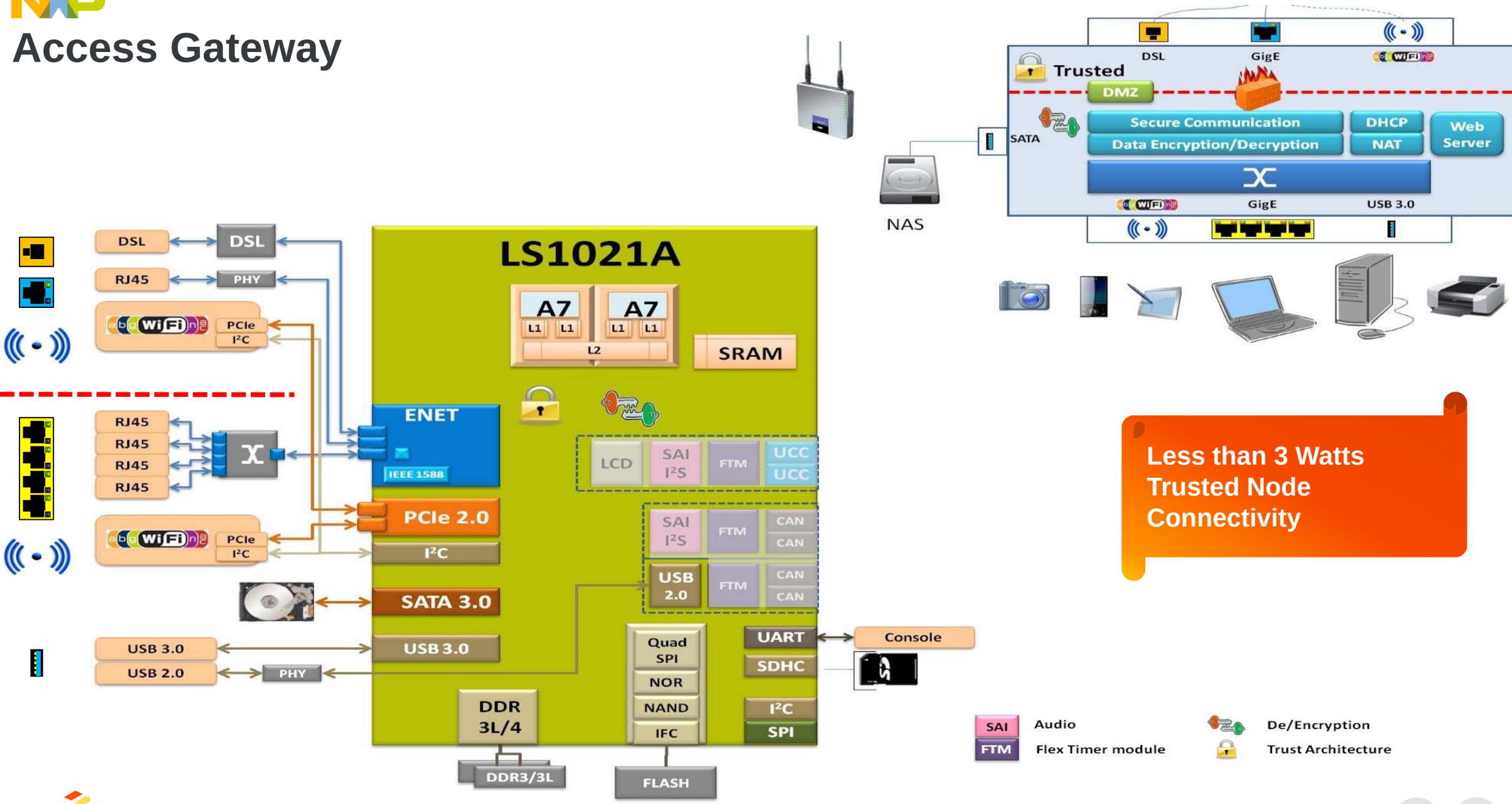
LS1021 in Action

Secure Gateway

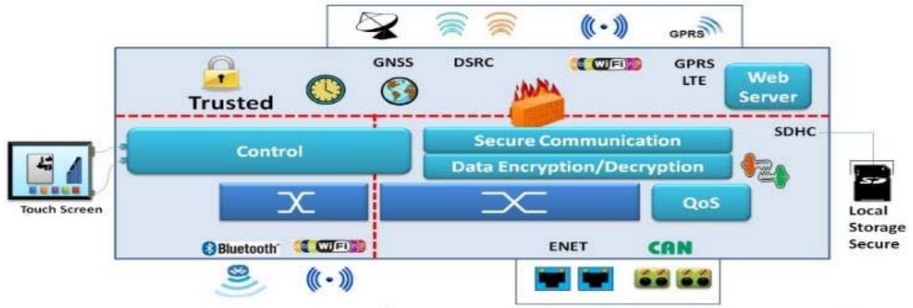


Less than 3Watts
Trusted Node
Crypto

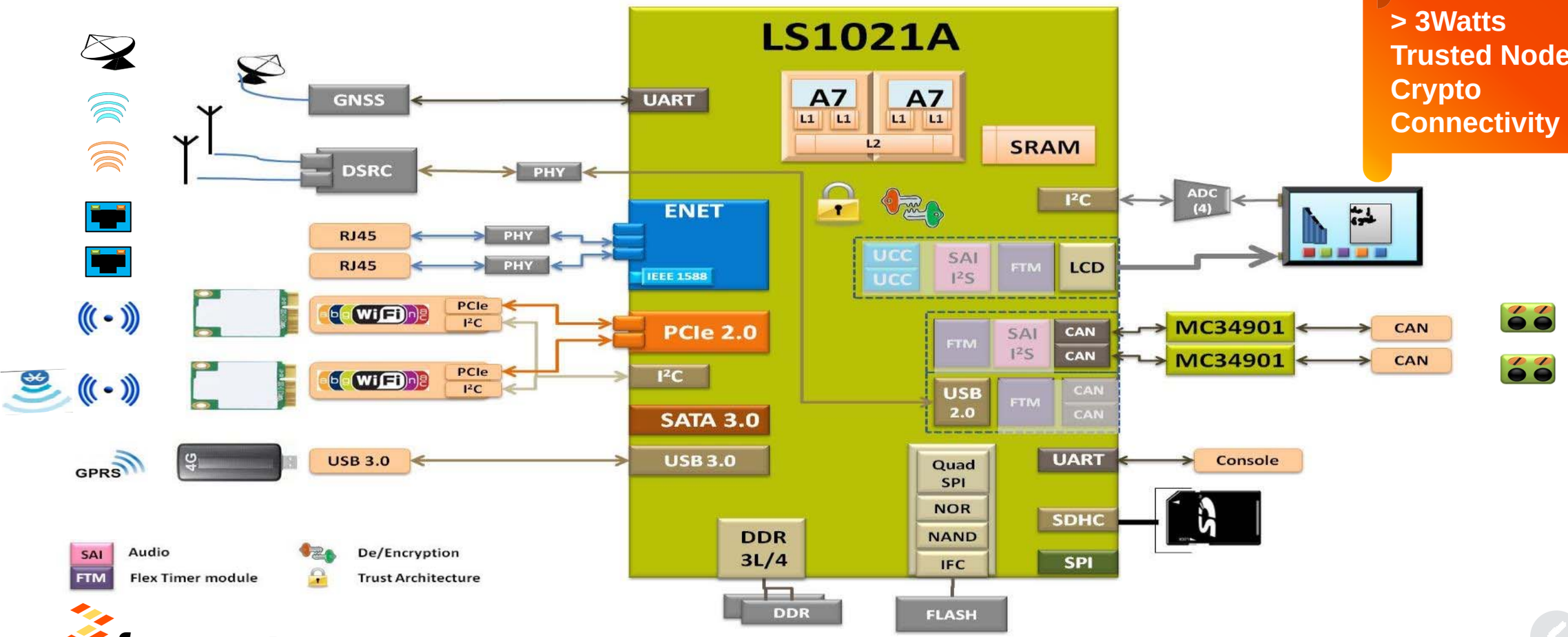
Access Gateway



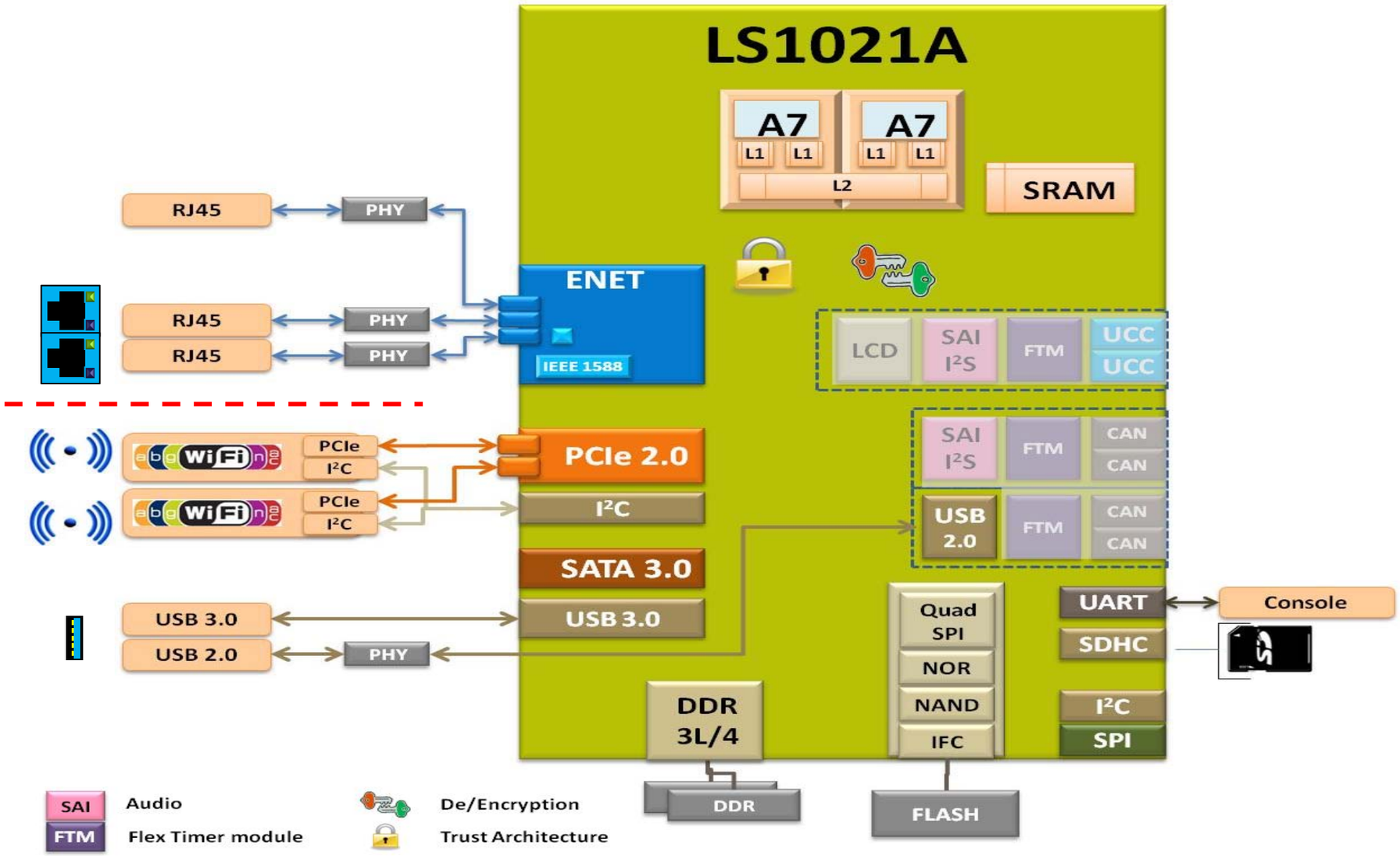
Mobile Wireless Gateway [Car]

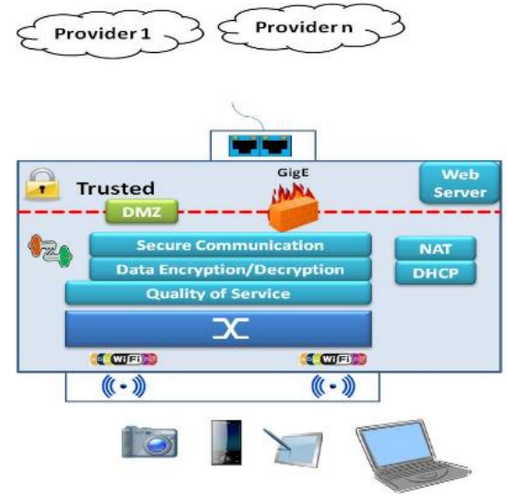


> 3Watts
> Trusted Node
> Crypto
> Connectivity



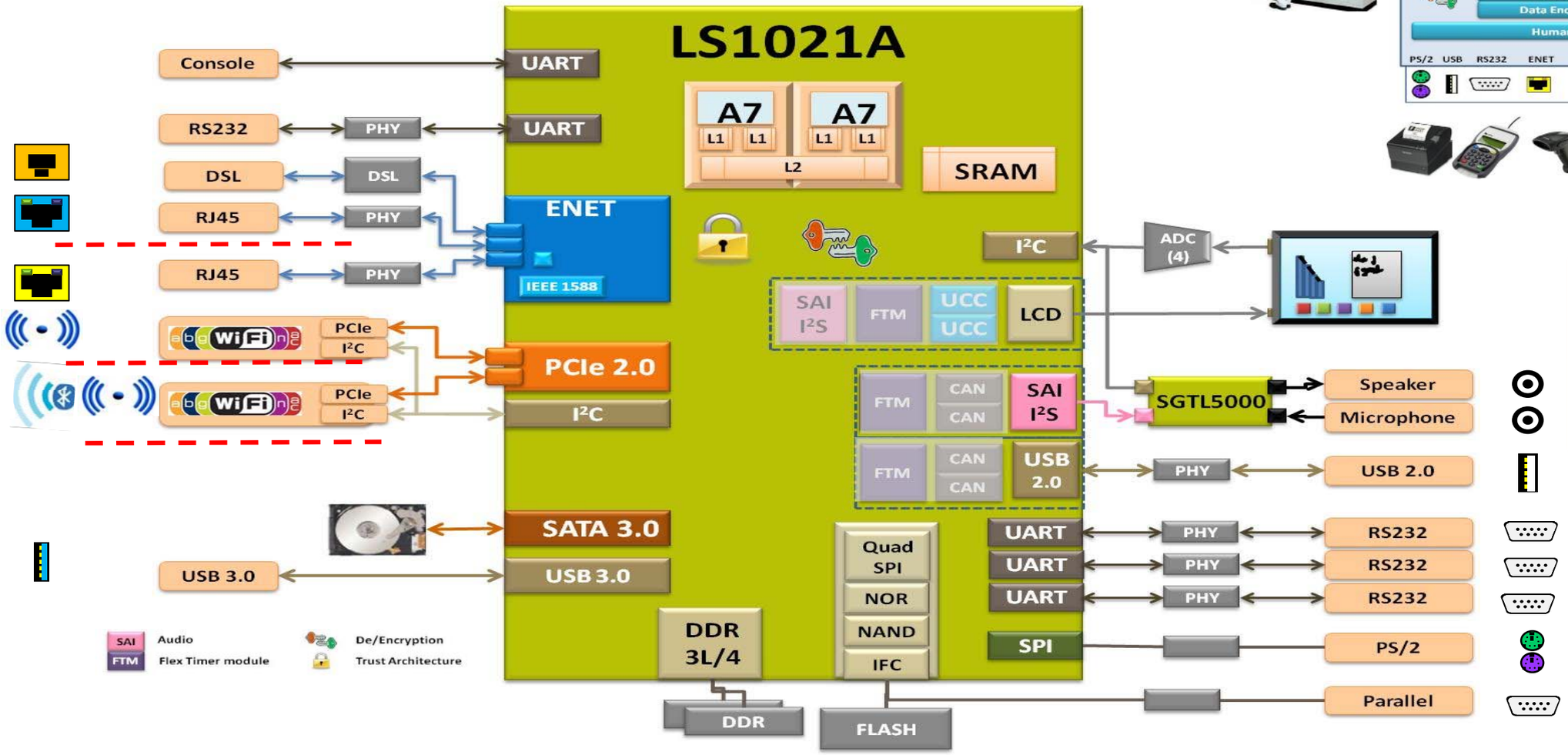
Wireless Hot Spot





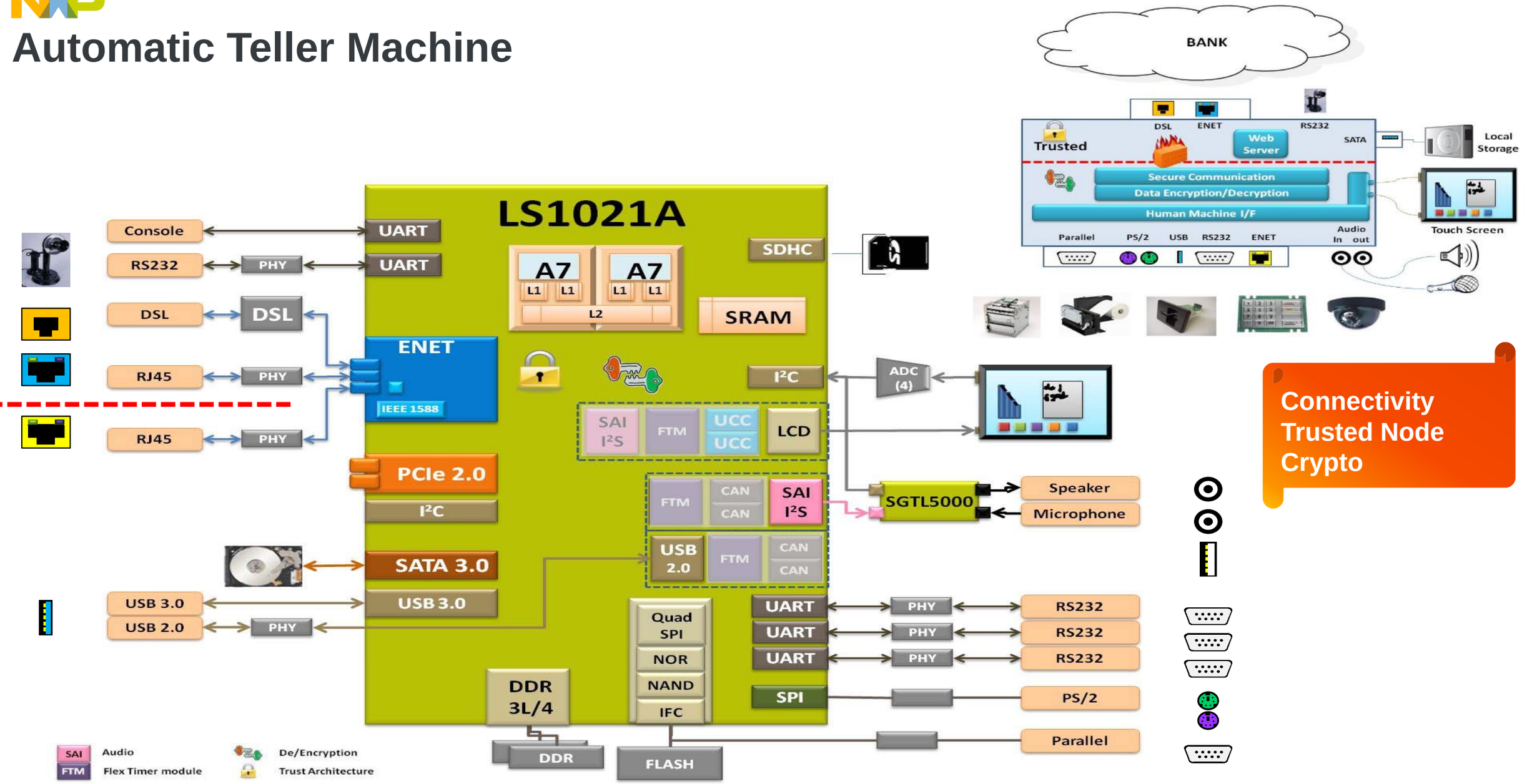
Less than 3Watts
Trusted Node
Crypto

Point of Sale Station



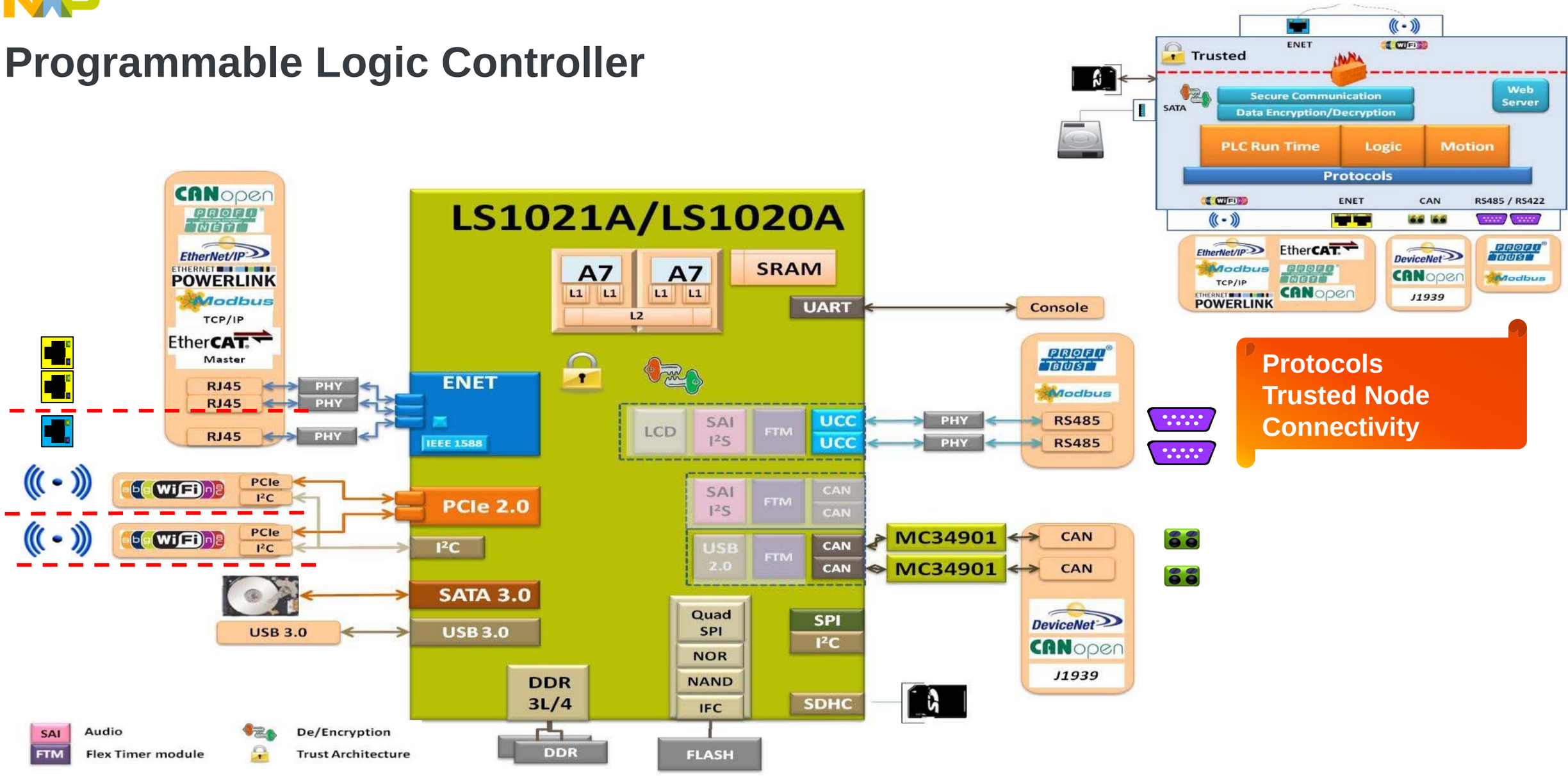
Connectivity
Trusted Node
Crypto

Automatic Teller Machine

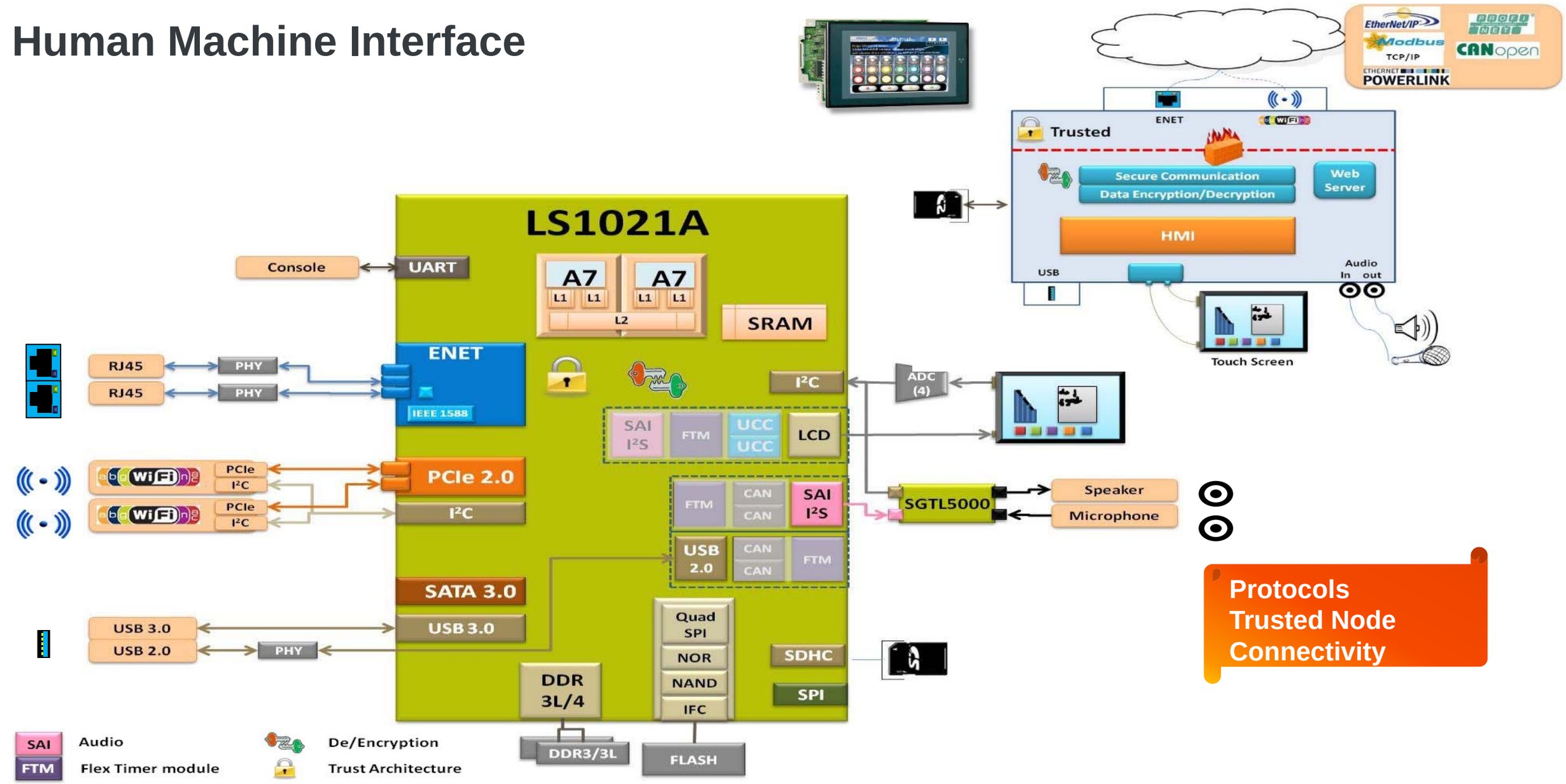


Connectivity
Trusted Node
Crypto

Programmable Logic Controller

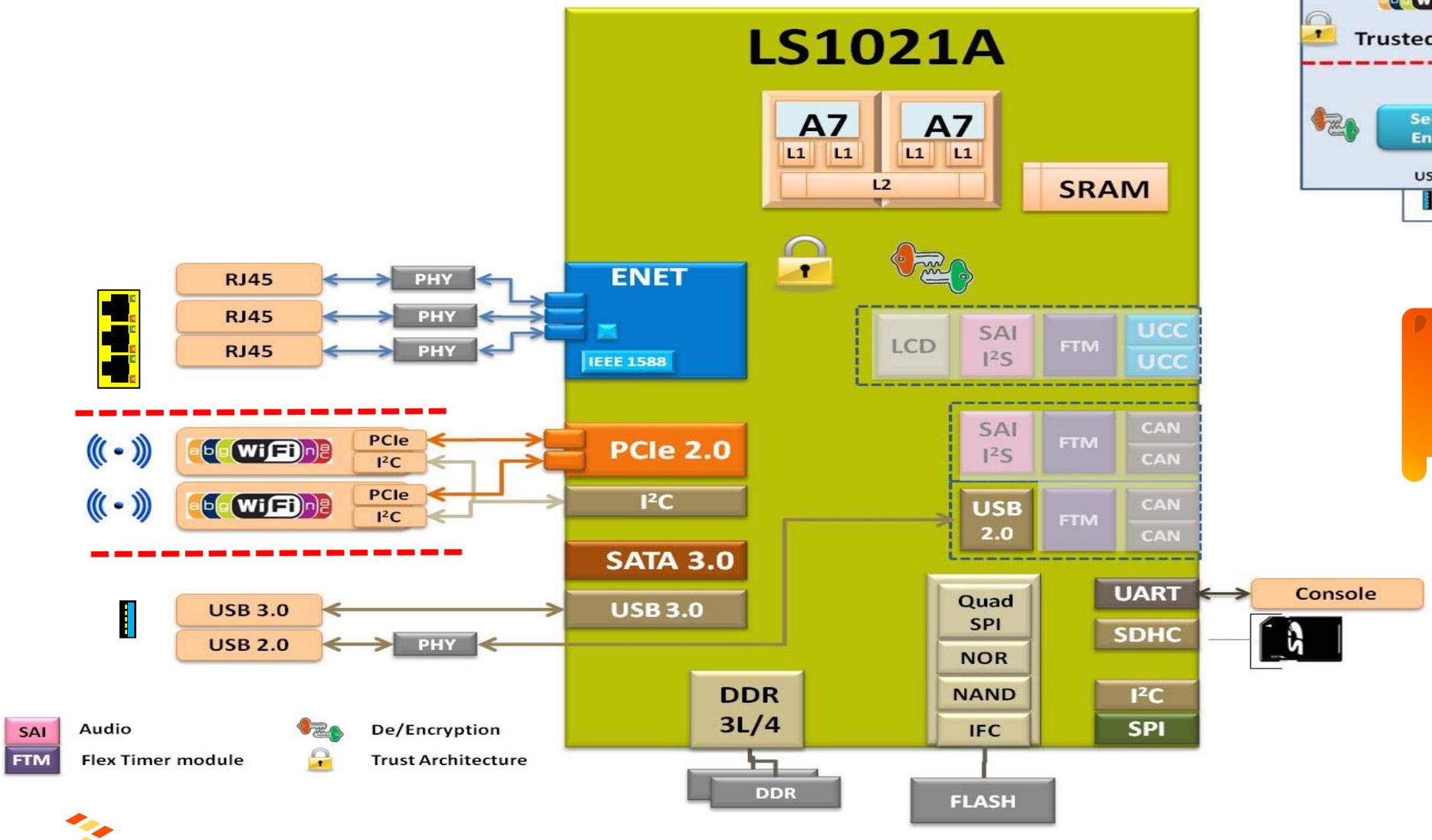


Human Machine Interface



Protocols
Trusted Node
Connectivity

Secure Wireless Access point



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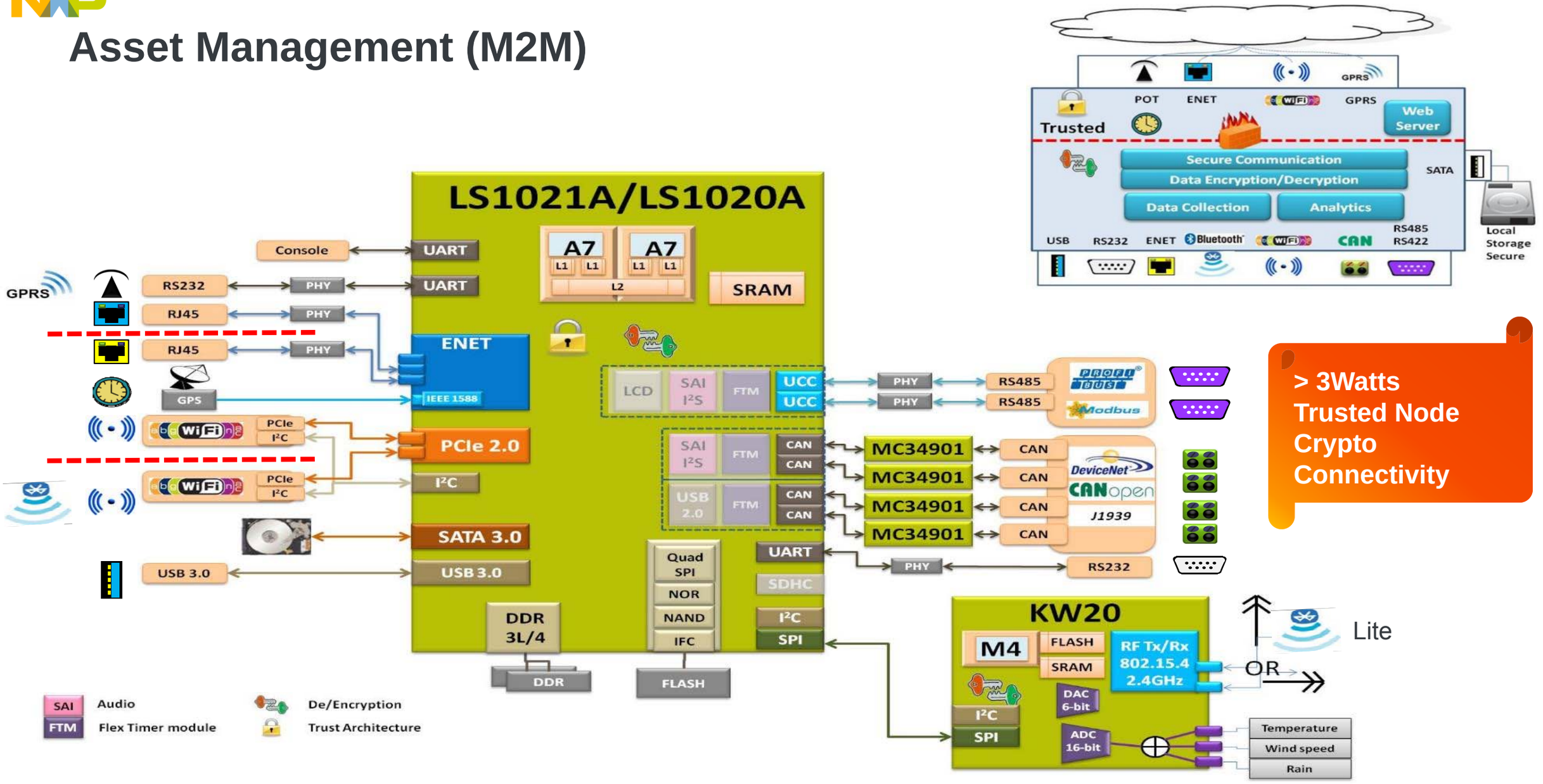
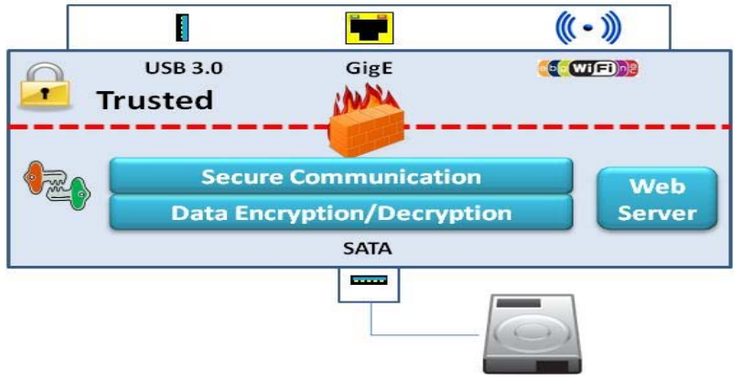
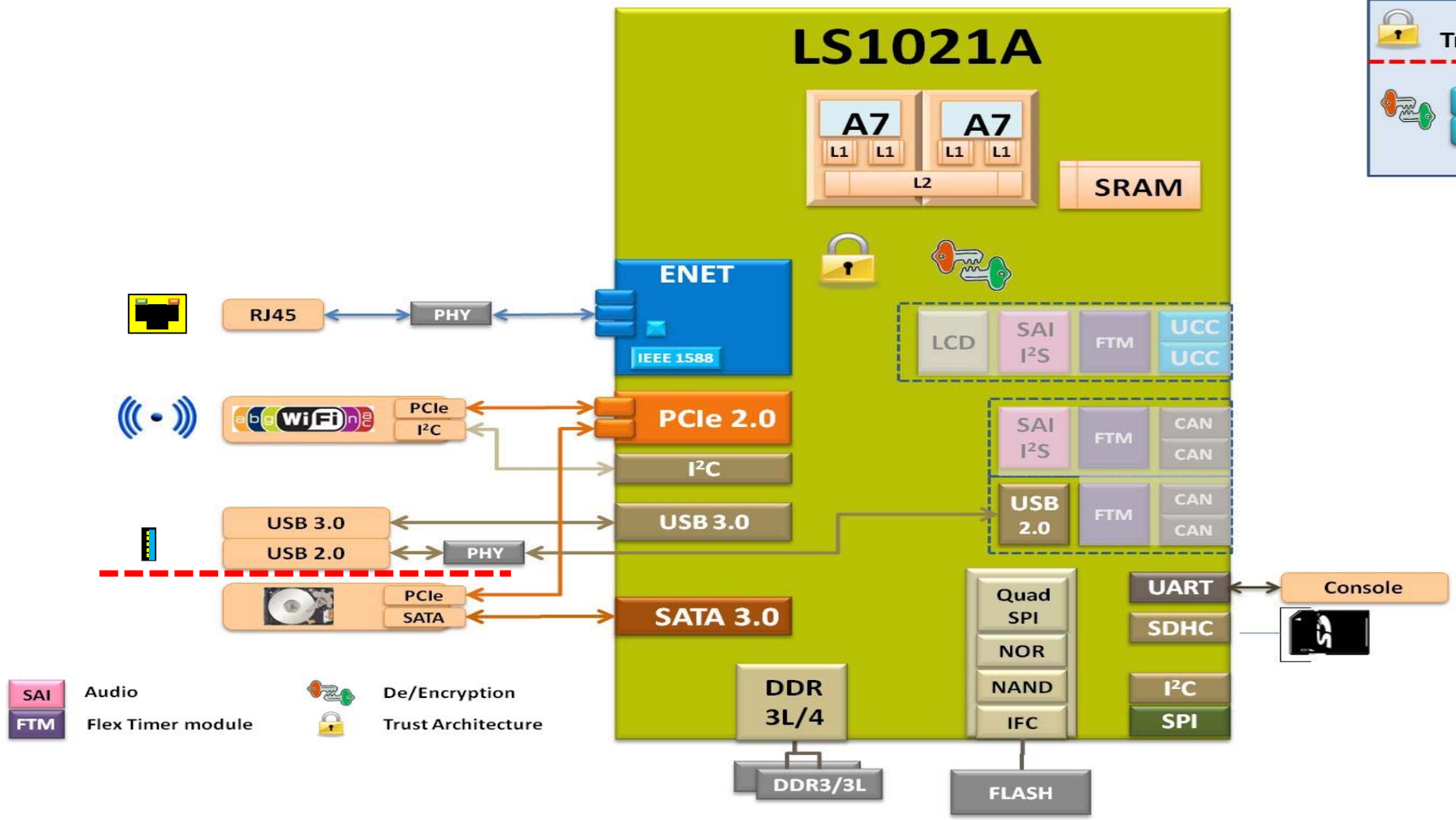
Asset Management (M2M)



> 3Watts
Trusted Node
Crypto
Connectivity

Secure Network Attached Storage





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www.Freescale.com