


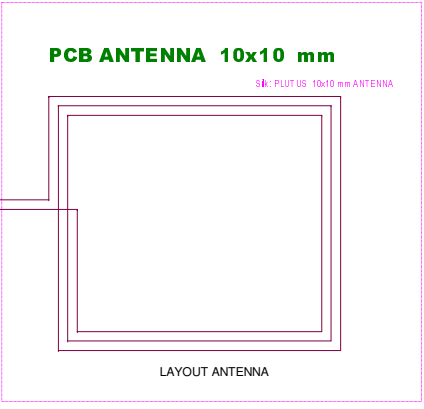
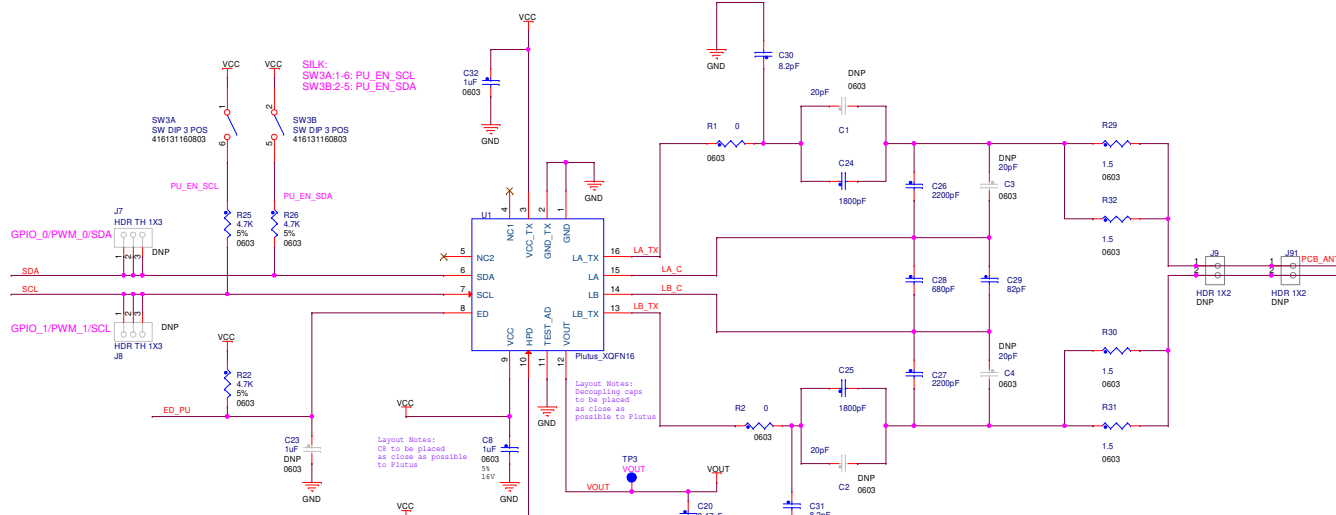
Table of Contents	
1	TITLE, TOC & REV
2	NTAG I2C XQFN16 ANT

Revision History			
Rev	Description	Date	Approved
X1	First Draft	01-Nov-2019	Jeremy
X2	A070 Release	06-Nov-2019	Jeremy
A	A085 Release 1. Added Ferrite Bead to USB Shield pins. 2. Changed Coin cell Battery Holder to CR2032	14-Nov-2019	Jeremy
A1	Changed Matching Network capacitors with 1% Tolerance	27-Nov-2019	Jeremy

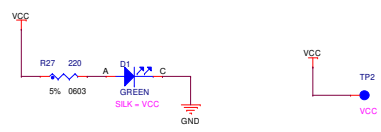
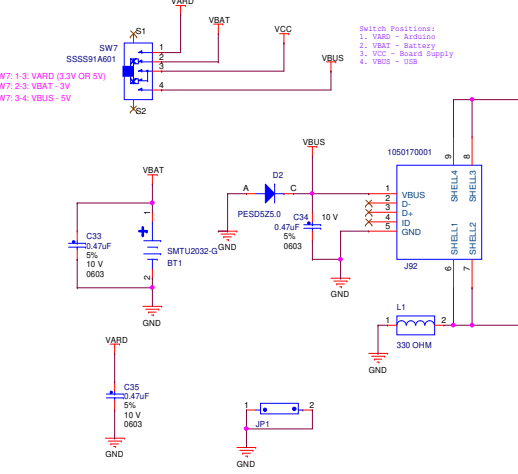
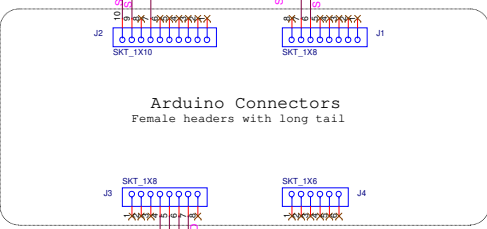
X-OM2NTA5332

NTAG 5 Link - Active Board

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Designer: Ench	Drawing Title: X-OM2NTA5332		
Drawn by: Vasudharajan N	Page Title: TITLE, TOC & REV		
Approved: Jeremy	Size C	Document Number SCH-45998 PDF: SPF-45998	Rev A1
Date: Thursday, November 28, 2019		Sheet 1 of 2	



Note: LAYOUT - Trace Antenna (RF Critical):
 Use '0M23511ARD_Final' for placement, Routing, should reproduce the Original design without Mismatch



DNP TABLE:

REF DES	ASSY OPT	PAGE NAME
J7,C4,C23,J8,C3,C1,J9,J91,C2	DNP	02-NTAG I2C XQFN16

SWITCH TABLE:

REF DES	SWITCH(DEFAULT)	SWITCH(OPTION1)	SWITCH(OPTION2)	SWITCH(OPTION3)	PAGE NAME
SW6	OFF: DISABLE VARD <-> ARDUINO	VARD <-> P1V8 3V3 BRD	VARD <- P5V0 ARDUINO		02-NTAG I2C XQFN16
SW3B,SW3A	OFF: DISABLE VCC	ON: ENABLE VCC			02-NTAG I2C XQFN16
SW3C	OFF: NC	ON: NC			02-NTAG I2C XQFN16
SW1	OFF	ON			02-NTAG I2C XQFN16
SW7		SW7: 2-3: VBAT - 3V	SW7: 1-3: VARD (3.3V OR 5V)	SW7: 3-4: VBUS - 5V	02-NTAG I2C XQFN16

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Drawing Title: **X-OM2NTA5332**

Page Title: **NTAG I2C XQFN16 ANT**

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