

PTN3363

HDMI/DVI level shifter with active DDC buffer, supporting
3.4 Gbit/s operation

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Objective product brief

1. General description

PTN3363 is a high-speed level shifter device which converts four lanes of low-swing AC-coupled differential input signals to DVI v1.0 and HDMI v1.4b compliant open-drain current-steering differential output signals, up to 3.4 Gbit/s per lane to support 36-bit deep color mode, 4K × 2K video format or 3D video data transport. Each of these lanes provides a level-shifting differential active buffer, with built-in Equalization, to translate from low-swing AC-coupled differential signaling on the source side, to TMDS-type DC-coupled differential current-mode signaling terminated into 50 Ω to 3.3 V on the sink side. Additionally, the PTN3363 provides a single-ended active buffer for voltage translation of the HPD signal from 5 V on the sink side to 3.3 V on the source side and provides a channel with active buffering and level shifting of the DDC channel (consisting of a clock and a data line) between 3.3 V source-side and 5 V sink-side. The DDC channel is implemented using active I²C-bus buffer technology providing redriving and level shifting as well as disablement (isolation between source and sink) of the clock and data lines.

The low-swing AC-coupled differential input signals to the PTN3363 typically come from a display source with multi-mode I/O, which supports multiple display standards, for example, DisplayPort, HDMI and DVI. While the input differential signals are configured to carry DVI or HDMI coded data, they do not comply with the electrical requirements of the DVI v1.0 or HDMI v1.4b specification. By using PTN3363, chip set vendors are able to implement such reconfigurable I/Os on multi-mode display source devices, allowing the support of multiple display standards while keeping the number of chip set I/O pins low.

The PTN3363 main high-speed differential lanes feature low-swing self-biasing differential inputs which are compliant to the electrical specifications of *DisplayPort Standard v1.2a* and/or *PCI Express Standard v1.1*, and open-drain current-steering differential outputs compliant to DVI v1.0 and HDMI v1.4b electrical specifications. The I²C-bus channel actively buffers as well as level-translates the DDC signals.

PTN3363 is powered from a single 3.3 V power supply consuming a small amount of power and is offered in a 32-terminal HVQFN32 package.



2. Features and benefits

2.1 High-speed TMDS level shifting

- Converts four lanes of low-swing AC-coupled differential input signals to DVI v1.0 and HDMI v1.4b compliant open-drain current-steering differential output signals
- TMDS level shifting operation up to 3.4 Gbit/s per lane (340 MHz TMDS clock) supporting 4K × 2K 3 Gbit/s and 3D video formats
- Programmable receive equalization
- Integrated 50 Ω termination resistors for self-biasing differential inputs
- Programmable high-impedance termination resistors for HDMI re-driver usage with external 50 Ω termination resistors
- Back-current safe outputs to disallow current when device power is off and monitor is on
- Disable feature to turn off TMDS inputs and outputs and to enter low-power condition
- Selectable differential output termination on TMDS channels

2.2 DDC level shifting

- Integrated DDC buffering and level shifting (3.3 V source to 5 V sink side and vice versa)
- Rise time accelerator on connector side DDC ports
- Up to 400 kHz I²C-bus clock frequency
- Back-power safe sink-side terminals to disallow backdrive current when power is off or when DDC is not enabled

2.3 HPD level shifting

- HPD non-inverting level shift from 0 V on the sink side to 0 V on the source side, or from 5 V on the sink side to 3.3 V on the source side
- Integrated 200 kΩ pull-down resistor on HPD sink input guarantees 'input LOW' when no display is plugged in
- Back-power safe design on HPD_SINK to disallow backdrive current when power is off

2.4 HDMI dongle detection support

- Incorporates I²C-bus slave ROM
- Responds to DDC read to address 81h
- Feature enabled by pins DDET and DDC_EN (must be enabled for correct operation in accordance with DisplayPort interoperability guideline)

2.5 General

- ESD resilience to 8 kV HBM, 1 kV CDM
- Back-current-safe design on all sink-side main link, DDC and HPD terminals
- Transparent operation: no re-timing or software configuration required
- 32-terminal HVQFN32 package