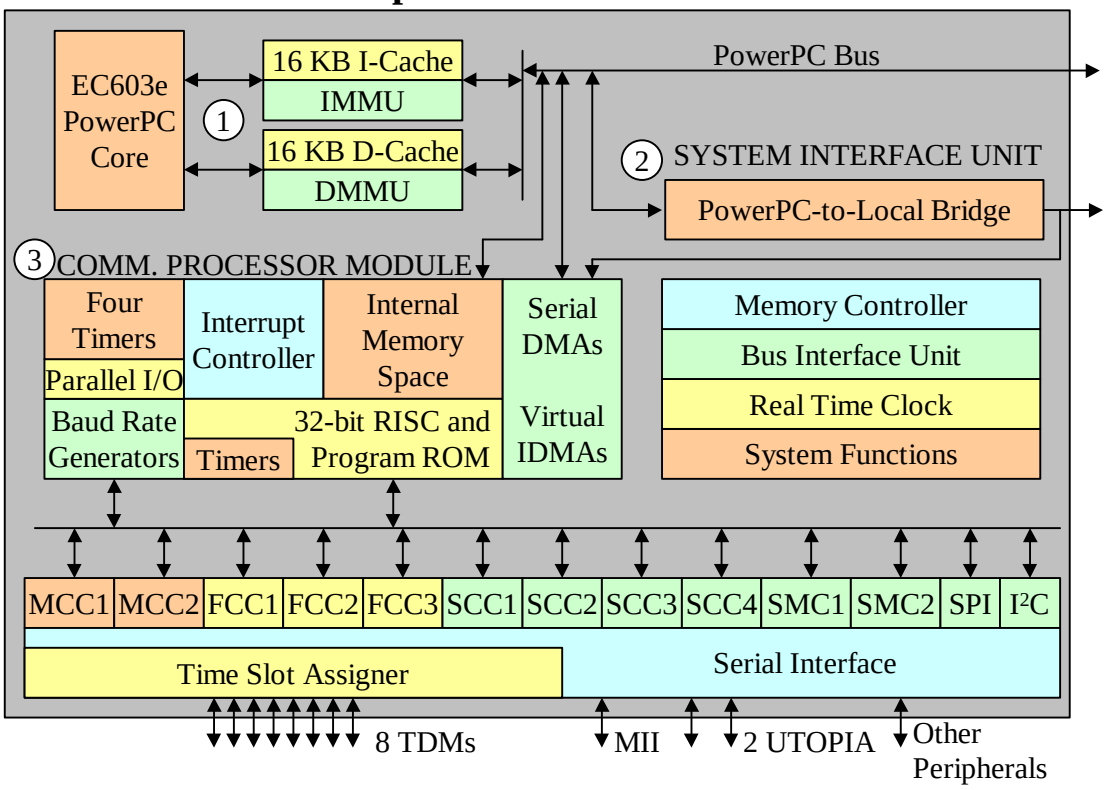
MPC8260 Architecture

What you will learn

- What are the basic blocks and their function?
- What is the function of each component in the blocks?
- What performance can I expect from each component?
- How internal data flows
- What are the pin groups?
- How to calculate CPM (Communications Processor Module) performance
- What is an example application?

What are the Basic Components?



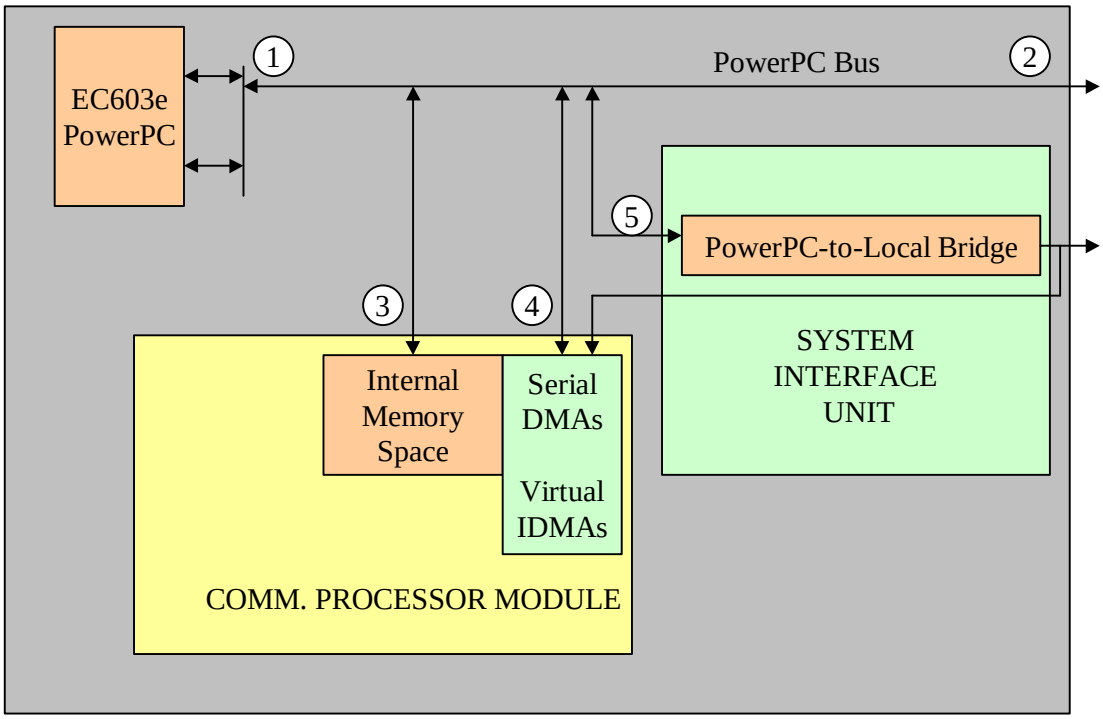
1. This diagram shows most of the functional blocks of the MPC8260. But they all are in 1 of 3 major blocks.

2. PowerPC - the processor is the 603e PowerPC including 16K bytes each of instruction and data cache, and an instruction and data MMU. The 603e is capable of 140 MIPS at 100 MHz or 280 MIPS at 200 MHz.

3. System Interface Unit - includes the bridging functions shown, the memory controller, and a number of system functions.

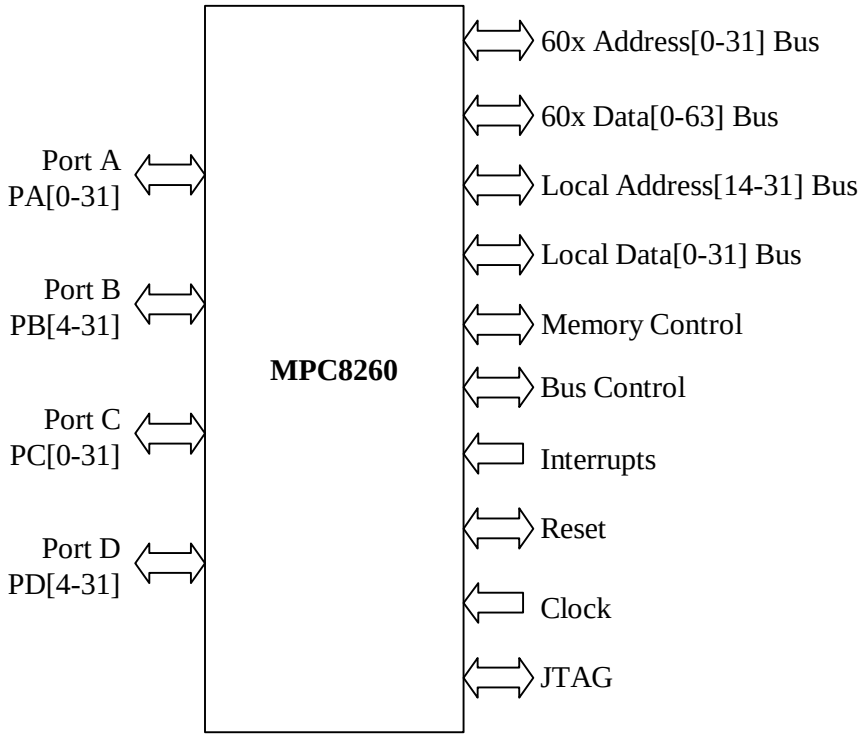
4. Communications Processor Module - includes all the communications devices, both the ones that were on the MPC860 and the new ones, the FCCs and MCCs.

How Data Flows



Data Path	Description
1 to 2	PowerPC to PowerPC Bus - used for fetches, loads, and stores by the 603 that miss in the cache or are not cacheable. Addresses are processed by the MMU.
1 to 3	PowerPC to Internal Memory space - used for accesses to registers and dual-port RAM. Addresses are processed by the MMU; data should not be cached.
4 to 2	Communications Devices to PowerPC Bus - used for data transfers and buffer descriptor accesses; transfers are burstable. Addresses are not processed by the MMU; data should not be cached.
4 to 3	Communications Devices to Internal Memory Space - used for data transfers and buffer descriptor accesses; transfers are not burstable. Addresses are not processed by the MMU; data should not be cached.
1 to 5	PowerPC to Local Bridge - used for loads and stores by the 603 that miss in cache or are not cacheable. Addresses are processed by the MMU.
4 to 5	Communications Devices to PCI Bridge or Local Bridge - used for data transfers and buffer descriptor accesses; transfers are burstable. Addresses are not processed by the MMU; data should not be cached.

What are the Pinouts?



Pin Description

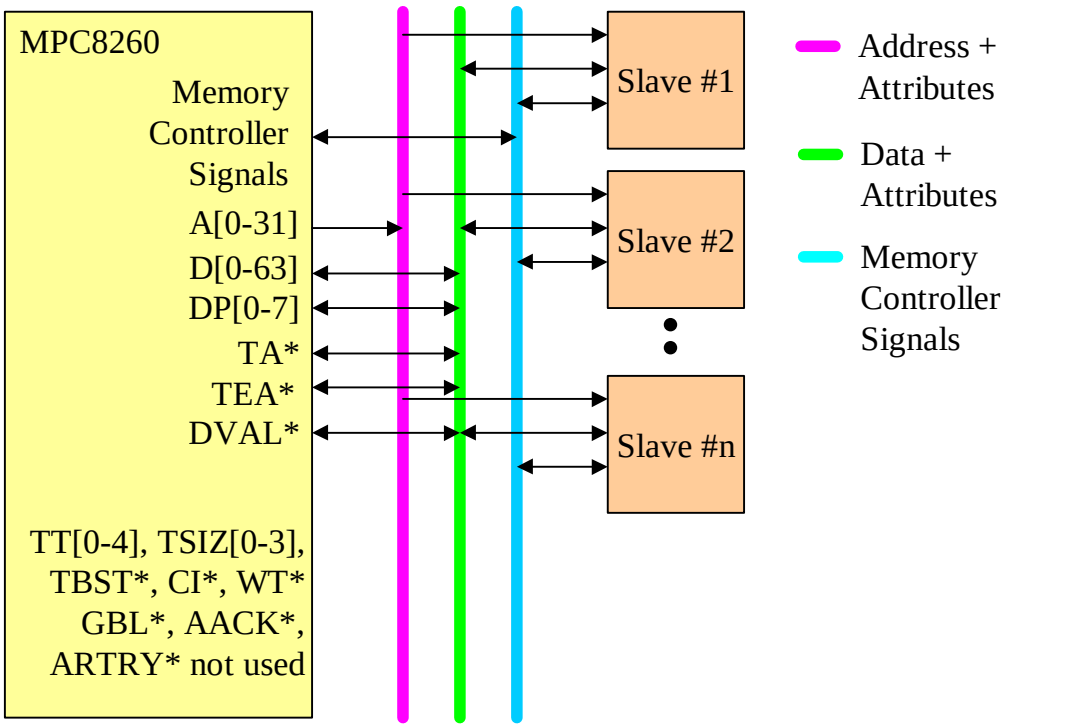
1. 60x Address Bus - 32-bit address bus with 4-bit parity.
2. 60x Data Bus - 64-bit data bus with 8-bit parity.
3. Local Address Bus - 18-bit address bus.
4. Local Data Bus - 32-bit data bus with 4-bit parity.
5. Memory Control - memory interface pins for the memory controller
6. Bus Control - device interface pins for external masters, additional memory and peripherals.
7. Interrupts - eight external interrupt pins.
8. Reset - reset pins
9. Clock - external oscillator input and multiplier frequency pins
10. JTAG - standard JTAG pins
11. Port A, B, C, and D - general purpose I/O pins and communication device pins.

What is the Single MPC8260 Bus Mode?

Definition

The single MPC8260 bus mode means the only bus master is the 8260. The memory controller controls all devices on the external pins.

Block Diagram



Description

- The pins shown as not used should not be used for anything.
- BCTL[0-1] are usable.

8260 Single Mode Restrictions

In single 8260 mode, the following is not possible:

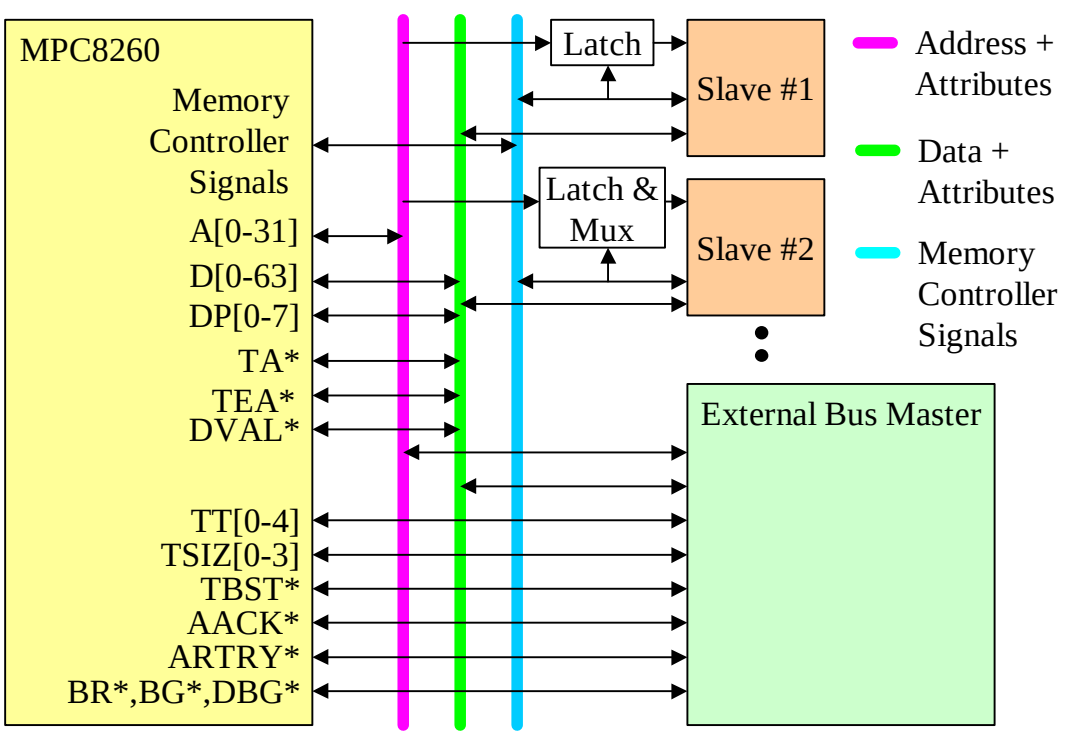
1. No other bus masters.
2. No L2 cache.

What is the 60x Compatible Bus Mode?

Definition

The 60x-compatible bus mode can include one or more bus masters including L2 cache.

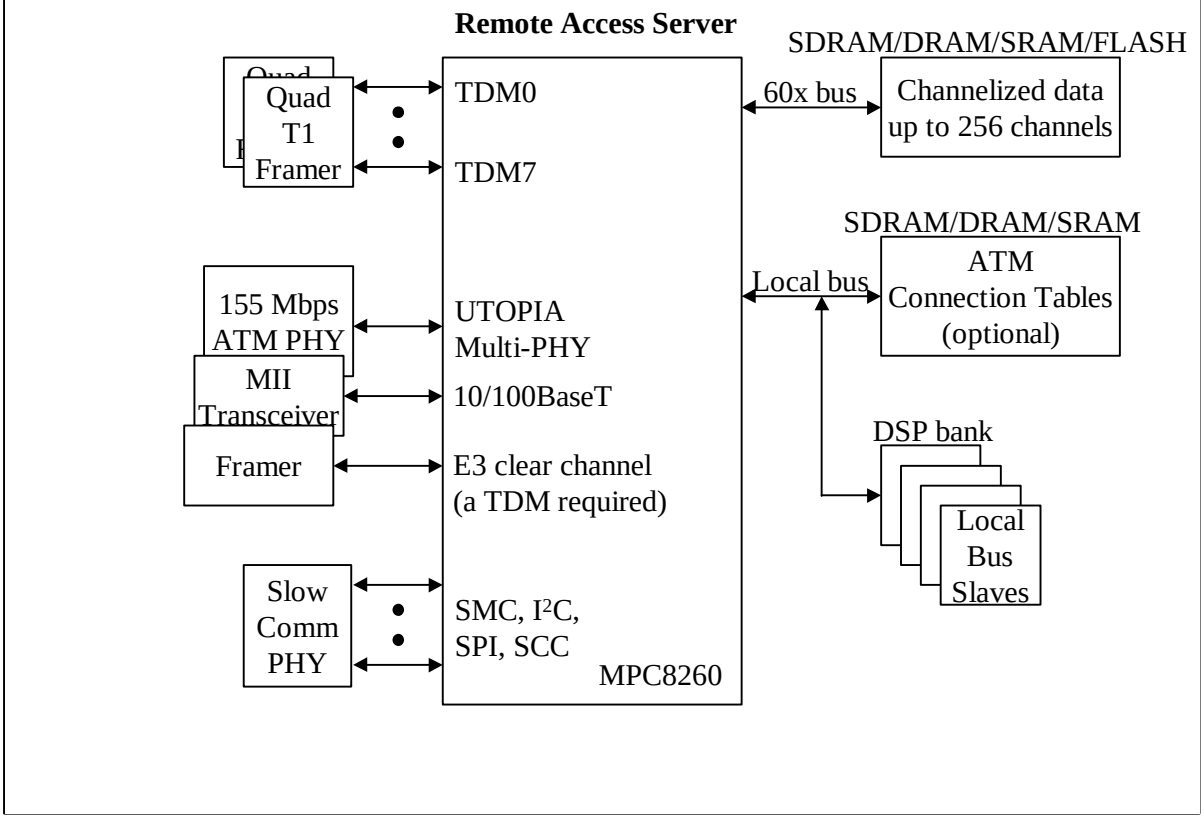
Block Diagram



Description

1. If the 8260 is used in no pipeline mode(BCR[PLDP]=1), the latches are not required; however, the multiplexers are. Putting the 8260 in no pipeline mode will typically result in a 10-30% performance reduction.
2. TT[0-4] indicates the transfer type. For example, a basic single-beat read is 0b01010. For a complete description of the TT codes, see page 5-10 in the UM.
3. TSIZ[0-3] and TBST* together indicate the size of the requested data transfer. For example, a transfer of 8 bytes would have TSIZ[0-3]=0000 and TBST*=1. For a complete list of transfer size encodings, see p. 5-13 in the UM.
4. In this mode, L2 cache can be implemented. Performance increase with an L2 cache is application-dependent, but one estimate might be an increase of 25% for a typical RTOS using a 512 Kbyte L2 cache.

What is an Example Application?



Description

1. An access server concentrate low speed traffic from many users to a higher speed pipe. In this example, the low speed traffic from many users comes from the TDM buses. The high speed pipe is the Ethernet or ATM connection.
2. An example is an internet provider. Low speed traffic comes from the users who are dialed in over the phone. High speed traffic is transferred on to the internet.
3. The DSPs run modem software.
4. Data to/from the TDMs is processed by the MCCs and stored in RAM on the 60x bus.
5. If the ATM connection and if address compression are used, the ATM connection tables must be on the local bus. (The word optional in the block means the a CAM could optionally be used for address mapping; however, it too must be on local bus) If they are on 60x bus, a latency problem can occur. Optionally, the ATM buffer descriptors and buffers can also be on the local bus.

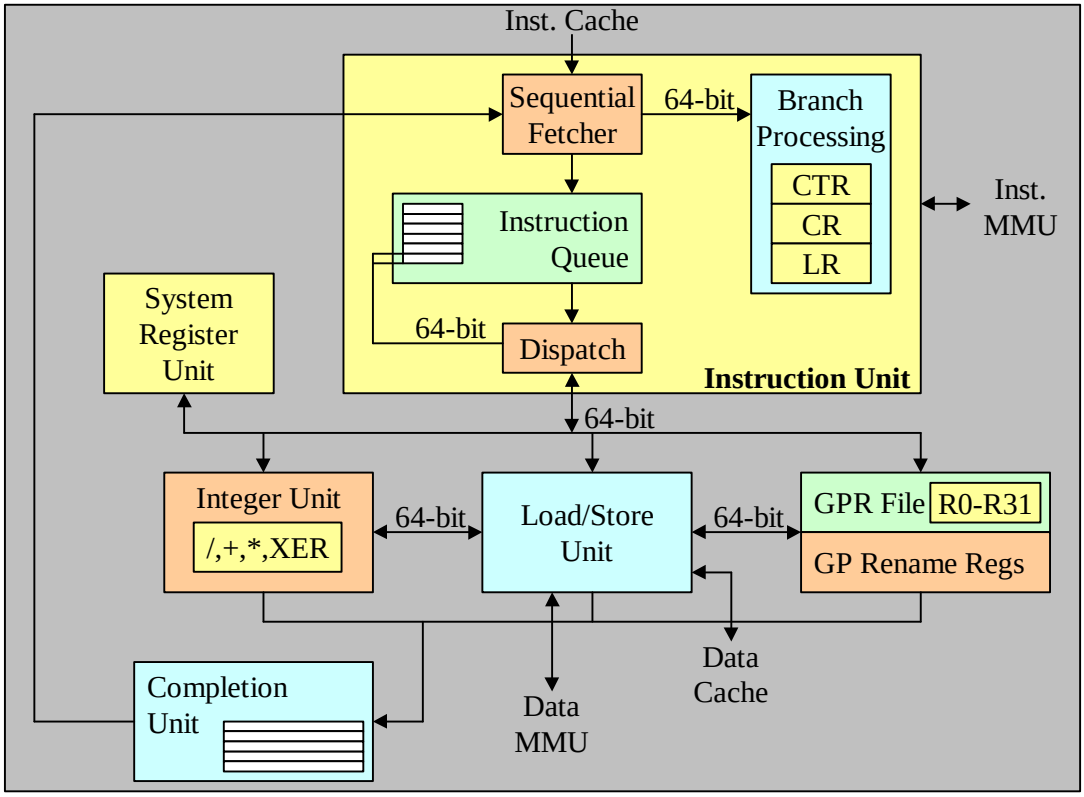
MPC8xx Functionality Not Supported by PowerQUICC II(1 of 2)

Function	MPC8xx	PowerQUICC 2
Clock Input	Low Frequency crystal or external oscillator	External oscillator at bus frequency
Low Power	Several low power modes	One low power mode
RTC Power	Battery back-up power	No battery back-up power
Debug	Background debug mode	COP
Byte order	True little-endian mode	No true little-endian mode
PCMCIA	Two ports	None
Infra-Red	SCC2	Not available
QMC	Four SCCs (64 channels)	Two MCCs (256 channels)
MAC	Available	Not available
PIP	Available	Not available
HDLC	Synchronous and asynchronous	Synchronous only
PWM	Eight PWM timers	None

MPC8xx Functionality Not Supported by PowerQUICC II(2 of 2)

Function	MPC8xx	PowerQUICC 2
Ethernet	Parallel CAM interface and 1 byte sample from port B	CAM interface not available

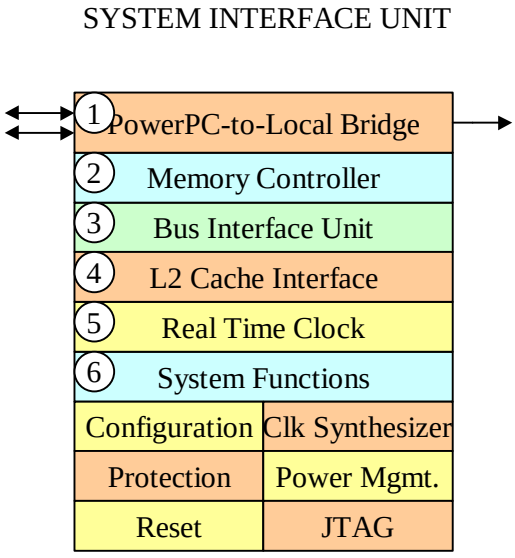
What are the 603e Components?



Unit Descriptions

1. Sequential Fetcher - fetches the instructions from the instruction cache into the instruction queue.
2. Branch Processing Unit - extracts branch instructions from the fetcher and uses static branch prediction on unresolved conditional branches to allow the instruction unit to fetch instructions from a predicted target instruction stream while a conditional branch is evaluated.
3. Instruction Queue - holds as many as six instructions and loads up to two instructions from the instruction unit during a single cycle.
4. Dispatch - dispatches instructions to their respective execution units at a maximum rate of two instructions per cycle.
5. Integer Unit - executes all integer instructions.
6. Load/Store Unit - executes all load and store instructions and provides the data transfer interface between the GPRs and the cache/memory subsystem.
7. System Register Unit - executes various system-level instructions, including condition register logical operations and move to/from special-purpose register instructions.
8. Completion Unit - tracks instructions from dispatch through execution, and then retires, or “completes” them in program order.

What are the Basic SIU Components?



Block Summary

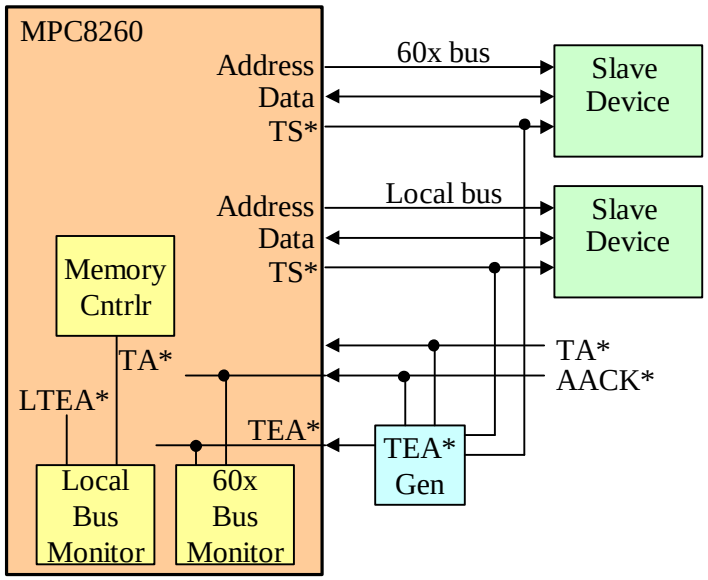
1. PowerPC-to-Local Bridge - allows 603 to access locations on local bus.
2. Memory Controller - supports 12 banks of SRAM, DRAM, and SDRAM.
3. Bus Interface Unit - interfaces the 60x bus to the CPM
4. L2 Cache Interface -easy interface to an L2 cache
5. Real-time Clock - provides an interrupt every second.
6. System Functions

• Configuration - configures various system pins such as those for data parity.
• Protection - hardware and software watchdogs
• Reset - reset monitoring and generation.
• Clock synthesizer - generates internal clocks from external clock oscillator
• Power management - controls normal and low power
• JTAG - IEEE 1149.1 test access port.

What is the Bus Monitor?

Definition The MPC8260 operates the same as the MPC860 except that:
1. The timeout period applies to both 60x bus and Local bus, and
2. There are separate enabling bits for 60x bus and Local bus.

Example



1. When the 8260 accesses a slave device, it requires...
2. TA* (Transfer Acknowledge) or AACK* to be asserted to indicate data can be latched by the 8260 (if a read access) or to indicate data has been latched by the slave device (if a write access) or the address has been latched if an address tenure only. If none of these are asserted, e.g. if the address is non-existent, then...
3. TEA* must be asserted for the 8260 to terminate the cycle.

Asserting Transfer Error Acknowledge

To assert TEA*, the user can either:
1. Add external logic or
2. Enable the bus monitor; the local bus monitor and 60x bus monitor can be enabled individually.

Initializing the Bus Monitor

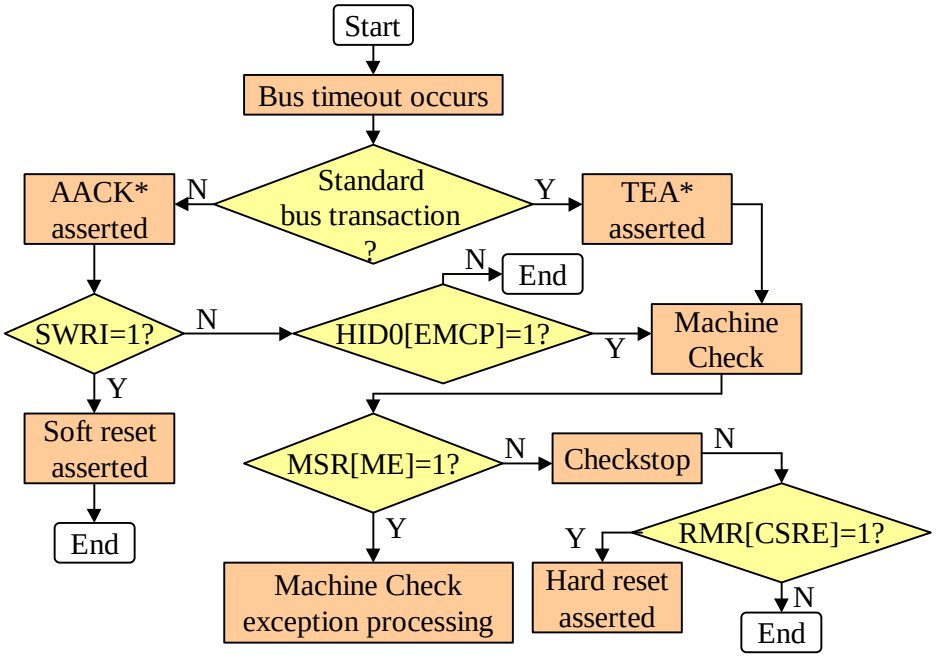
The bus monitor is enabled by initializing two parameters:
1. The length of the bus monitor timeout and
2. Bus monitor enable, local and 60x.

How a Bus Timeout is Processed

Introduction

A bus timeout is processed according to the type of bus transaction and the value of SYPCR[SWRI].

Flow of Operation



Description

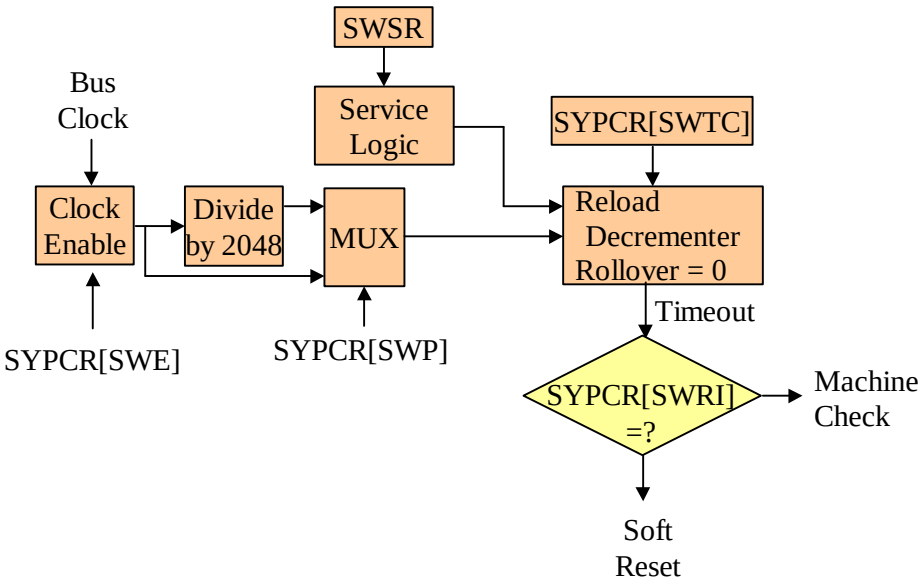
1. If a bus timeout occurs for a standard bus transaction, a machine check occurs.
2. If a bus timeout occurs for a non-standard bus transaction, either a machine check or a soft reset occurs depending on SYPCR[SWRI].
3. The response of a machine check depends on the state of the ME bit of the Machine State Register.
4. If ME=1, then machine check exception processing occurs.
5. If ME=0, then the 8260 enters the Checkstop state. If the CSRE bit in the RMR is set, hard reset is asserted.

What is the Software Watchdog?

Definition

To prevent system lockout in case the software becomes trapped in loops with no controlled exit, the 8260 has a software watchdog.

Flow Diagram



Timeout Prevention

1. To prevent a timeout, the software must…
   - Write 0x556C to SWSR followed by…
   - Write 0xAA39 to SWSR
2. If the software "gets lost" these writes will not occur which will cause a timeout.

Constraint

The software watchdog is enabled after reset. If it is not needed, the user must clear SYPCR[SWE]. Once a write to the SYPCR occurs, the state of SYPCR[SWE] cannot be changed.

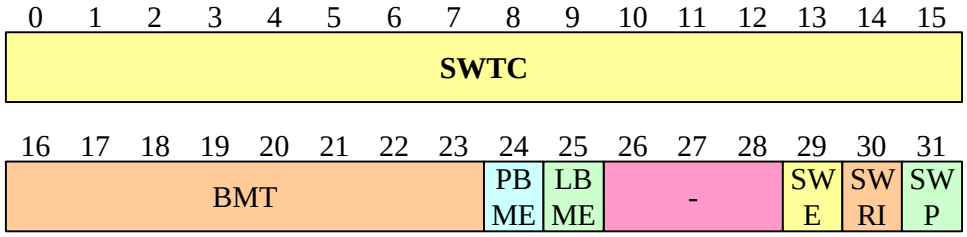
How to Initialize the Hardware and Software Watchdogs

Introduction

Initialization for the hardware and software watchdogs is shown below.

Programming Model

SYPCR - System Protection Control Register P. 4-33



Example

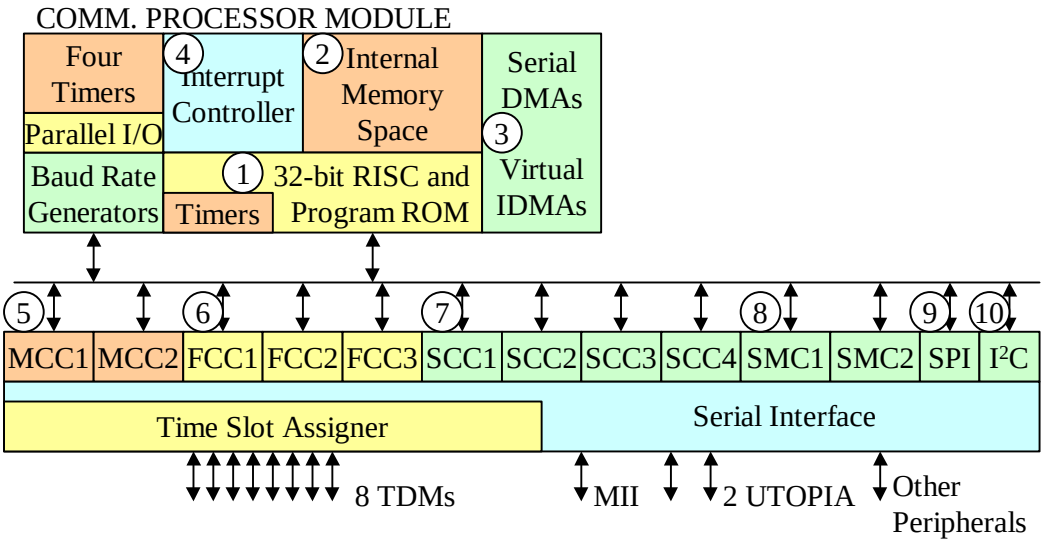
Initialize SYPCR for the following:

- A bus monitor timeout of 80 clocks for 60x bus only
- A software watchdog timeout of 1 ms assuming a 66 MHz bus clock. If a timeout occurs, a machine check should be the response.

SWTC = Timeout * BusClkFreq/(1 or 2048)
= 10^{-3} * 66 * 10^{6}/2048
= 32

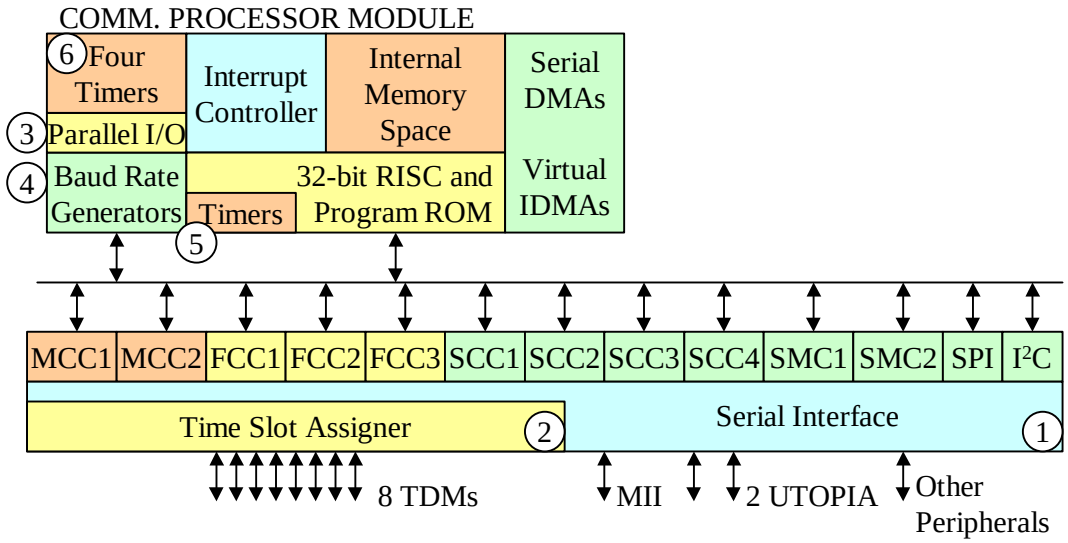
```
pimm->SYPCR = 32<<16 + (80/8)<<8 + 0x85;
```

What are the Basic CPM Components? (1 of 2)



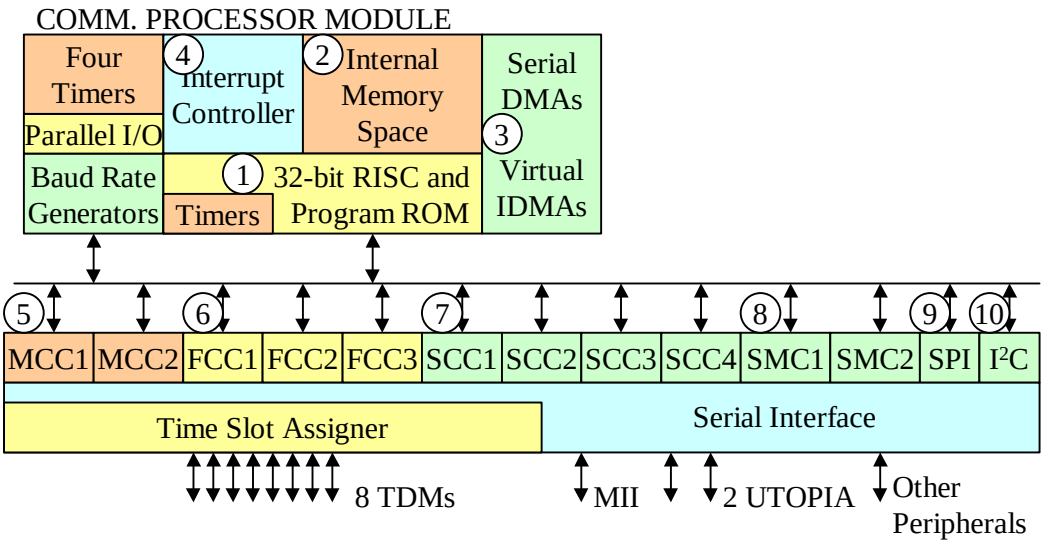
No.	Function
1	RISC and ROM - handles the serial communication devices, virtual DMA, timers, etc.
2	Internal Memory Space - interfaces the RISC to the PowerPC. Consists of registers and dual port RAM.
3	SDMA - transfers data between the communications devices and buffers which may be on 60x bus or local bus. IDMA - transfers data as specified by the user: memory-to-memory, device-to-memory, and memory-to-device.
4	Interrupt Controller - processes all interrupt sources.
5	Multi-channel Communication Controller - each MCC transfers data between 128 logical channels; external interface only through TDMs.
6	Fast Communication Controller - serial communication controllers optimized for synchronized high-rate protocols: HDLC, Ethernet, and ATM.
7	Serial Communication Controller - same as MPC860 SCCs.
8	Serial Management Controller - same as MPC860 SMCs.
9	Serial Peripheral Interface - same as MPC860 SPI.
10	InterIntegrated Circuit - same as MPC860 I^2C.

What are the Basic CPM Components? (2 of 2)



No.	Function
1	Serial Interface - connects the physical layer serial pins to the communication devices.
2	Time Slot Assigner - multiplexes data from any combination of the communication devices (except SPI and I^2C).
3	Parallel I/O - ports A, B, C, and D when configured as I/O.
4	Baud Rate Generators - internal clock sources for the FCCs, SCCs and SMCs.
5	Internal Timers - same as MPC860 internal timers except no PWM available.
6	General Purpose Timers - same as MPC860.

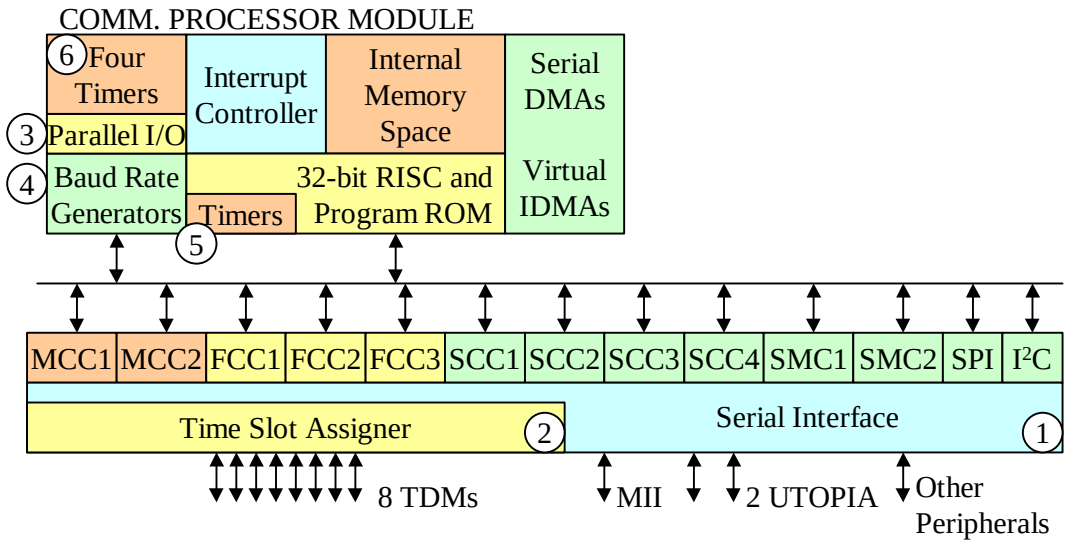
What is the Performance of the CPM Components? (1 of 2)



- Supports an aggregate serial bit rate up to 710 Mbps @ 133 MHz.

No.	Function
1	RISC and ROM - executes one instruction per clock.
2	Internal Memory Space - accessible by RISC in one clock cycle. Accesses outside of the CPM are two cycles.
3	SDMA - transfers data at a rate required by the protocol, as much as an 8 word burst. IDMA - transfers data a byte, half-word, word, doubleword or an 8 word burst.
4	Interrupt Controller -
5	Multi-channel Communication Controller - transfers HDLC and transparent data at a rate up to 256, 64Kbps channels.
6	Fast Communication Controller - transfers data up to 155 Mbps in ATM mode.
7	Serial Communication Controller - up to 62.5 MHz at 133 MHz CPM clock.
8	Serial Management Controller - up to 8.31 MHz at 133 MHz CPM clock.
9	Serial Peripheral Interface - up to 66.5 MHz at 133 MHz CPM clock, slave mode.
10	InterIntegrated Circuit - up to 2766 KHz at 133 MHz CPM clock.

What is the performance of the CPM Components? (2 of 2)



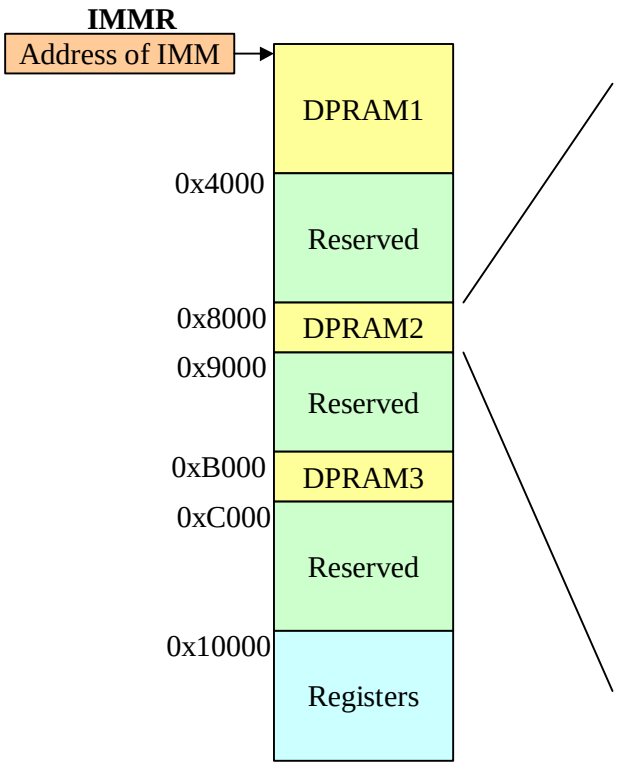
No.	Function
1	Serial Interface - up to 1/2 the CPM clock rate.
2	Time Slot Assigner -up to 256, 64 Kbps channels.
3	Parallel I/O -
4	Baud Rate Generators - can be driven by the internal BRGCLK which can be as fast as the CPM clock divided by 2.
5	Internal Timers - driven by the CPM clock divided by 1024, maximum rate.
6	General Purpose Timers - driven by the CPM clock, maximum rate.

Examples of Protocols Supported Concurrently

FCC1	FCC2	FCC3	MCC	CPM Clock	60x Bus Clock
155Mbps ATM	100BaseT	100BaseT		133 MHz	66 MHz
100BaseT	100BaseT	100BaseT		133 MHz	66 MHz
155Mbps ATM			128*64Kbps channels	133 MHz	66 MHz
100BaseT	100BaseT		128*64Kbps channels	133 MHz	66 MHz
155Mbps ATM			256*64Kbps channels	166 MHz	66 MHz
100BaseT			256*64Kbps channels	133 MHz	66 MHz
45Mbps HDLC			256*64Kbps channels	133 MHz	66 MHz
45Mbps HDLC	100BaseT		256*64Kbps channels	166 MHz	66 MHz
100BaseT			16*576Kbps channels	166 MHz	66 MHz

1. Here's a few examples the give an idea of the capability of PowerQUICC 2.
2. Two FCCs both operating at 155 Mbps is not possible except under resricted conditions which include: AAL5 only, long frames, and simple APC (CBR and UBR).

How to Locate the Internal Memory

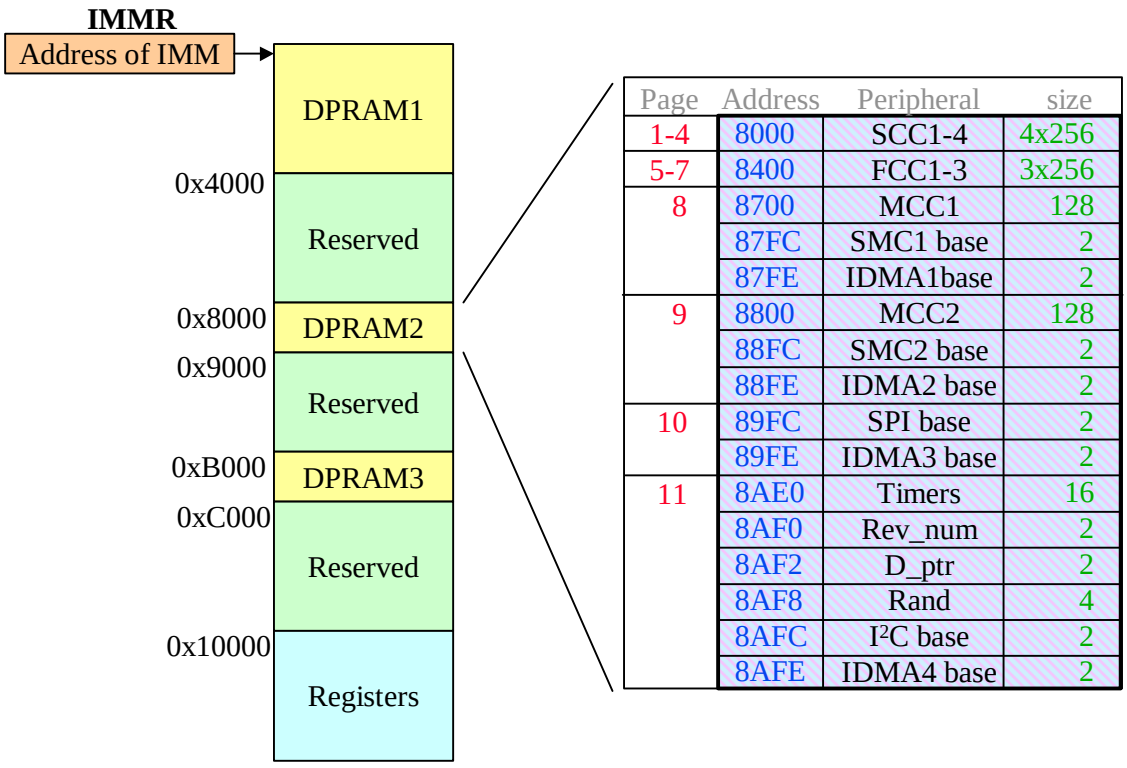


Page	Address	Peripheral	size
1-4	8000	SCC1-4	4x256
5-7	8400	FCC1-3	3x256
8	8700	MCC1	128
	87FC	SMC1 base	2
	87FE	IDMA1base	2
9	8800	MCC2	128
	88FC	SMC2 base	2
	88FE	IDMA2 base	2
10	89FC	SPI base	2
	89FE	IDMA3 base	2
11	8AE0	Timers	16
	8AF0	Rev_num	2
	8AF2	D_ptr	2
	8AF8	Rand	4
	8AFC	I^2C base	2
	8AFE	IDMA4 base	2

Description

1. The IMMR register points to the location of the internal memory map. IMMR is a special purpose register.
2. DPRAM1 is typically used for buffer descriptors and tables.
3. DPRAM2 is used for device parameter RAM.
4. DPRAM3 is typically used as an FCC temporary storage area for the CPM.
5. Rev_num is the microcode revision.

Exercise - How to Locate the Internal Memory



Page	Address	Peripheral	size
1-4	8000	SCC1-4	4x256
5-7	8400	FCC1-3	3x256
8	8700	MCC1	128
	87FC	SMC1 base	2
	87FE	IDMA1base	2
9	8800	MCC2	128
	88FC	SMC2 base	2
	88FE	IDMA2 base	2
10	89FC	SPI base	2
	89FE	IDMA3 base	2
11	8AE0	Timers	16
	8AF0	Rev_num	2
	8AF2	D_ptr	2
	8AF8	Rand	4
	8AFC	I^2C base	2
	8AFE	IDMA4 base	2

1. If IMMR = 0x96000102, then the internal memory map is located at the following address (see page 8-33 in UM): _____.

2. The register BCR is at the following address (see page 2-1 in UM): _____.

3. The MCC2 parameter block begins at the following address (see page 11-19 in UM): _____.

4. The HDLC specific parameter RAM for FCC2 begins at the following address (see page 29-4 in UM): _____.