June 24, 2010

PHY-Less Ethernet Implementation Using Freescale Power Architecture® Based Microprocessors

FTF-NET-F0568

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Session Introduction

- This session focuses on some of the considerations of designing an Ethernet solution with a Freescale processor but without an external transceiver (PHY).
- The importance of these considerations can greatly reduce the probability of encountering design issues based on the chosen Ethernet interface or attachment unit interface (AUI). Media independent interface (MII), reduced gigabit MII (RGMII), and serial gigabit MII (SGMII) are examples used for this session.
- I am a member of the applications support team and have worked on several customer tickets inquiring about various products and their capability to perform to specifications without an external PHY.

Session Objectives

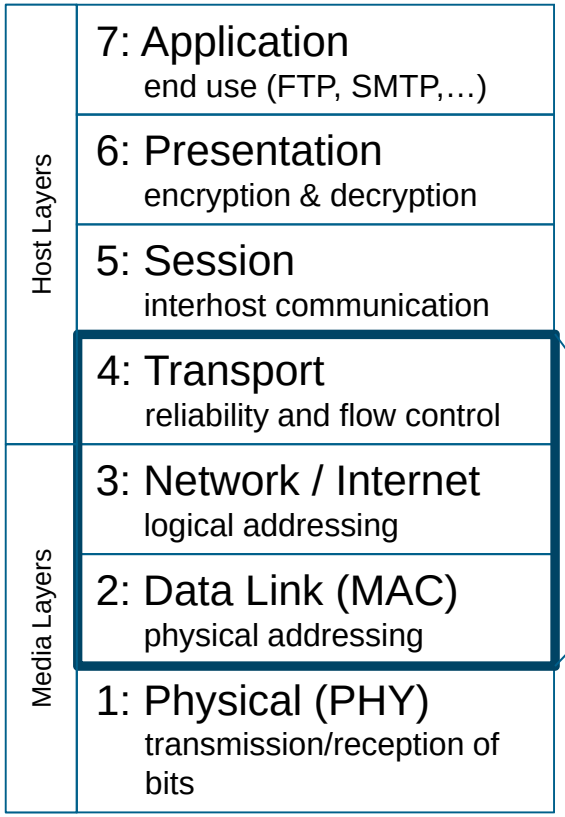
- After completing this session you will have an understanding of:
  - The caveats of no PHY with the MII interface in Half-Duplex Mode
  - The expectations of no PHY with the RGMII interface
  - The expectations of no PHY with the SGMII interface
  - The basic principles to apply to any chosen interface

Agenda

- Supported Layers of the Open System Interconnection (OSI) Model
- Supported Ethernet Interfaces (AUIs)
- Role of the Transceiver (Ethernet PHY)
- Cases When a PHY Is Not Needed
- Design Considerations for Freescale Processors Built on Power Architecture Technology
- Summary

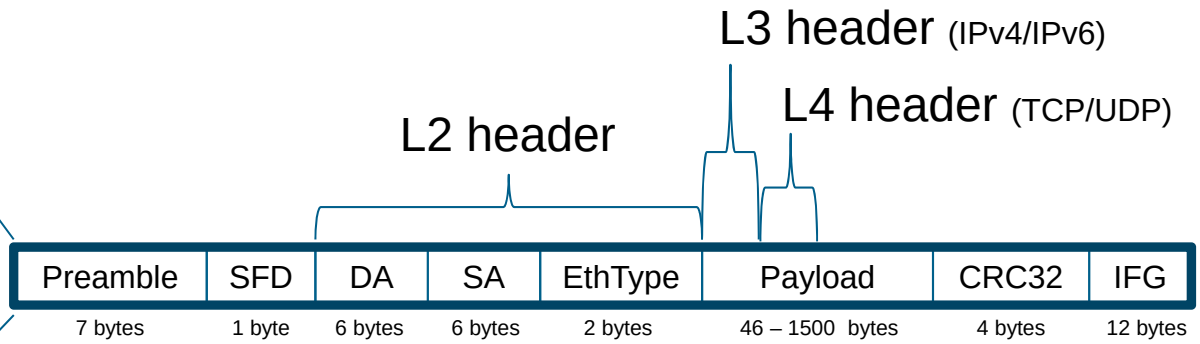
Supported Layers of the Protocol Stack by Freescale Ethernet Hardware

OSI Model Layers



Media Access Control (MAC)

Ethernet Type II Frame



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Supported Ethernet Physical Interfaces (AUIs)

INTERFACE	SPEED (Mbps)	DUPLEX
MII (Media Independent Interface)	10 / 100	Full / Half
RMII (Reduced MII)[1]	10 / 100	Full / Half
SMII (Serial MII)[1]	10 / 100	Full / Half
GMII (Gigabit MII)[2]	10 / 100 / 1000	Full
RGMII (Reduced GMII)[1]	10 / 100 / 1000	Full / Half
SGMII (Serial GMII)[1]	10 / 100 / 1000	Full / Half
XAUI (TEN Attachment Unit Interface)	10,000	Full
TBI (Ten Bit Interface)	1000	Full
RTBI (Reduced TBI)	1000	Full
FIFO (8/16-bit)	GMII Style (Platform Clk/4.2) Encoded (Platform Clk/3.2)	Full

Controllers CPM-FCC (8280,8560), QE-UEC (8360), FEC (880), TSEC (8560), eTSEC (8572), dTSEC (P4080), 10G (P4080), VeTSEC (P1020)
(Not all interfaces supported for each controller. Must refer to each products specific documentation.)

[1]Half Duplex -10/100 is supported on this interface via encoding methods because there are no physical COL and CRS signals.
[2] 10/100 supported via “fallback mode to MII”

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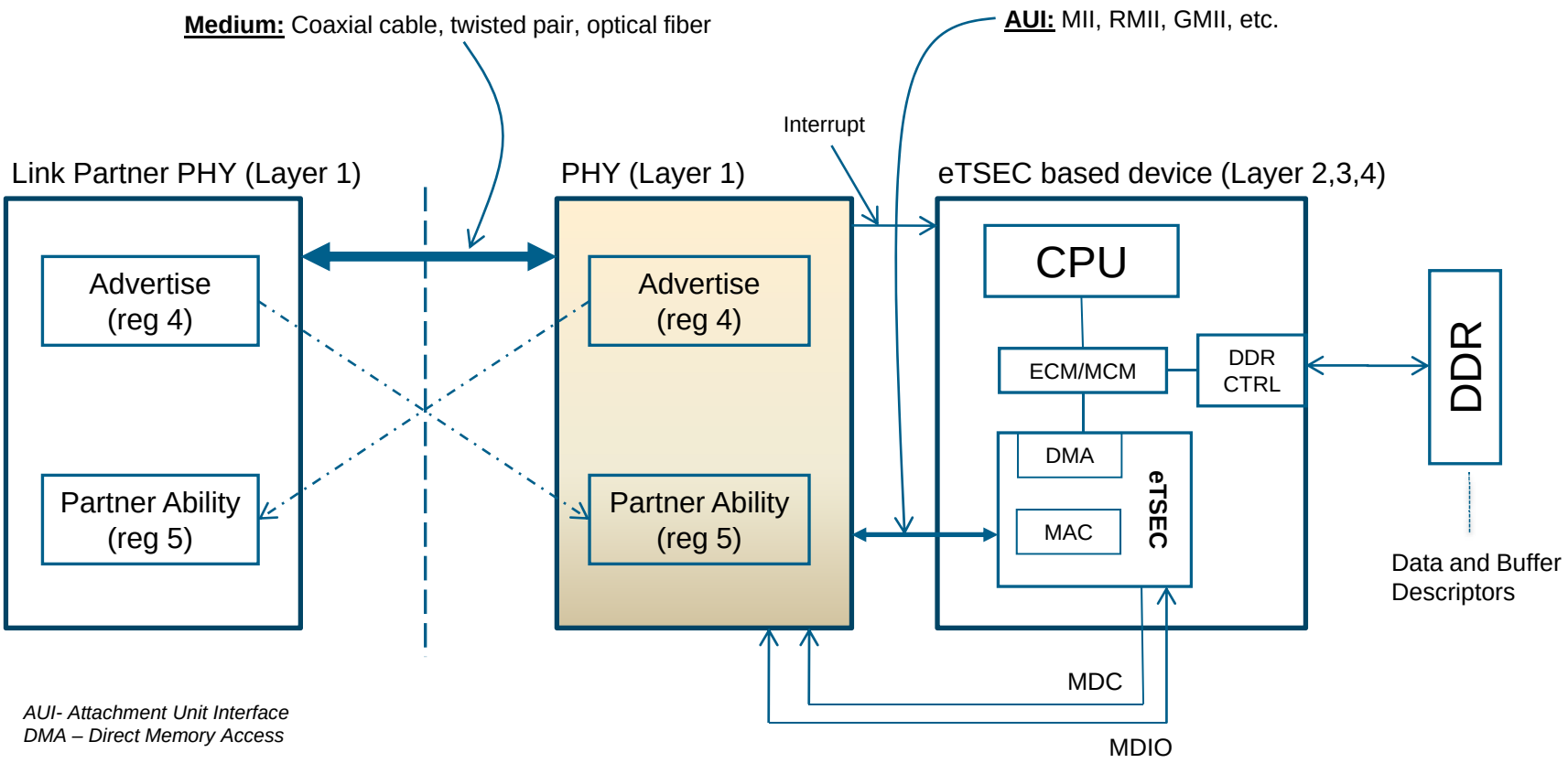
Role of the Transceiver

- Transceivers are called Medium Attachment Units (MAUs) in IEEE 802.3



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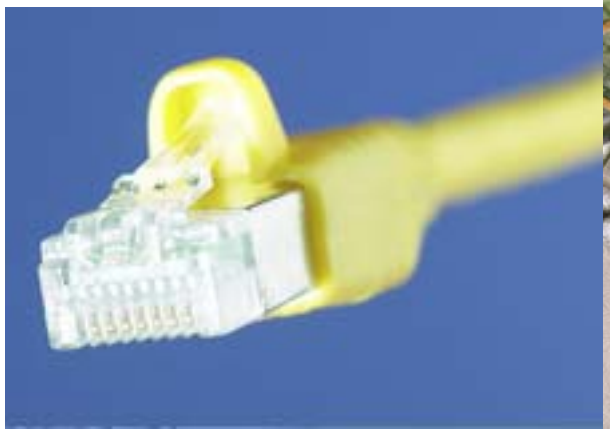
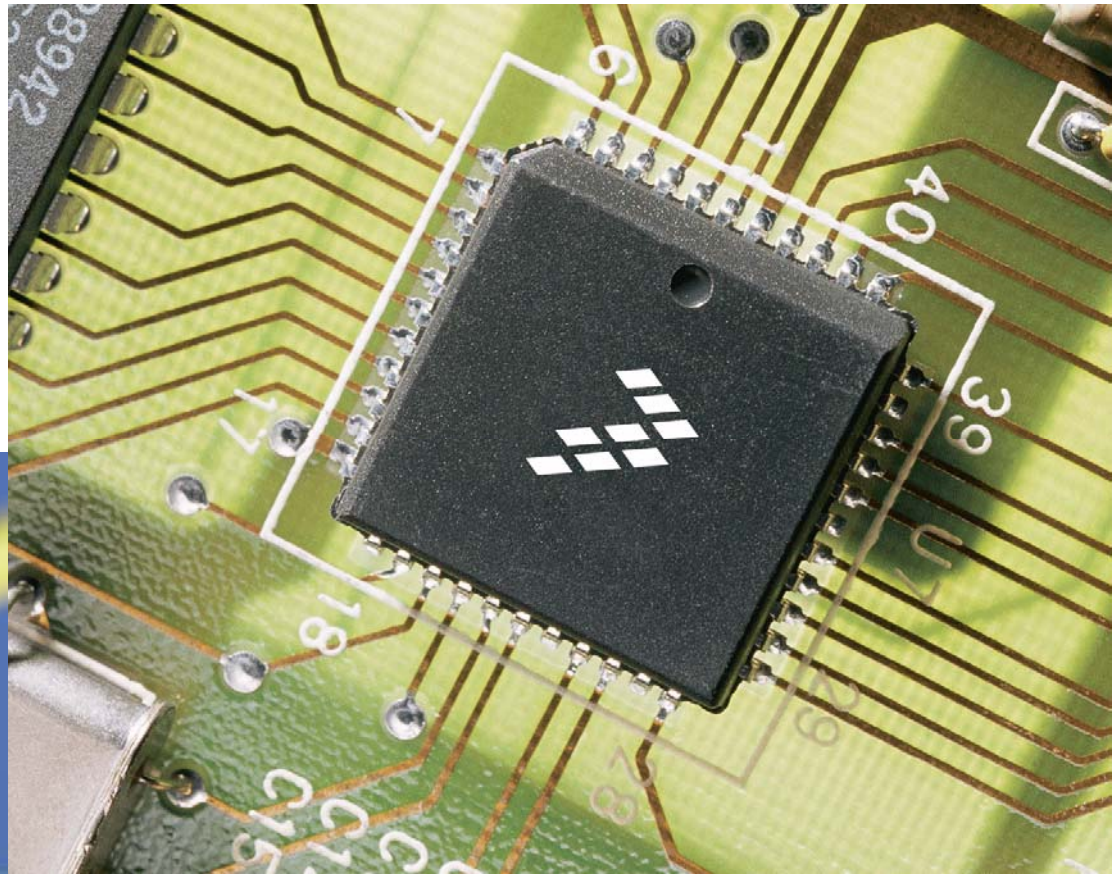
Possible Reasons PHY Is Not Needed

- Cost
- Real Estate
- Medium Distance
- Others





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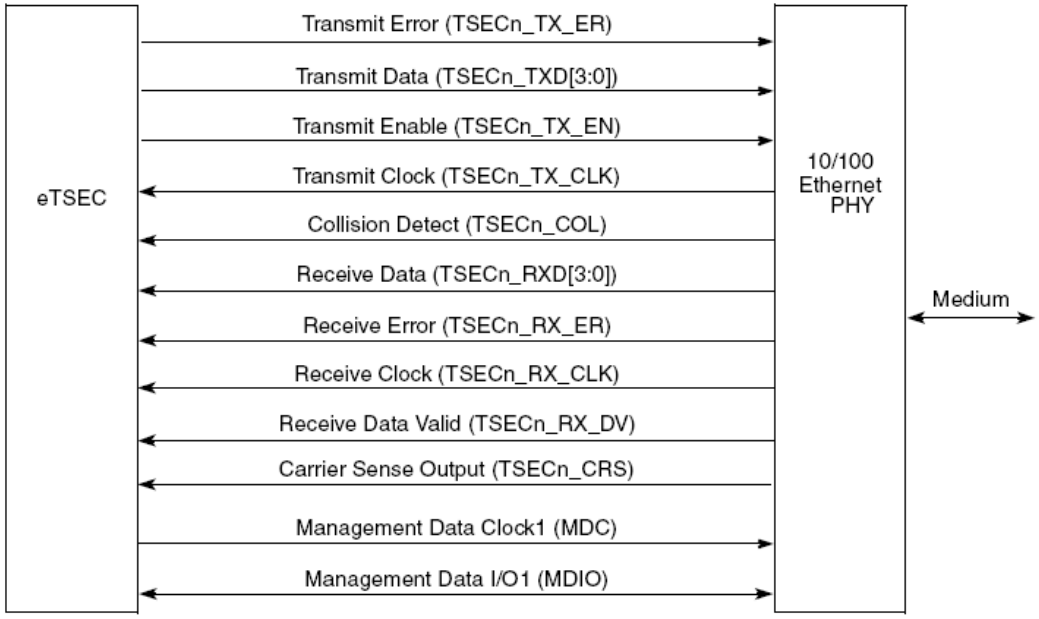
MII Half-Duplex with a PHY

- COL and CRS are active
- Clock speed 2.5 MHz or 25 MHz
- Collisions are normal and a back-off algorithm is used
- PHY manages the detection of collisions
- PHY manages the detection of the carrier
- Should be no reception when transmitting (No MAC loopback for Half-Duplex Mode)



[1] The management signals (MDC and MDIO) are common to all of the Ethernet controllers' connections in the system, assuming that each PHY has a different management address.

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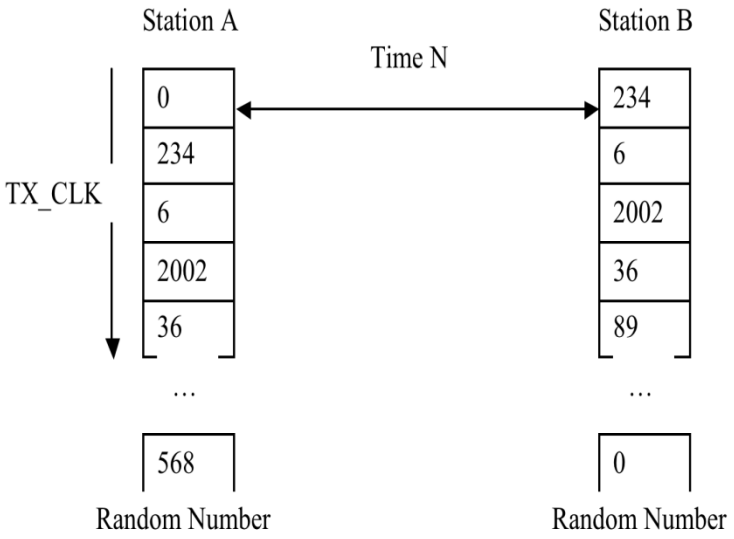
Linear Feedback Shift Register and Back-off Algorithm

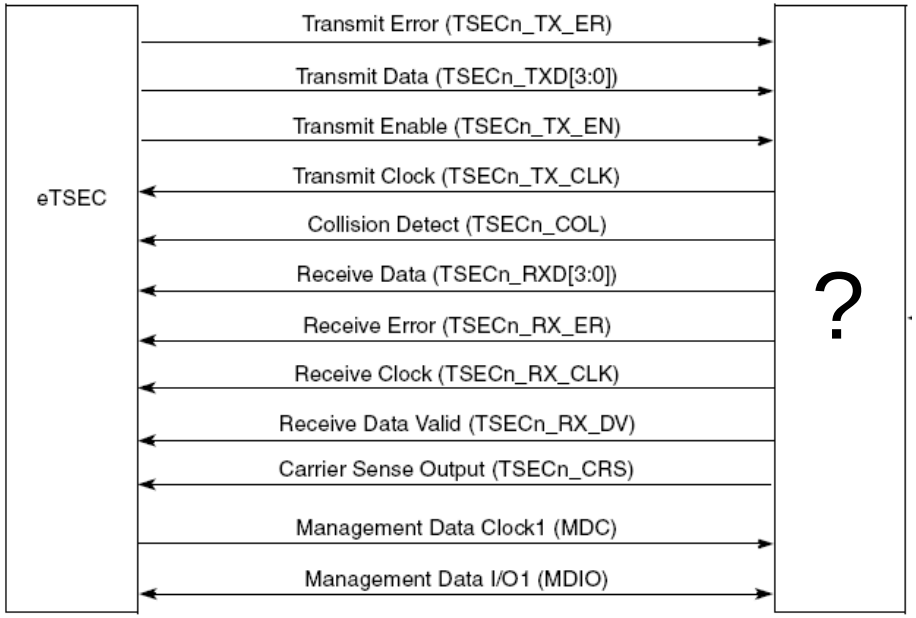
- Typically, when the PHY detects a collision event, it asserts the COL signal to the MPC8548. The MPC8548 then employs a back-off algorithm to determine the number of time slots to wait before retransmitting. One time slot equals 512 bits. The MAC-calculated back-off time is a multiple of 1 time slot and a generated ***random*** value. The MPC8548 processor employs the IEEE® standard 802.3™ back-off algorithm.
- '***random***' is based on hardware from an 11-bit linear feedback shift register (LFSR). The LFSR starts with a seed value based on the polynomial function implemented. For each Tx clock, the logic generates a pseudo-random number for use in the back-off time calculation. To add to the randomness, bit 2 of the 32-bit CRC from the eTSEC is XORed with bit 2 of the LFSR.

MPC8548 is used only as an example



MII Half-Duplex Without a PHY

- COL and CRS are active
- Clock speed 2.5 MHz or 25 MHz
- Collisions are normal and a back-off algorithm is used
- **Who** manages the detection of collisions?
- **Who** manages the detection of the carrier?
- Should be no reception when transmitting (No MAC loopback for Half-Duplex Mode)
- **What** are we connected to?
  - A bus
  - Point-to-point device
  - Backplane traces
  - A connector



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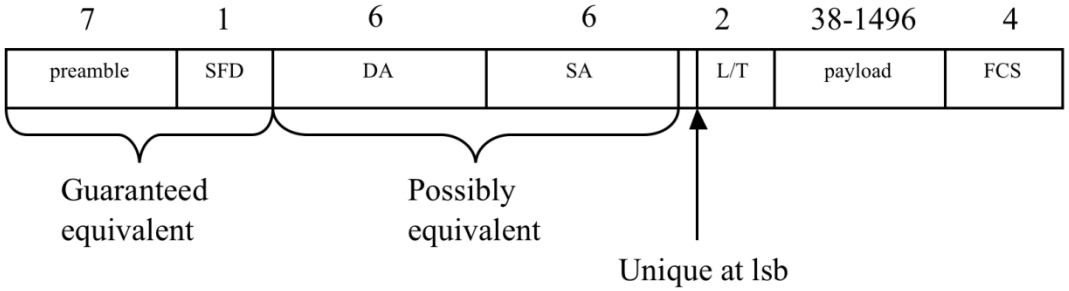
PHY-Less MII Half-Duplex Caveats

- Carrier Sense and Collision Detect ***must*** be provided.
- By default, if more than 15 collision events are detected before a successful transmission, the MPC8548 processor reports excessive collisions and no longer attempts to transmit the data. Software must take steps to re-enable the eTSEC transmitter.
- Because the values from the LFSR are deterministic, MAC-to-MAC connections can become synchronized relative to Tx clocks and generate identical backoff times, causing the devices in the system to re-transmit at the same time. This can lead to an excessive collision event.
- The logic that controls the assertion of the COL signal must ensure it only asserts after the preamble, SFD, DA, SA, and Type fields of an Ethernet frame (22 bytes into the frame). Since each Tx clock sends a nibble of data over the MII, this equates to 44 Tx clocks. In addition, the devices should exhibit a soft reset at different points in time while the Tx clock is running. Furthermore, the logic that drives the Rx_DV signal must not assert it to an MPC8548 processor that is concurrently transmitting and asserting TX_EN.



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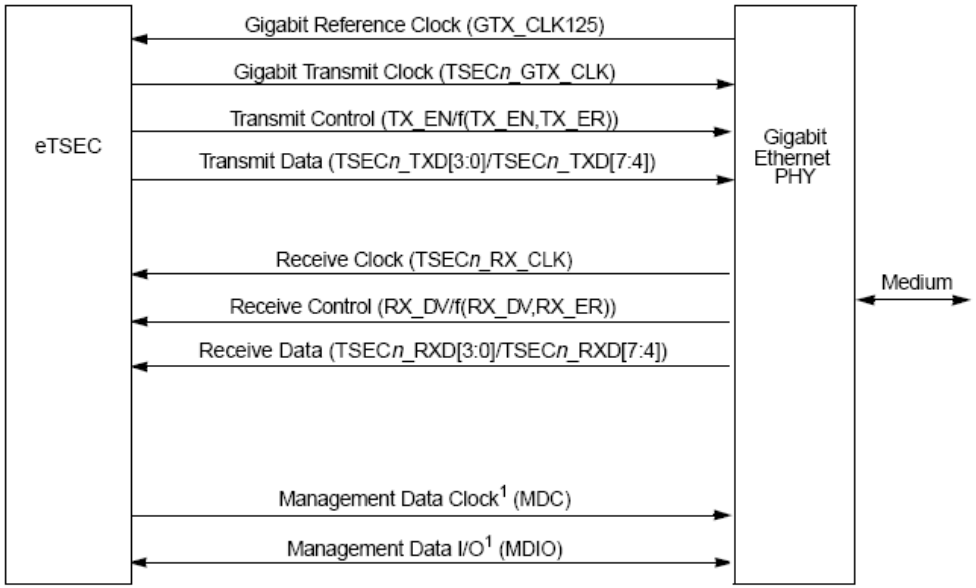
PHY-Less MII

- Ensure signal integrity
  - monotonic clock edges
  - meet rise/fall time and other timing requirements
  - matched I/O levels
- Point-to-Point connections
- Bus connections if there is an arbiter for CRS and COL

RGMII with a PHY

- External 125 MHz clock source is needed
- eTSEC outputs TX 125 MHz clock
- eTSEC has internal dividers to support 100 Mbps and 10 Mbps
- Half-Duplex is encoded (No COL and CRS signals used)
- TX and RX have different timings for the data (needed delay provided by trace or PHY)



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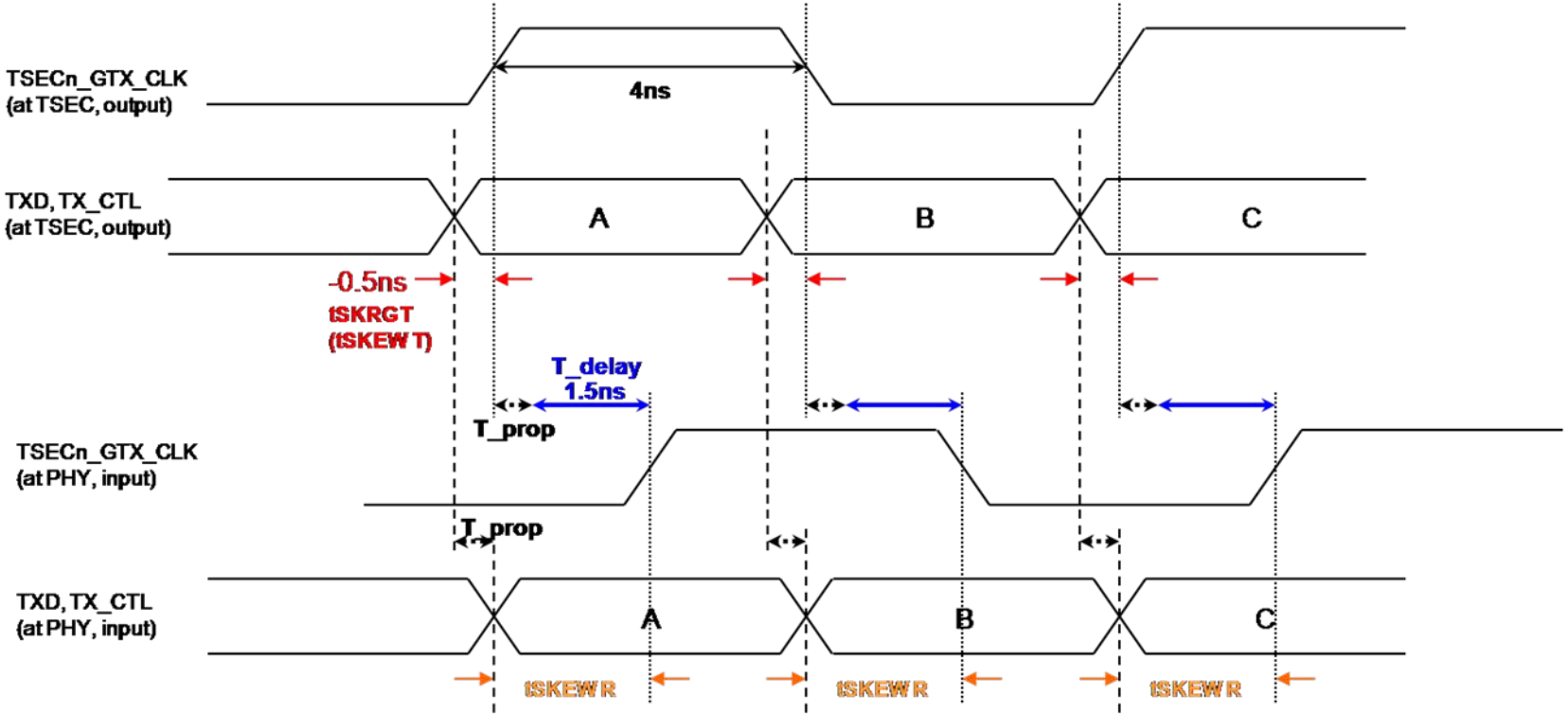
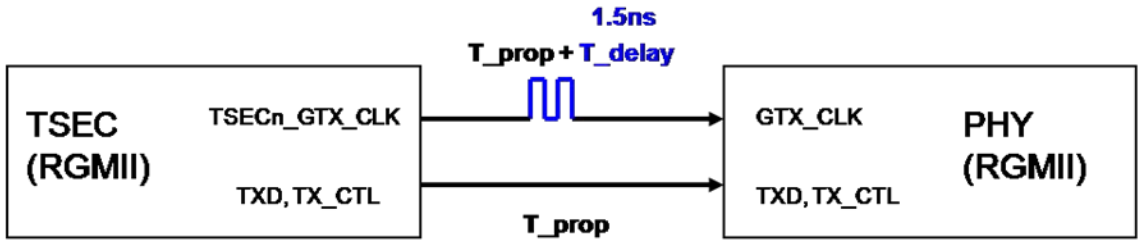
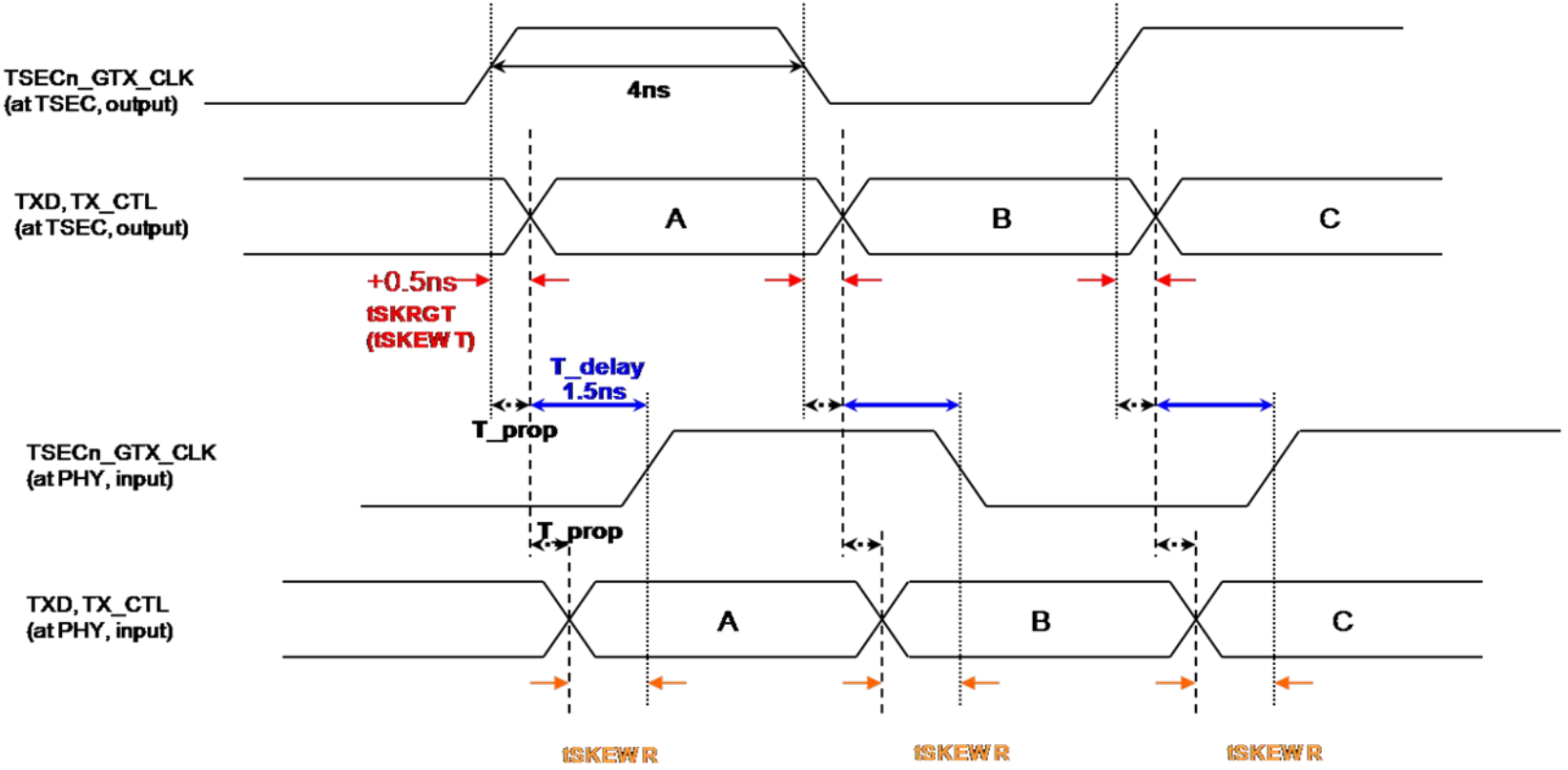
Tx Data leads the GTX_CLK (-0.5ns)



Spec	Min	max
tSKEW T	-0.5ns	0.5ns
tSKEW R	1ns	2.8ns



Tx Data lags GTX_CLK (+0.5ns)



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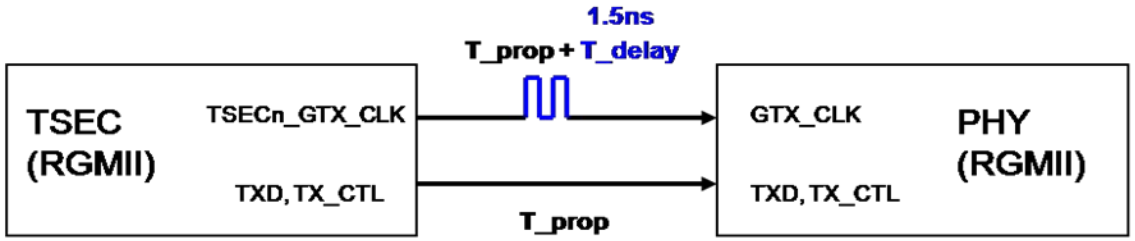

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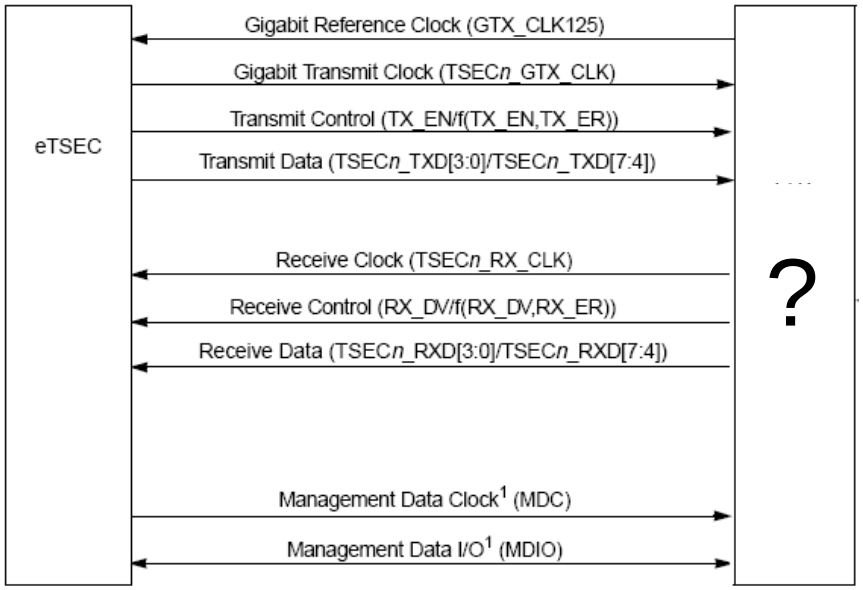

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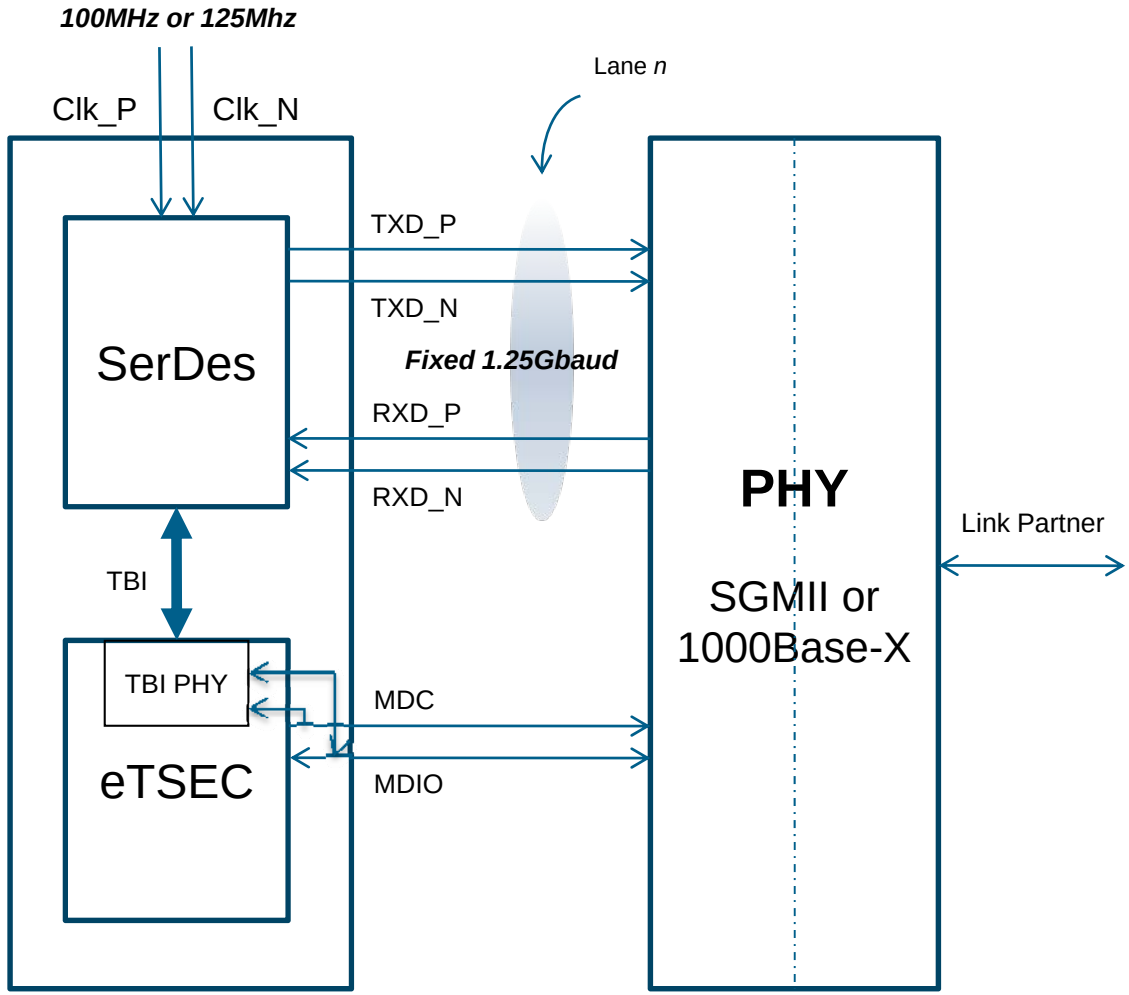
PHY-Less RGMII

- Ensure signal integrity
  - monotonic clock edges
  - meet rise/fall time and other timing requirements
  - matched I/O levels
  - TX and RX input skew specifications
- Point-to-point connection only

SGMII with a PHY

- SerDes block is used (differential signaling)
- Ten Bit Interface (TBI) interface signals are routed to the SerDes block
- 10/100/1000 Mbps supported with rate adaptation logic for SGMII. 1000Base-X is only 1 Gbps.
- Internal TBI PHY is used to establish the link (Speed fixed at 1000Mbps)
- Advertisement registers may have two formats: 1000Base-X or SGMII. SW determines which is used.



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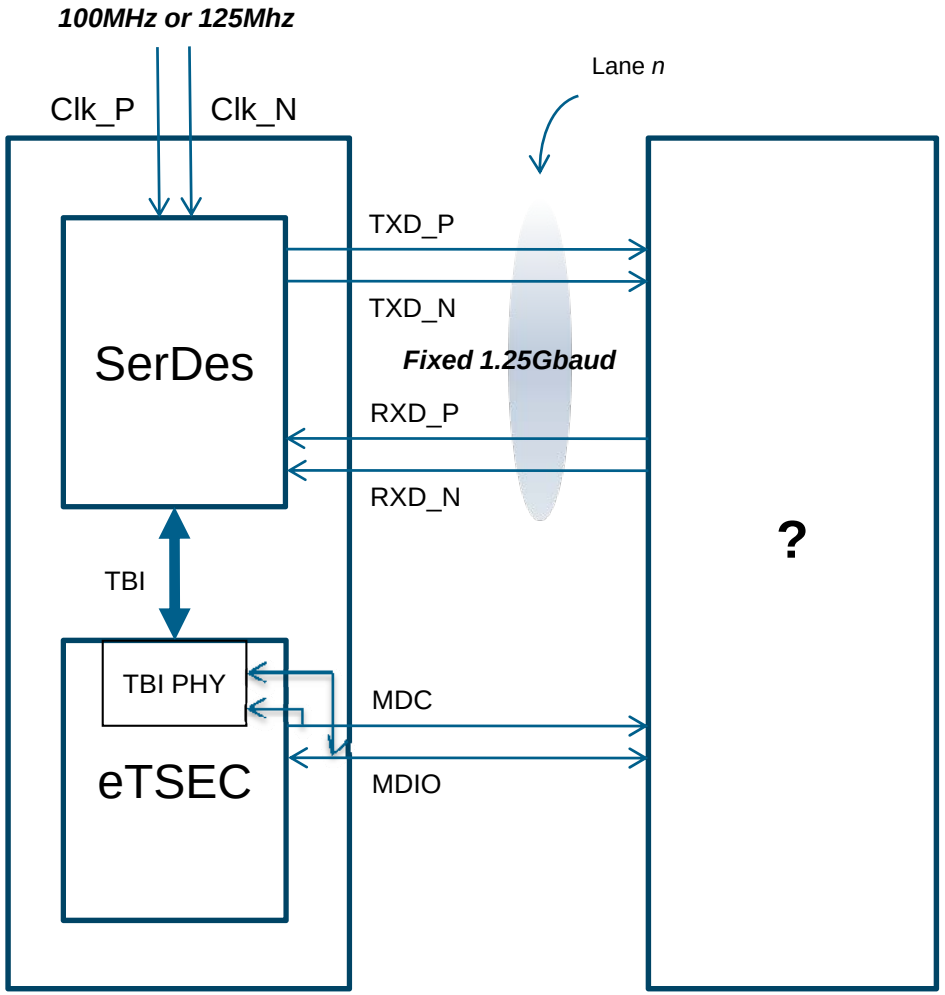

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PHY-Less SGMII

- Freescale processor employs built in TBI PHY
- Pay attention to trace length; Under 12 inches is OK
- SGMII and 1000Base-X format of Advertisement Registers read by software to determine capabilities
- 1000Base-X is 1 Gbps only. SGMII allows 10/100Mbps
- No auto-negotiation assumes link is good and TBI SR[Link Status] is set
- SerDes control registers are used.
- Ensure signal integrity
- Point-to-point connection only

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Session Summary

- Many physical interface options (AUIs) are available for an Ethernet solution
- Freescale designs to an interface specification, so in most cases operation without a PHY is possible if the interface signal requirements are met. Timings, IO levels, etc.
- Input Output Buffer Information Specification (IBIS) modeling can help determine signal degradation to/from our device across the interconnect.
- For MII Half-Duplex mode, Bit 2 of the 32-bit CRC mentioned is not active until the payload portion of the Ethernet frame. Therefore, the calculated back-off times of multiple eTSEC devices can be identical until the randomness of bit 2 of the 32-bit CRC is introduced.
- For SGMII, differential signaling should not be a problem for traces less than 12 inches.

For Further Information

- Visit http://www.freescale.com/powerquicc
- Request help at NSDsupport@freescale.com

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Session Closing

- You should understand
  - In most cases PHYless operation will work
  - IBIS modeling can help determine signal integrity
  - Where to find more information


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