June, 2010

DDR2 and DDR3 Deep Dive

FTF-NET-F0686

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Presenter Title

freescale™ semiconductor

Agenda

- Basic DDR SDRAM
  - Memory Organization & Operation
  - Read and write timing
  - Electrical signaling & termination
- PowerQUICC DDR Controllers
  - Features & Capabilities
  - Initialization & Register Configurations
  - Pitfalls / Debug Tips
  - Board design Pitfalls / Debug Tips

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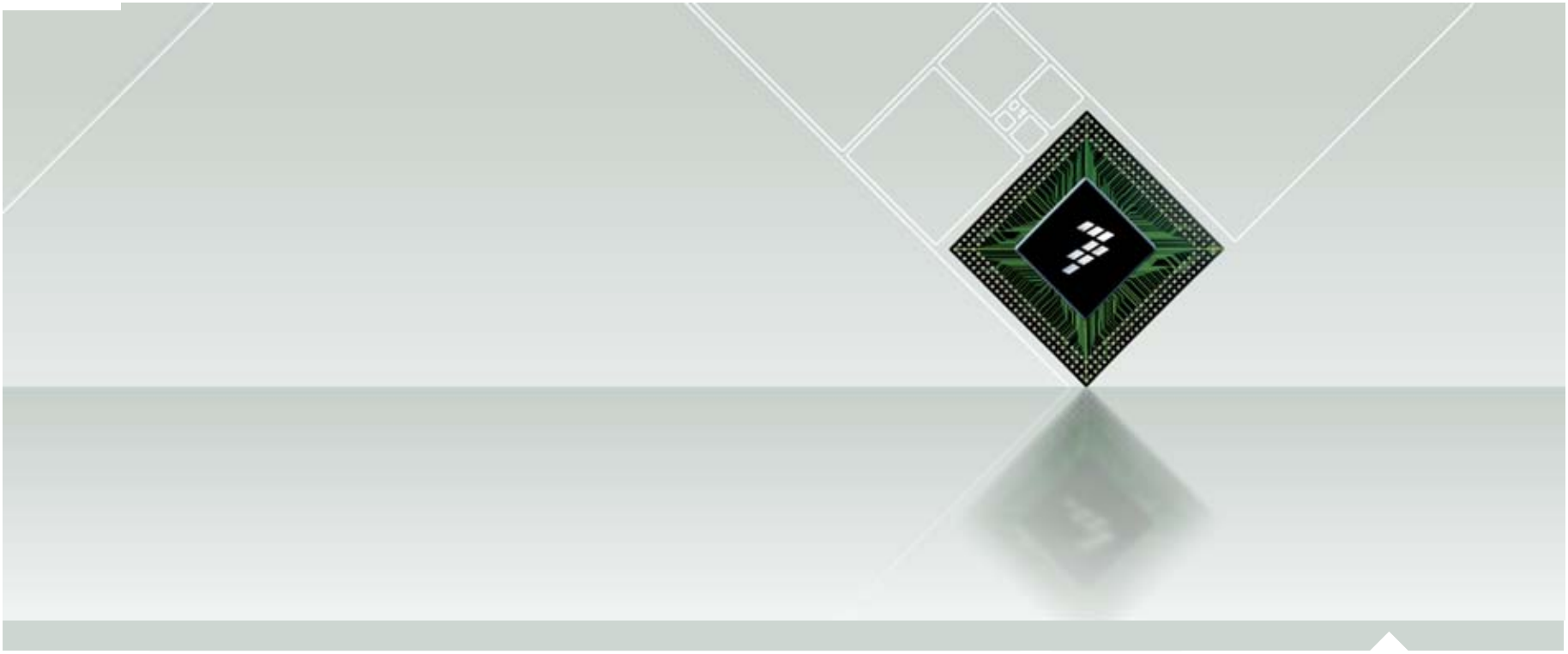

Basic DDR SDRAM

Memory Organization & Operation

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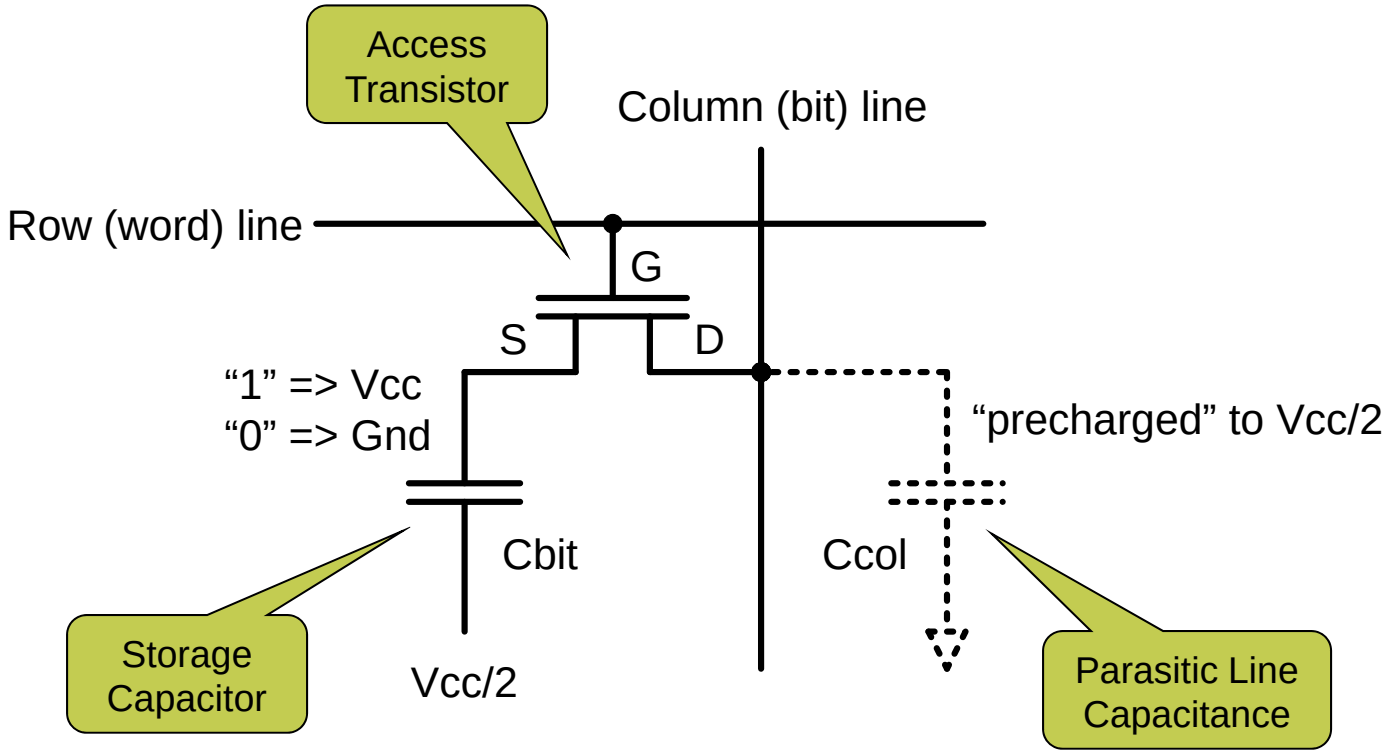
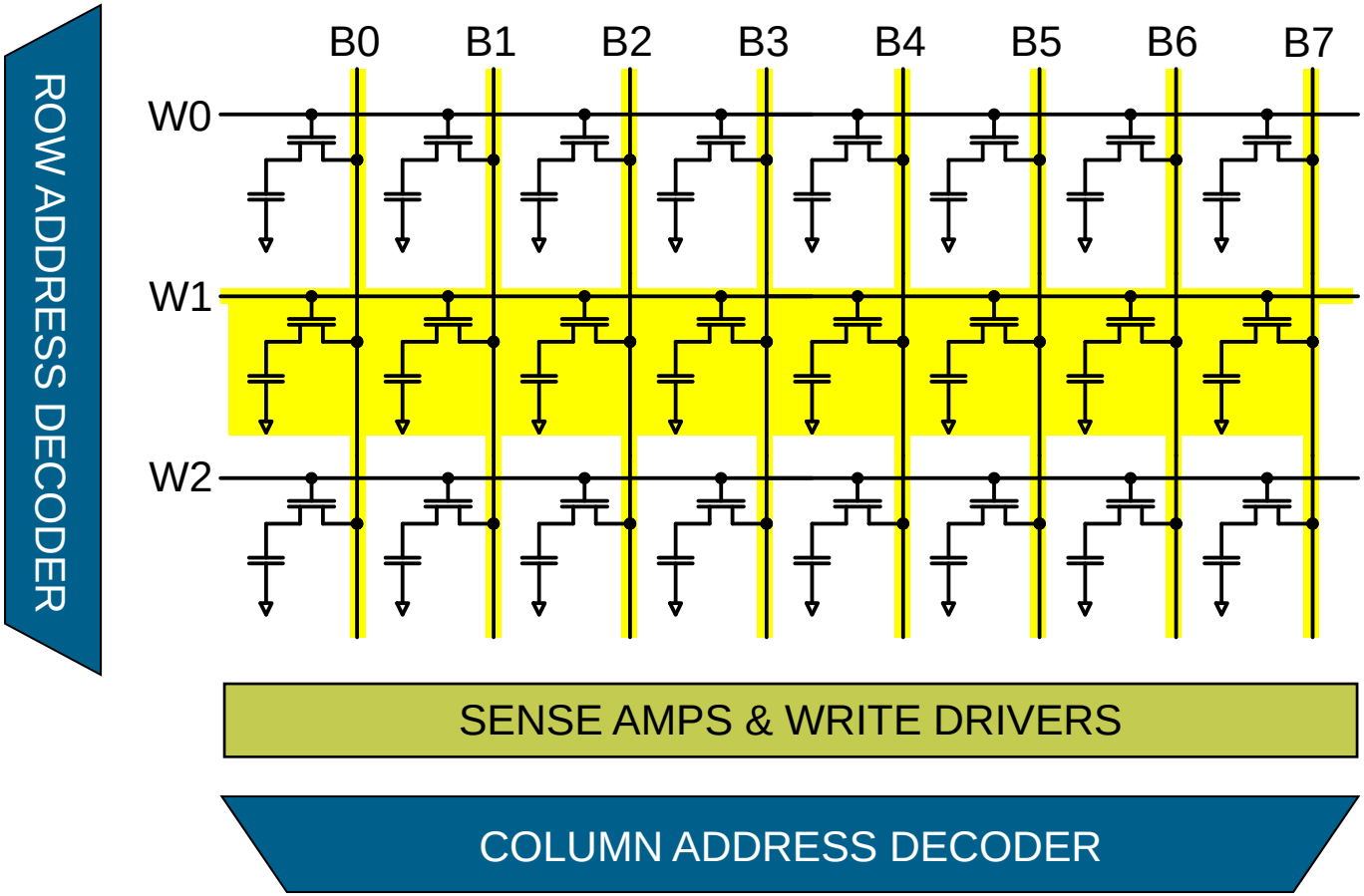
Single Transistor Memory Cell

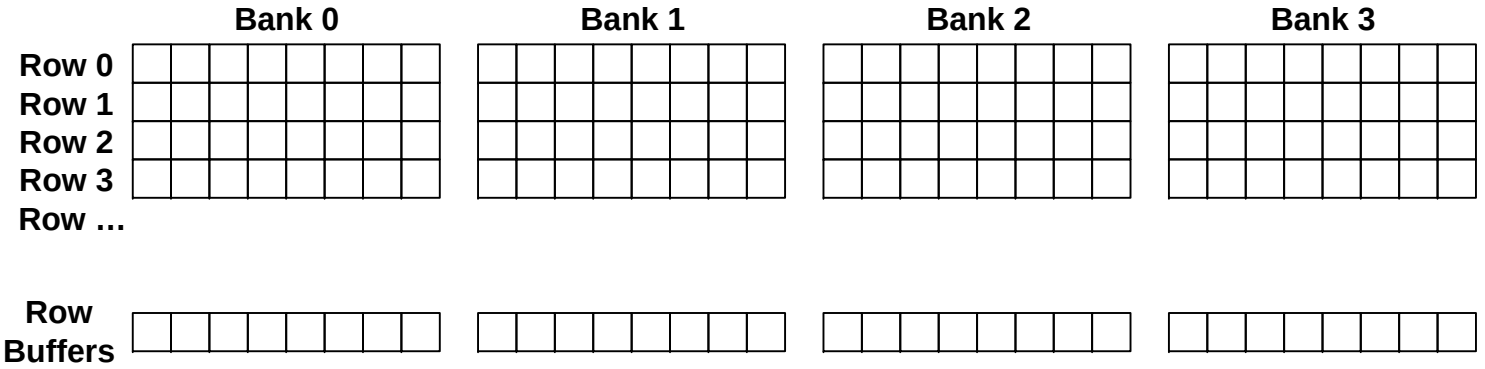


Memory Arrays



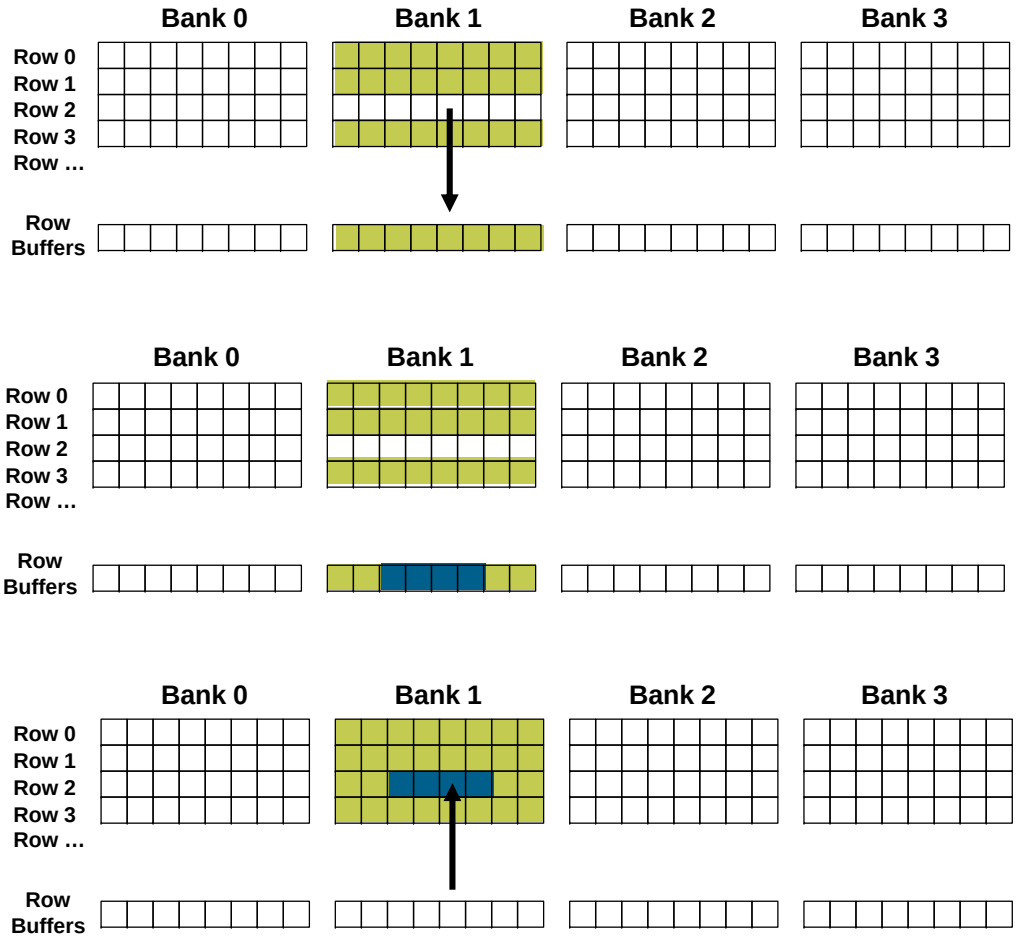
Internal Memory Banks

- Multiple arrays organized into banks
- Multiple banks per memory device
  - DDR1 – 4 banks, 2 bank address (BA) bits
  - DDR2 & DDR3– 4 or 8 banks, 2 or 3 bank address (BA) bits
  - Can have one active row in each bank at any given time
- Concurrency
  - Can be opening or precharging a row in one bank while accessing another bank
- May be referred to as “internal”, “logical” or “sub-” banks



Memory Access

- A requested row is ***ACTIVATED*** and made accessible through the bank's row buffer.
- ***READ*** and/or ***WRITE*** are issued to the active row.
- The row is ***PRECHARGED*** and is no longer accessible through the bank's row buffer.



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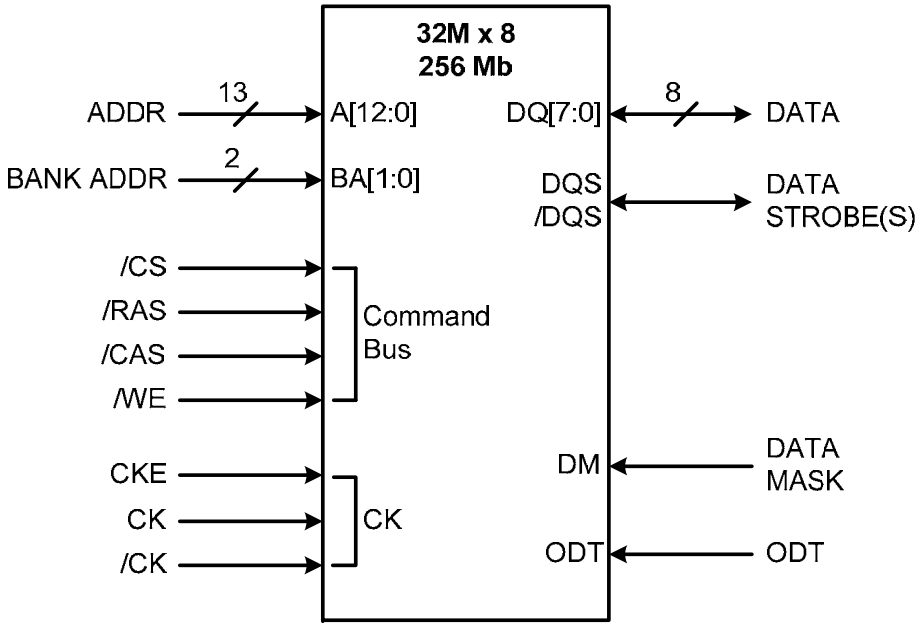
Example – DDR2 SDRAM

- Infineon HYB18T256800AF or Micron MT47H32M8

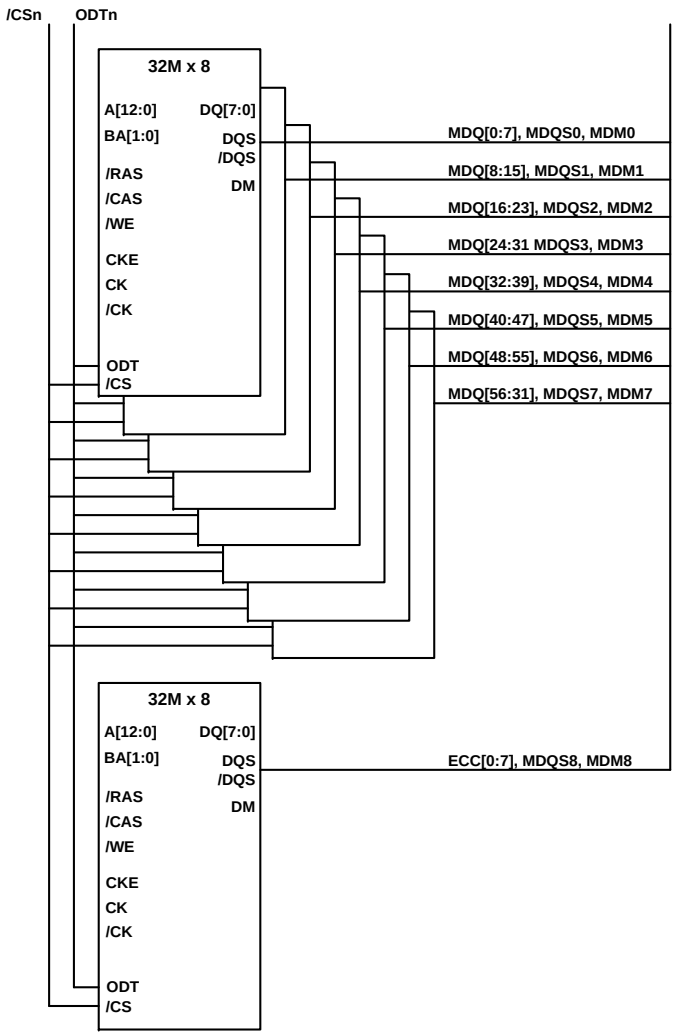
- 32M x 8 (8M x 8 x 4 banks)
- 256 Mb total

- 13-bit row address
  - 8K rows
- 10-bit column address
  - 1K bits/row (8K total when you take into account the x8 width)
- 2-bit bank address



Example – DDR2 DIMM

- Infineon HYS72T3200HU or Micron MT9HTF3272A
- 9 each 32M x 8 memory devices
- 32M x 72 overall
- 256 MB total
- Single “rank”
- 9 “byte lanes”



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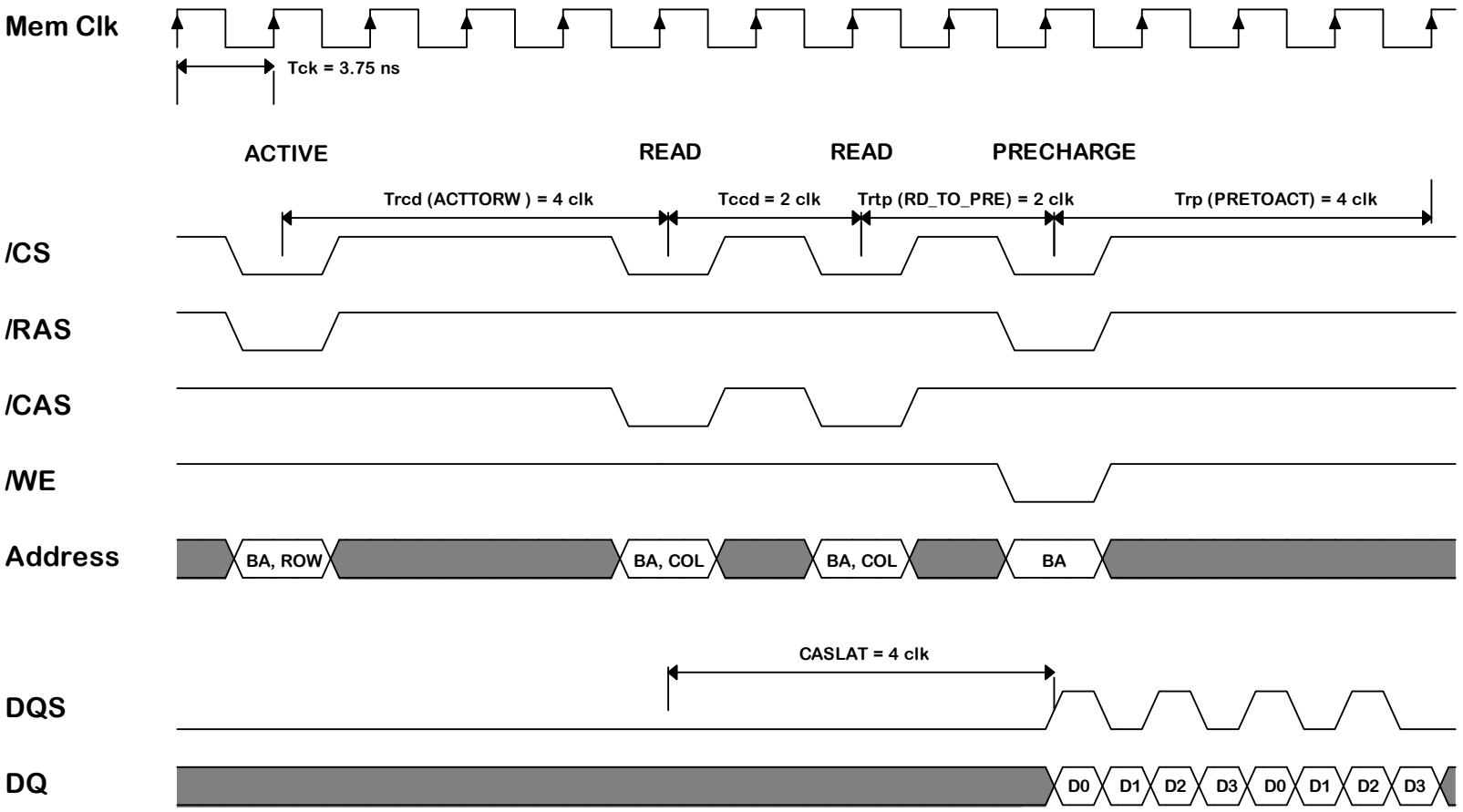
DDR1/DDR2/DDR3 Basic Command Summary

Command	/CS	/RAS	/CAS	/WE	ADDR
NOP	H	X	X	X	X
NOP	L	H	H	H	X
ACTIVE	L	L	H	H	BA, Row
READ	L	H	L	H	BA, Col
WRITE	L	H	L	L	BA, Col
PRECHARGE	L	L	H	L	BA
PRECHARGE ALL	L	L	H	L	A[10]
REFRESH	L	L	L	H	X
LOAD MODE REGISTER	L	L	L	L	Bank, OpCode

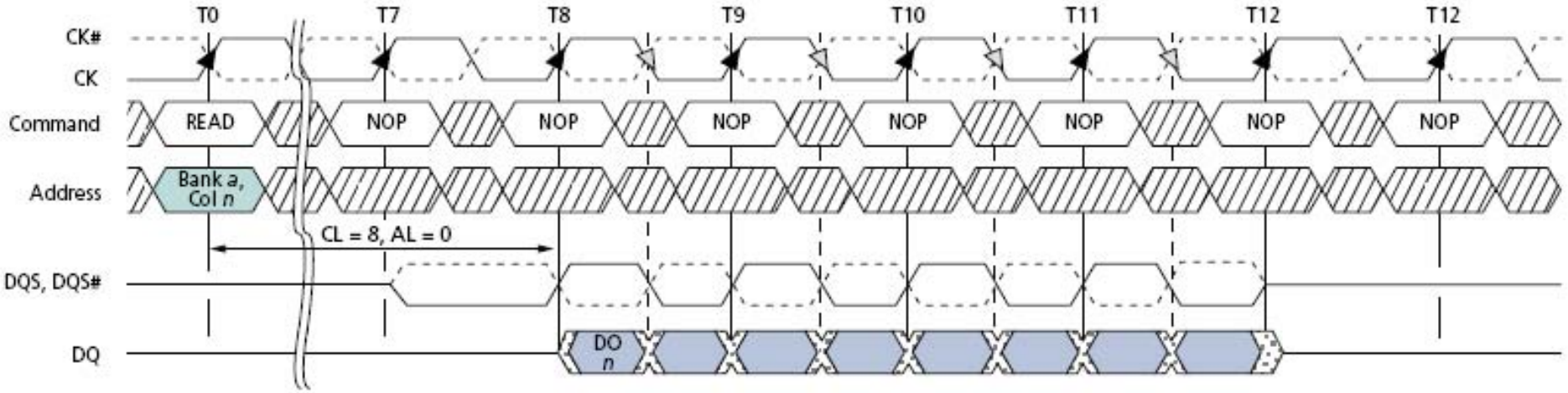
Read/Write Bursting

- Activating and/or precharging rows can be time consuming
- Once a row is open, only the bank and starting column address are needed for R/W bursts
  - Memory device increments an internal column address counter
- Cache line oriented:
  - For a 64-bit wide memory bus:
    - 4-Beat burst => 32 bytes
    - 8-Beat burst => 64 bytes
  - For a 32-bit wide memory bus:
    - 8-Beat burst => 32 bytes

DDR2-533 Read Timing Example



DDR3 Read Timing Example



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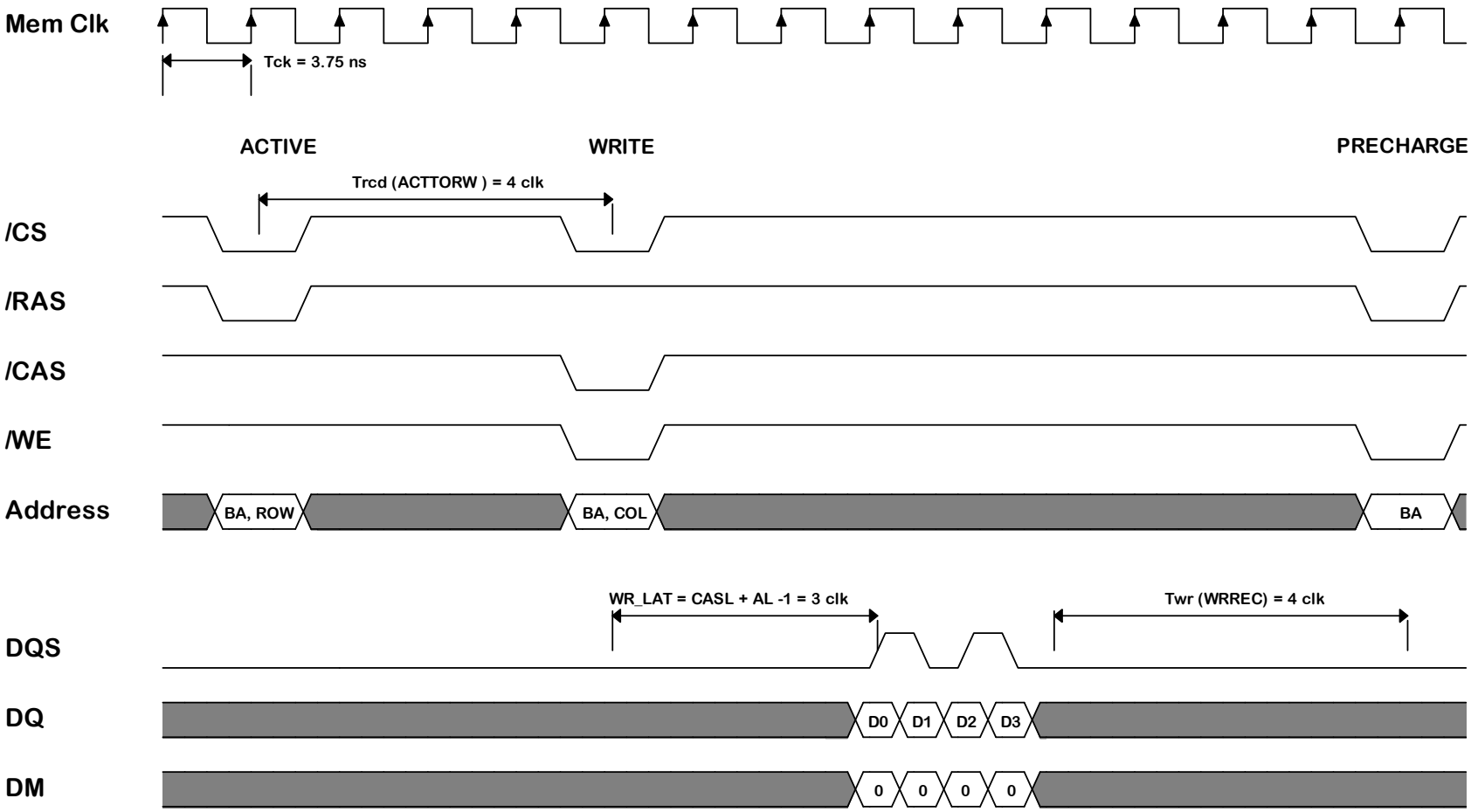
DDR2-533 Write Timing Example



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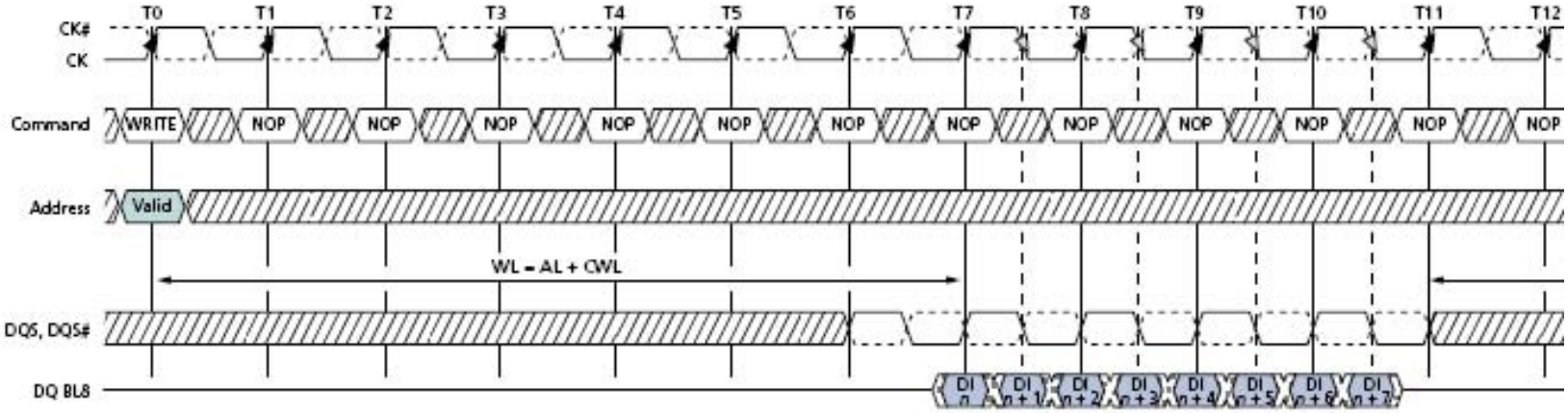
DDR3 Write Timing Example



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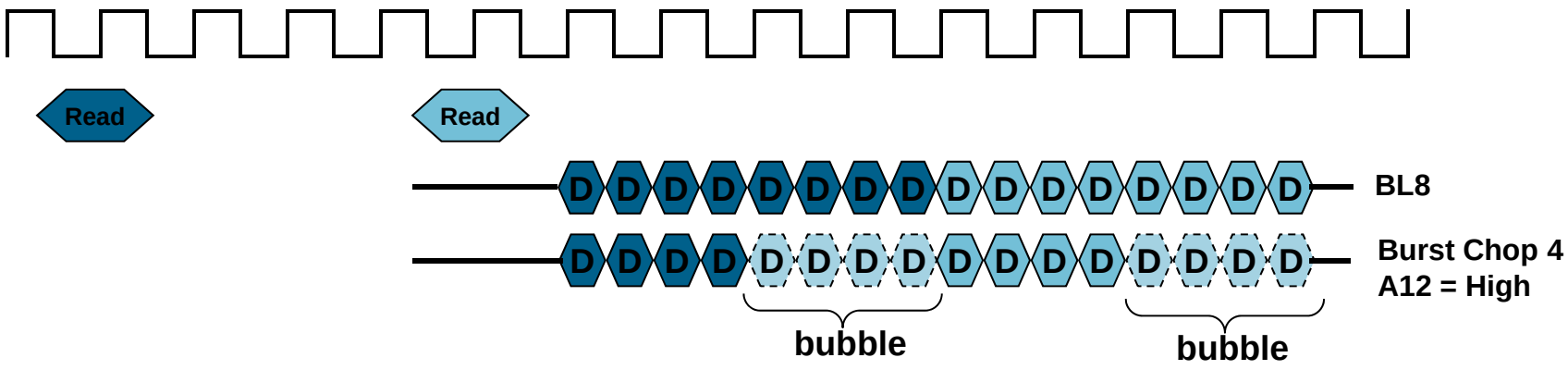
Burst Length

- Burst Length control (BC4/8 on the fly)
  - 8-bit pre-fetch is standard for DDR3 memories
  - Thus, burst length of 8 is default

- DDR3's also support 'pseudo BL4' using burst chip



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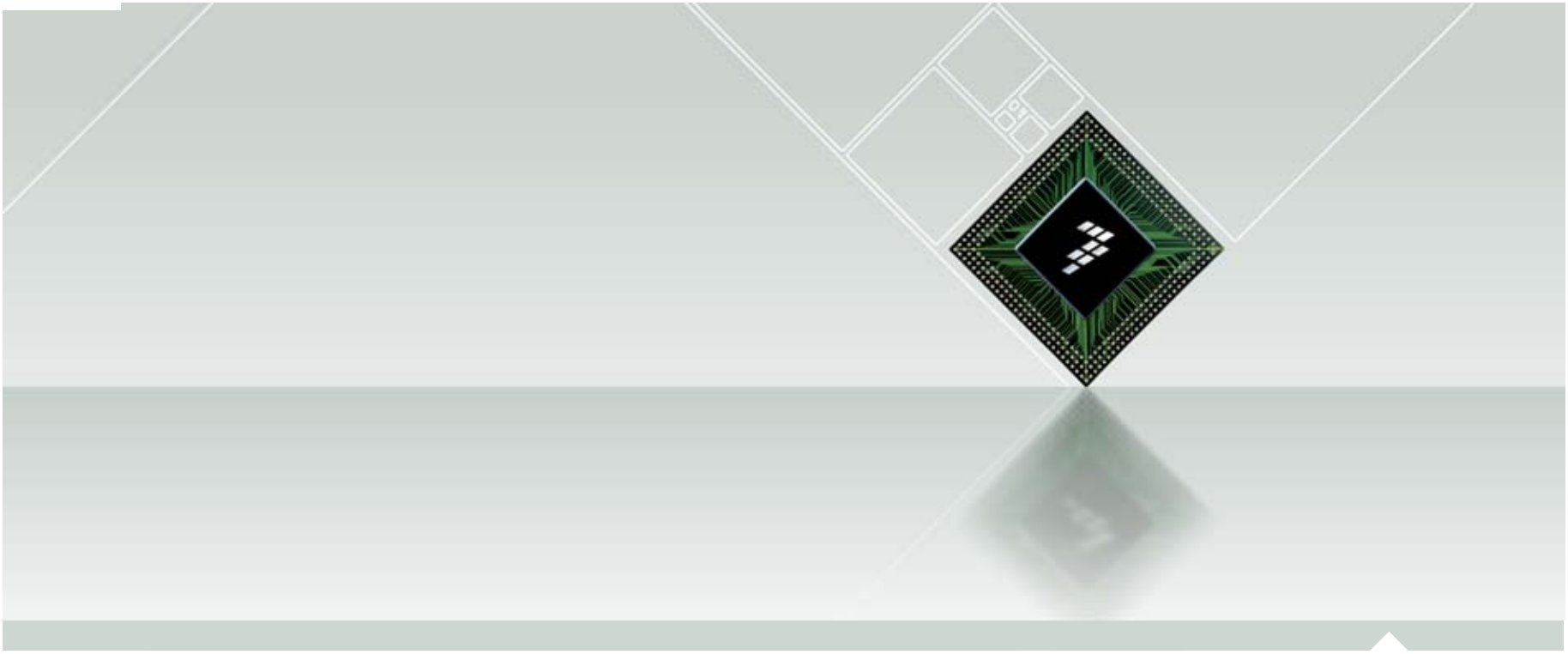
DDR1/DDR2/DDR3 Comparison

Feature	DDR1	DDR2	DDR3
Package	TSOP	BGA only	BGA only
Voltages	2.5V Core, 2.5V I/O	1.8V Core, 1.8V I/O	1.5V Core, 1.5V I/O
Densities	64Mb-1Gb	256Mb-4Gb	256Mb-8Gb
Internal Banks	4	4 or 8	8
Prefetch	2	4	8
Data Rate	266-400 Mbps	400–800 Mbps	800–1600 Mbps
CAS / READ Latency	2, 2.5, 3 Clk	3, 4, 5 + AL Clk	5, 6, 7+ AL Clk
WRITE Latency	1	READ Latency - 1	CAS write Latancy
I/O Signaling	SSTL_2	SSTL_18	SSTL_15
Termination	Parallel termination to V_{TT} for all signals	On-die for data group. V_{TT} termination for address, command, and control	On-die termination for data, address, command, and control
Data Strobes	Single Ended	Single or Differential	Differential



Basic DDR SDRAM Functionality

Electrical Signaling & Termination

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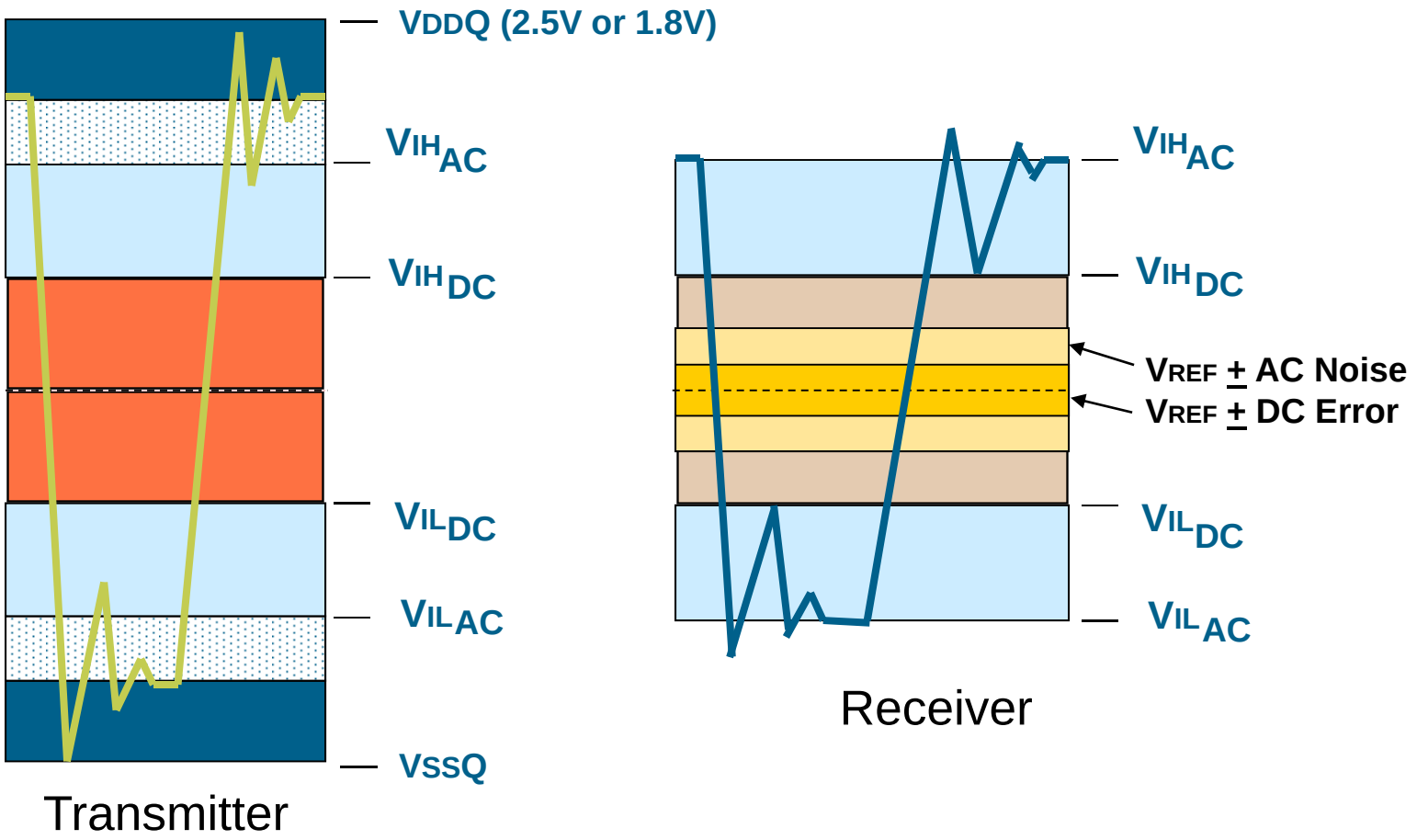
DDR1/DDR2/DDR3 Electrical Signaling Overview

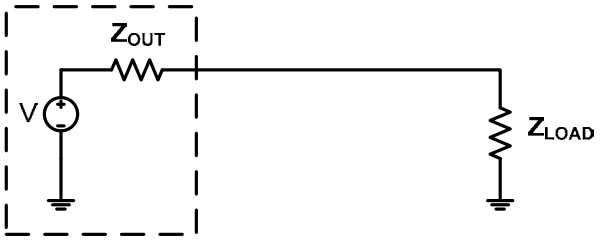
- DDR1/DDR2/DDR3 use SSTL (Stub Series Terminated Logic)
  - Receiver has differential inputs
  - Input signal is compared to a reference voltage, V_{REF}
  - $V_{REF} = V_{DDQ}/2$ and is expected to track V_{DDQ}
  - Termination voltage, $V_{TT} = V_{REF}$ and is expected to track V_{REF}

Parameter	DDR1	DDR2	DDR3
V_{DDQ}	2.5 ± 0.2 V	1.8 ± 0.1 V	1.5 ± 0.075 V
V_{REF}	(0.49 – 0.51) * V_{DDQ}	(0.49 – 0.51) * V_{DDQ}	(0.49 – 0.51) * V_{DDQ}
V_{REF} AC Noise	±2% V_{REF}(dc)	±2% of V_{REF}(dc)	±1% of V_{REF}(dc)
V_{TT}	V_{REF} ± 40 mV	V_{REF} ± 40 mV	V_{REF} ± 40 mV
V_{IH}(ac)	V_{REF} + 310 mV	V_{REF} + 250 mV	V_{REF} + 175 mV
V_{IL}(ac)	V_{REF} - 310 mV	V_{REF} – 250 mV	V_{REF} – 175 mV
V_{IH}(dc)	V_{REF} + 150 mV	V_{REF} + 125 mV	V_{REF} + 100 mV
V_{IL}(dc)	V_{REF} - 150 mV	V_{REF} - 125 mV	V_{REF} - 100 mV

DDR1/DDR2/DDR3 SSTL Signaling



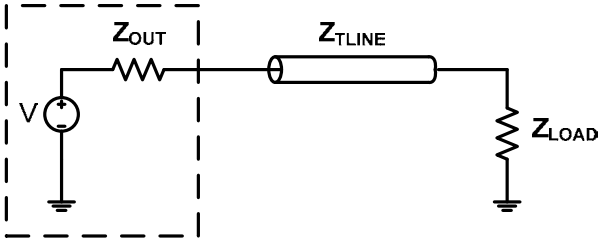
Impedance Matching



Usually want Z_O as low as possible and Z_L as high as possible, but:

% reflection = $(Z_L - Z_O) / (Z_L + Z_O) * 100\%$

so impedances need to be matched



For high frequencies and/or fast rise times, all connections have to be treated as transmission lines and impedances need to be matched at multiple interfaces

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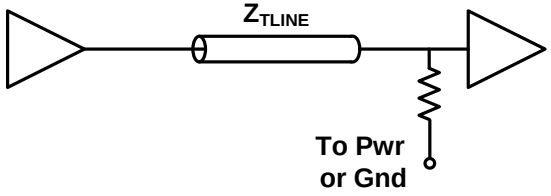
Termination Options

At the Source:

Series

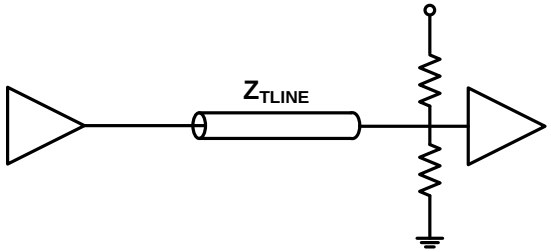
$R + Z_{OUT} = Z_{TLINE}$

At the Destination:



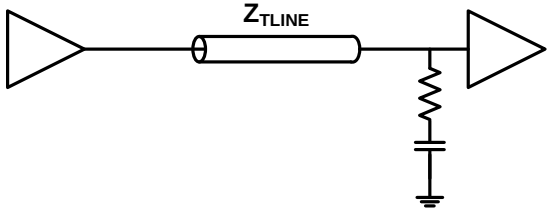
Parallel

$R = Z_{TLINE}$



Thevenin

$R = 2 * Z_{TLINE}$

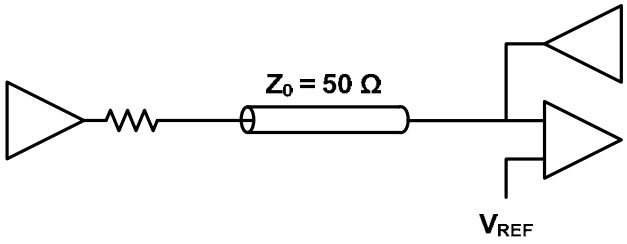


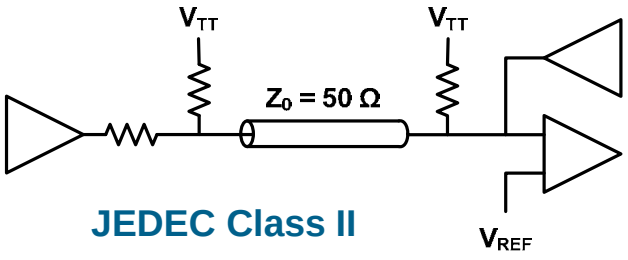
RC

$R = Z_{TLINE}$

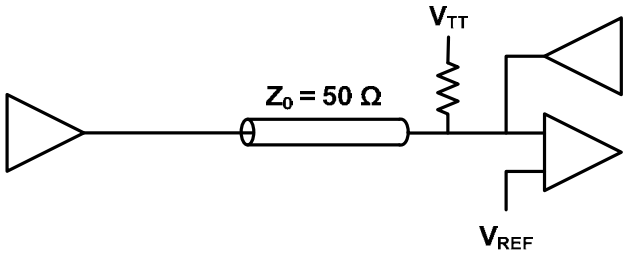
$C = 20\text{-}600\ pF$

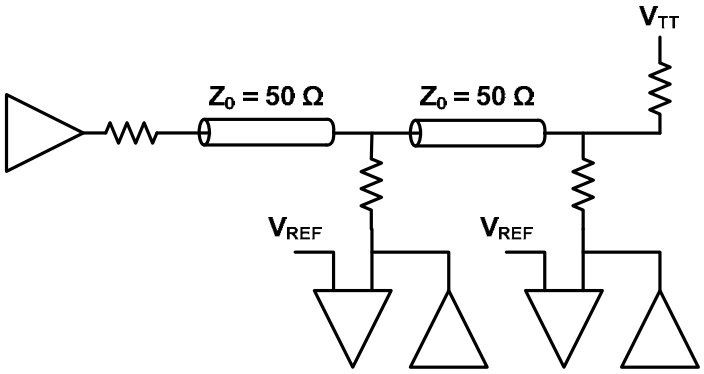
Termination Options Discussed in SSTL Specs

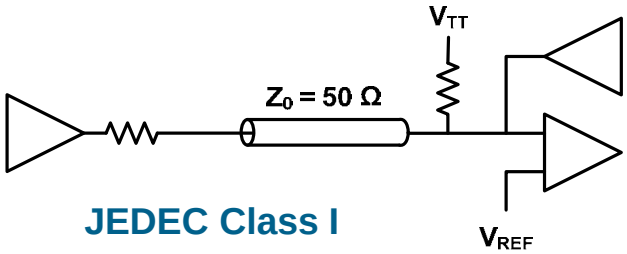




JEDEC Class II







JEDEC Class I

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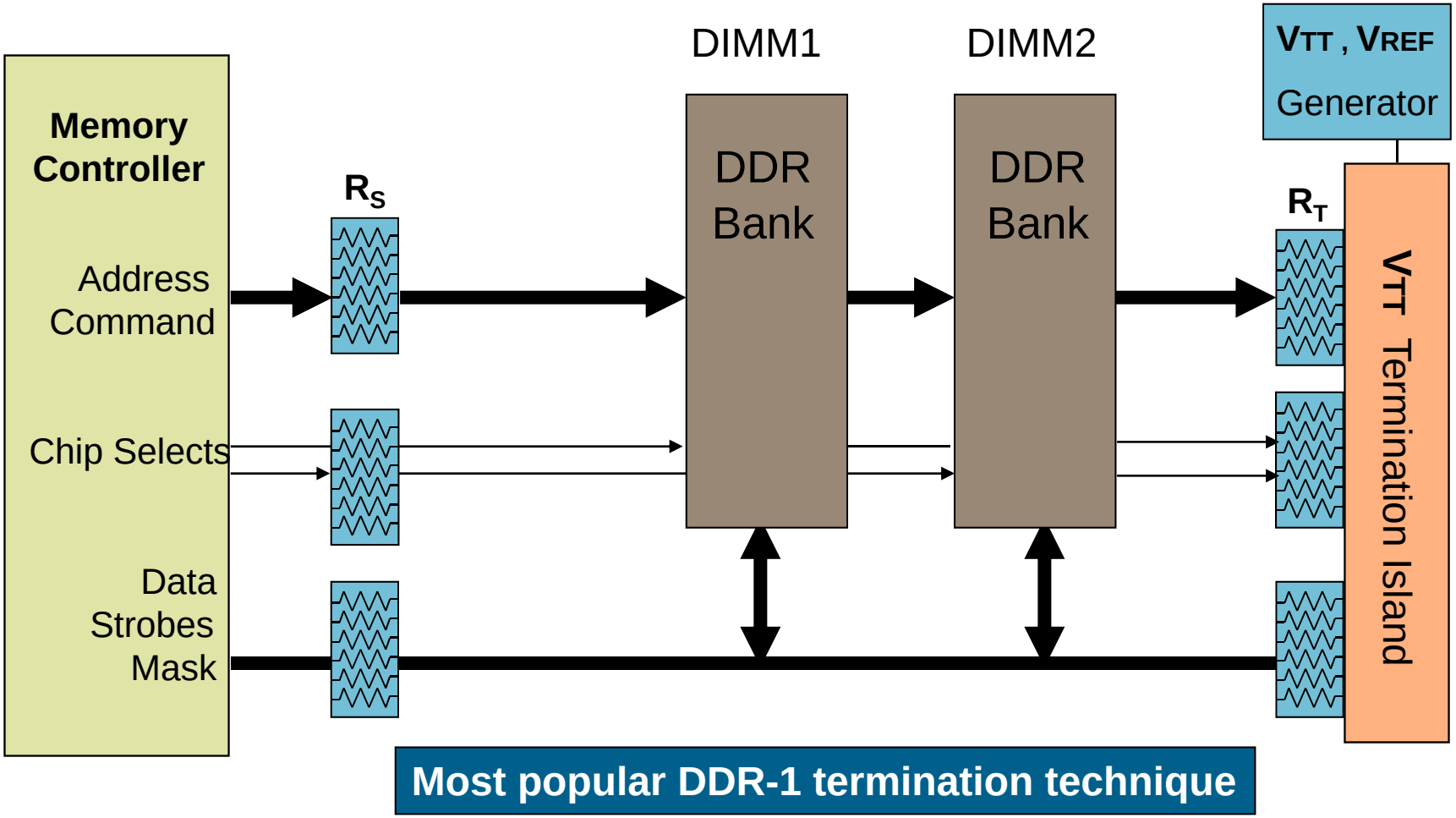
DDR1 Termination



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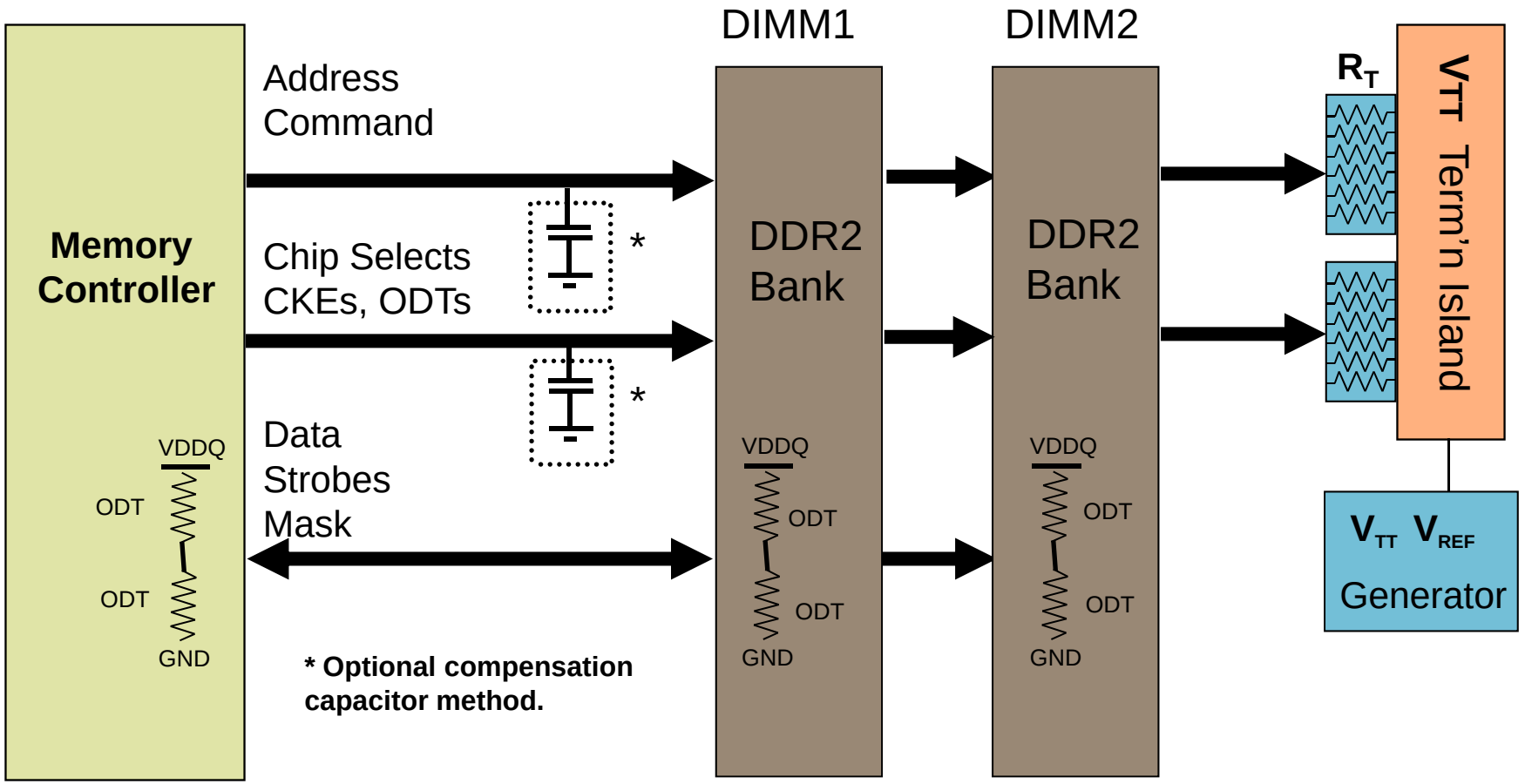
DDR2 Termination



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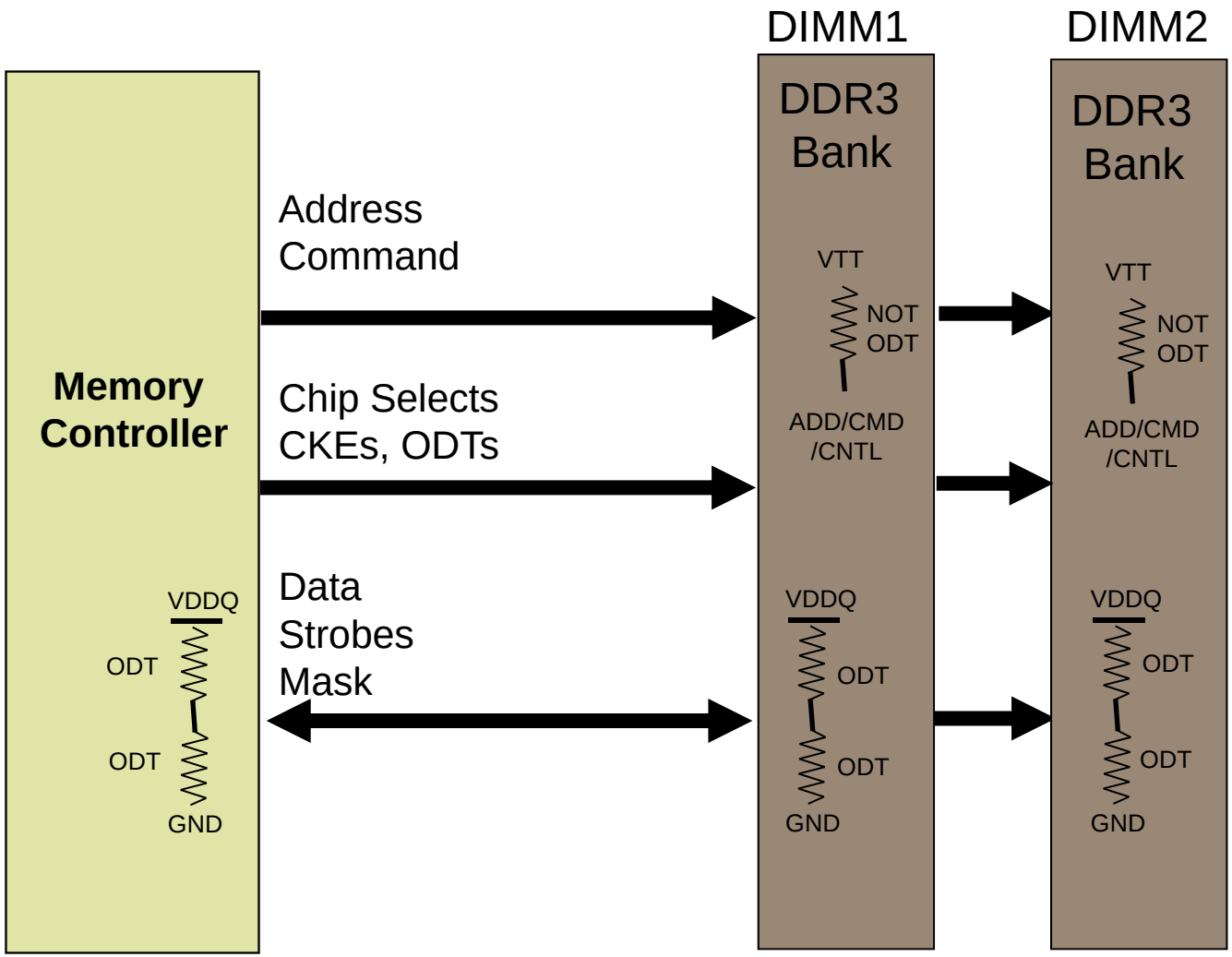
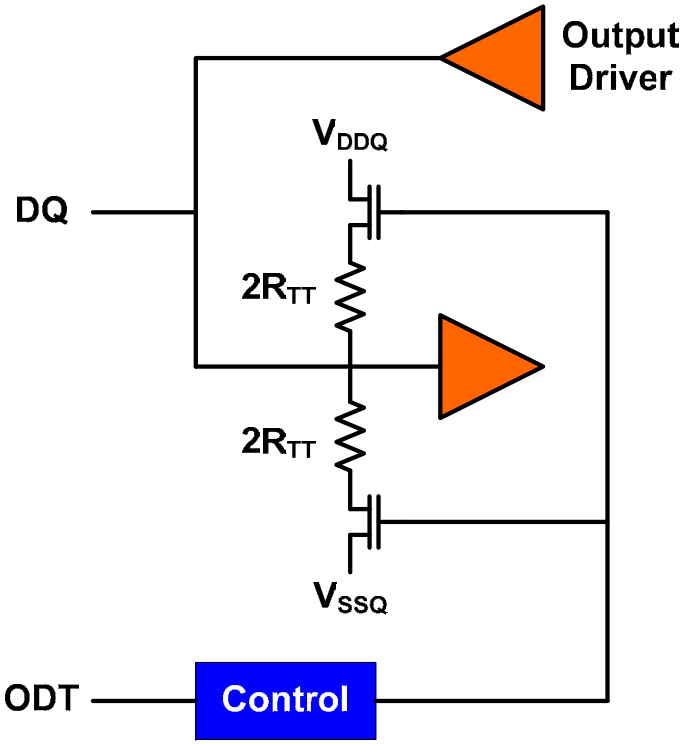
DDR3 Termination



On-Die Termination (ODT)

- Termination can be turned on and off as needed
- One ODT pin per SDRAM device
- One ODT pin per rank for DIMMs
  - Most applications use one per slot (Micron, Samsung)
- R_{TT} for the SDRAM devices is set in the Extended Mode Register (150, 75 or 50 Ω for DDR2)

  (120, 60 or 43 Ω for DDR3)



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ODT Settings – Micron Design Guide

- Dependent upon board topology
- One ODT pin per module
- Guidelines can be provided, but:
  - **Simulate**
  - **Verify using a scope**

- Recommendations for DDR2-533 two-DIMM systems:

	Controller	Near Slot Populated	Far Slot Populated	Near Slot, Both Populated	Far Slot, Both Populated
Write to near module	OFF	150 Ohms		OFF	75 Ohms
Write to far module	OFF		150 Ohms	75 Ohms	OFF
Read from near module	75 Ohms	OFF			
Read from far module	75 Ohms		OFF		
Read from near module	150 Ohms			OFF	75 Ohms
Read from far module	150 Ohms			75 Ohms	OFF

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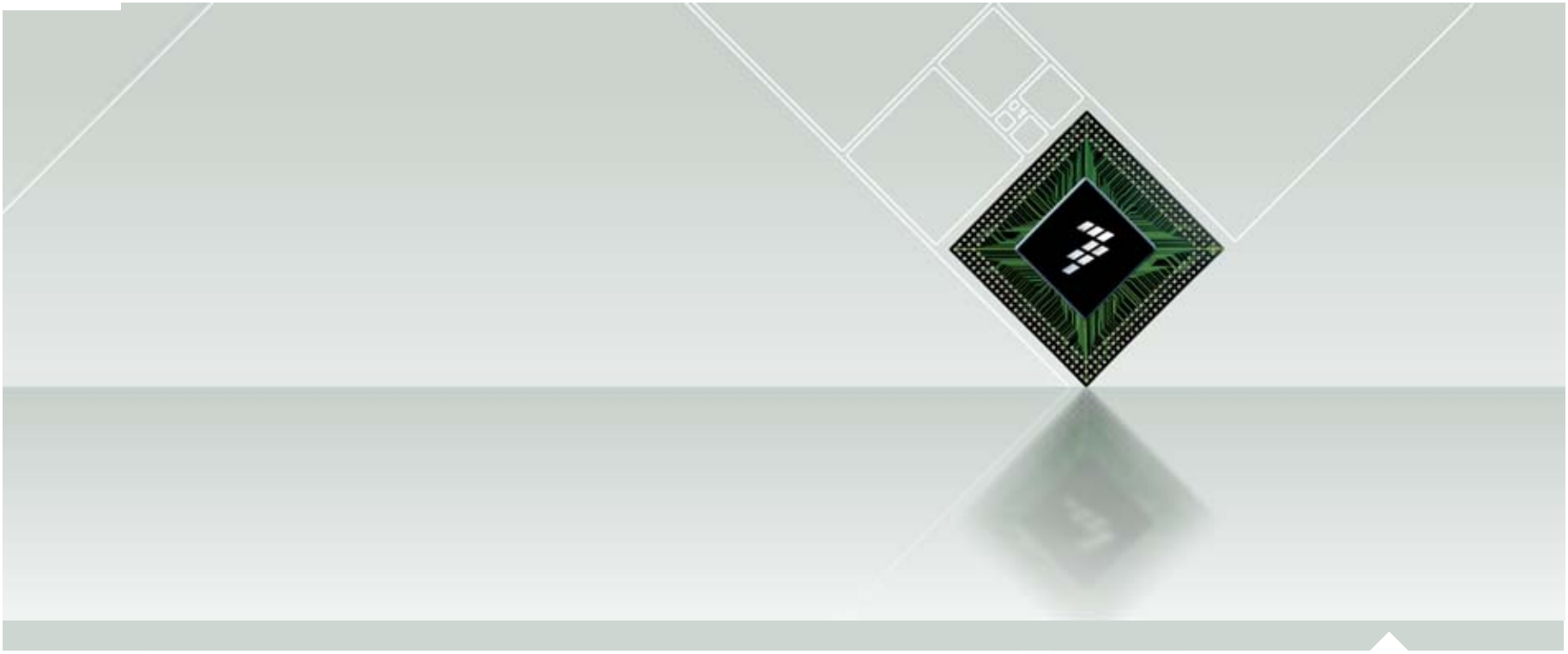

PowerQUICC DDR Controllers

Features & Capabilities

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DDR1/DDR2/DDR3 Controller Features & Capabilities

- Supports most JEDEC standard x8, x16, x32 DDR1 & 2 & 3 devices
- Memory device densities from 64Mb – through 4Gb
- Data rates up to: 333 Mb/s for DDR1, 800 Mb/s for DDR2 and DDR3
- Devices with 12-16 row address bits, 8-11 column address bits, 2-3 logical bank address bits
- Data mask signals for sub-doubleword writes
- Up to four physical banks (chip selects)
- Physical bank sizes up to 4GB, total memory up to 16GB per controller
- Physical bank interleaving between 2 or 4 chip selects
- Memory controller interleaving when more than 2 controllers are available
- Unbuffered or registered DIMMs

DDR1/DDR2/DDR3 Controller Features & Capabilities (cont.)

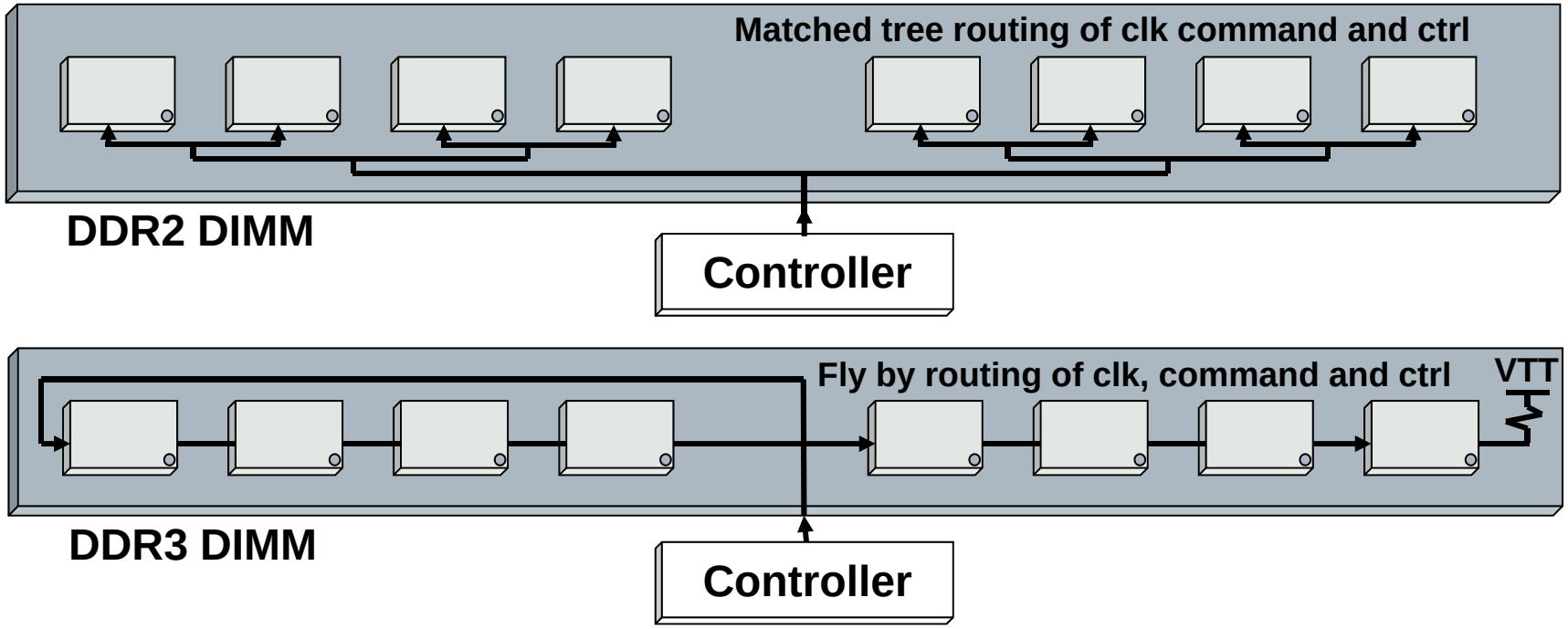
- Up to 32 open pages
  - Open row table
  - Amount of time rows stay open is programmable
- Auto-precharge, globally or by chip select
- Self-refresh
- Up to 8 posted refreshes
- Automatic or software controlled memory device initialization
- ECC: 1-bit error correction, 2-bit error detection, detection of all errors within a nibble
- ECC error injection
- Read-modify-write for sub-doubleword writes when using ECC
- Automatic data initialization for ECC
- Dynamic power management

DDR2/DDR3 Controller additional Features & Capabilities

- Partial array self refresh
- Address & command parity for Registered DIMM
- Independent driver impedance setting for data, address/command, and clock
- Mirrored DIMM supported
- Automatic CPO (operational)
- Write-leveling for DDR3
- Automatic ZQ calibration for DDR3
- Fixed or On-the-fly Burst chop mode for DDR3
- Asynchronous RESET for DDR3
- Synchronous & Asynchronous clock-in option

Fly By Routing Topology

- Introduction of “Fly-by” architecture
  - Address, command, control & clocks
  - Improved signal integrity…enabling higher speeds
  - On module termination



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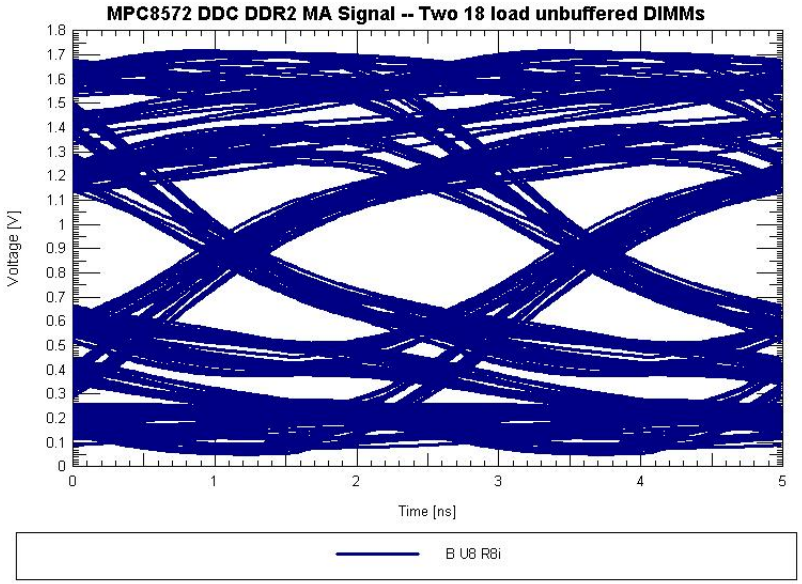
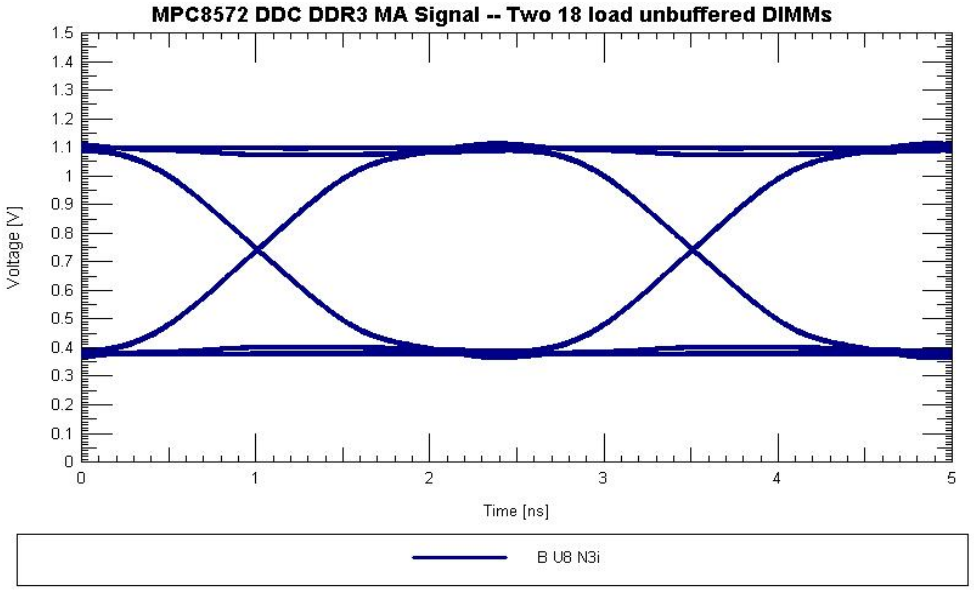
Fly By Routing Improved SI

DDR2 Matched tree routing



DDR3 Fly by routing



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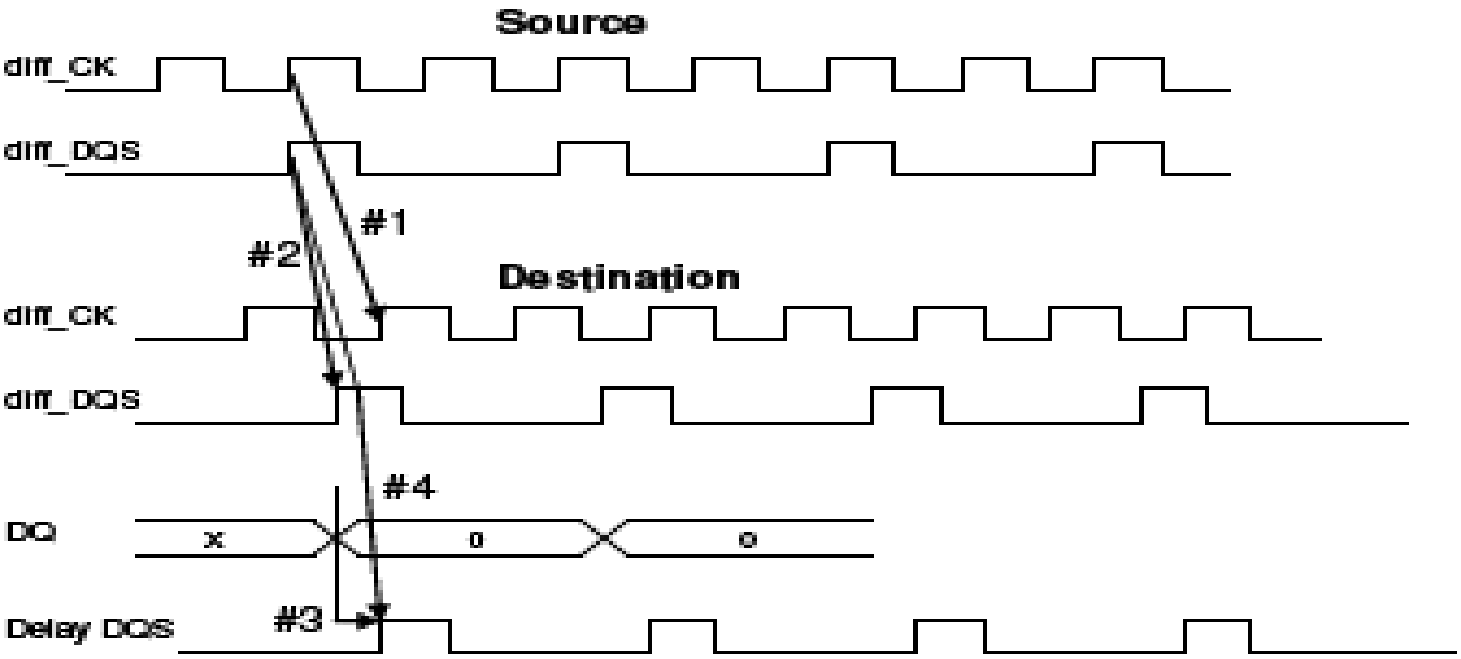
What is write leveling

During a write cycle, the skew between the clock and strobes are increased due to the fly-by topology. The write leveling will delay the strobe (and the corresponding data lanes) for each byte lane to reduce/compensate for this delay.



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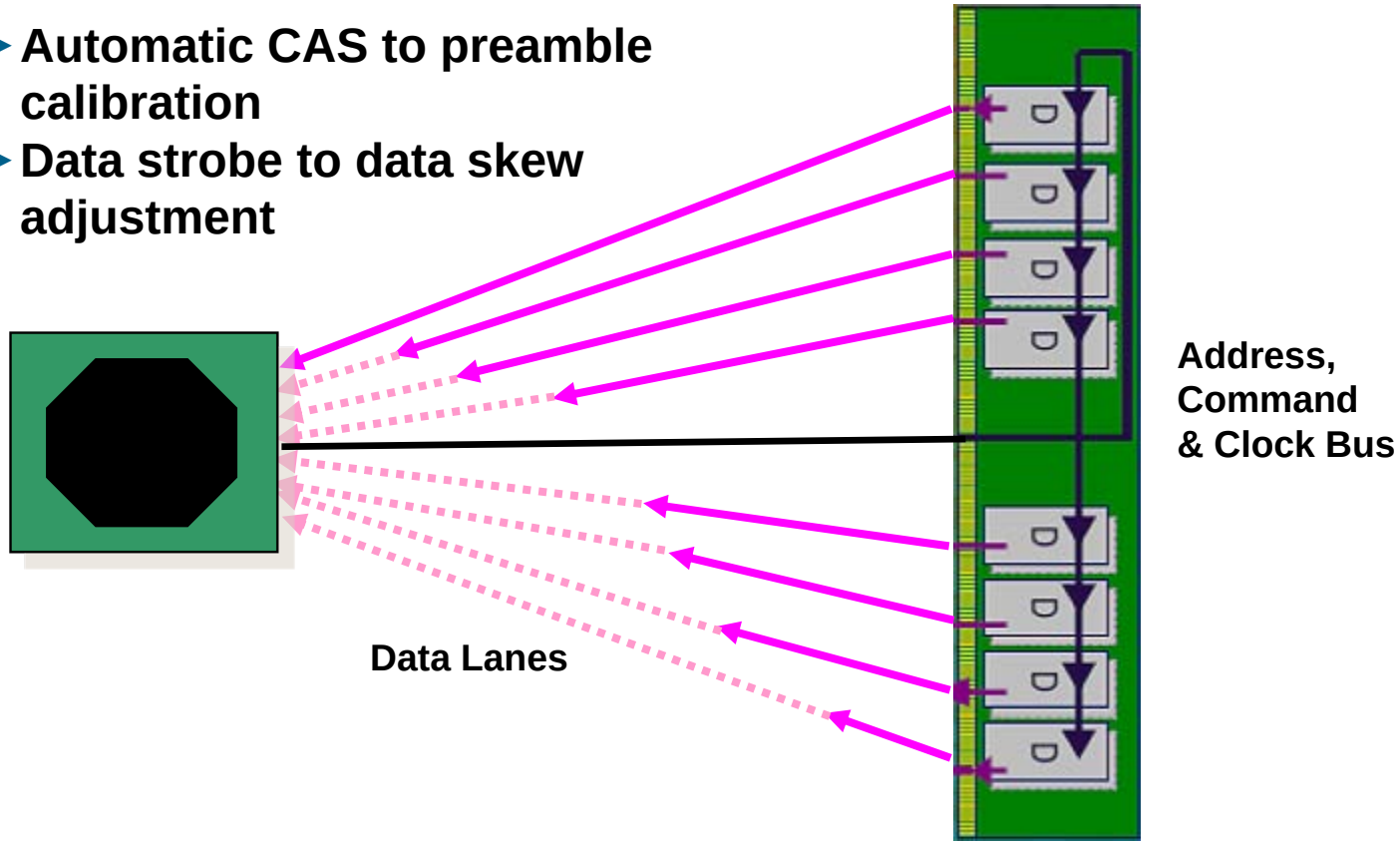
Read Adjustment

- Automatic CAS to preamble calibration
- Data strobe to data skew adjustment



Instead of JEDEC's MPR method, Freescale controllers use a proprietary method of read adjust method. Auto CPO will provide the expected arrival time of preamble for each strobe line of each byte lane during the read cycle to adjust for the delays cased by the fly-by topology.

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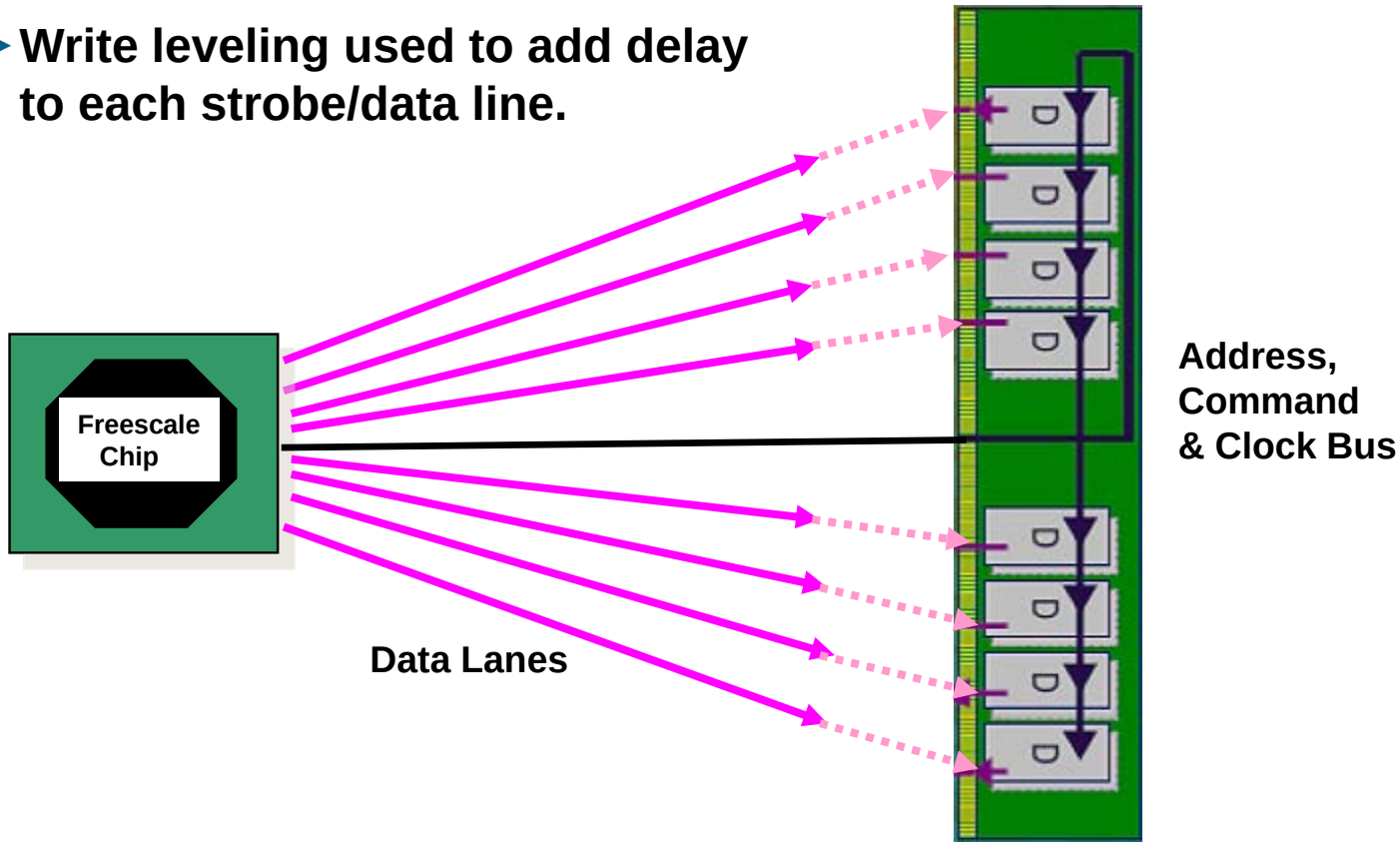
Write Adjustment

- **Write leveling used to add delay to each strobe/data line.**



Write leveling sequence during the initialization process will determine the appropriate delays to each strobe/data byte lane and add this delay for every write cycle.

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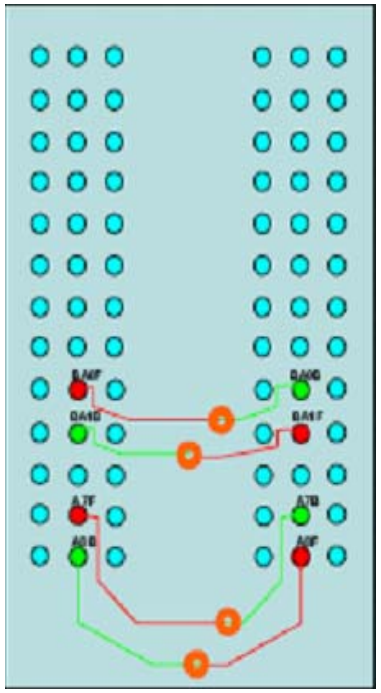
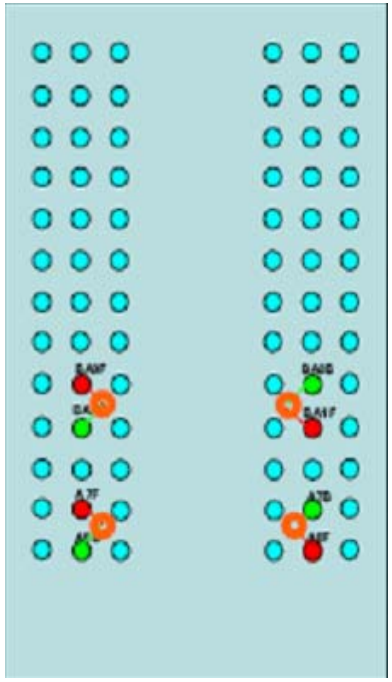
DIMM Mirroring…

- The DDR3 IP fully supports address mirroring

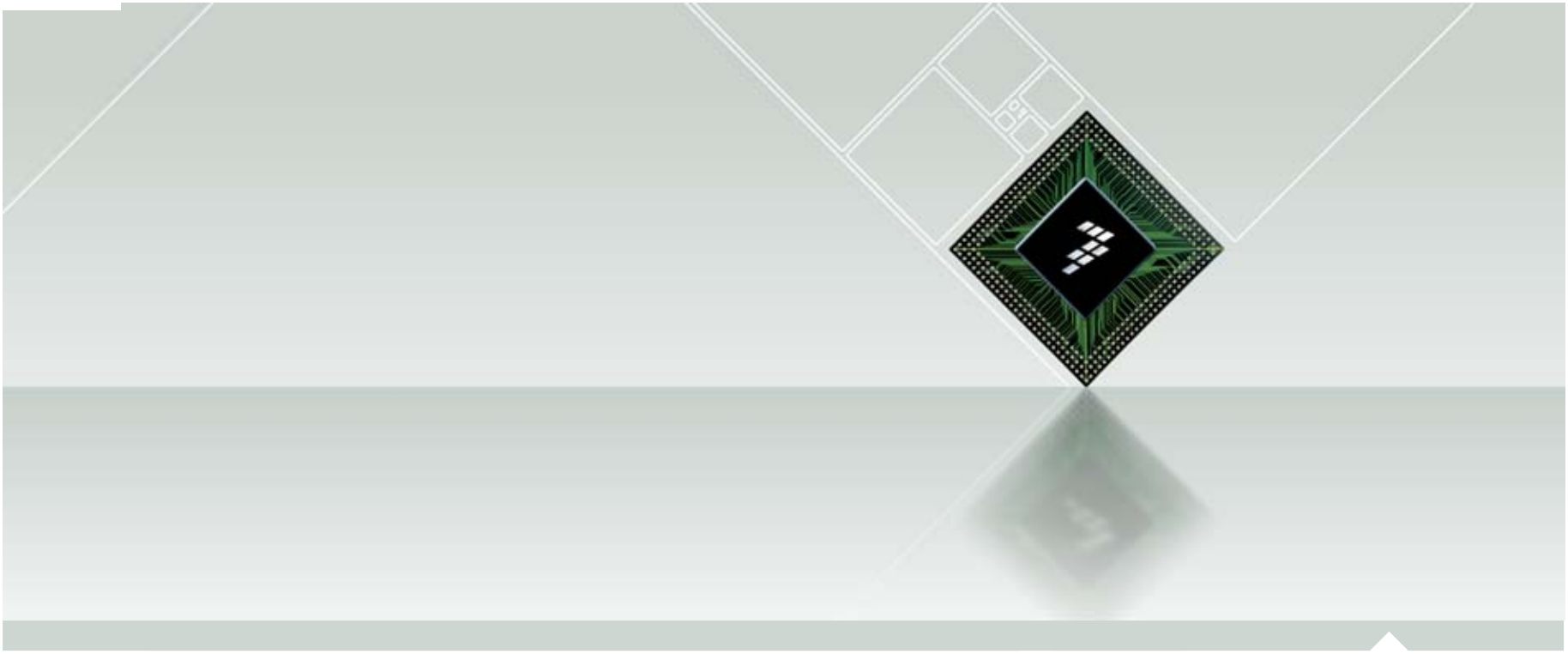


Non-Mirrored



Mirrored

Edge Connector Signal	SDRAM Pin, Standard	SDRAM Pin, Mirrored
A0	A0	A0
A1	A1	A1
A2	A2	A2
A3	A3	A4
A4	A4	A3
A5	A5	A6
A6	A6	A5
A7	A7	A8
A8	A8	A7
A9	A9	A9
…	…	…
A15	A15	A15
BA0	BA0	BA1
BA1	BA1	BA0
BA2	BA2	BA2



PowerQUICC DDR Controllers

Initialization and Register Configurations

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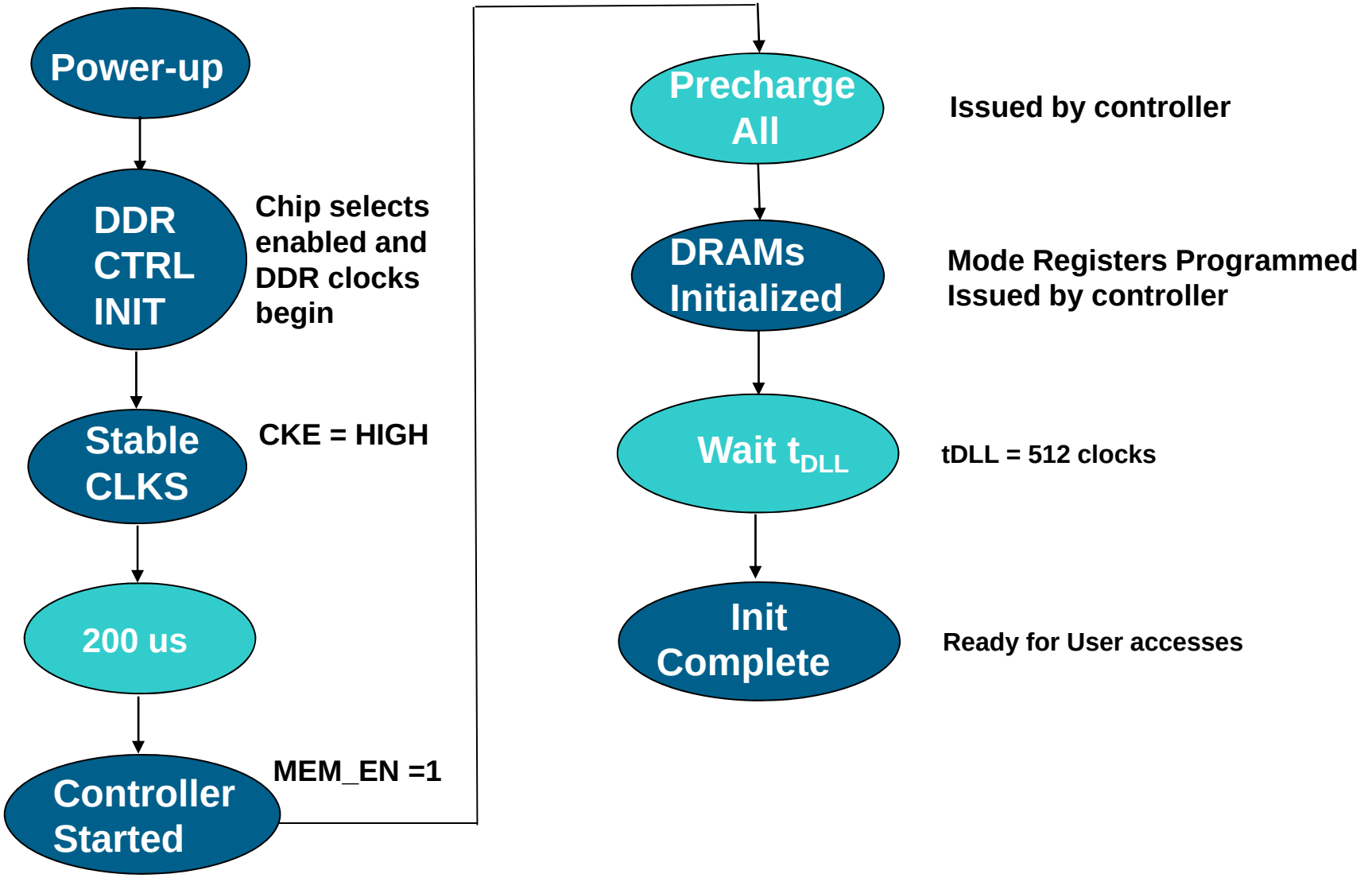
DDR2 Initialization Flow



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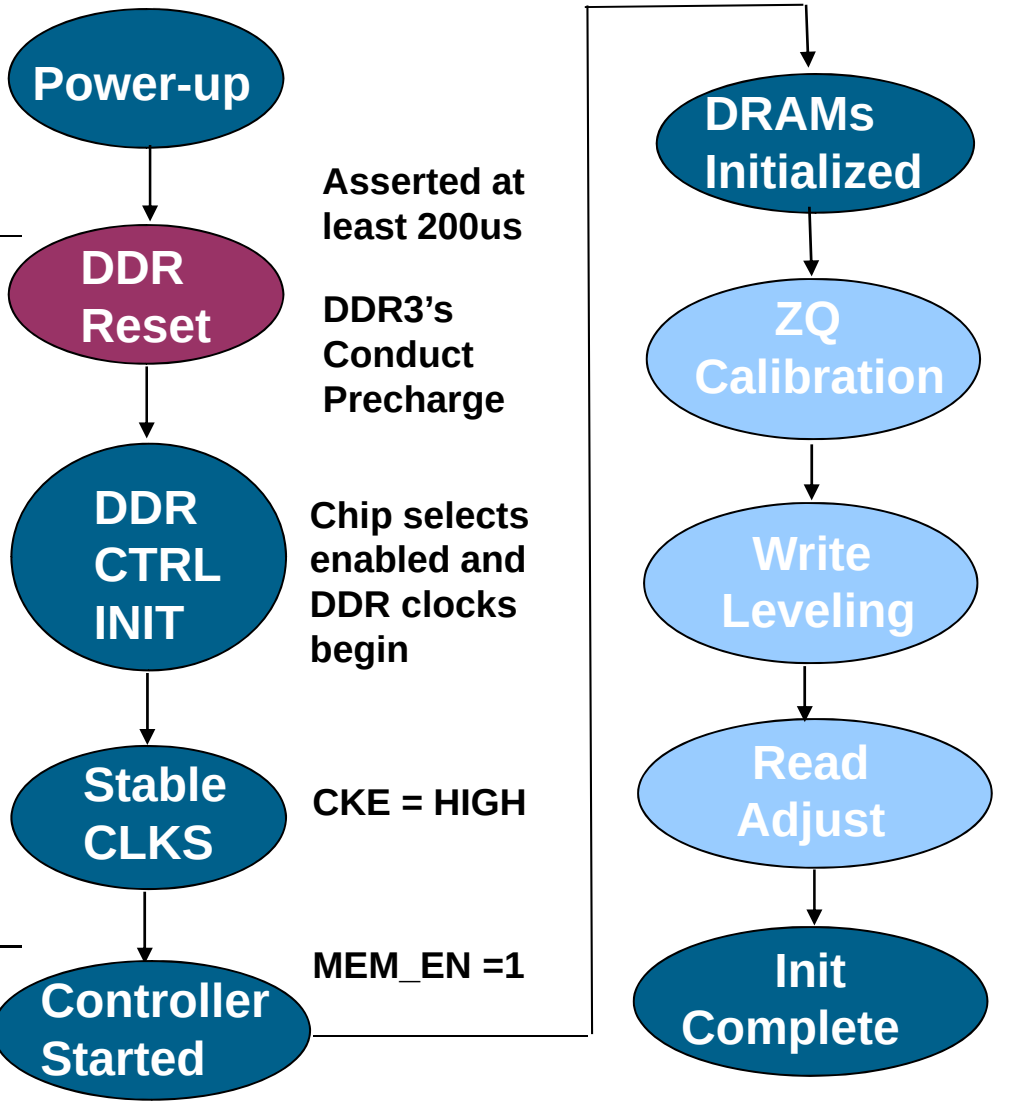
DDR3 Initialization Flow



Need at least 500us from reset deassertion to the controller being enabled.

Timed loop may be needed.

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Register configuration

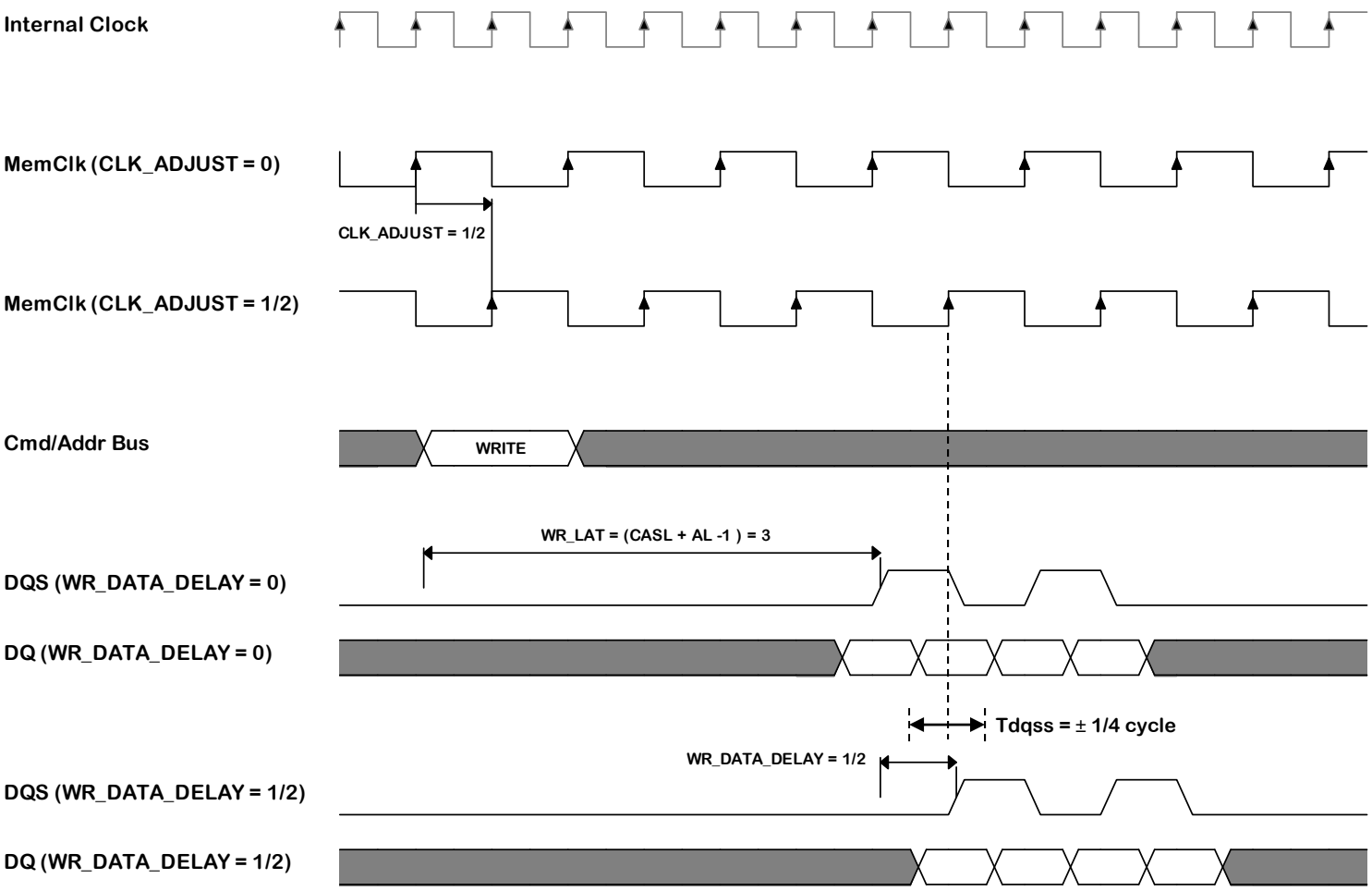
Two general type of registers to be configured in the memory controller

- First register type are set to the DRAM related parameter values, that are provided via SPD or DRAM datasheet
- Second register type are the Non-SPD values that are set based on customer's application. For example:
  - On-die-termination (ODT) settings for DRAM and controller
  - driver impedance setting for DRAM and controller
  - Clock adjust, write data delay, Cast to preamble override (CPO)
  - 2T or 3T timing,
  - Burst type selection (fixed or on-fly burst chop mode)
  - Write-leveling start value (WRLVL_START)

What Can We Adjust to Optimize the Timing?

- CLK_ADJUST
- WR_DATA_DELAY
- CPO
- 2T_EN, 3T_EN
- WRLVL_EN
- Burst chop mode

CLK_ADJUST & WR_DATA_DELAY



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Pitfalls / Debug Tips - Clock Adjust

- Addr/Cmd are always launched from the same location, memory clock is shifted with DDR_SDRAM_CLK_CNTL[CLK_ADJUST]
  - Used to meet setup/hold for Addr/Cmd
- Use a scope to verify that clock is centered inside of the Addr/Cmd valid eye.
  - Look at heavily loaded signal (/RAS, /CAS, /WE, Addr, BA)
  - Look at lightly loaded signal (/CS, ODT, CKE)

Bits	Name	Description
0–4	—	Reserved
5–8	CLK_ADJUST	Clock adjust 0000 Clock will be launched aligned with address/command 0001 Clock will be launched 1/8 applied cycle after address/command 0010 Clock will be launched 1/4 applied cycle after address/command 0011 Clock will be launched 3/8 applied cycle after address/command 0100 Clock will be launched 1/2 applied cycle after address/command 0101 Clock will be launched 5/8 applied cycle after address/command 0110 Clock will be launched 3/4 applied cycle after address/command 0111 Clock will be launched 7/8 applied cycle after address/command 1000 Clock will be launched 1 applied cycle after address/command 1001–1111Reserved
9–31	—	Reserved

Pitfalls / Debug Tips – Write Data Delay

- Controlled via TIMING_CFG_2[WR_DATA_DELAY]
- Used to meet t_{DQSS} timing requirements
  - In addition to compensating for CLK_ADJUST setting
- Verify using a scope
  - Must be measured after DDR_SDRAM_CLK_CNTL[CLK_ADJUST] has been optimized
- WR_DATA_DELAY field is ignored by memory controller when DDR3 is used and write-levelling is enabled.

19–21	WR_DATA_DELAY	Write command to write data strobe timing adjustment. Controls the amount of delay applied to the data and data strobes for writes. See Section 9.5.9, "DDR SDRAM Write Timing Adjustments," for details.	
		000 0 clock delay	100 1 clock delay
		001 1/4 clock delay	101 5/4 clock delay
		010 1/2 clock delay	110 3/2 clock delay
		011 3/4 clock delay	111 Reserved

Pitfalls / Debug Tips - CAS to Preamble

- Set via TIMING_CFG_2[CPO]
- Use application note AN2583 section 4.2 to calculate
- Must be calculated after DDR_SDRAM_CLK_CNTL[CLK_ADJUST] has been optimized
- Use the center value if more than one valid CPO available
- DDR3 should select Automatic CPO calibration

Bits	Name	Description
4–8	CPO[1]	$\overline{\text{MCAS}}$-to-preamble override. Defines the number of DRAM cycles between when a read is issued and when the corresponding DQS preamble is valid for the memory controller. For these decodings, "READ_LAT" is equal to the CAS latency plus the additive latency. 00000 READ_LAT + 1 00001 Reserved 00010 READ_LAT 00011 READ_LAT + 1/4 00100 READ_LAT + 1/2 00101 READ_LAT + 3/4 00110 READ_LAT + 1 00111 READ_LAT + 5/4 01000 READ_LAT + 3/2 01001 READ_LAT + 7/4 01010 READ_LAT + 2 01011 READ_LAT + 9/4 01100 READ_LAT + 5/2 01101 READ_LAT + 11/4 01110 READ_LAT + 3 01111 READ_LAT + 13/4 10000 READ_LAT + 7/2 10001 READ_LAT + 15/4 10010 READ_LAT + 4 10011 READ_LAT + 17/4 10100 READ_LAT + 9/2 10101 READ_LAT + 19/4 10110–11110 Reserved 11111 Automatic calibration (recommended)

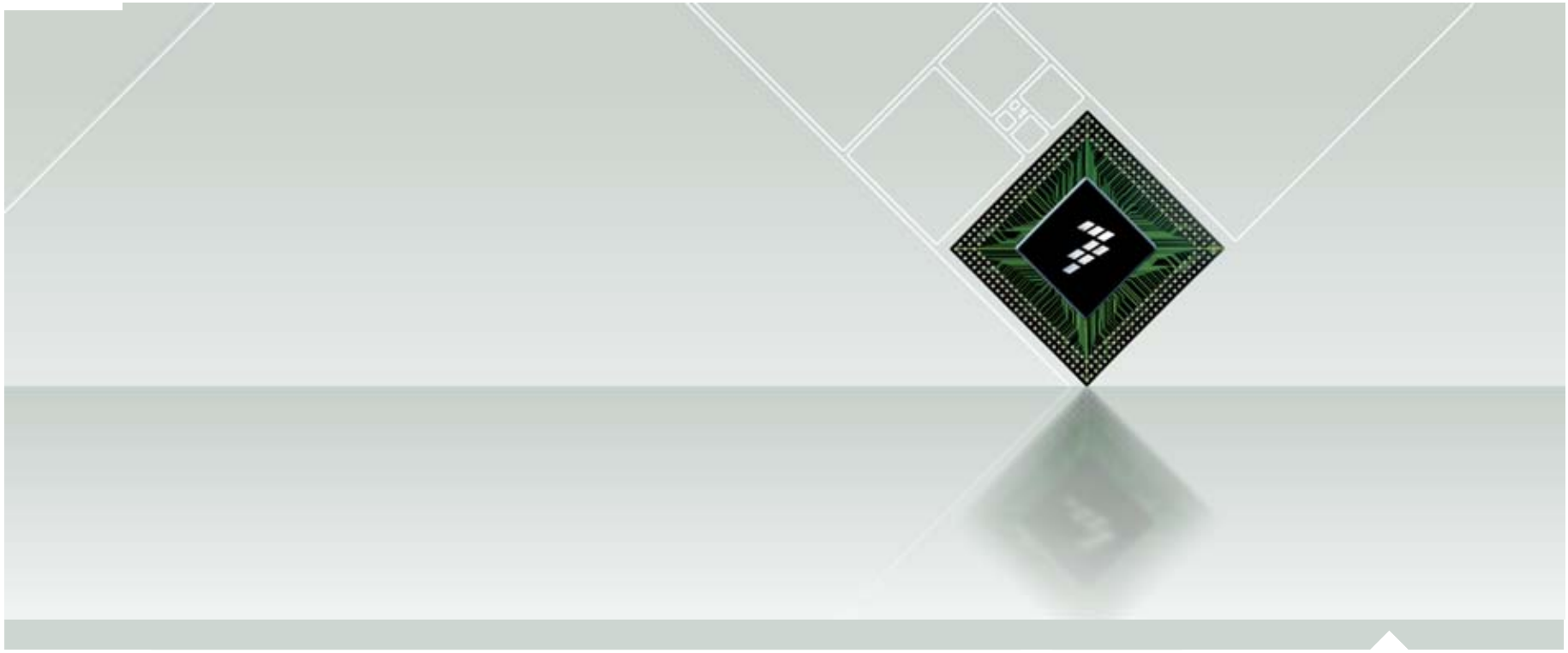
2T/3T Timing

- Puts Addr/Cmd signals on the bus for 2 or 3 clock cycles instead of 1
- Does not affect Control signals

- When to use?
  - Two dual-rank unbuffered DIMMs
  - 36 loads on Addr/Cmd lines

- Typically not required for:
  - One dual-rank unbuffered DIMM
  - 18 loads on Addr/Cmd lines

- When not to use?
  - Registered DIMMs



PowerQUICC DDR Controllers

Pitfalls / Debug Tips

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Pitfalls / Debug Tips - DDR Type POR Configuration

Table 4-16. DDR DRAM Type

Functional Signal	Reset Configuration Name	Value (Binary)	Meaning
LGPL0, LGPL1 Default (11)	cfg_dram_type[0:1]	00	Reserved
		01	DDR1 2.5V, CKE low at reset
		10	Reserved
		11	DDR2 1.8V, CKE low at reset (default)

Table 4-20. DDR DRAM Type

Functional Signal	Reset Configuration Name	Value (Binary)	Meaning
LGPL0/LFCLE Default (1)	cfg_dram_type	0	DDR3 1.5 V, CKE low at reset
		1	DDR2 1.8 V, CKE low at reset (default)

Pitfalls / Debug Tips - ECC and DDR Error Registers

- ECC should be enabled if possible
  - DDR_SDRAM_CFG[ECC_EN] enables ECC
  - DDR_SDRAM_CFG_2[D_INIT] initializes data and ECC in DRAM
  - If ECC cannot be enabled, it may be more difficult to detect DDR generated errors

- ERR_DETECT register should be checked for DDR errors
  - ACE – Automatic calibration error
  - MBE – Multi-bit ECC error
  - SBE – Single-bit ECC error
  - MSE – Memory select error

Pitfalls / Debug Tips - CAS Latency / Write Latency / Additive Latency

- Program write latency based on DRAM type
  - DDR1 -> Write latency = 1 DRAM cycle
  - DDR2 -> Write latency = (Read latency – 1) DRAM cycles
  - DDR3 -> Write latency = CWL
- Programming CAS latency too high can degrade performance
  - Check DRAM datasheet based on frequency used and specific DRAM device
- When ODT is used, other rules must be followed to allow ODT to assert early enough
  - DDR2: Write latency + additive latency >= 3 cycles
  - DDR3: set as required per specified DDR3 datasheet value.

Pitfalls / Debug Tips - DDR Mode Registers

- Values programmed into DDR mode registers must match DDR controller configuration registers
  - CAS latency
  - Burst length
  - Write recovery
    - Not a straight decode in Mode Register
  - Active powerdown exit time
  - Additive latency
  - Differential DQS enable

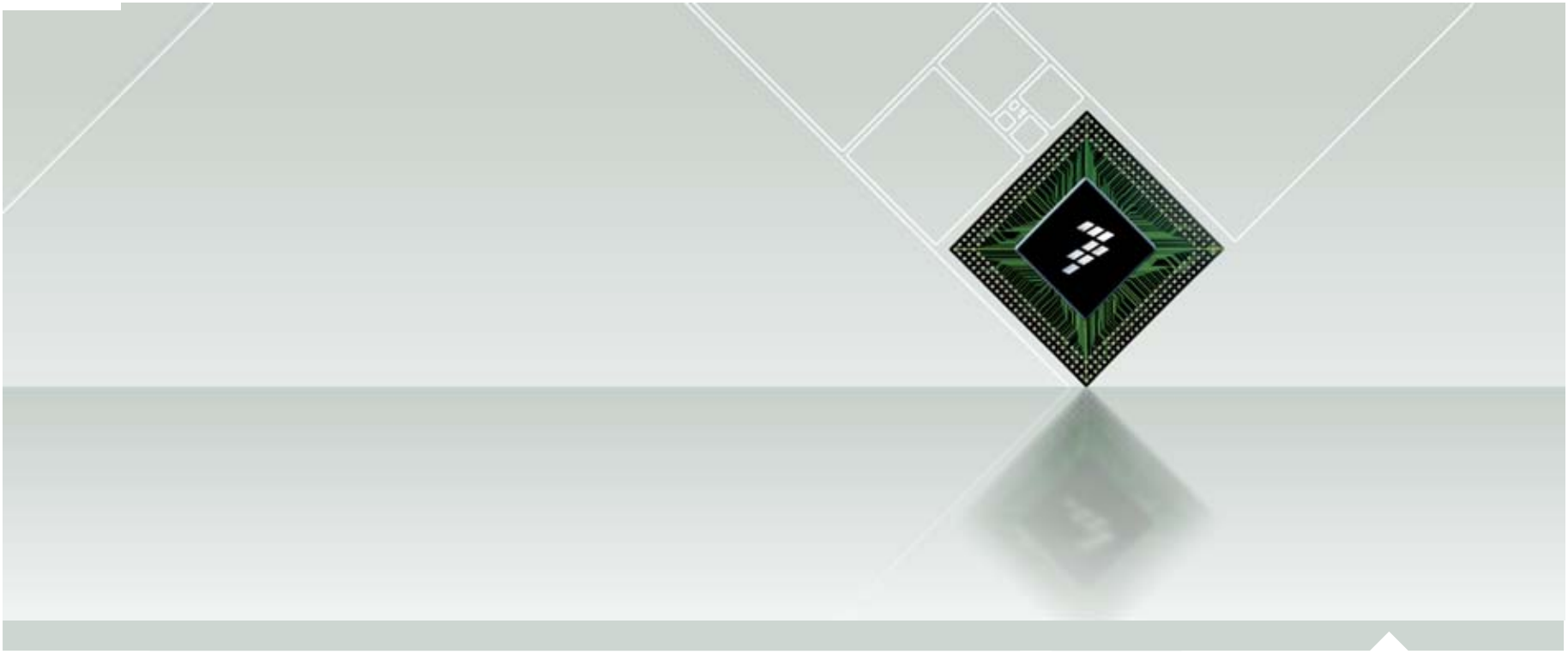
- DLL reset and ODC calibration fields are controlled automatically by the DDR controller

*Pitfalls / Debug Tips - Programming t_{wtr}, t_{rrd}, and t_{rtp}

- Use caution when calculating:
  - TIMING_CFG_1[WRTORD] (t_{wtr})
  - TIMING_CFG_1[ACTTOACT] (t_{rrd})
  - TIMING_CFG_2[RD_TO_PRE] (t_{rtp})
  - DDR2: Minimum value for each parameter is 2 DRAM clocks
  - DDR3: Minimum value for each parameter is 4 DRAM clocks

Pitfalls / Debug Tips - 200 us Delay

- 200 µs for DDR2 and 512 us for DDR3 must pass between stable clocks and CKE assertion
- Clocks are stable after DDR_SDRAM_CLK_CNTL[CLK_ADJUST] is programmed and any chip select has been enabled via CSn_CONFIG[CS_n_EN]
- CKE is asserted after DDR_SDRAM_CFG[MEM_EN] is set
- Software must provide delay between these 2 steps



Board design

Pitfalls / Debug Tips

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Board Design Pitfalls Summary

- Pitfall 1 Noisy Vref: Care must be taken to isolate Vref
- Pitfall 2 Weak Vref: Insure adequate current for Vref
- Pitfall 3 Ref Plane: Insure excellent reference plane for all DDR signals
- Pitfall 4 Data Tuning: Data bits within 10 mil, Byte lanes within 0.5”
- Pitfall 5 Proper Termination: Discrete implementations require term.
- Pitfall 6 POR Config: Insure correct DDR (2/3) is set for controller
- Pitfall 7 Expandability: Hook up unused address lines
- Pitfall 8 Incorrect Topology: Insure use of JEDEC routing topologies
- Pitfall 9 Separate VDDQ/VDDIO : VDDQ and VDDIO are common on DDR DIMM Modules, not on controller.

Design Pitfalls Summary (Continued)

- Pitfall 10 Slew Rate: Must account for de-rated slew rate for system timing (See JEDEC Table)
- Pitfall 11 Testability: Insure there is test and measurement access to DDR signals
- Some other noteworthy pitfalls
  - Not using ECC
    - Highly Recommended for first prototypes. De-pop for production
  - Missing pull-up on MAPAR_ERR (registered DIMMs) and MAPAR_OUT

Pitfall 1 – Noisy VREF

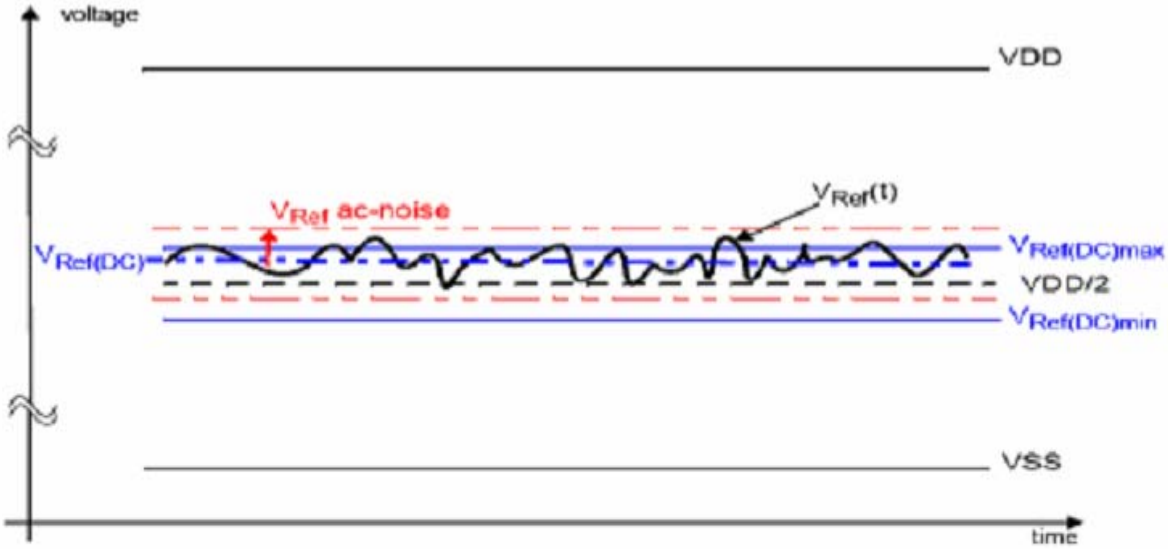

Figure 80 — Illustration of $V_{Ref(DC)}$ tolerance and V_{Ref} ac-noise limits

- VRef(t) may temporarily deviate from VRef(DC) by no more than +/- 1% VDD
- VRef(DC) is the linear average of VRef(t) over a very long period of time (e.g. 1 sec)

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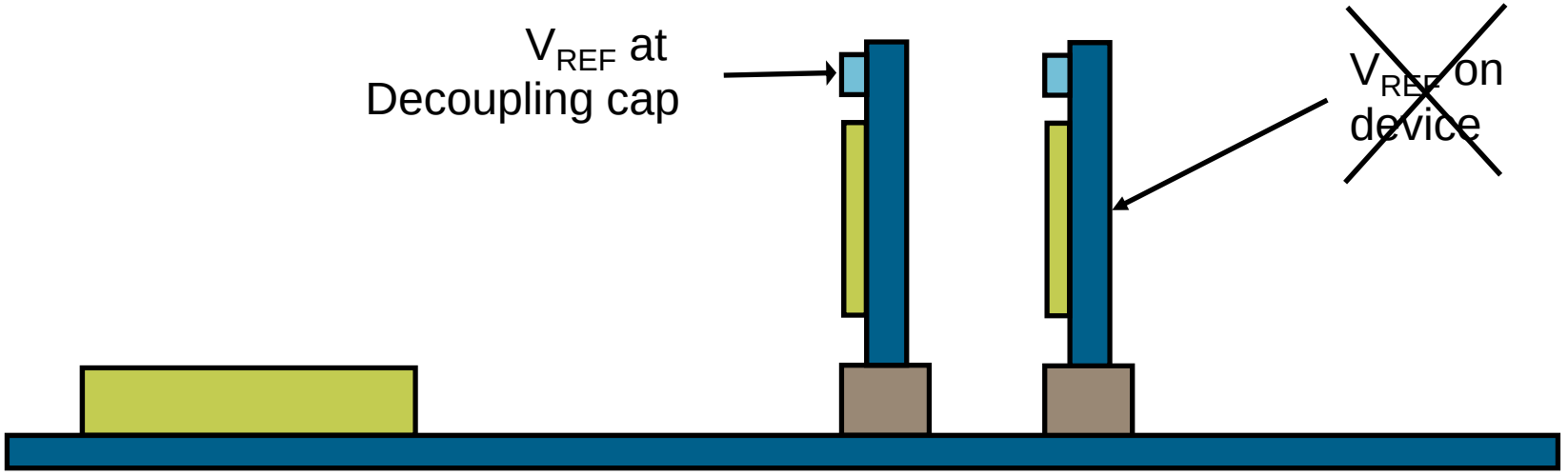
Pitfall 1 – Measuring V_{REF}

- **Measuring at device will likely give greater than 50 mV peak-to-peak**
  - Result of coupled noise from DDR device
- **V_{REF} system noise should be measured at capacitor nearest the memory device**



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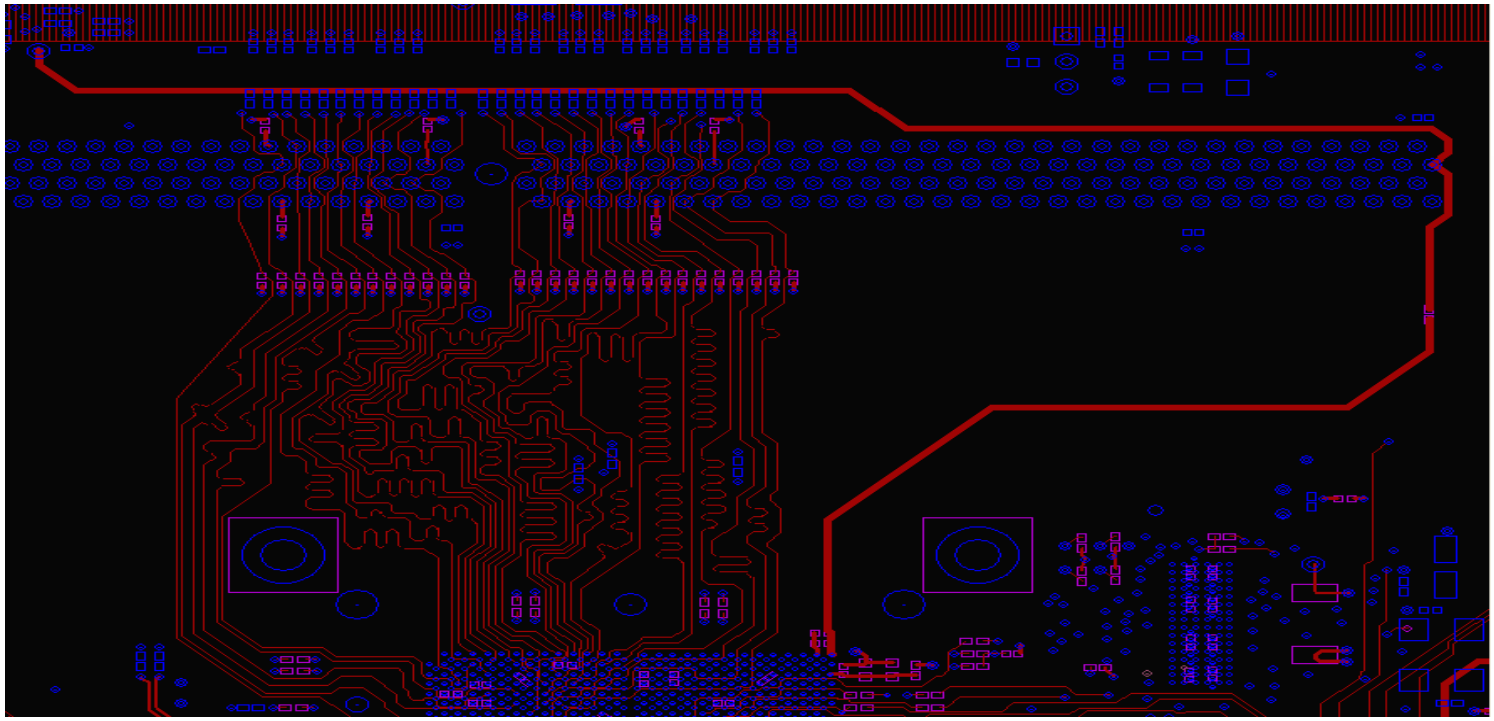
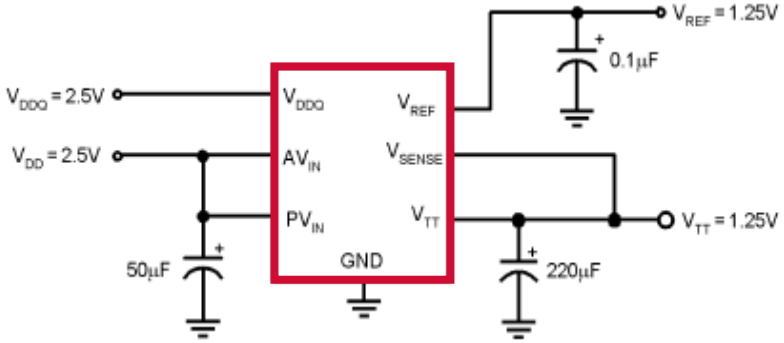
Pitfall 1 – Protecting VREF

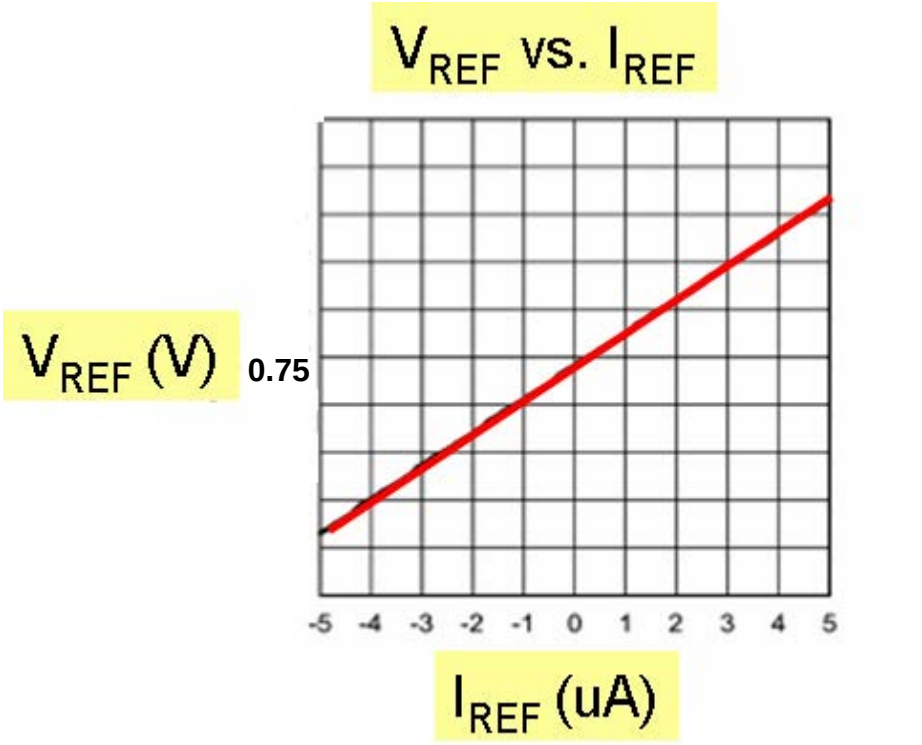
V_{REF}		
18.	Has V_{REF} been routed with a wide trace? (Minimum of 20–25 mil recommended.)	
19.	Has V_{REF} been isolated from noisy aggressors? In addition, maintain at least a 20–25 mil clearance from V_{REF} to other traces. If possible, isolate V_{REF} with adjacent ground traces.	
20.	Has V_{REF} been proper decoupled? Specifically, decouple the source and each destination pin with 0.1uf caps.	



Pitfall 2 – Wimpy V_{REF} source

- V_{REF} current consumption is typically 1.5-2.0 mA
- For most DDR regulators…. this is easily handled





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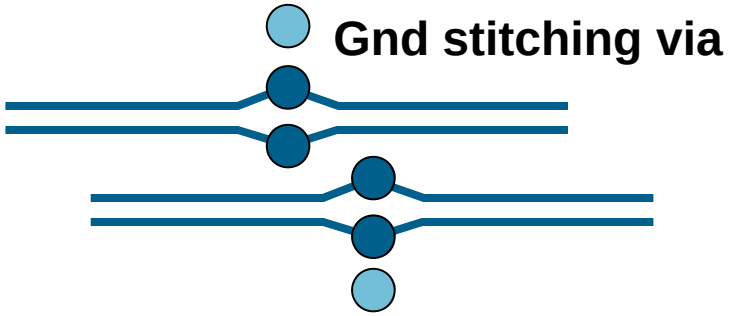
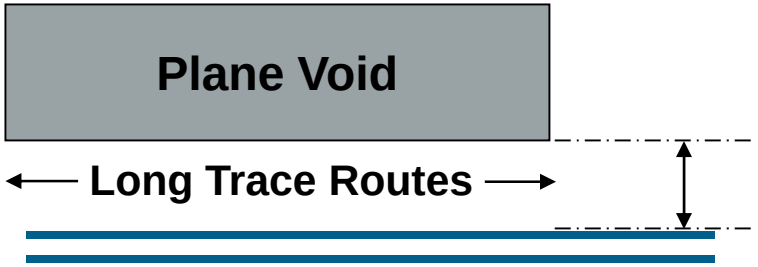
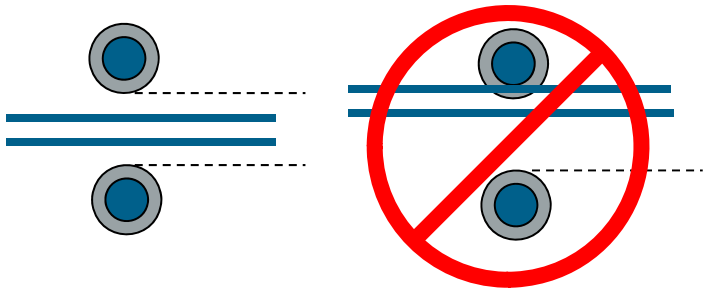
Pitfall 3 – Reference Plane discontinuities

- Contiguous reference plane
- Use stitching vias if switching layers
- Keep away from plane voids
- Avoid crossing plane splits
- Avoid trace over anti-pad







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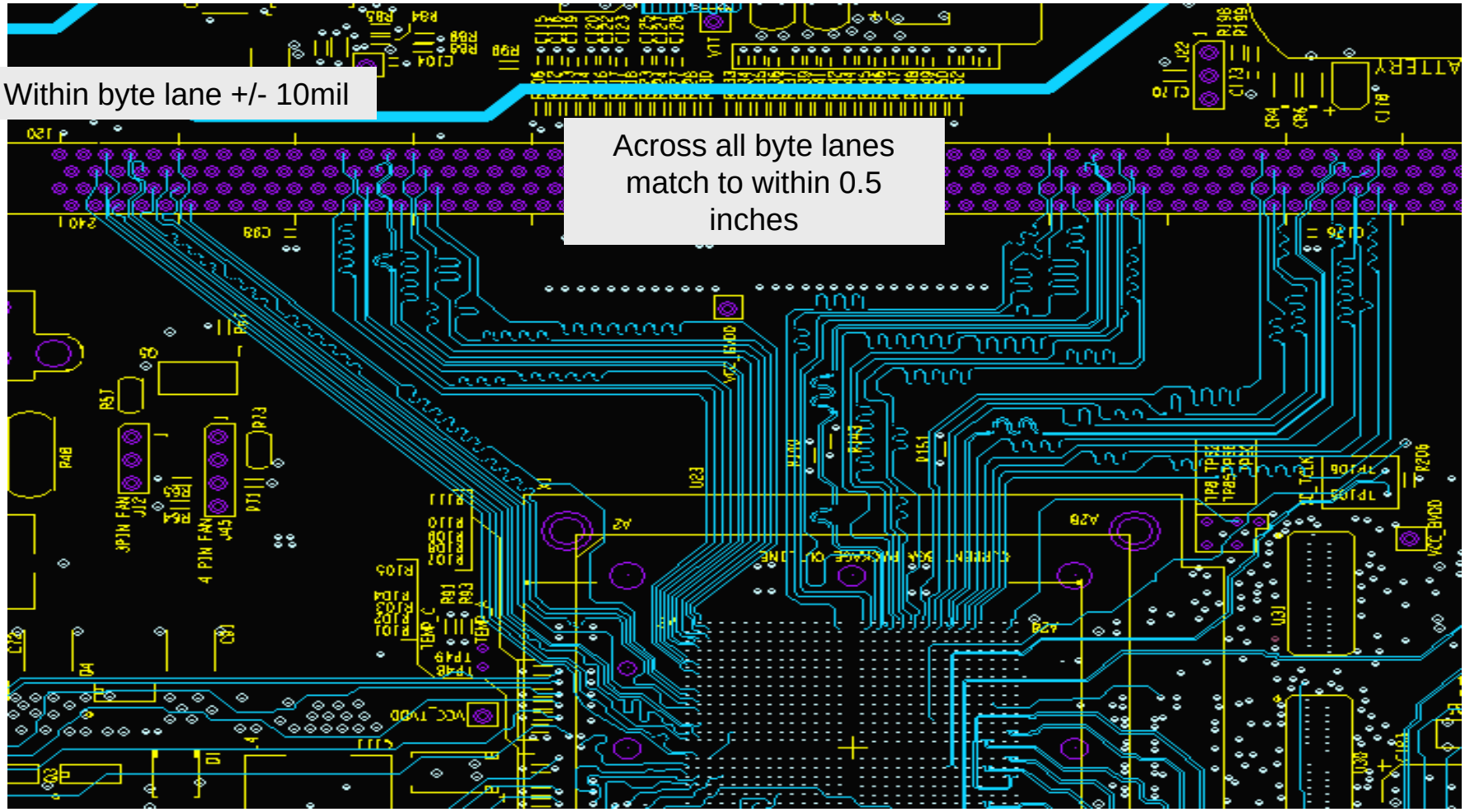
Pitfall 4 – Data Tuning



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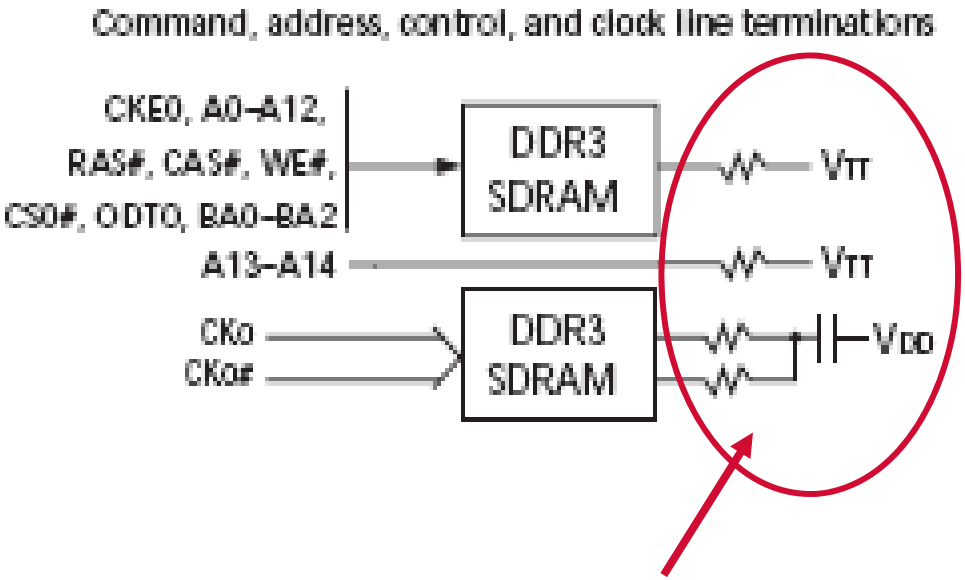
Pitfall 5 – Forgetting Termination



Still needed for soldered-down implementations.

DIMM modules have the termination on the module.

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Pitfall 6 – POR config selection

Table 4-18. DDR DRAM Type

Functional Signal	Reset Configuration Name	Value (Binary)	Meaning
TSEC2_TXD[1] Default (1)	cfg_dram_type	0	DDR2 1.8V, CKE low at reset
		1	DDR3 1.5V, CKE low at reset (default)

Above example assumes 8572. Other devices may utilize a different functional pin for the POR setting

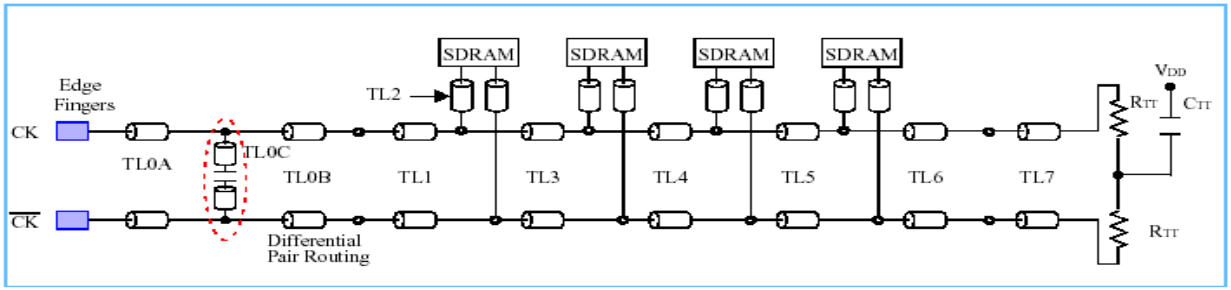
Pitfall 7 – Expandability

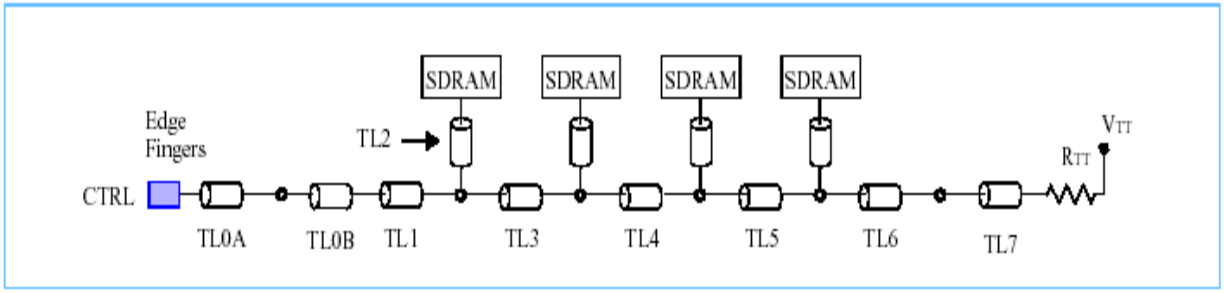
Signal Name	Pin Nomenclature	Signal Type	Function
A13	NC	No connection to internal die. Okay to run trace to PCB pad.	Used on x4/x8 512 Mb and 1 Gb devices and all configurations of the 2 Gb or 4Gb.
A14	NC	No connection to internal die. Okay to run trace to PCB pad.	Used on x4/x8 2 Gb devices and all 4 Gb configurations.
A15	NC	No connection to internal die. Okay to run trace to PCB pad.	Used on 4 Gb (x4/x8).
BA2	NC	No connection to internal die. Okay to run trace to PCB pad.	Used on all configurations of the 1 Gb, 2 Gb, and 4 Gb.

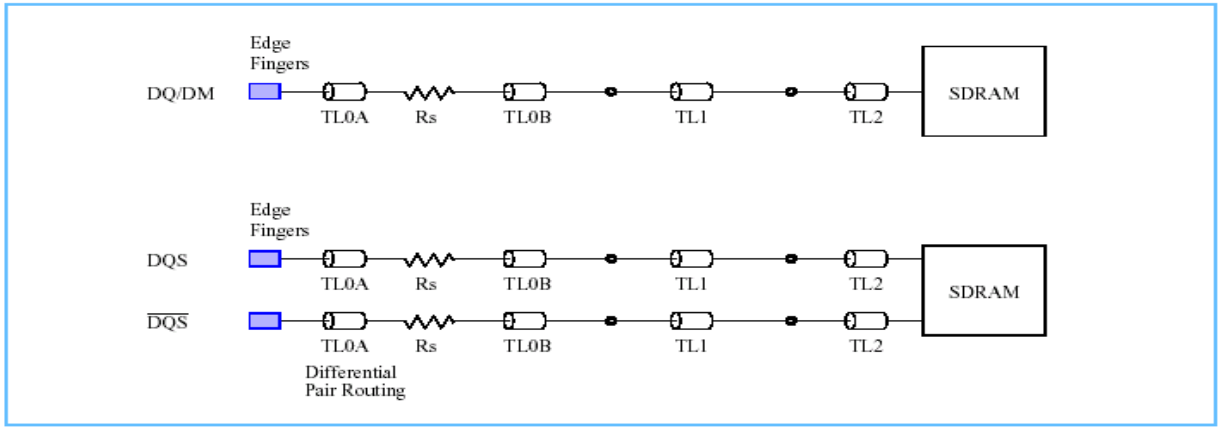
Rule of thumb:

For DDR3 - Every address (A0-A15), and all three bank address (BA0-BA2) line from our controllers should be connected to the memory subsystem.

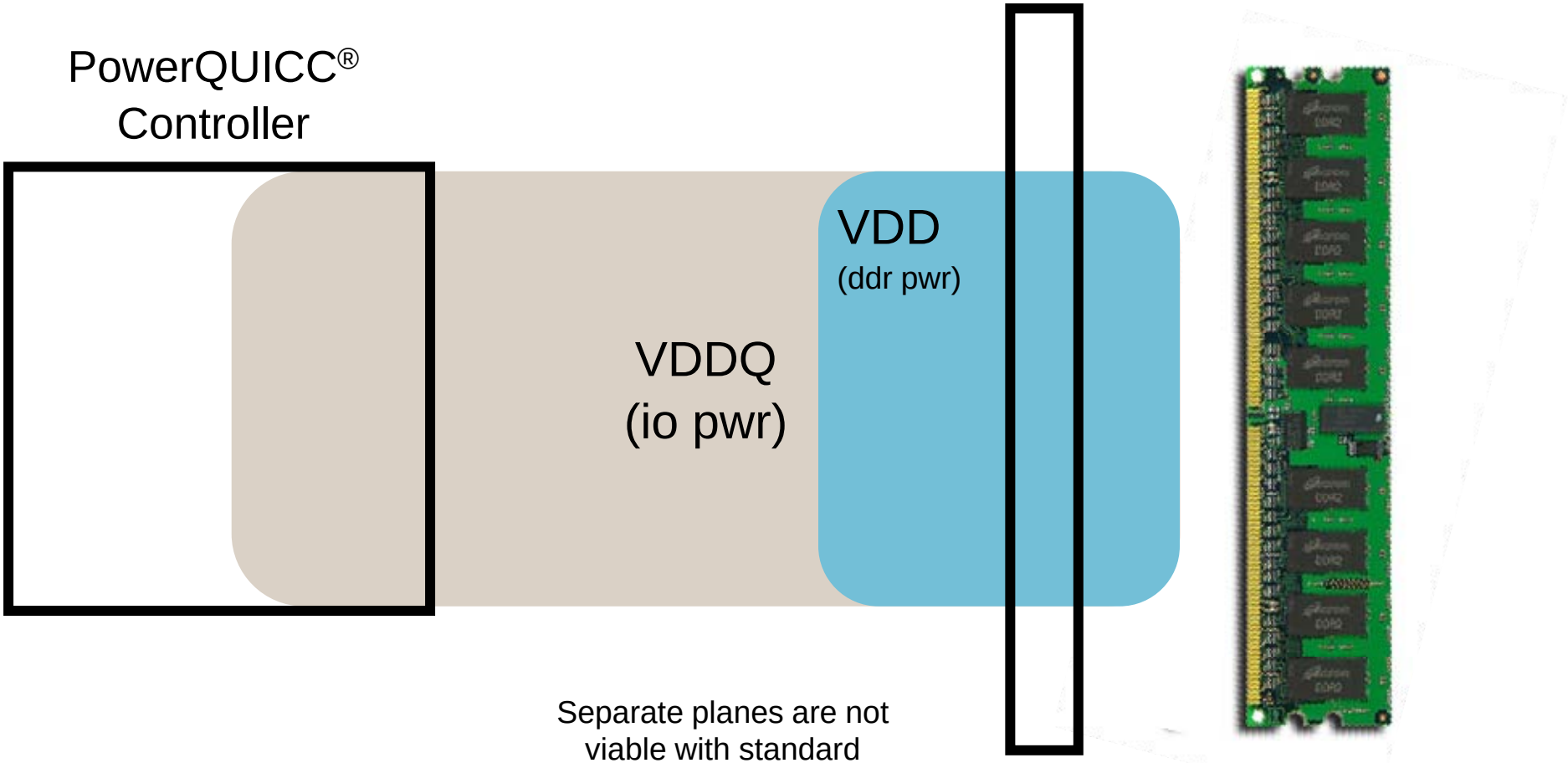
Pitfall 8 – Not using proven JEDEC topologies







Pitfall 9 – Separate VDDQ/VDDIO



Separate planes are not viable with standard JEDEC DIMM memory modules

VDDQ & VDDIO are same plane on the modules

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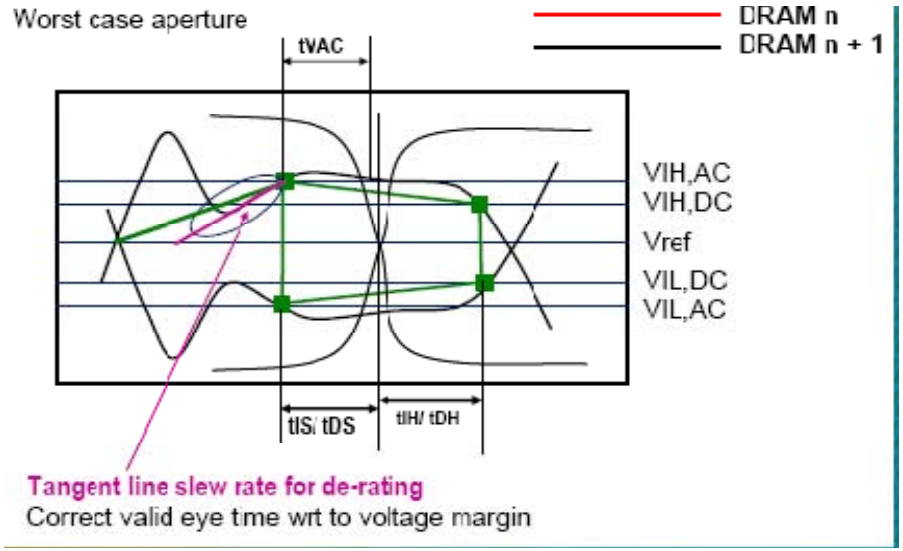
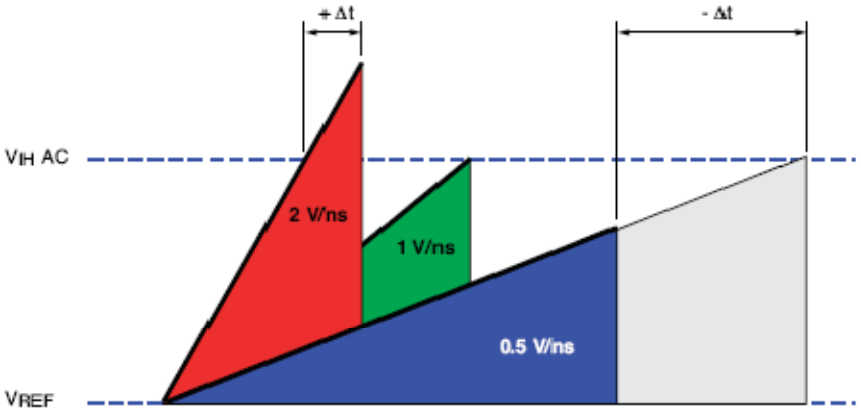
Pitfall 10– Slew Rate De-rating (setup & hold)





Source: Xcell Journal

Table 47 — Derating values for DDR2-667, DDR2-800

		ΔtIS and ΔtIH Derating Values for DDR2-667, DDR2-800							
		CK,CK Differential Slew Rate							
		2.0 V/ns		1.5 V/ns		1.0 V/ns			
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	Units	Notes
Com-mand/Ad-dress Slew rate (V/ns)	4.0	+150	+94	+180	+124	+210	+154	ps	1
	3.5	+143	+89	+173	+119	+203	+149	ps	1
	3.0	+133	+83	+163	+113	+193	+143	ps	1
	2.5	+120	+75	+150	+105	+180	+135	ps	1
	2.0	+100	+45	+130	+75	+160	+105	ps	1
	1.5	+67	+21	+97	+51	+127	+81	ps	1
	1.0	0	0	+30	+30	+60	+60	ps	1
	0.9	-5	-14	+25	+16	+55	+46	ps	1
	0.8	-13	-31	+17	-1	+47	+29	ps	1
	0.7	-22	-54	+8	-24	+38	+6	ps	1
	0.6	-34	-93	-4	-53	+26	-23	ps	1
	0.5	-60	-125	-30	-95	0	-65	ps	1
	0.4	-100	-188	-70	-158	-40	-128	ps	1
	0.3	-168	-292	-138	-262	-108	-232	ps	1
	0.25	-200	-375	-170	-345	-140	-315	ps	1
	0.2	-325	-500	-295	-470	-265	-440	ps	1
	0.15	-517	-708	-487	-678	-457	-648	ps	1
	0.1	-1000	-1125	-970	-1095	-940	-1065	ps	1

Source: JEDEC 79-2C

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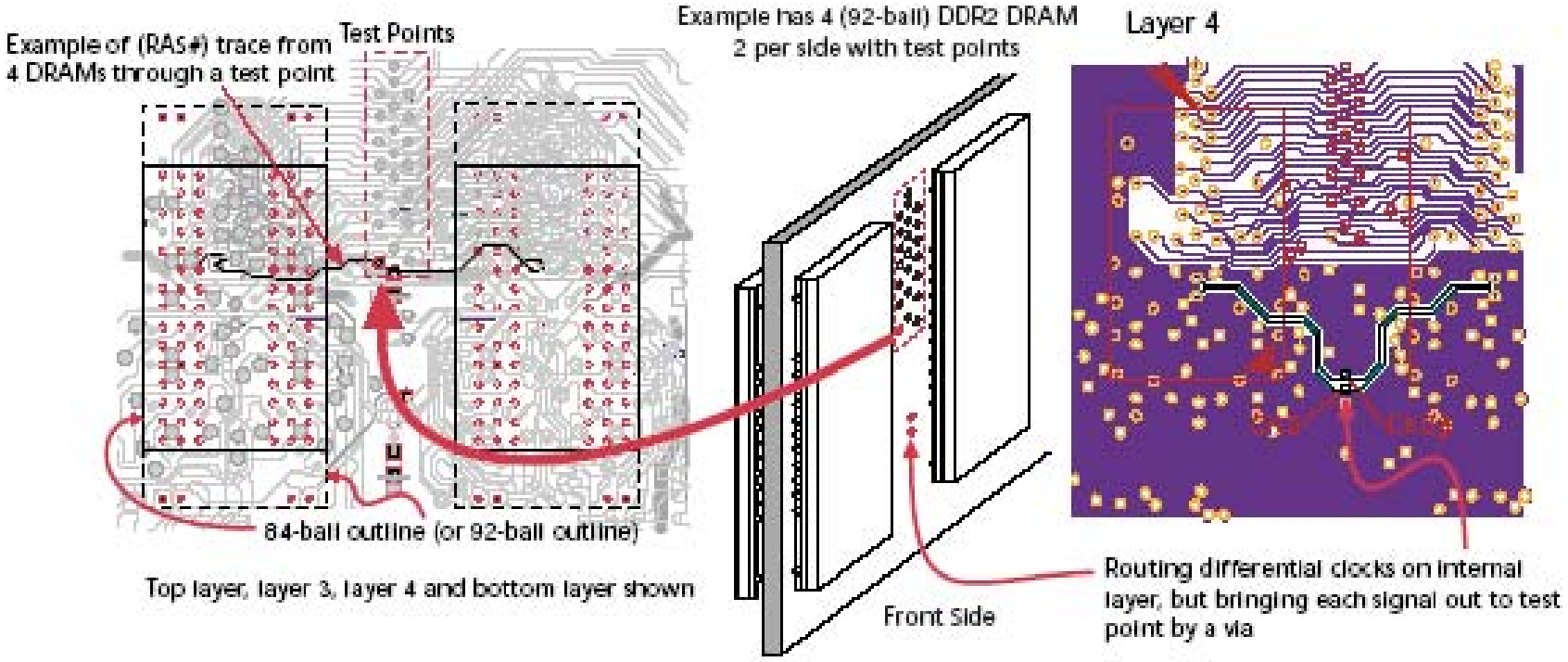
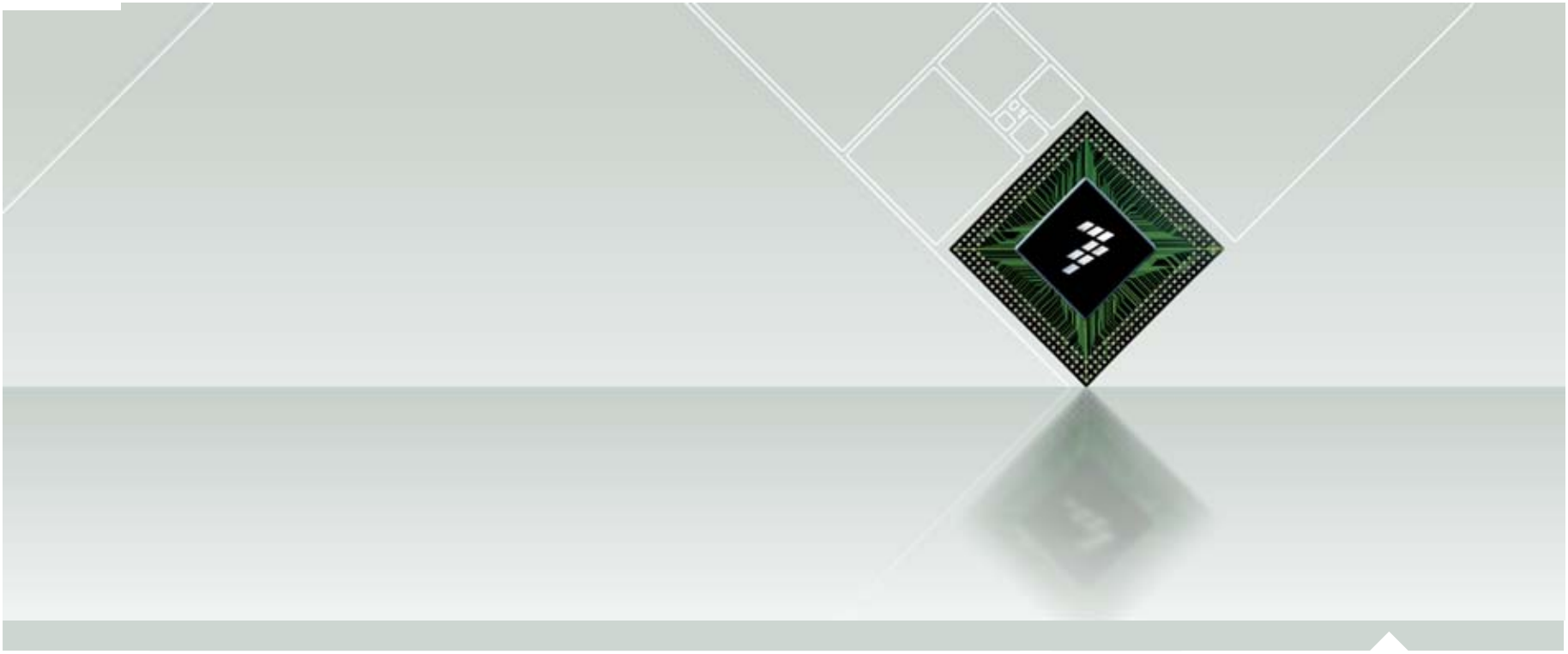
Pitfall 11 – No debug or testability on BGA devices





References

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Useful References

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- Freescale AppNotes:
  - AN2582 Hardware and Layout Design Considerations for DDR Memory Interfaces
  - AN2910 Hardware and Layout Design Considerations for DDR2 Memory Interfaces
  - AN2583 Programming the PowerQUICCIII / PowerQUICCII Pro DDR SDRAM Controller
  - AN3369 PowerQUICC DDR2 SDRAM Controller Register Setting Considerations
  - AN3939 PQ & QorIQ Interleaving
  - AN3940 Layout Design Considerations for DDR3 Memory Interface
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  - JESD79-2B DDR2 SDRAM Specification
  - JESD79-3A DDR3 SDRAM Specification


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