June, 2010

Leveraging the QorIQ Data Path Acceleration Architecture (DPAA) for Wireless Applications

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Agenda (time/presenter to be removed)

- Challenges in Wireless Industry
- QorIQ Application Mapping
- Data Path Acceleration – quick recap.
- Packet I/O
- PME – traffic monitoring and management
- SEC – Ciphering and packet formatting
- Use-case: Voice packet processing
- Use-case: HSPA, mobile broadband

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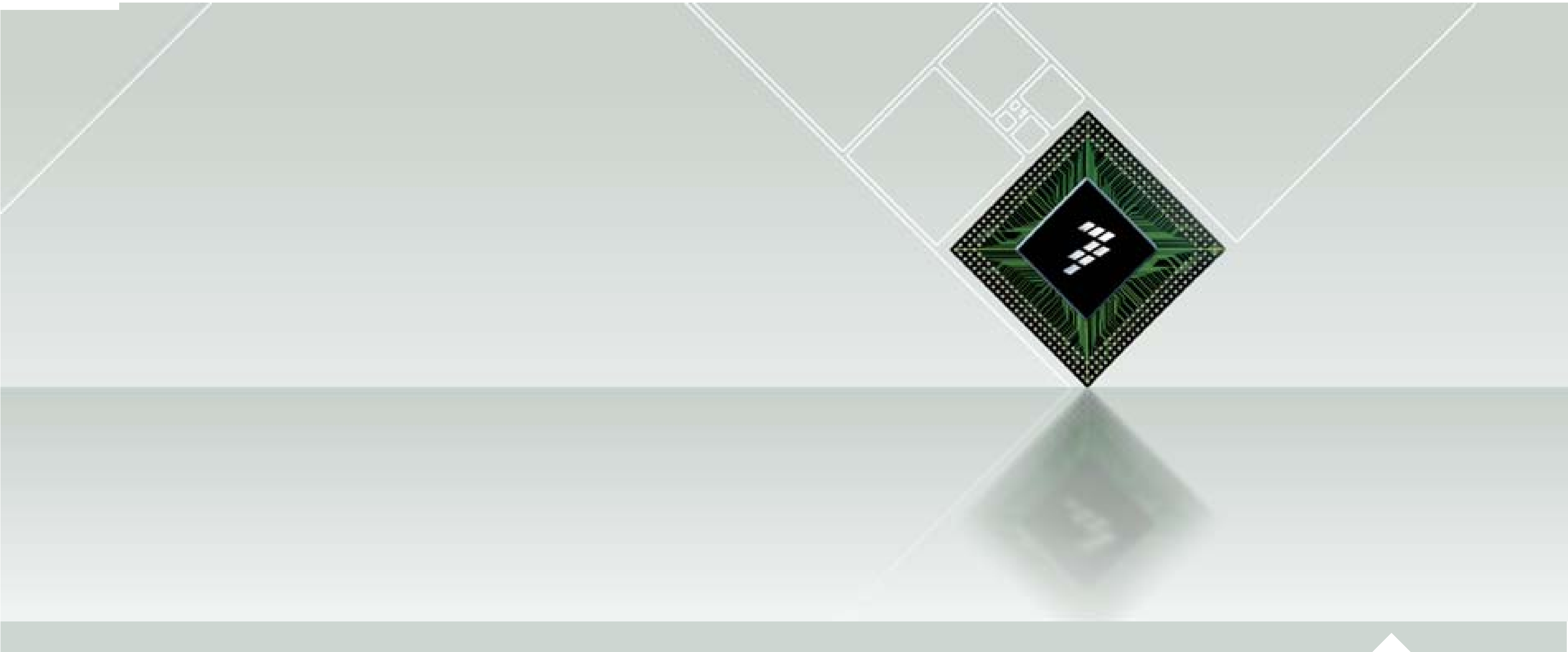

Challenges in Wireless Industry

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Trends / Challenges

- Mobile broadband has taken off
  - High bandwidths
  - High user peak rates
  - Low network latency

- Smart Phones (iphone etc) require intensive signaling, i.e. control processing.

- WCDMA follows the LTE track in development
  - Competitive performance with HSPA+
  - Support for flat architecture

- Home base-station, will 2010/11 be the break through?
- All IP? Investments in ATM needs smooth migration, i.e. IP over ATM.
- Content Caches in field to offload main pipe to Internet?

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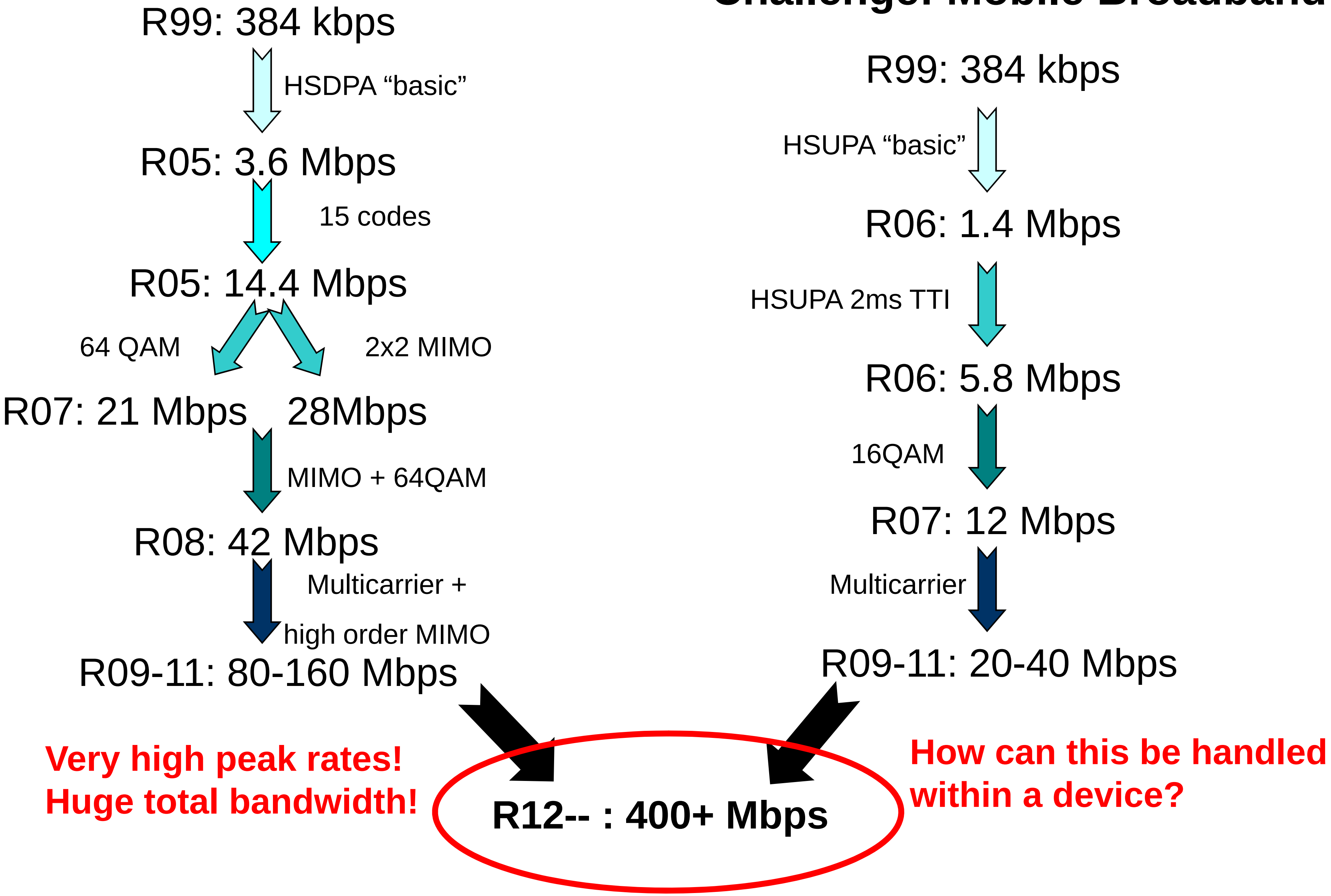
Challenge: Mobile Broadband



R99: 384 kbps

HSDPA “basic”

R05: 3.6 Mbps

15 codes

R05: 14.4 Mbps

64 QAM

2x2 MIMO

R07: 21 Mbps

28Mbps

MIMO + 64QAM

R08: 42 Mbps

Multicarrier +

high order MIMO

R09-11: 80-160 Mbps

R99: 384 kbps

HSUPA “basic”

R06: 1.4 Mbps

HSUPA 2ms TTI

R06: 5.8 Mbps

16QAM

R07: 12 Mbps

Multicarrier

R09-11: 20-40 Mbps

Very high peak rates!
Huge total bandwidth!

R12-- : 400+ Mbps

How can this be handled within a device?

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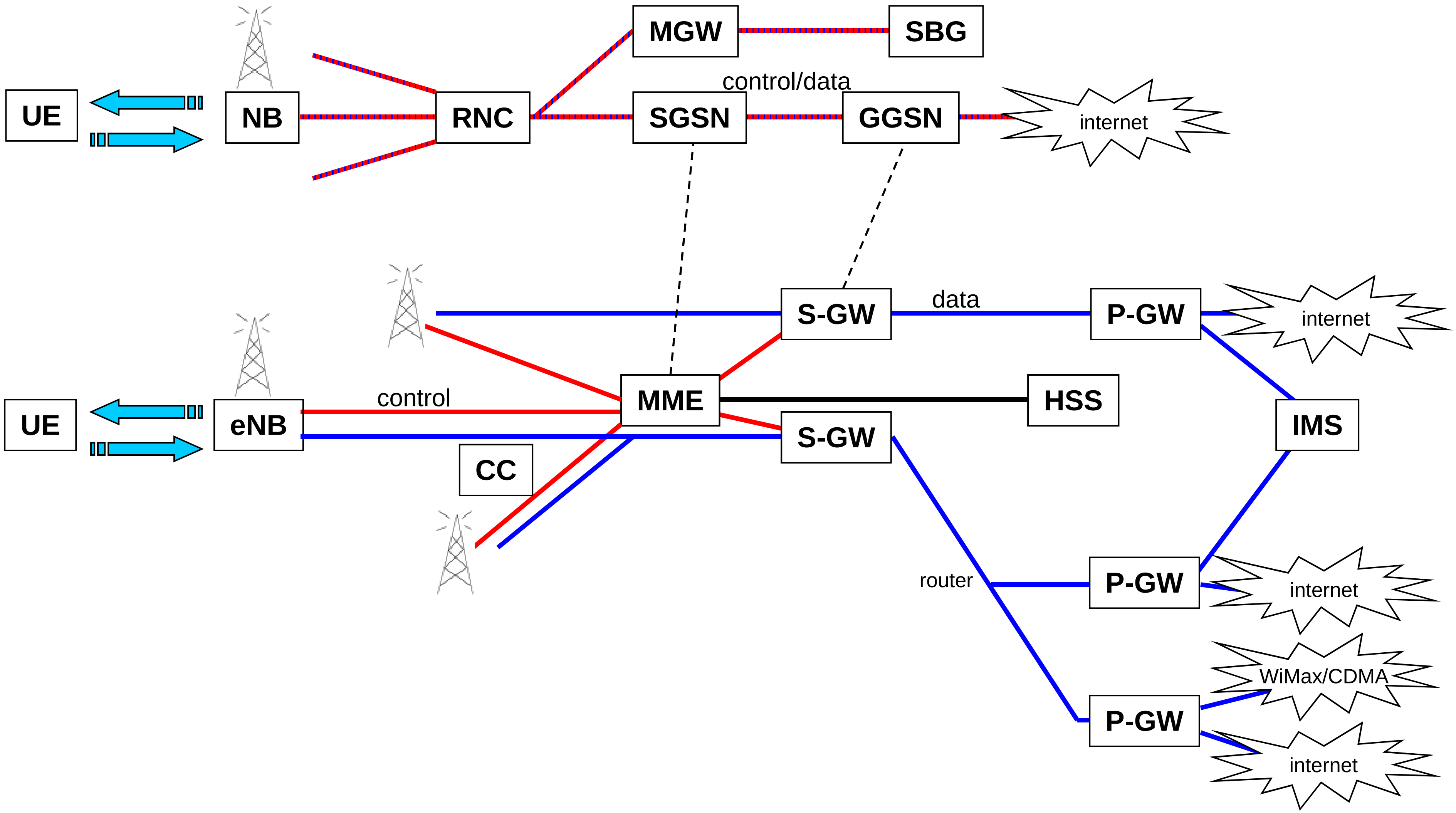
WCDMA and LTE Core Networks



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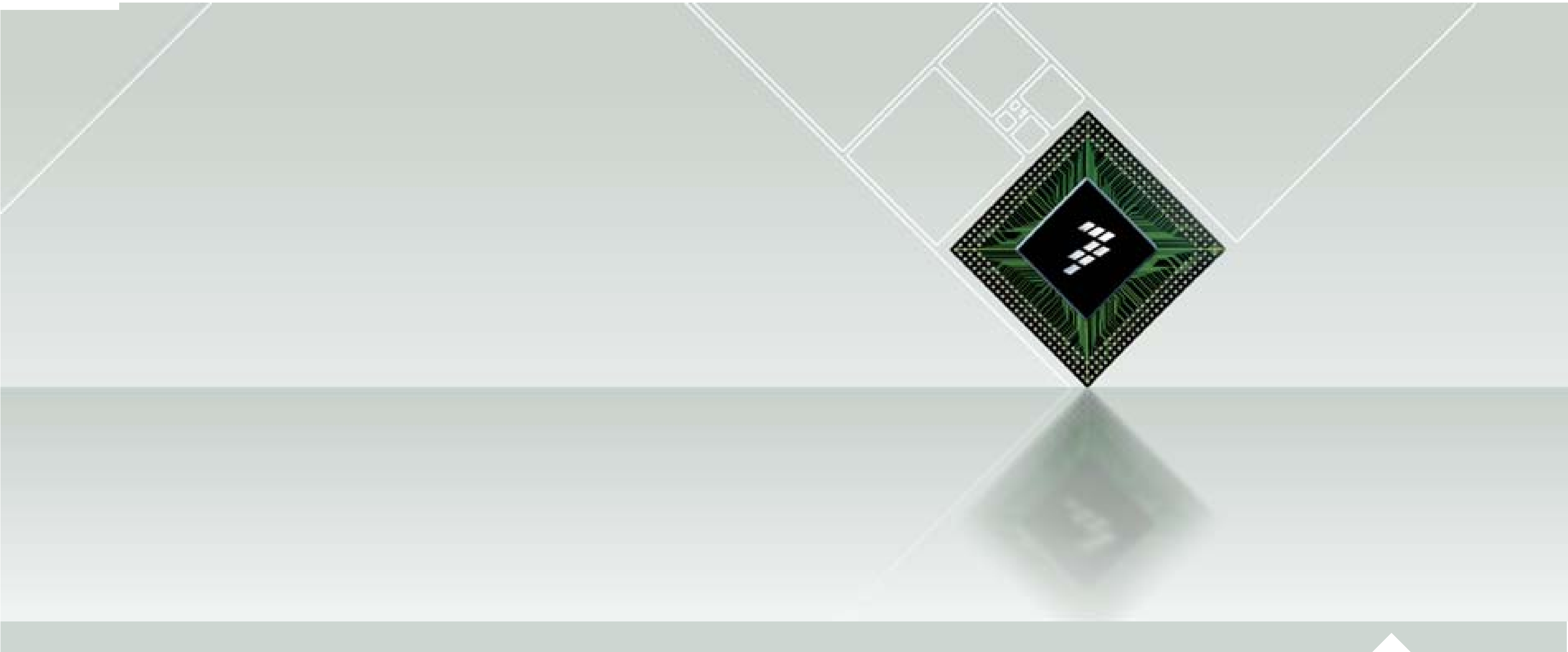

QorIQ Application Mapping

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QorIQ™ Investment Continues Our Embedded Leadership Tradition

▶ Our 15+ year Heritage:

▶ 3rd Generation Data Path

- Gen-1: CPM MPC8260
- Gen-2: QUICC Engine™ MPC8360
- Gen-3: DPAA QorIQ P4080

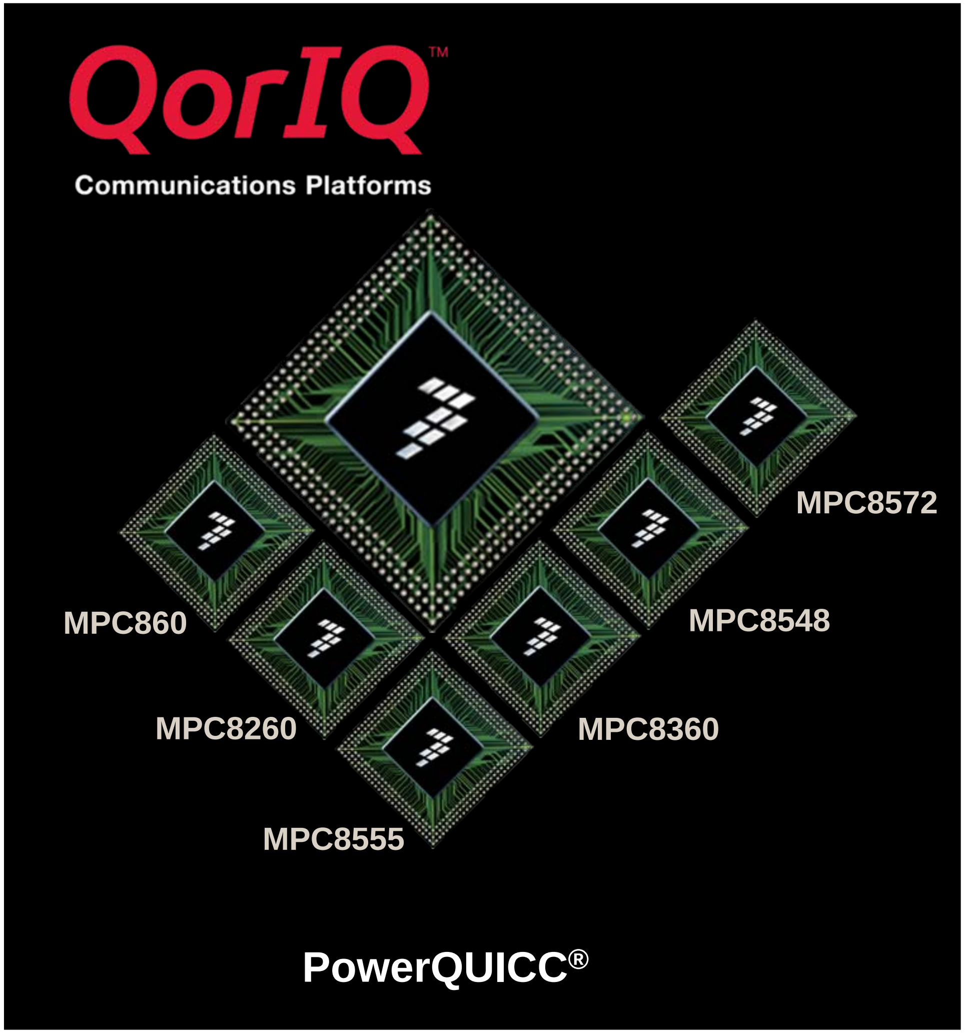
▶ Accelerating Connectivity

- eTSEC
- SEC 4.0
- PME 2.0
- PCIe, Serial RapidIO®, XAUI

▶ Power Architecture™ ISA

- e500 PowerQUICC® III
- e500 QorIQ P1, P2 platforms
- e500mc QorIQ P3, P4 platforms

▶ Long life cycle management for industry



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QorIQ™ Platform Levels matching Wireless Applications

45nm PLATFORMS / PRODUCTS

QorIQ P5

Highest-performing embedded processors
PRODUCTS: P5010 / P5020

QorIQ P4

Octal and Quad core family
PRODUCTS: P4080
P4040

QorIQ P3

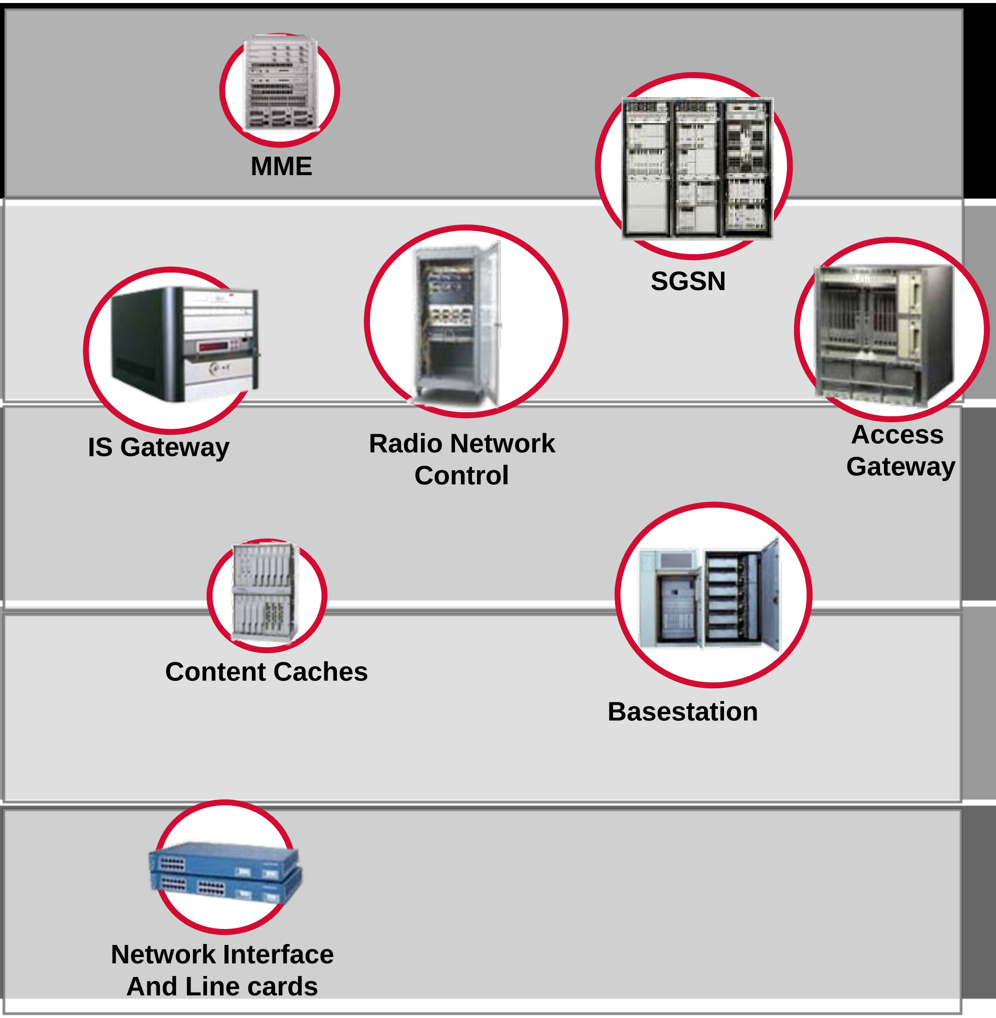
Quad core family – entry level MC
PRODUCTS: P3040 / P3041

QorIQ P2

High performance Dual and Single Core
PRODUCTS:
P2020 and P2010

QorIQ P1

Low Power Dual and Single Core
PRODUCTS: P1020 , P1011, P1010



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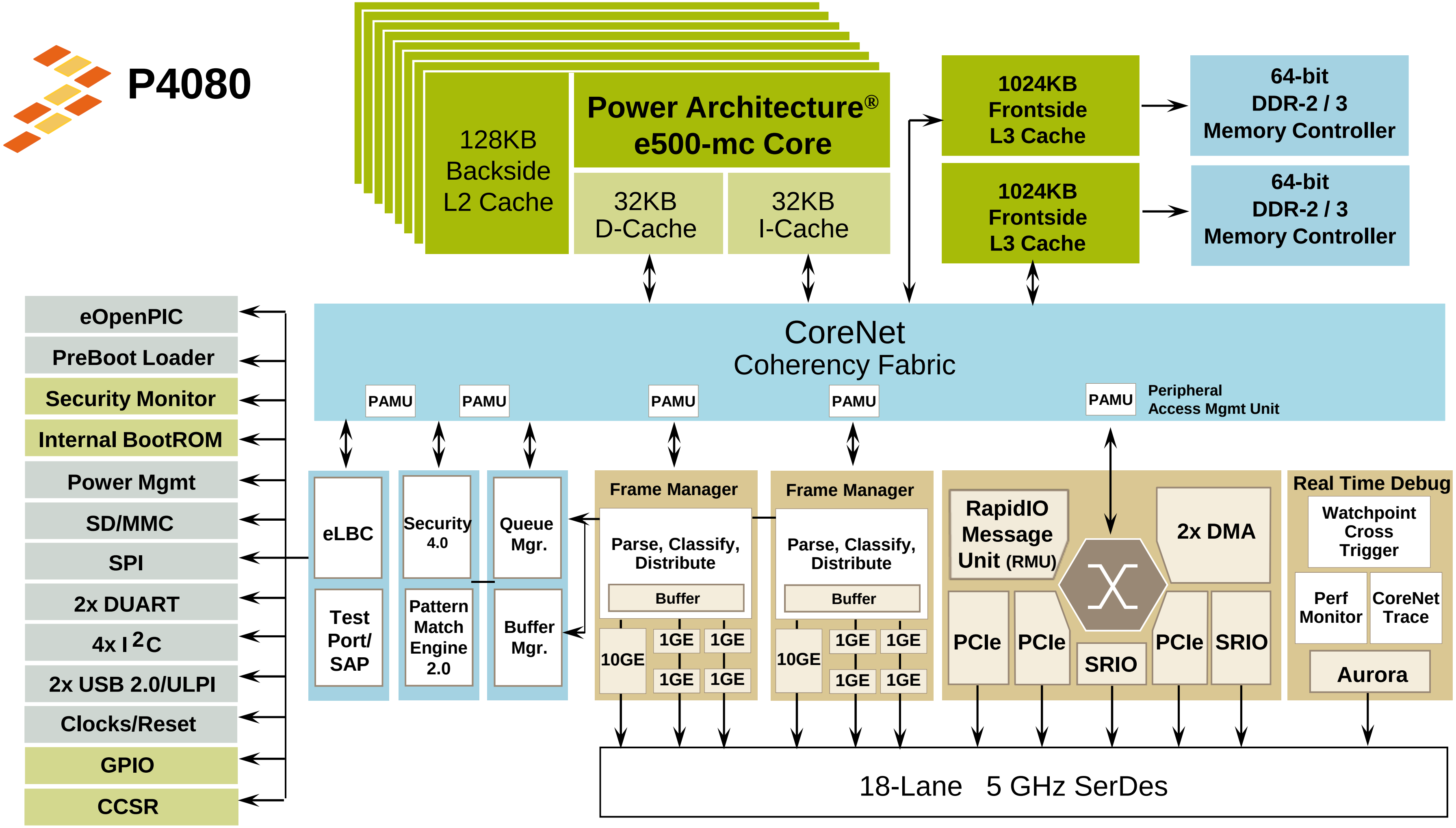
QorIQ P4 Series P4080 Block Diagram



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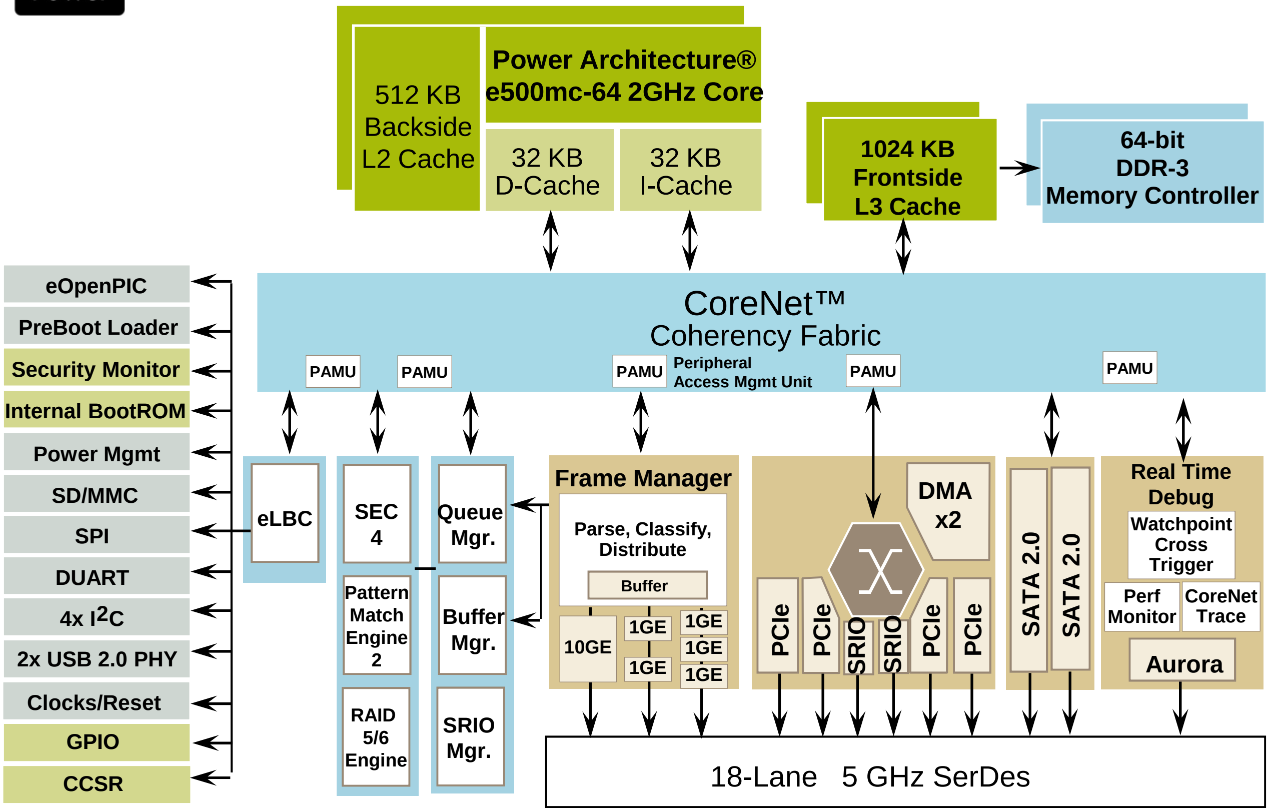
QorIQ P5 Series P5020 Block Diagram



- **2x e500mc-64 core, built on Power Architecture® technology**
  - 2x 64-bit cores (up to 2+ GHz) with 512 KB backside L2 cache
  - Dual 1MB Shared L3 cache w/ECC
- **Memory Controller**
  - Dual 32/64-bit DDR3/3L w/ECC up to 1.3 GHz
- **Ethernet**
  - 5 x 10/100/1000 Ethernet controllers
  - 1 x 10GE controller (XAUI)
- **High Speed Interconnect**
  - 4 PCI Express® 2.0 controllers
  - 2 Serial RapidIO® 1.3 + 2.0 controllers
  - 2 SATA 3Gb/s
  - 2 USB 2.0 with PHY
- **CoreNet Switch Fabric**
- **Trusted Architecture**
- **Data Path Acceleration Architecture**
  - Security Engine (SEC)
  - Pattern Matching Engine (PME)
  - RAID 5/6 Engine
  - Enhanced RapidIO Messaging (Rman)

- **Pin Compatible to P4080, P4040 & P3041**
- **45nm SOI Process**

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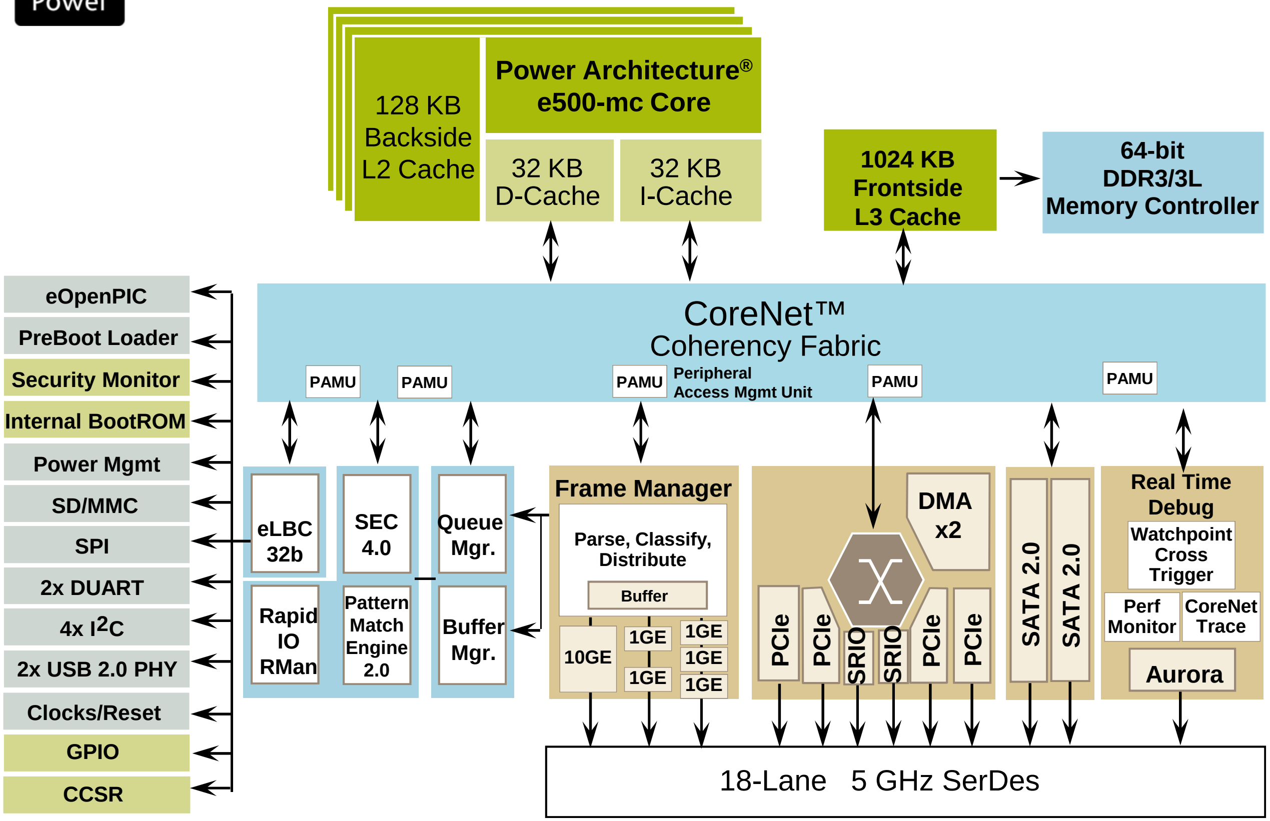
QorIQ P3 Series P3041 Block Diagram



- **Pin Compatible to P4080, P4040, P5020 & P5010**
- **45nm SOI Process**

Quad e500mc Power Architecture®

- 4 cores (up to 1.5GHz) with 128KB backside L2 cache
- 1MB Shared L3 Cache w/ECC

Memory Controller

- 32/64bit DDR3/3L w/ECC up to 1.3 GHz

Ethernet

- 5 x 10/100/1000 Ethernet Controllers
- 1 x 10GE Controllers

High Speed Interconnect

- 4 PCIe 2.0 Controllers
- 2 SRIO 1.3 + 2.0 Controllers
- 2 SATA 2.0
- 2 USB 2.0 w/PHY

CoreNet Switch Fabric

Trusted Architecture

Datapath Acceleration Architecture

- Security Engine (SEC)
- Pattern Matching Engine (PME)
- Enhanced RapidIO Messaging (Rman)

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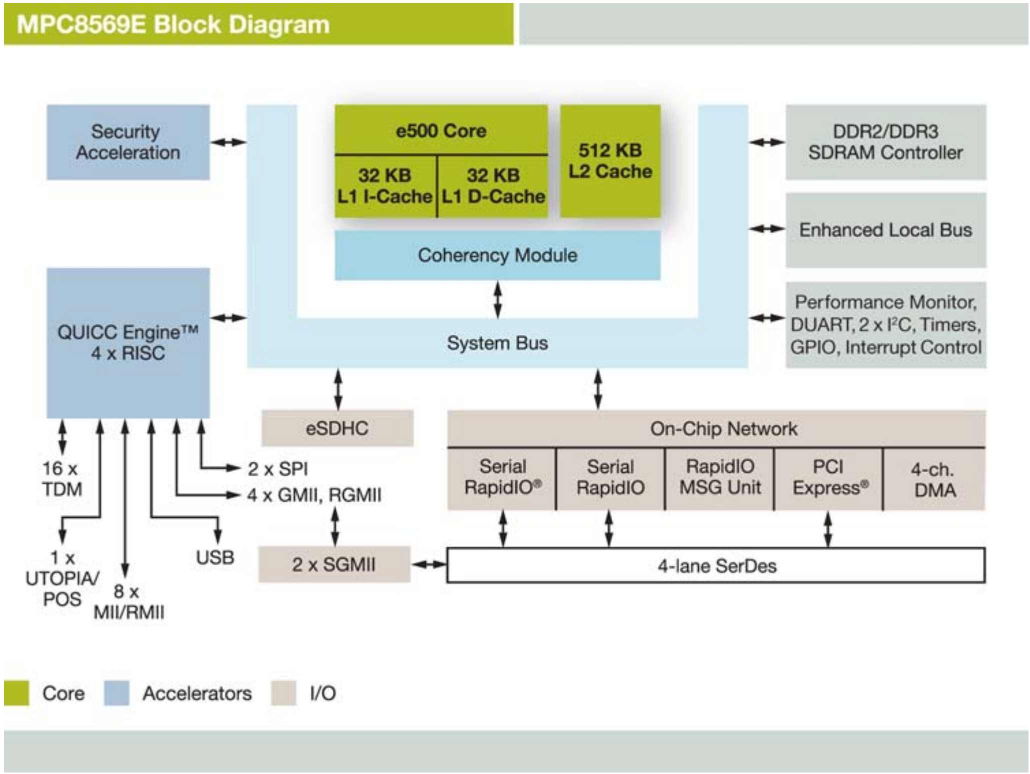
MPC8569 PowerQUICC III
Bridging the Gap to the All-IP Network



MPC8569E Block Diagram

- ▶ **e500 PowerPC** from 800MHz to 1.33 GHz
  - 512KB L2 Cache w/ ECC
  - 36bit physical addressing
  - Double Precision Floating Point
- ▶ **System Interfaces**
  - 64b or 2x32-bit DDR2/3 w/ ECC
  - 800 Mbps/pin data rate
  - 16-bit Local Bus for SRAM/Flash
  - Timers, DUART, 2xI²C, GPIO, SPI
  - USB 2.0 Full Speed
- ▶ **High Speed Serial Interfaces**
  - Dual SGMII
  - Dual x1 Serial RapidIO or PCI-Ex
- ▶ **QUICC Engine**
  - 4 RISCs up to 667 MHz
  - Maximum of 8 Ethernet interfaces, one per UCC:
    - 4 x Gigabit Eth (up to 2 w/SGMII)
    - Up to 8 x 10/100 Ethernet
  - Multi-PHY UTOPIA/POS-PHY L2 (16-bit)
  - IEEE1588 Support v2
  - 16 x T1/E1 (512 x 64kbps channels)
- ▶ **Security Engine (SEC3.0)**
  - ARC4, 3DES, AES, RSA/ECC, RNG, XOR, Single pass SSL/TLS, Kasumi, SNOW
- ▶ **Four-channel DMA**
- ▶ **45nm SOI process technology**
- ▶ **Target <7W Power (@ 800MHz e500)**

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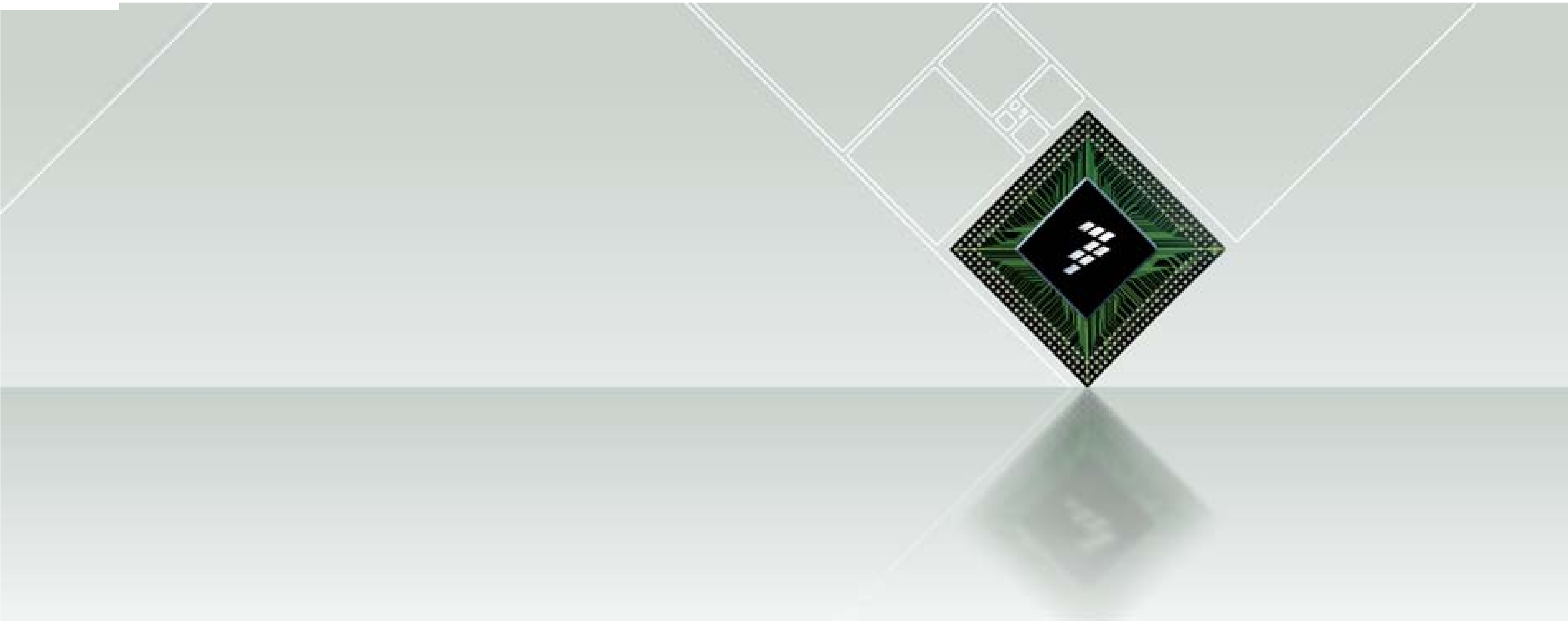

Data Path Acceleration: Quick Recap

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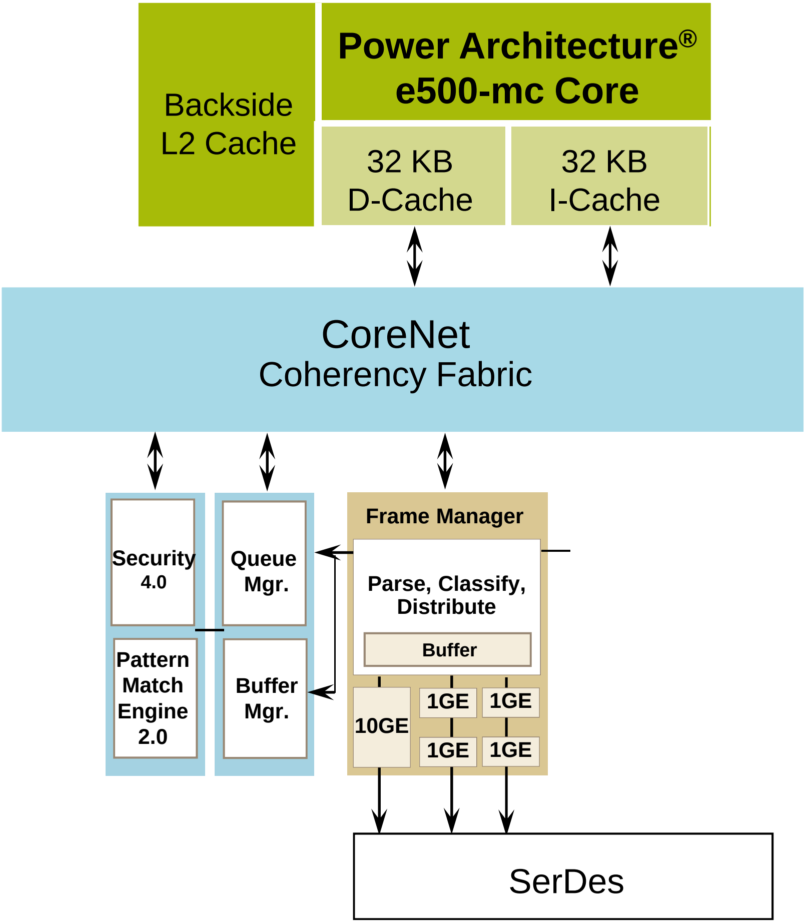
DPAA – Data Path Acceleration Architecture

- **Frame Manager:**
- Parse header information
- Classify to what destination the packet is targeted
  ex. MAC, IP, UDP destination
- Distribute packets to allow load balancing between cores
- Police flows to avoid DoS attacks



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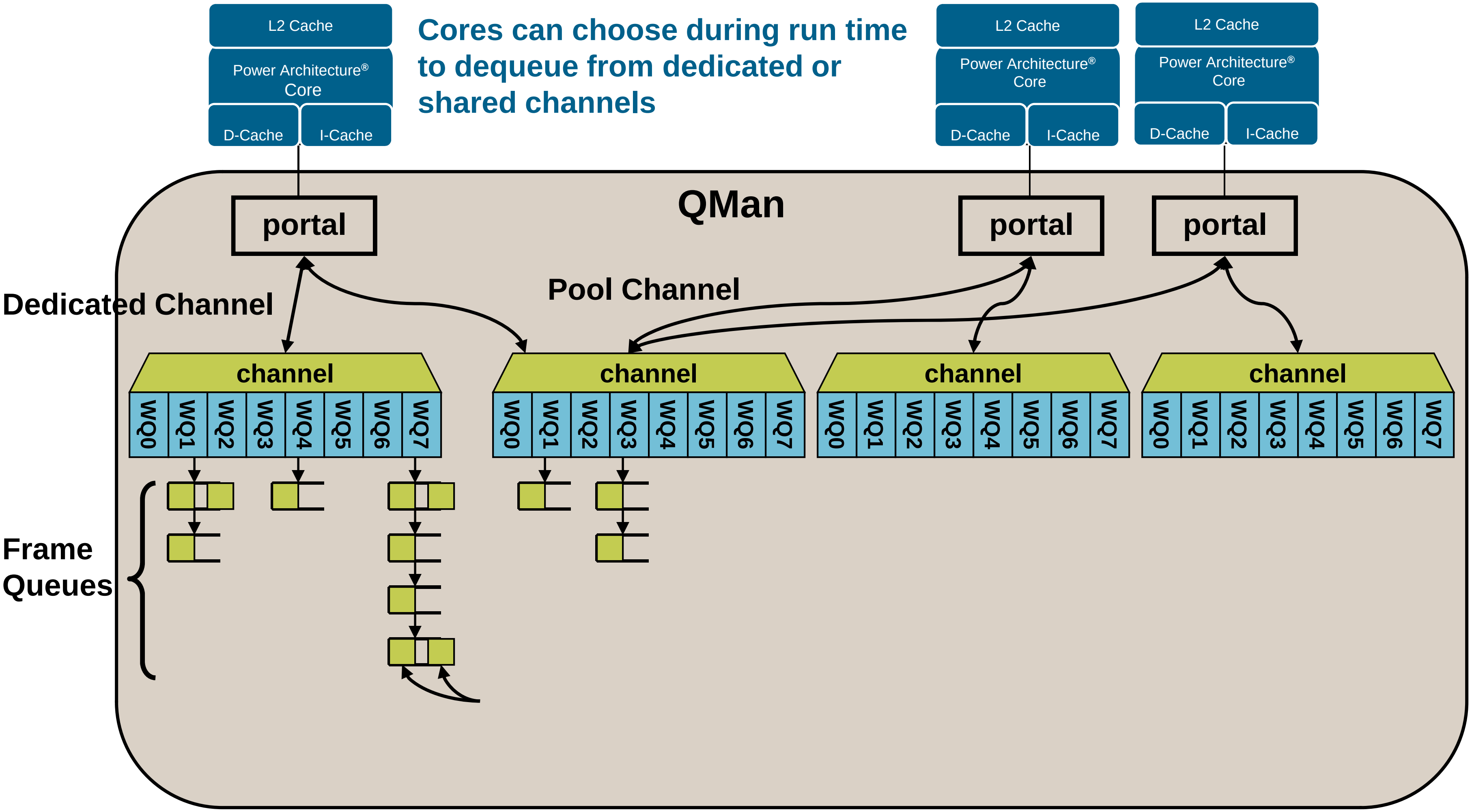
QMan Software Portals

Cores can choose during run time to dequeue from dedicated or shared channels



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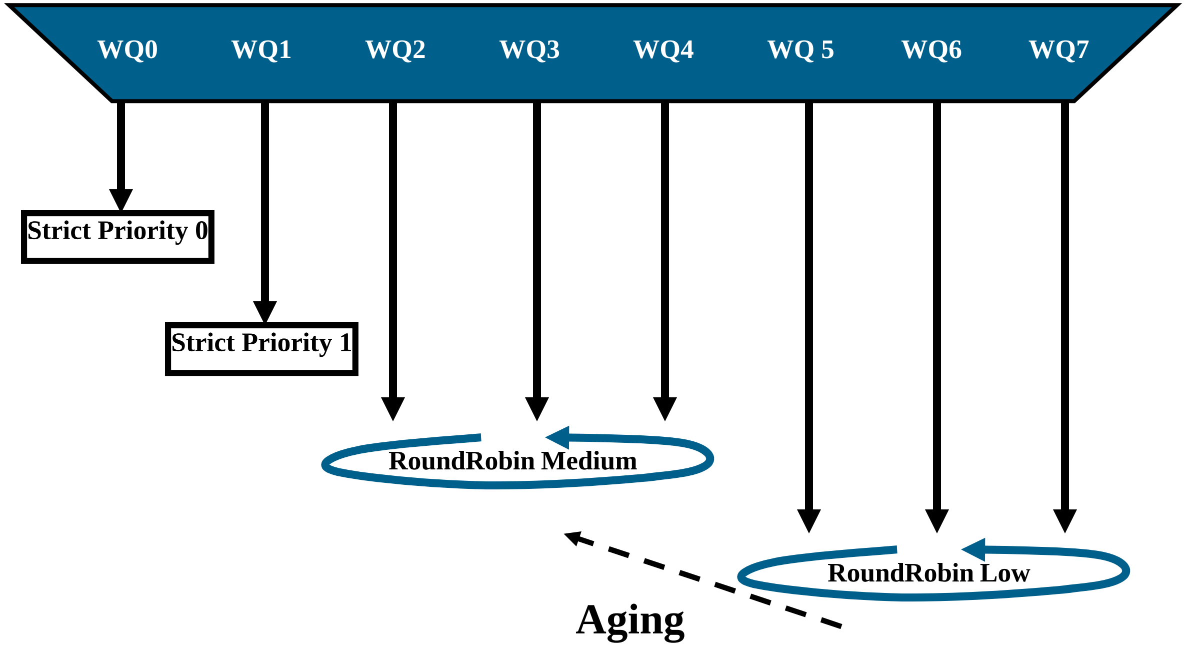
QoS supported through Channel Scheduler



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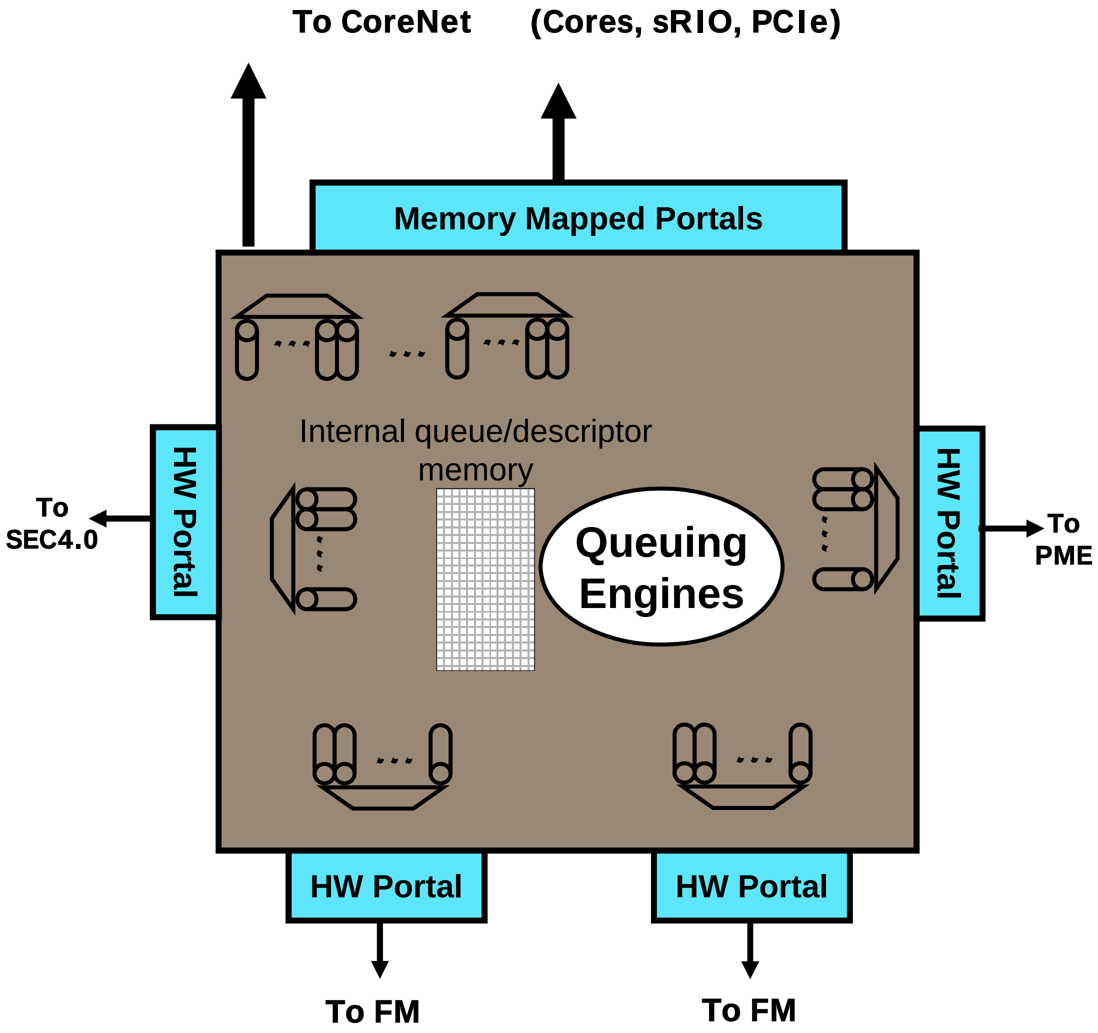
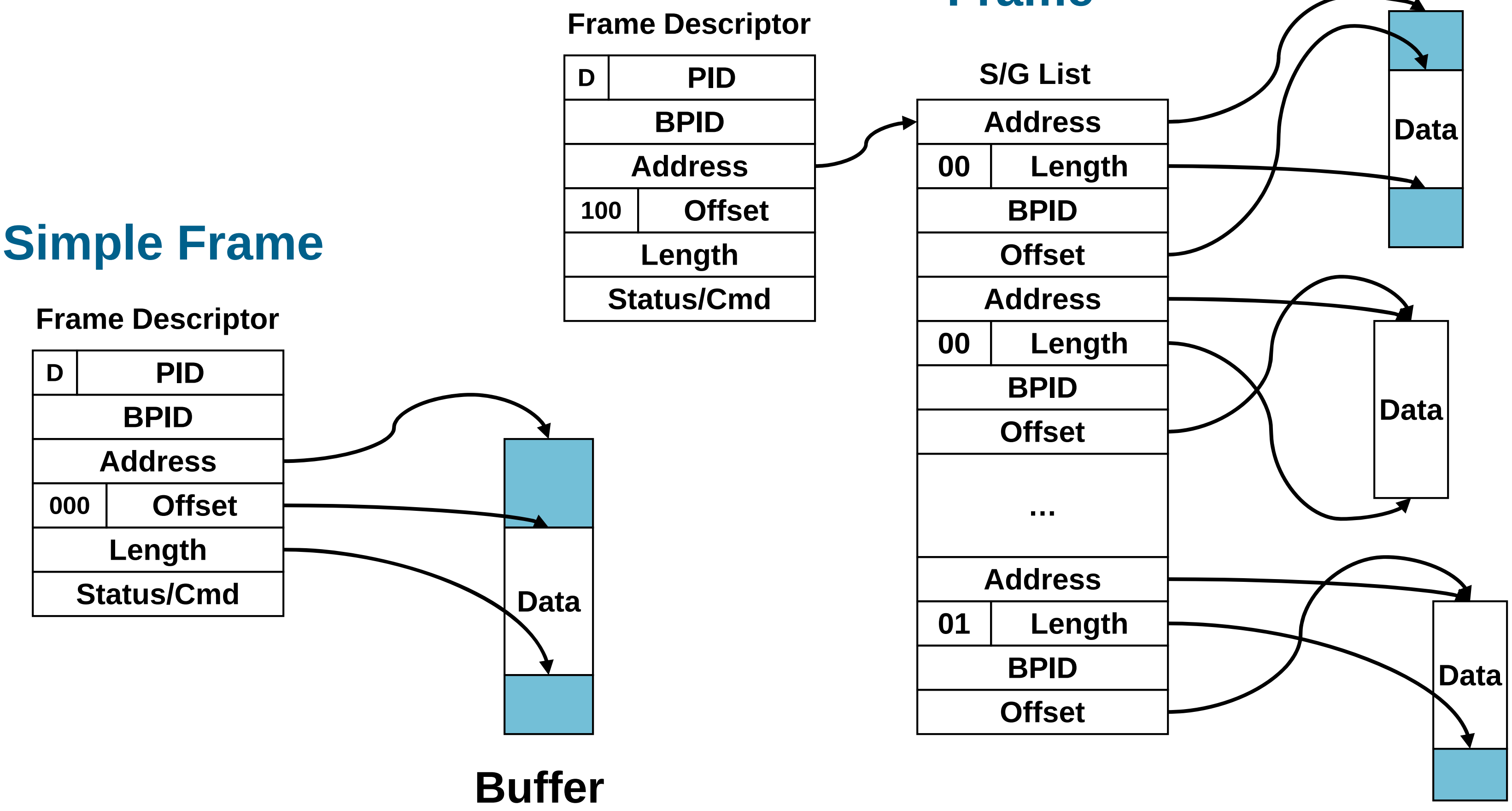
Queue Manager (QMan)



- QMan provides a set of building blocks
  - Frame queues (FQ) which are enqueued onto
    …Work queues (WQ) which are organized into
    …Channels with prioritized class scheduling between WQs
    … which can be used to build connections between blocks (cores, network I/Fs, HW accelerators)
- Frame queues are “logical” queues
  - Actual data is stored in memory buffers, QMan queues “ frame descriptors”
- QMan also supports active queue management:
  - Tail drop on FQs
  - WRED on groups of FQs
  - Tail drop on groups of FQs
- Channels can be shared between consumers which facilitates load spreading
- Channels may also be dedicated to a single consumer

Unified DPAA Frame Formats



Simple Frame

Frame Descriptor

D	PID
BPID	
Address	
000	Offset
Length	
Status/Cmd	

Buffer

Multi-buffer (Scatter/gather) Frame

Frame Descriptor

D	PID
BPID	
Address	
100	Offset
Length	
Status/Cmd	

S/G List

Address	
00	Length
BPID	
Offset	
Address	
00	Length
BPID	
Offset	
…	
Address	
01	Length
BPID	
Offset	

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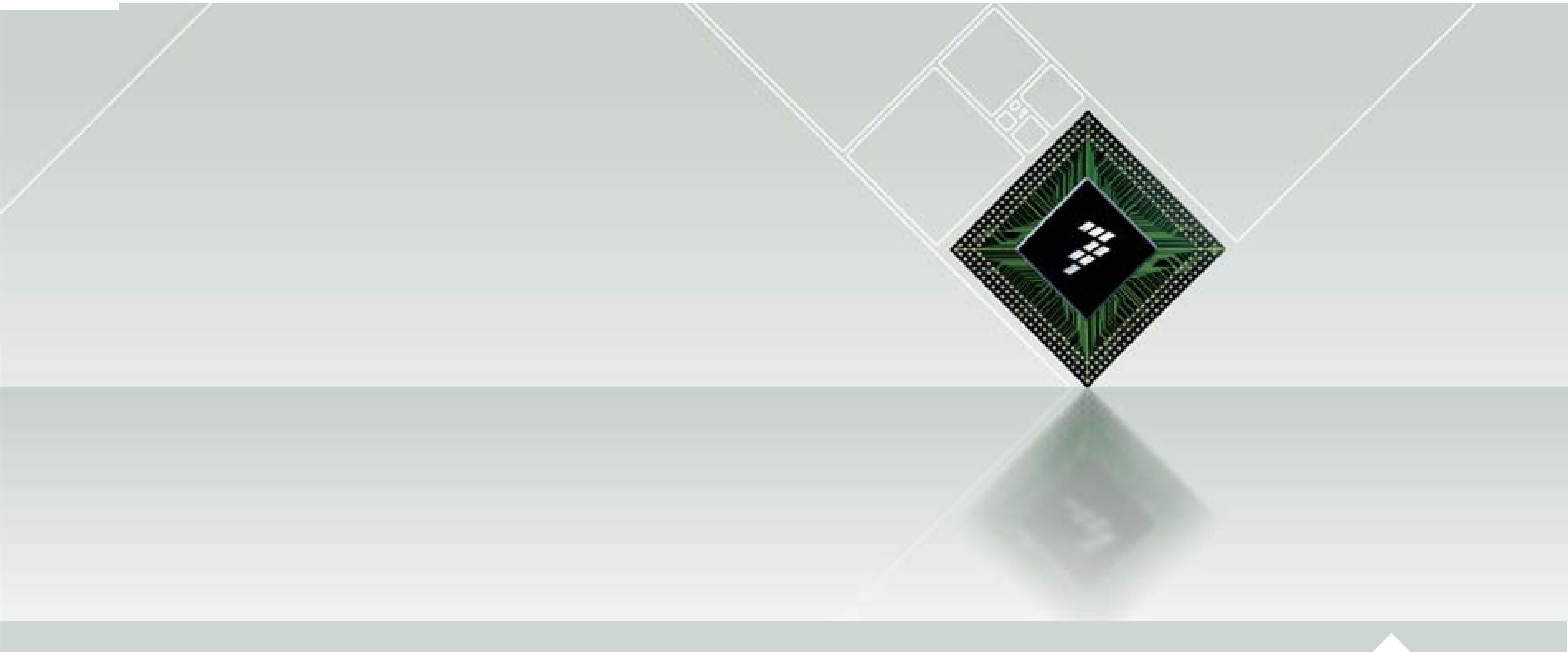

Packet I/O

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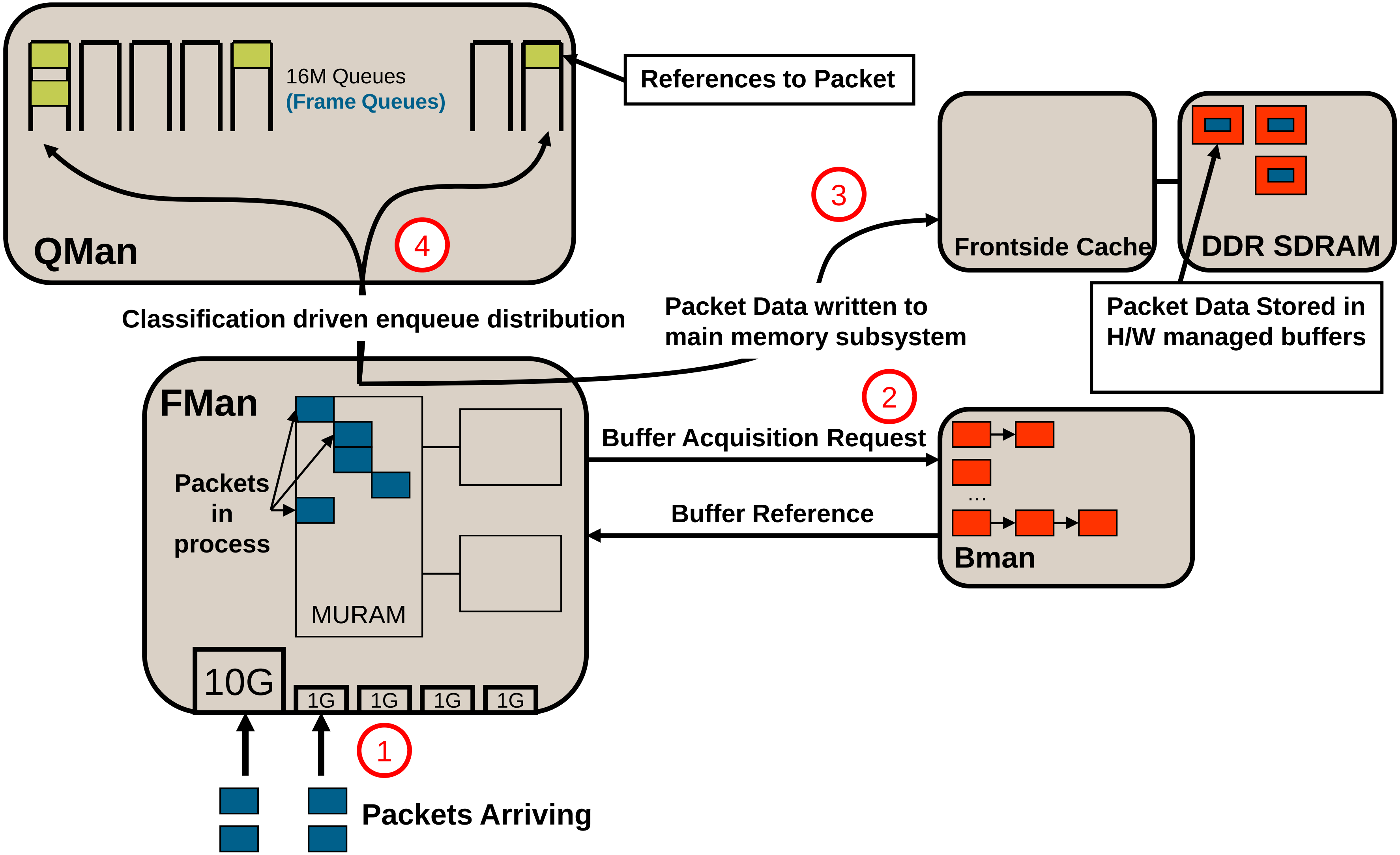
FMan/QMan Ingress Packet Processing


16M Queues
(Frame Queues)
QMan
4
References to Packet
3
Frontside Cache
DDR SDRAM
Classification driven enqueue distribution
Packet Data written to main memory subsystem
Packet Data Stored in H/W managed buffers
2
FMan
Packets in process
MURAM
Buffer Acquisition Request
Buffer Reference
...
Bman
10G
1G
1G
1G
1G
1
Packets Arriving

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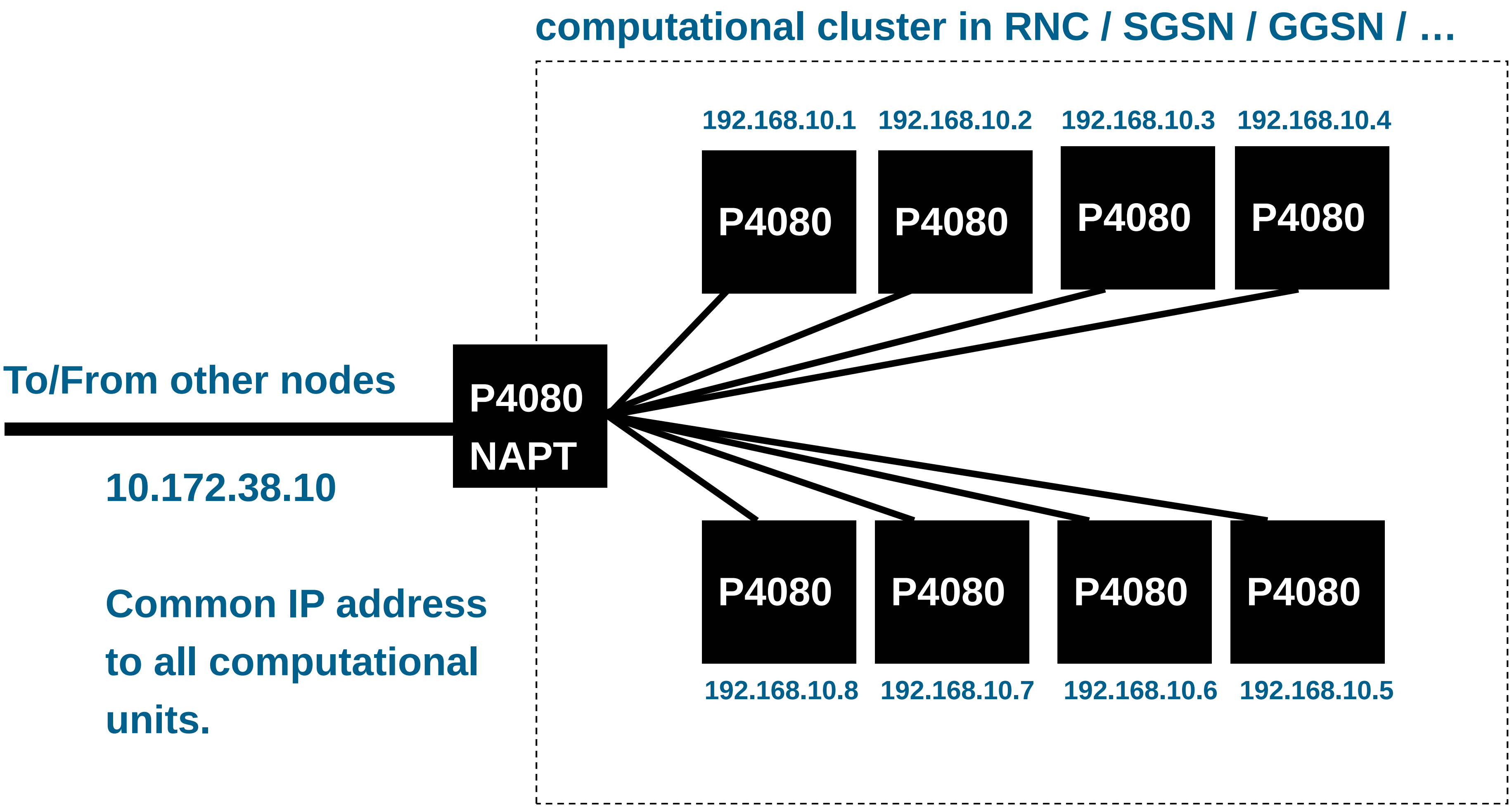
Example Location of NAPT Functionality



computational cluster in RNC / SGSN / GGSN / …

192.168.10.1 192.168.10.2 192.168.10.3 192.168.10.4

P4080 P4080 P4080 P4080

To/From other nodes

P4080
NAPT

10.172.38.10

P4080 P4080 P4080 P4080

192.168.10.8 192.168.10.7 192.168.10.6 192.168.10.5

Common IP address to all computational units.

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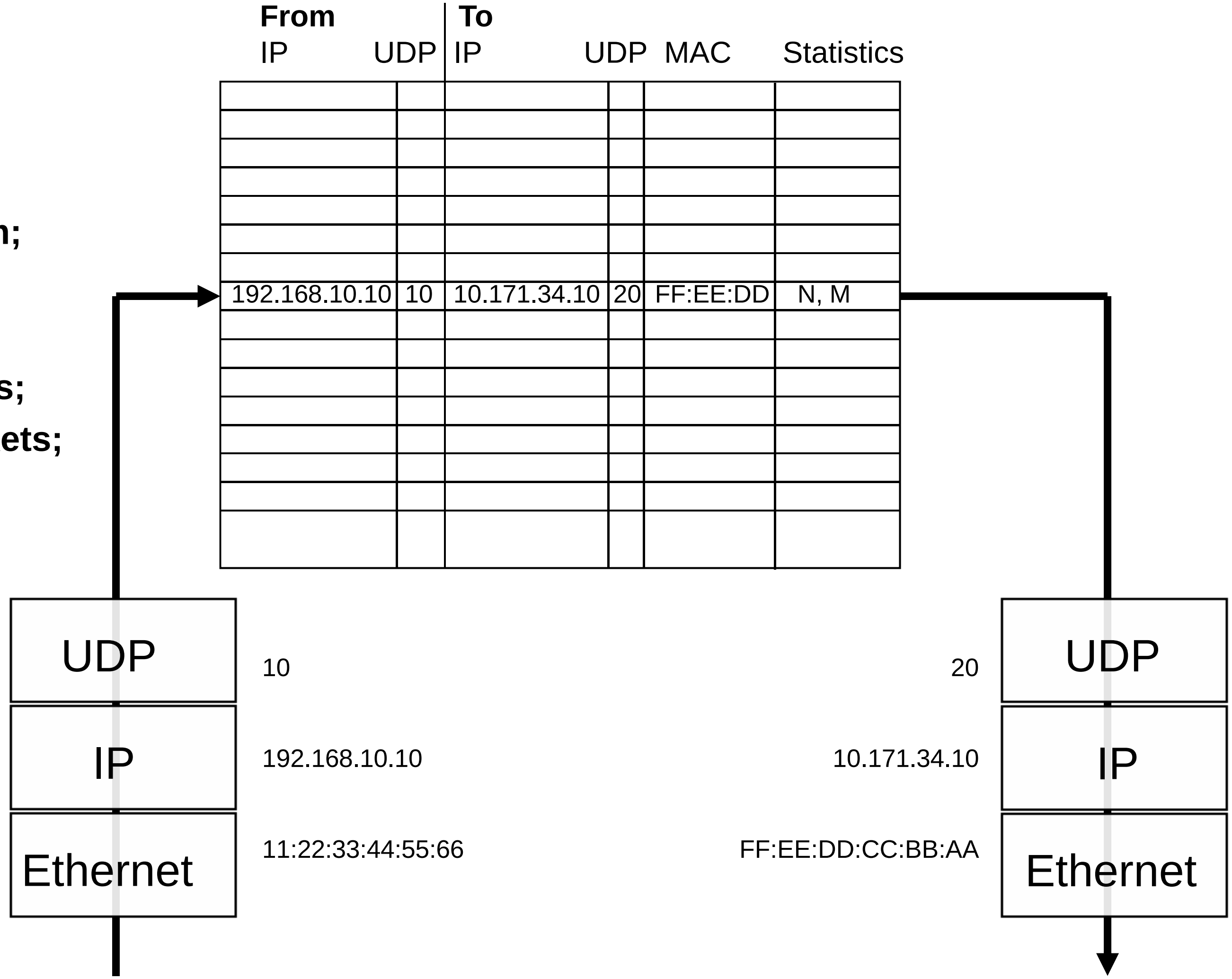
NAPT Basic Principle

```
typedef struct SHLL_node
{
SHLL_node                *Next;
uint32_t                 IpFrom;
uint32_t                 IpTo;
uint16_t                 PortFrom;
uint16_t                 PortTo;
union mac_address_t EthTo;
uint64_t                 StatBytes;
uint64_t                 StatPackets;
}
```



From		To			
IP	UDP	IP	UDP	MAC	Statistics
192.168.10.10	10	10.171.34.10	20	FF:EE:DD	N, M

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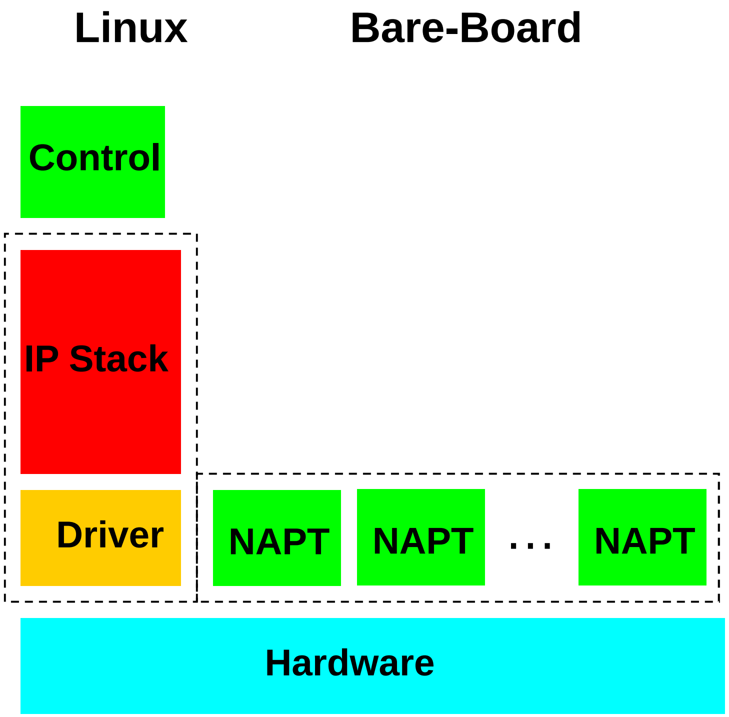
System Configuration: Linux® OS and Bare-metal

- Demo implementation based on separated slow- and fastpath

- Linux running on 1 core with control software on top

- 7 cores bare-metal application processing packets

- Hypervisor protects the partitions from each other



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Core / Accelerator Partition

- Frame Manager Ingress
  1. Buffer allocation in DDR
  2. Parser / classification / policing
  3. IP checksum
  4. UDP checksum
  5. Enqueue to core

Accelerator

- Software
  6. Dequeue from Frame Manager
  7. Translation lookup
  8. Enqueue to Frame Manager

Core

- Frame Manager Egress
  9. Dequeue from core
  10. Add UDP checksum
  11. Add IP checksum
  12. Buffer deallocation from DDR

Accelerator

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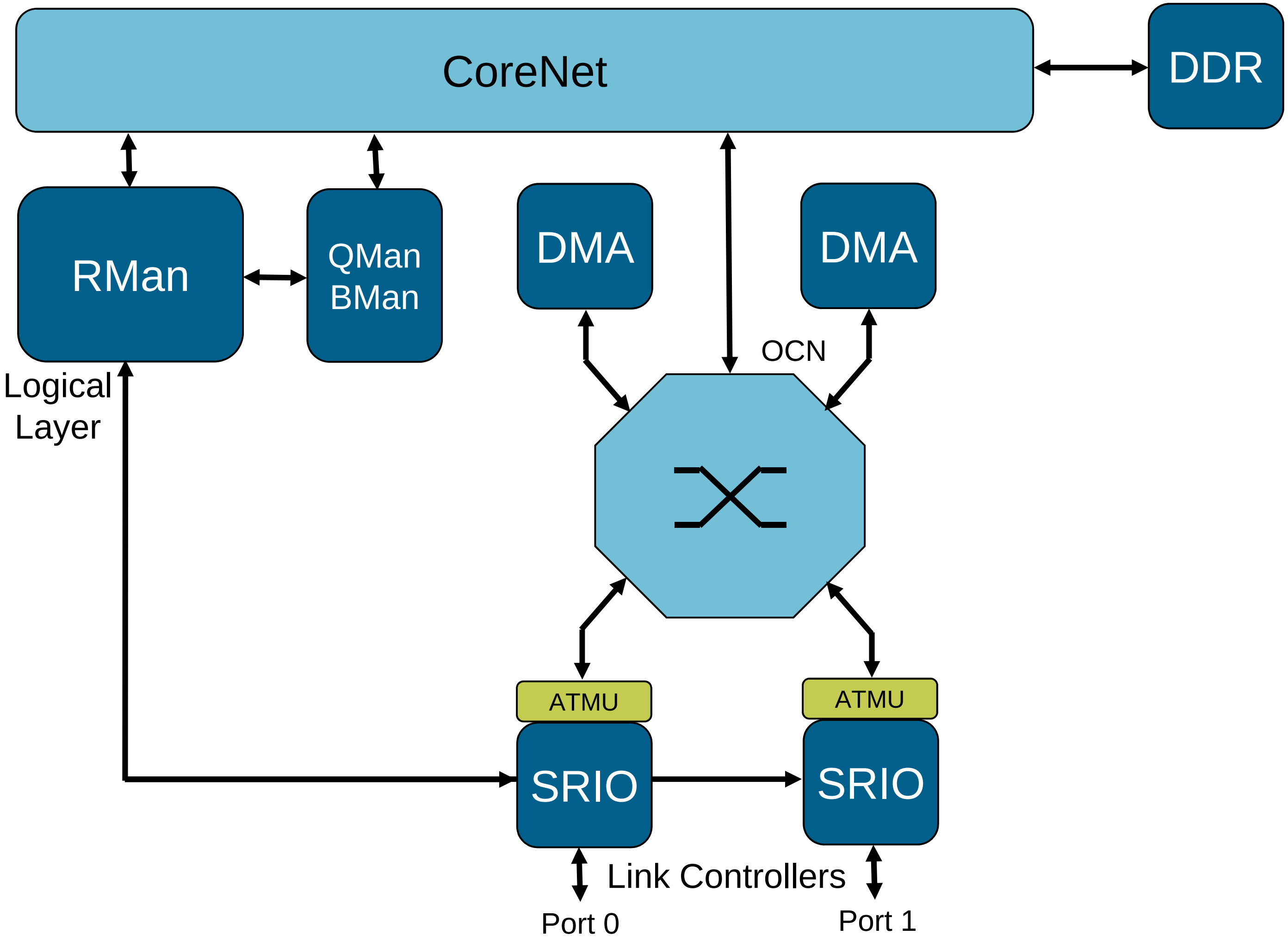
RMan Datapath



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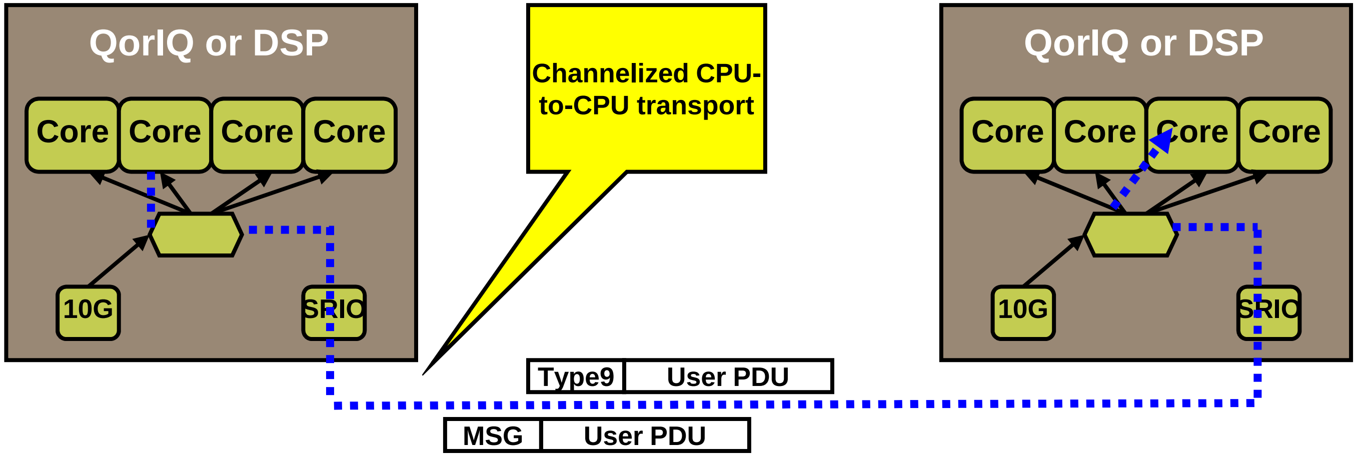
RMan for QorIQ: Greater Performance and Functionality

- Many queues allow multiple inbound/outbound queues per core
  - Hardware queue management via QorIQ Datapath Architecture (DPAA)
- Supports all messaging-style transaction types
  - Type 11 Messaging
  - Type 10 Doorbells
  - Type 9 Data Streaming
- Enables low overhead direct core-to-core communication

Device-to-Device Transport



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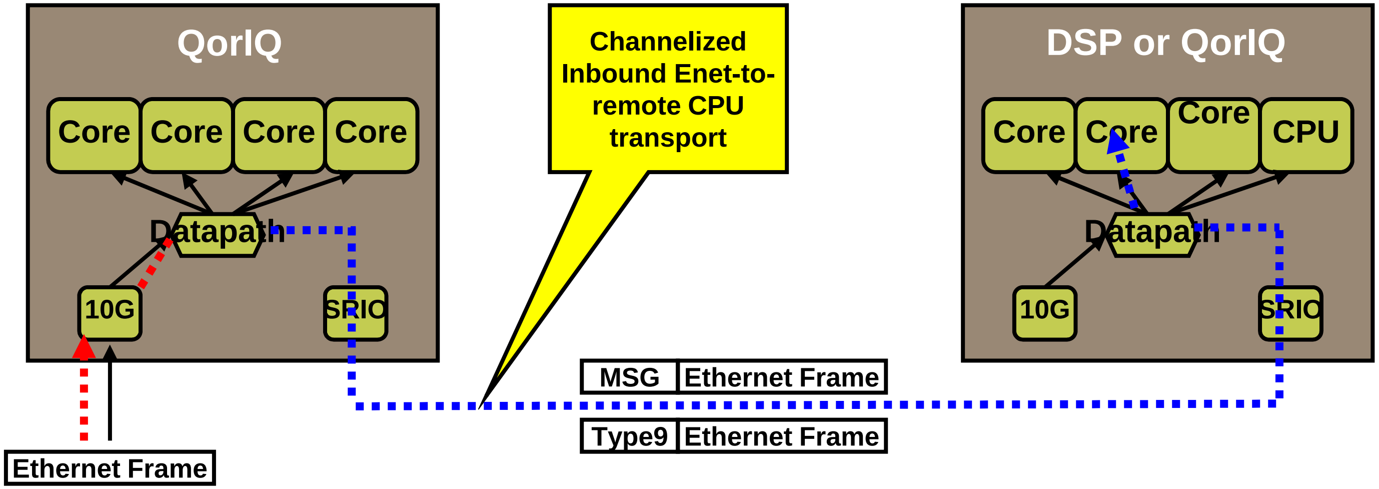
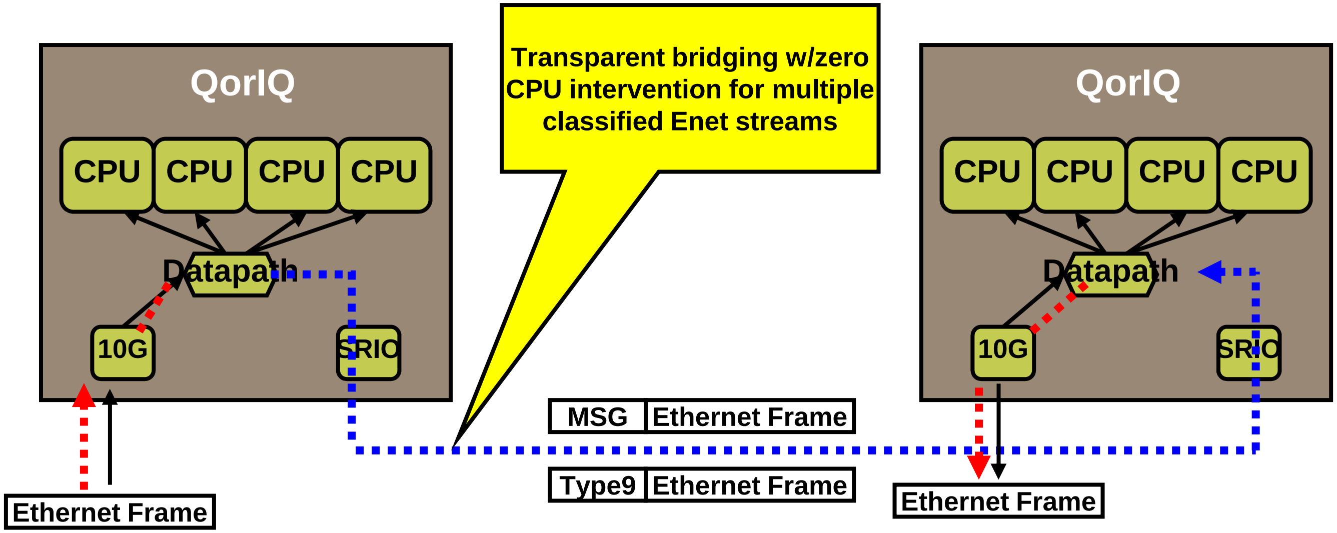
RMan Enables New Zero-CPU Overhead Use Models

Scalable Multicore System



Channelized Inbound Enet-to-remote CPU transport

Ethernet Bridging



Transparent bridging w/zero CPU intervention for multiple classified Enet streams

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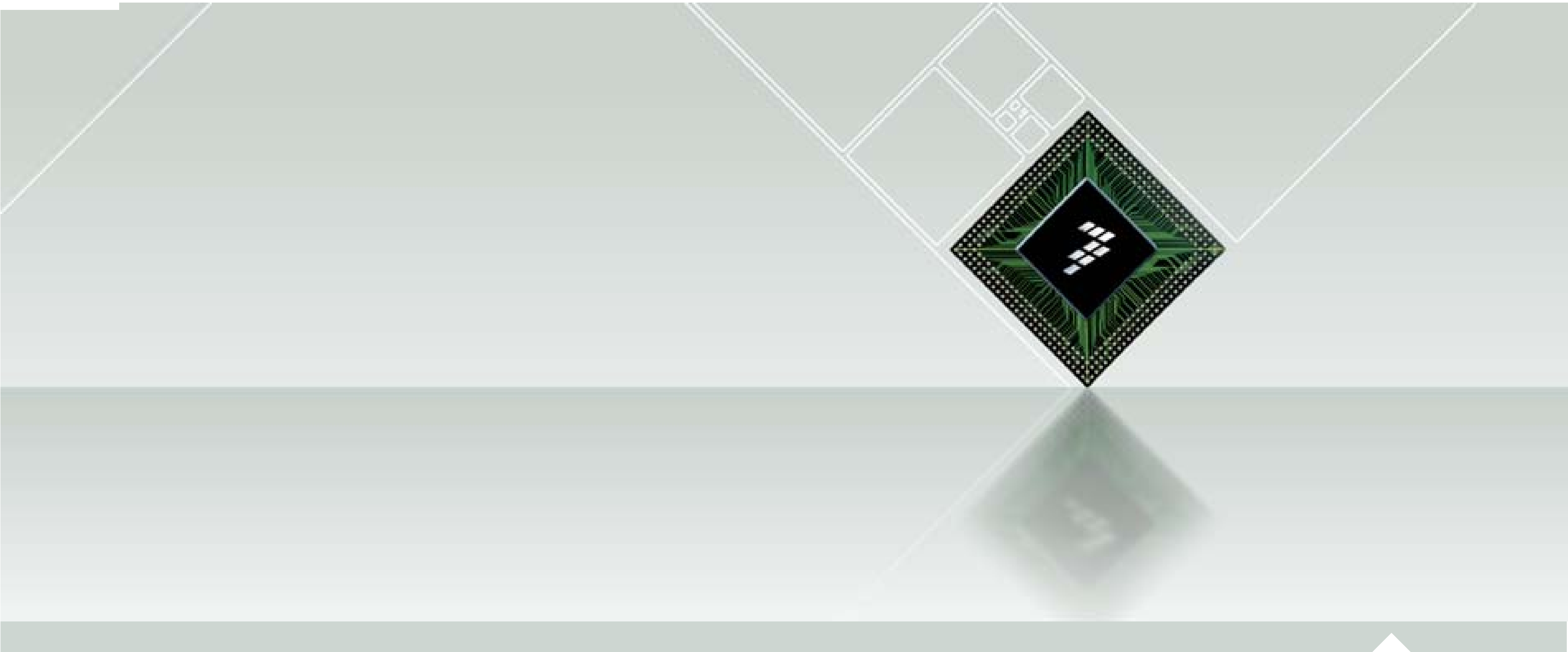

PME: Traffic Monitoring and Management

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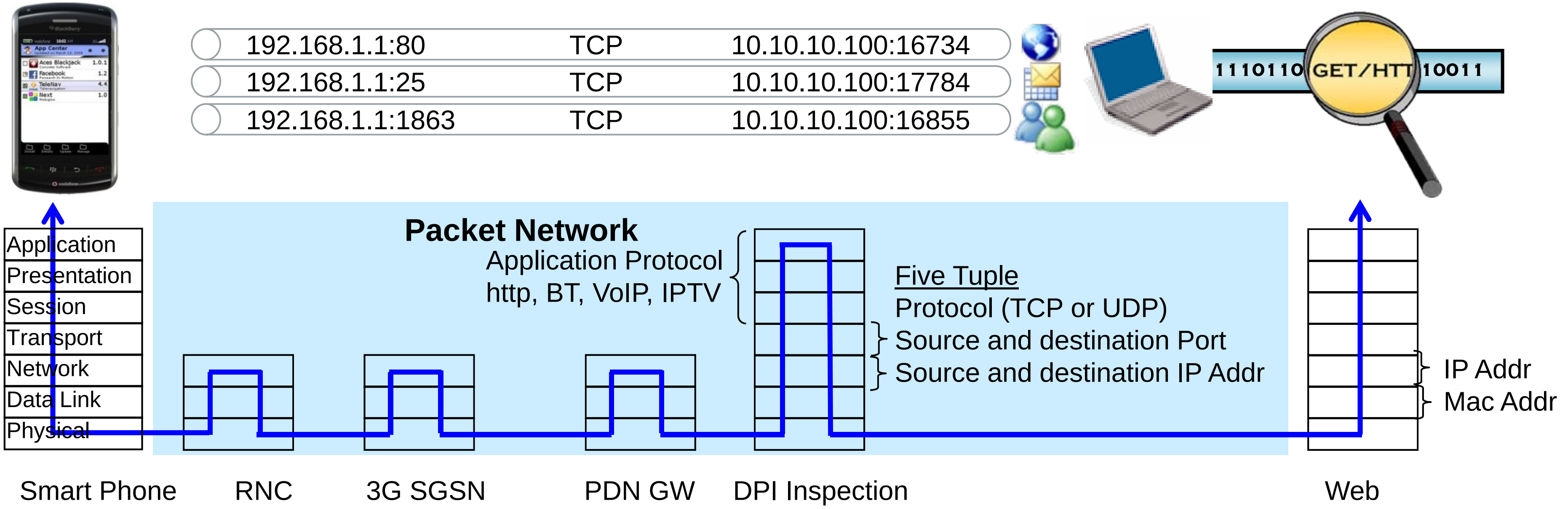
Deploy Deep Packet Inspection and Policy Control

- DPI enables companies to:
  - Understand the network traffic and pattern
  - Gather business intelligence
  - Identify trends and adapt to those trends
- Policy Control enables:
  - A smarter pipe requires fine-tuned network controls
  - Control and manage growing usage
  - Fair usage to all network users



192.168.1.1:80	TCP	10.10.10.100:16734
192.168.1.1:25	TCP	10.10.10.100:17784
192.168.1.1:1863	TCP	10.10.10.100:16855

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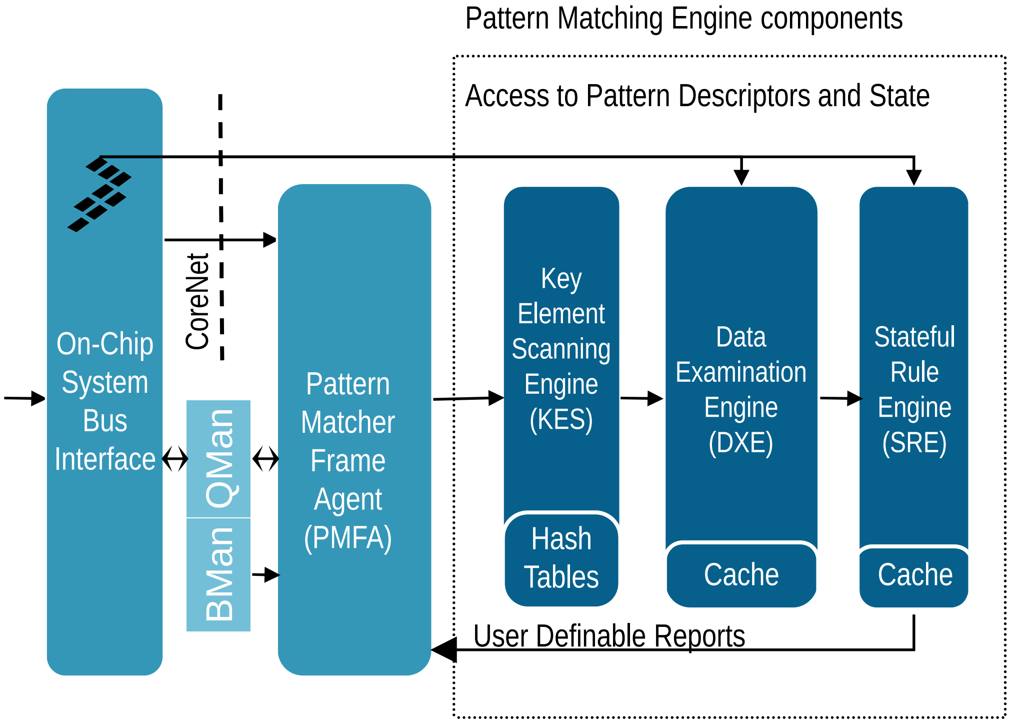
Policy Control: DPI with Pattern Matcher

- Regex support plus significant extensions:
  - Patterns can be split into 256 sets each of which can contain 16 subsets
  - 32K patterns of up to 128B length
  - 9.6 Gbps raw performance
- Combined hash/NFA technology
  - No “explosion” in number of patterns due to wildcards
  - Low system memory utilization
  - Fast pattern database compiles and incremental updates
- Stateful rules operate on a per session basis
  - User-defined logic reacts to pattern matches detected by the DXE
  - Can be used to further qualify the pattern match
  - Protocol state tracking (e.g. track the “normal” transitions of SMTP)



Pattern Matching Engine components
Access to Pattern Descriptors and State
On-Chip System Bus Interface
CoreNet
QMan
BMan
Pattern Matcher Frame Agent (PMFA)
Key Element Scanning Engine (KES)
Hash Tables
Data Examination Engine (DXE)
Cache
Stateful Rule Engine (SRE)
Cache
User Definable Reports

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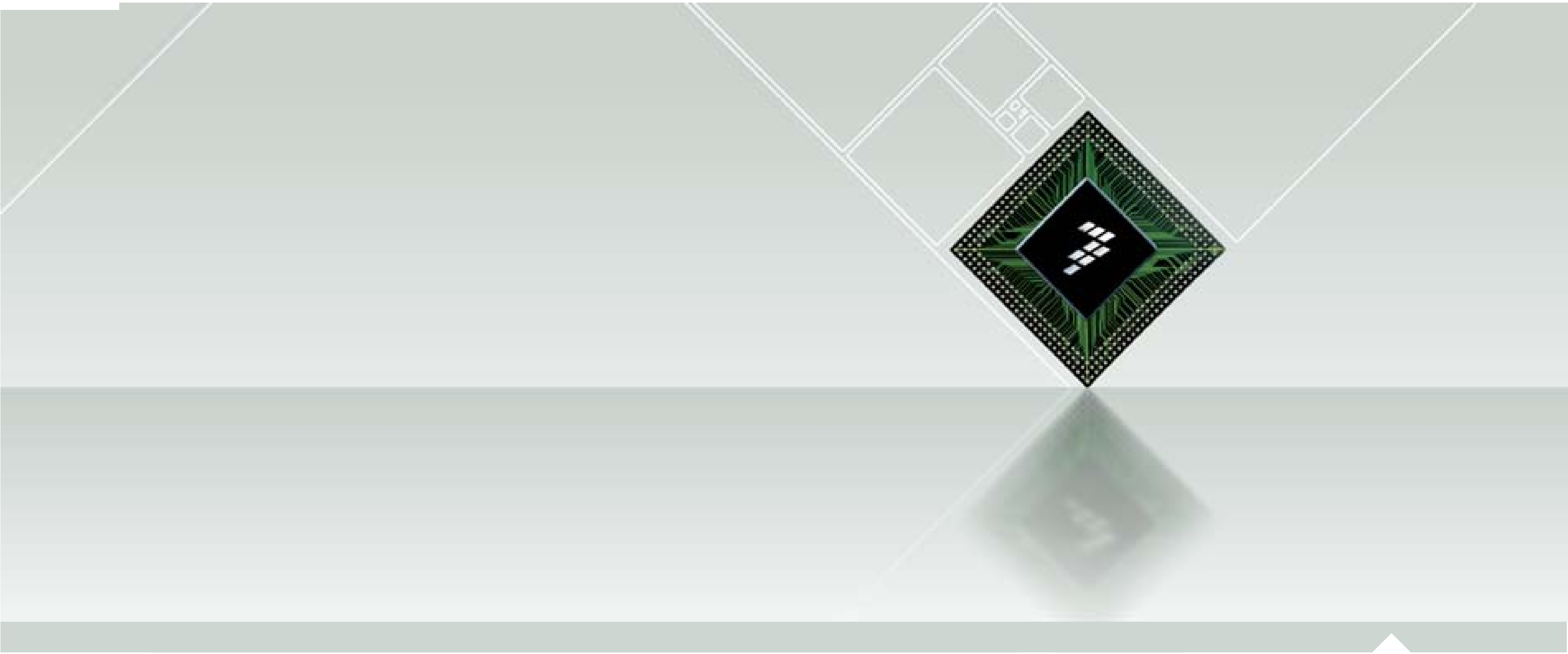

SEC: Ciphering and Packet Formatting

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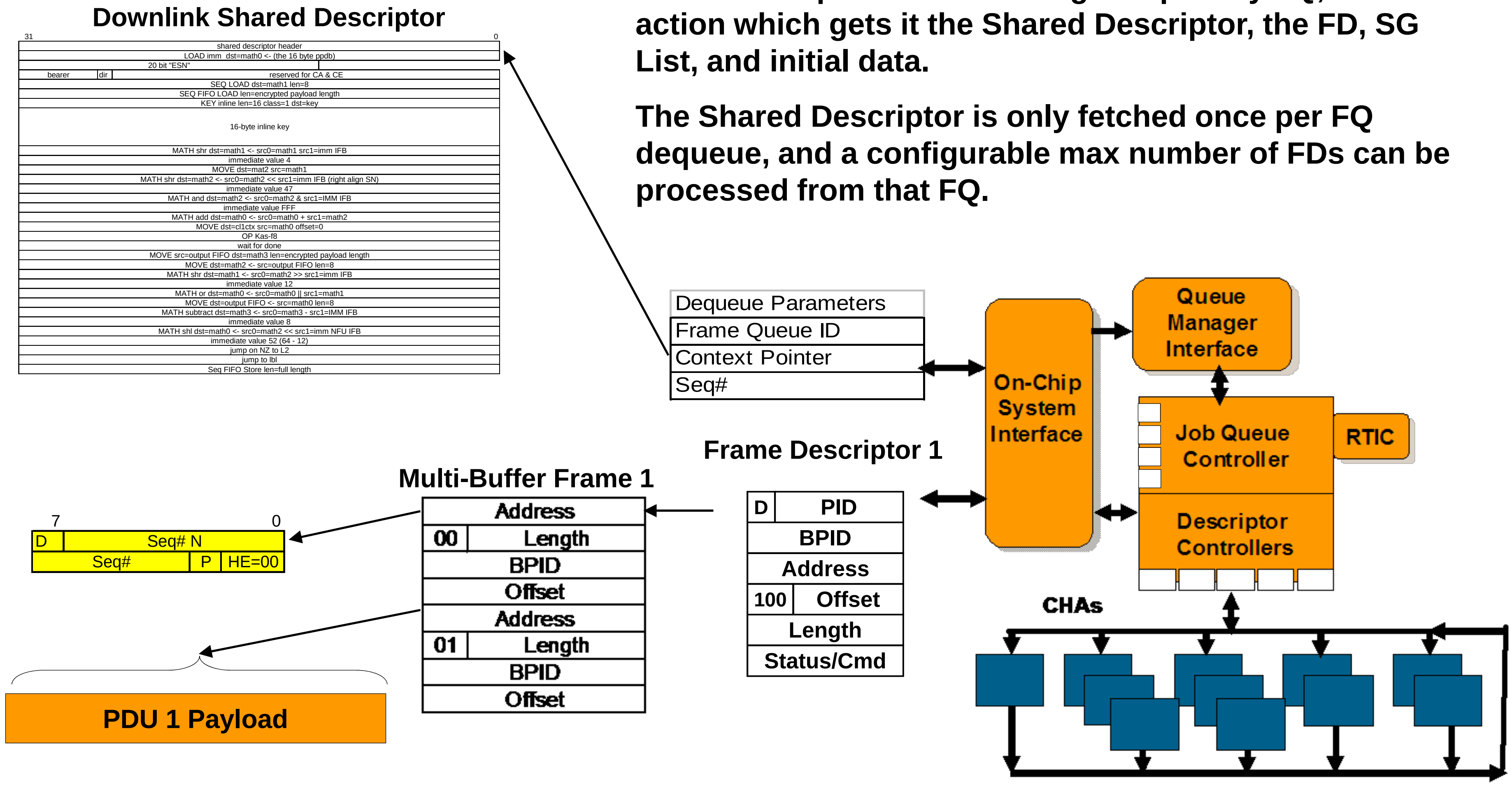
P4080 RLC AM Downlink Processing

The SEC dequeues from its highest priority FQ, an action which gets it the Shared Descriptor, the FD, SG List, and initial data.

The Shared Descriptor is only fetched once per FQ dequeue, and a configurable max number of FDs can be processed from that FQ.



Downlink Shared Descriptor

31		0
shared descriptor header		
LOAD imm dst=math0 <- (the 16 byte ppdb)		
20 bit "ESN"		
bearer	dir	reserved for CA & CE
SEQ LOAD dst=math1 len=8		
SEQ FIFO LOAD len=encrypted payload length		
KEY inline len=16 class=1 dst=key		
16-byte inline key		
MATH shr dst=math1 <- src0=math1 src1=imm IFB		
immediate value 4		
MOVE dst=mat2 src=math1		
MATH shr dst=math2 <- src0=math2 << src1=imm IFB (right align SN)		
immediate value 47		
MATH and dst=math2 <- src0=math2 & src1=IMM IFB		
immediate value FFF		
MATH add dst=math0 <- src0=math0 + src1=math2		
MOVE dst=cl1ctx src=math0 offset=0		
OP Kas-f8		
wait for done		
MOVE src=output FIFO dst=math3 len=encrypted payload length		
MOVE dst=math2 <- src=output FIFO len=8		
MATH shr dst=math1 <- src0=math2 >> src1=imm IFB		
immediate value 12		
MATH or dst=math0 <- src0=math0 || src1=math1		
MOVE dst=output FIFO <- src=math0 len=8		
MATH subtract dst=math3 <- src0=math3 - src1=IMM IFB		
immediate value 8		
MATH shl dst=math0 <- src0=math2 << src1=imm NFU IFB		
immediate value 52 (64 - 12)		
jump on NZ to L2		
jump to lbl		
Seq FIFO Store len=full length		

Dequeue Parameters
Frame Queue ID
Context Pointer
Seq#

Frame Descriptor 1

D	PID
BPID	
Address	
100	Offset
Length	
Status/Cmd	

Multi-Buffer Frame 1

Address	
00	Length
BPID	
Offset	
Address	
01	Length
BPID	
Offset	

7			0
D	Seq# N		
Seq#		P	HE=00

PDU 1 Payload

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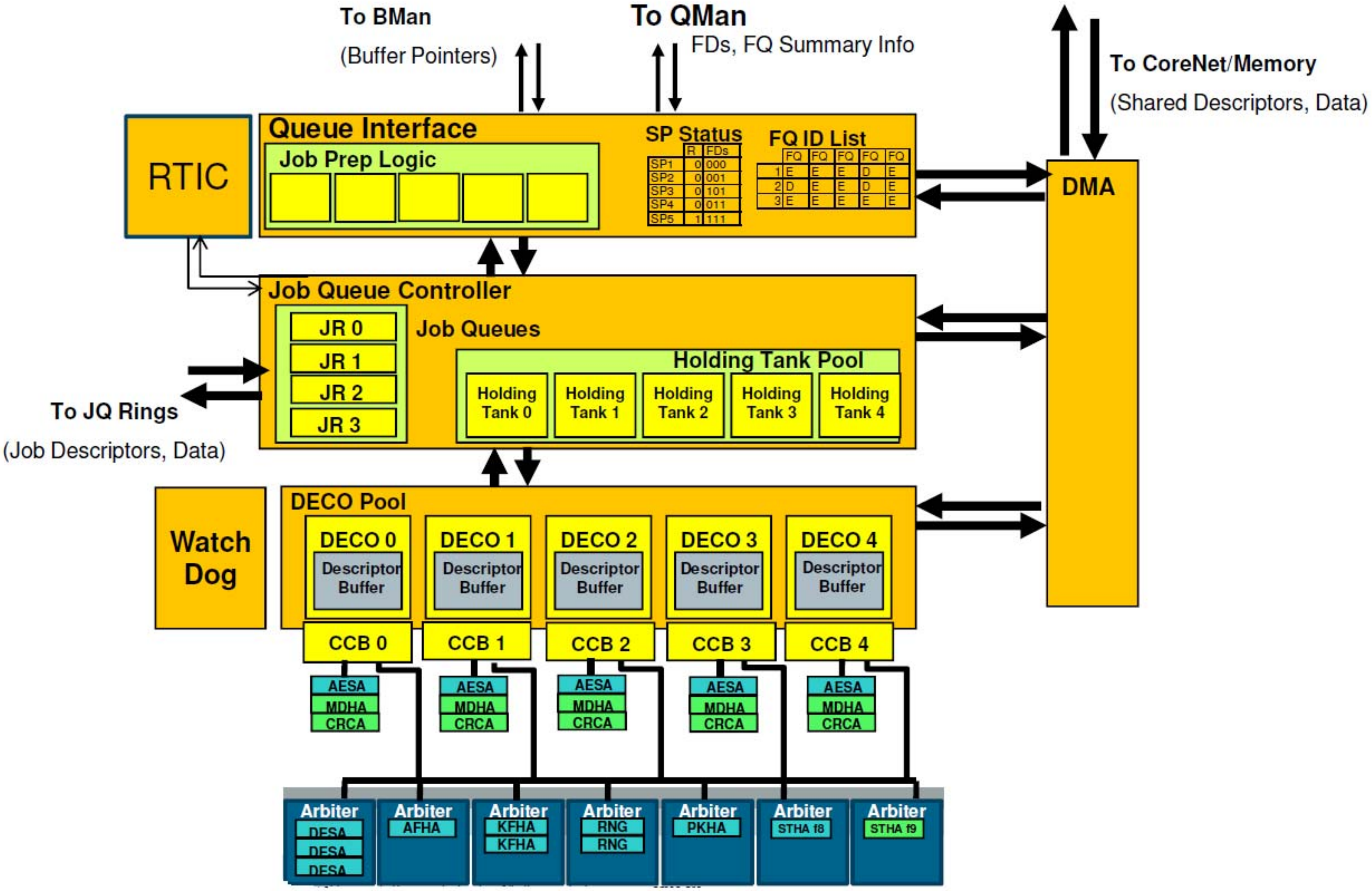
SEC 4.0 for P4080 rev2



To BMan

(Buffer Pointers)

To QMan

FDs, FQ Summary Info

To CoreNet/Memory

(Shared Descriptors, Data)

RTIC

Queue Interface

Job Prep Logic

SP Status

	R	FDs
SP1	0	000
SP2	0	001
SP3	0	101
SP4	0	011
SP5	1	111

FQ ID List

	FQ	FQ	FQ	FQ	FQ
1	E	E	E	D	E
2	D	E	E	D	E
3	E	E	E	E	E

DMA

Job Queue Controller

JR 0

JR 1

JR 2

JR 3

Job Queues

Holding Tank Pool

Holding Tank 0

Holding Tank 1

Holding Tank 2

Holding Tank 3

Holding Tank 4

To JQ Rings

(Job Descriptors, Data)

Watch Dog

DECO Pool

DECO 0

Descriptor Buffer

DECO 1

Descriptor Buffer

DECO 2

Descriptor Buffer

DECO 3

Descriptor Buffer

DECO 4

Descriptor Buffer

CCB 0

CCB 1

CCB 2

CCB 3

CCB 4

AESA MDHA CRCA

AESA MDHA CRCA

AESA MDHA CRCA

AESA MDHA CRCA

AESA MDHA CRCA

Arbiter DESA DESA DESA

Arbiter AFHA

Arbiter KFHA KFHA

Arbiter RNG RNG

Arbiter PKHA

Arbiter STHA f8

Arbiter STHA f9

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DECO Commands

- Load Commands:
  - [SEQ] KEY – Load cipher keys
  - [SEQ] LOAD – Load register
  - [SEQ] FIFO LOAD – Loads In/Out FIFO
- Store Commands:
  - [SEQ] STORE – Store register
  - [SEQ] FIFO STORE – Store In/Out FIFO
- MOVE – Move data between SEC registers.
- MATH – Perform arithmetic operation (sum, and, or, xor, bitshift, …)
- OPERATION – Execute cipher operation (Kasumi, Snow, AES, …)
- JUMP – Branch in the descriptor
- SEQ IN/OUT PTR – Sets pointer for in/out sequence data.
- JD/SD HEADER – First word in the descriptor.
- SIGNATURE – Last word in trusted descriptor.

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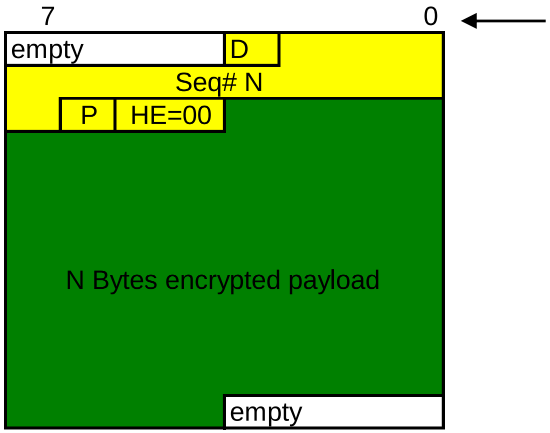
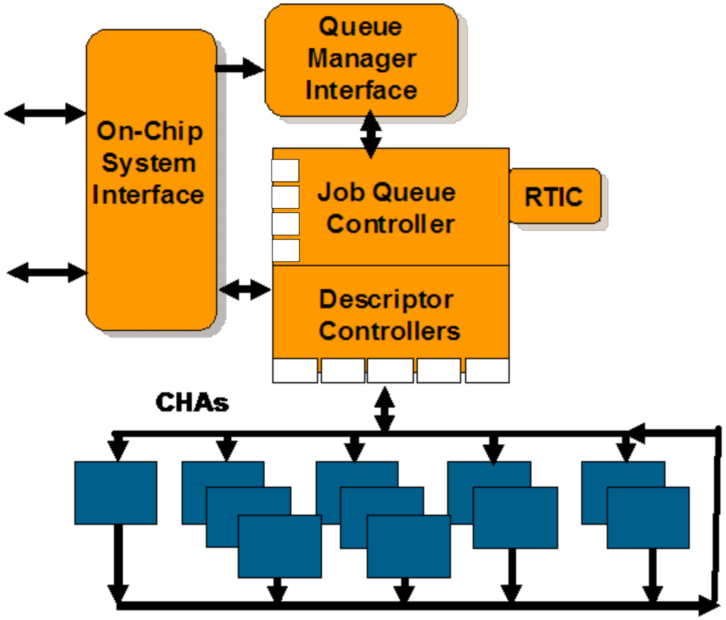
P4080 RLC AM Downlink Processing

An output Frame Descriptor is sent out from the SEC that in turn points to the generated output data. Input data is either left in memory but can also be freed and the buffer returned to BMan.



Output Frame Descriptor 1

D	PID
BPID	
Address	
000	Offset
Length	
Status/Cmd	



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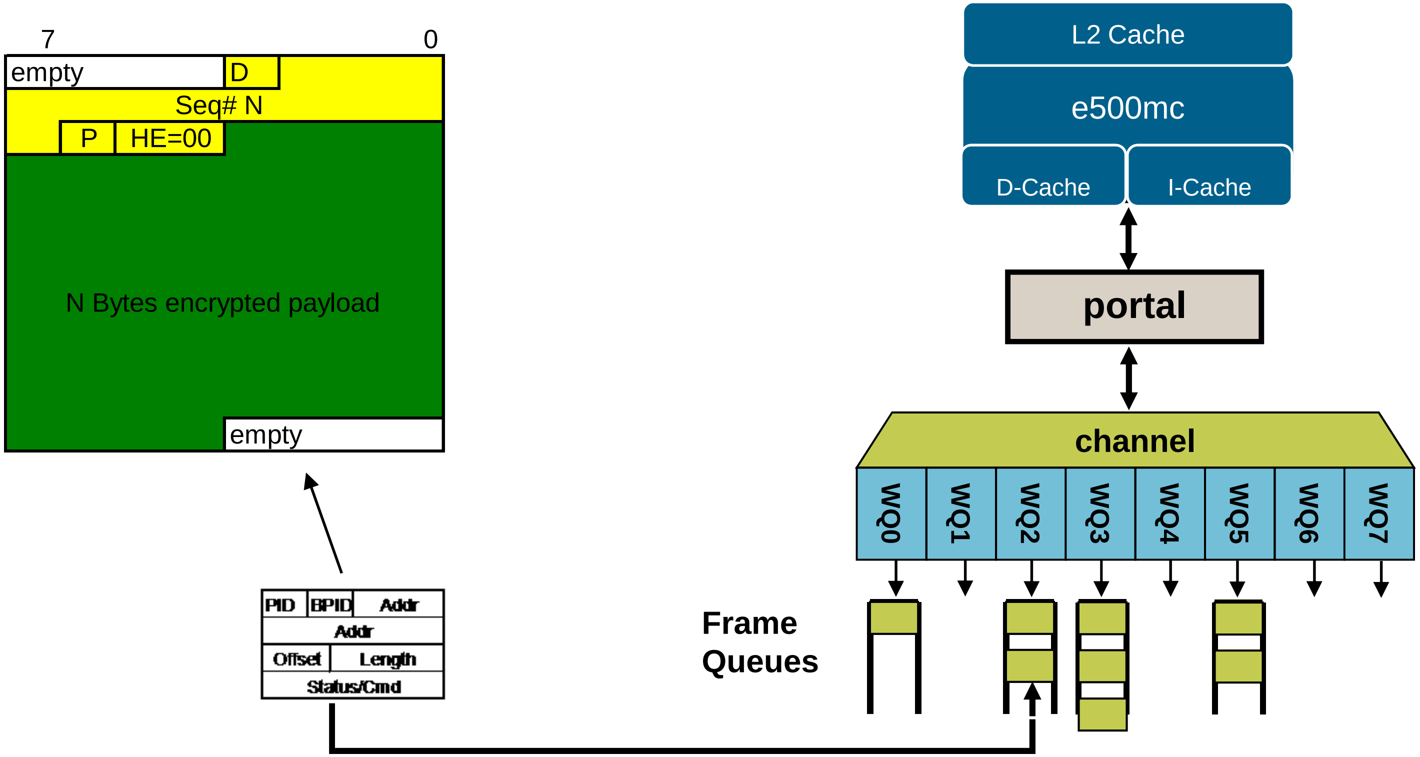
P4080 RLC AM Downlink Processing

The frame descriptors is enqueued into a work queue / channel back to a core for further processing.



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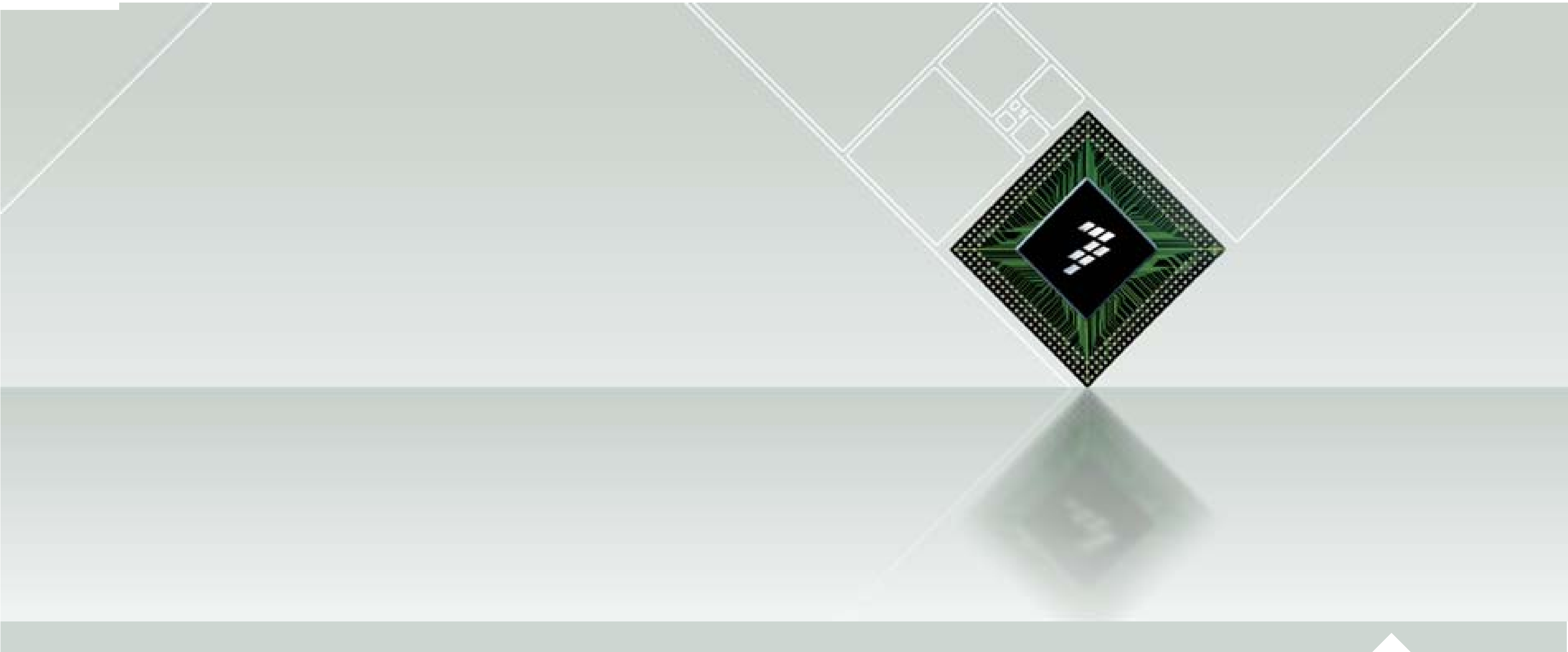

Use Case: Voice Packet Processing

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Challenge: Voice Packets

- Voice Packets are ciphered/formatted in RNC (3G) and (e)NB (LTE and 3G flat architecture).

- Voice packets are large to the number but small to the size (~20 bytes).

- Typically each active flow has a packet per ~20ms, i.e. it is not possible to group packets of same flow or latency will increase and phone conversation will not work (lag severely).

- Hardware Acceleration is a big benefit but overhead/byte of sending to accelerator has been a big problem since packets are so small.

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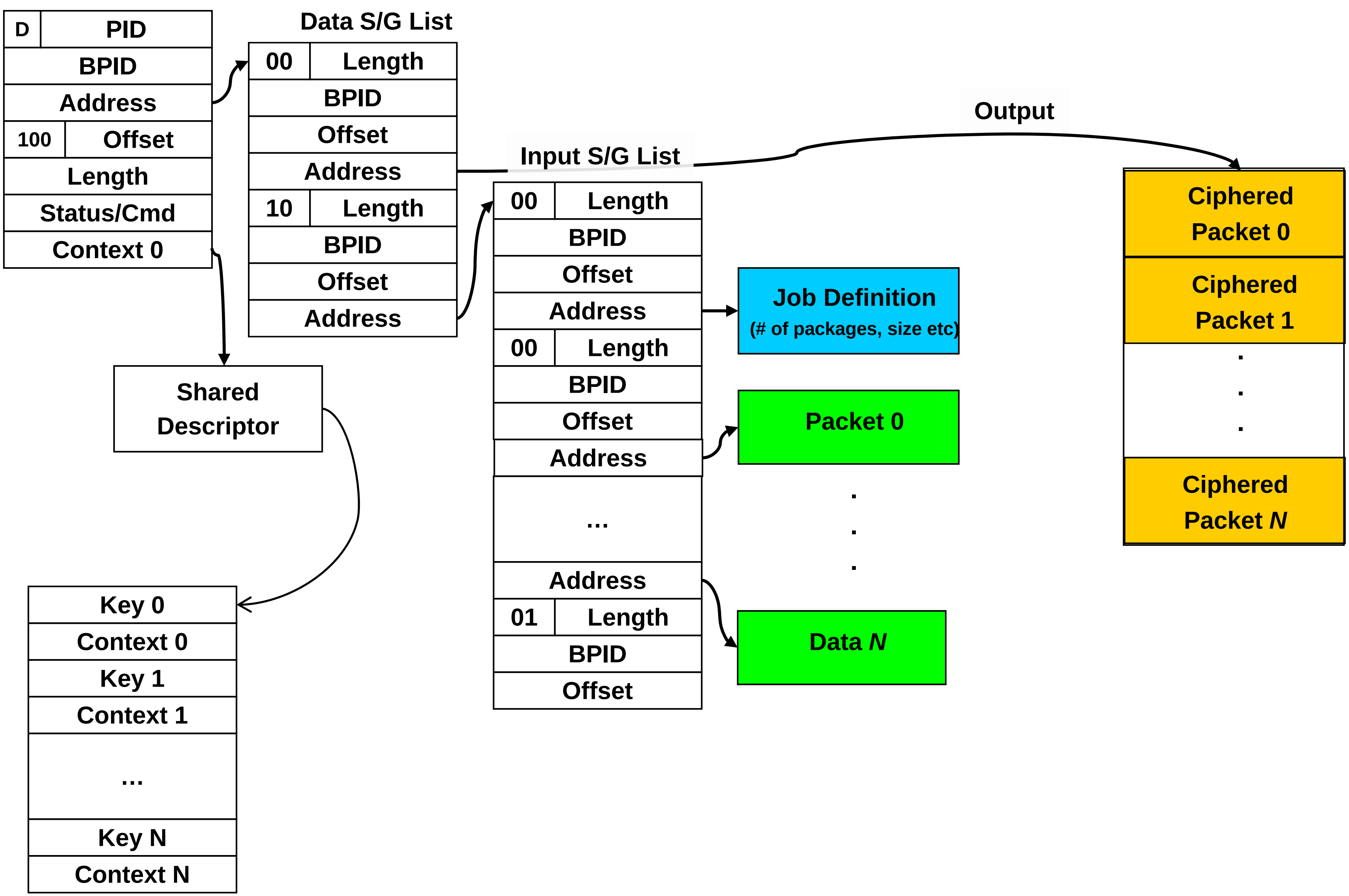
Per Flow Ciphering



Frame Descriptor

D	PID
BPID	
Address	
100	Offset
Length	
Status/Cmd	
Context 0	

Data S/G List

00	Length
BPID	
Offset	
Address	
10	Length
BPID	
Offset	
Address	

Input S/G List

00	Length
BPID	
Offset	
Address	
00	Length
BPID	
Offset	
Address	
…	
Address	
01	Length
BPID	
Offset	

Shared Descriptor

Key 0
Context 0
Key 1
Context 1
…
Key N
Context N

Job Definition
(# of packages, size etc)

Packet 0

. . .

Data *N*

Output

Ciphered Packet 0

Ciphered Packet 1

. . .

Ciphered Packet *N*

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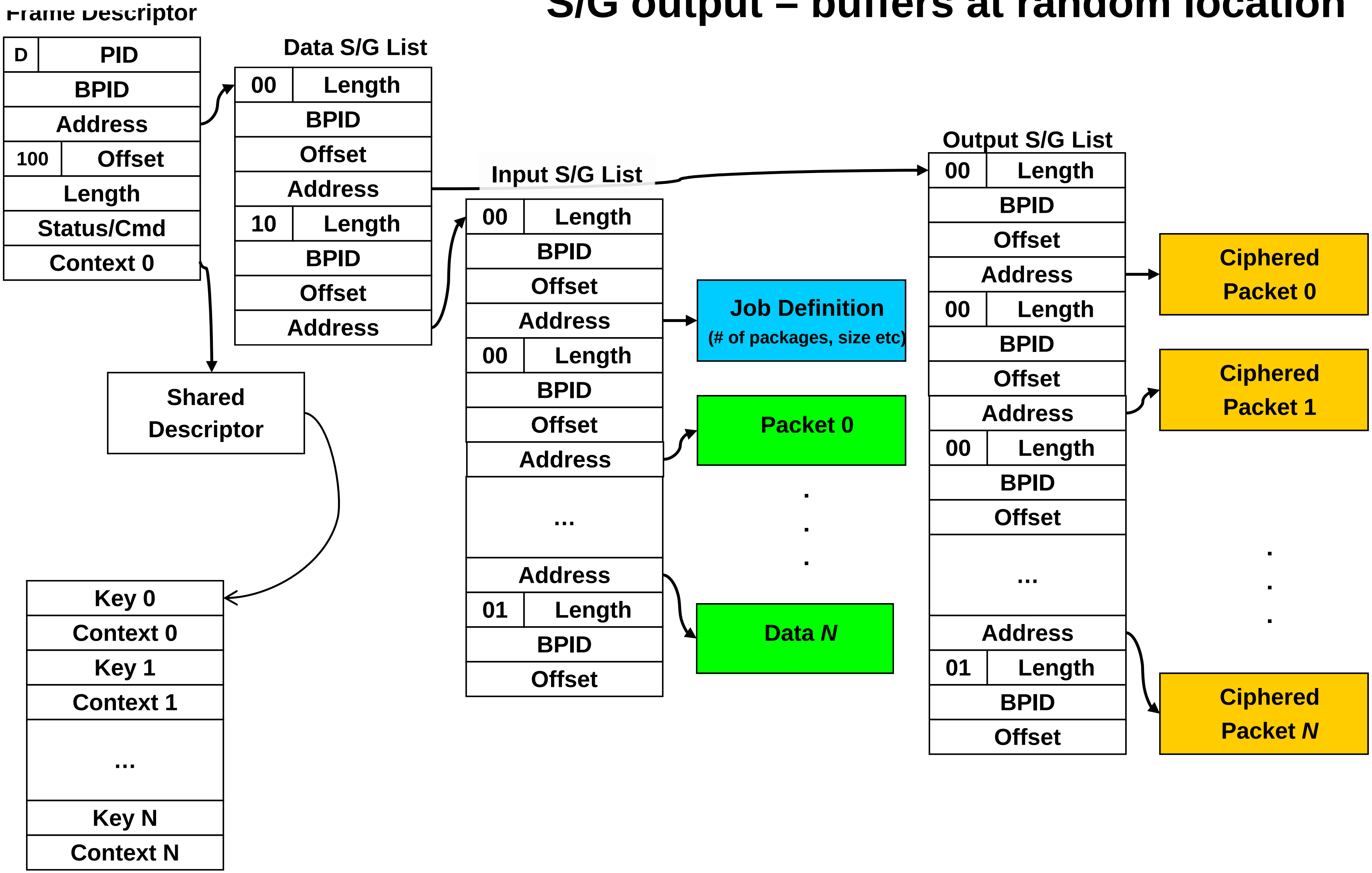
S/G output – buffers at random location



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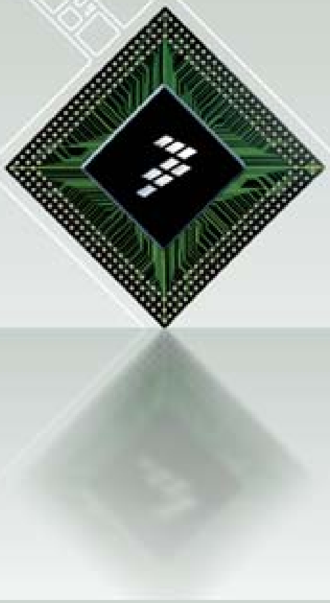

Use Case: HSPA Mobile Broadband

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Challenge: Data Packets

- Huge total bandwidth!
- Very high individual user peak rate.
- Complex protocol processing.

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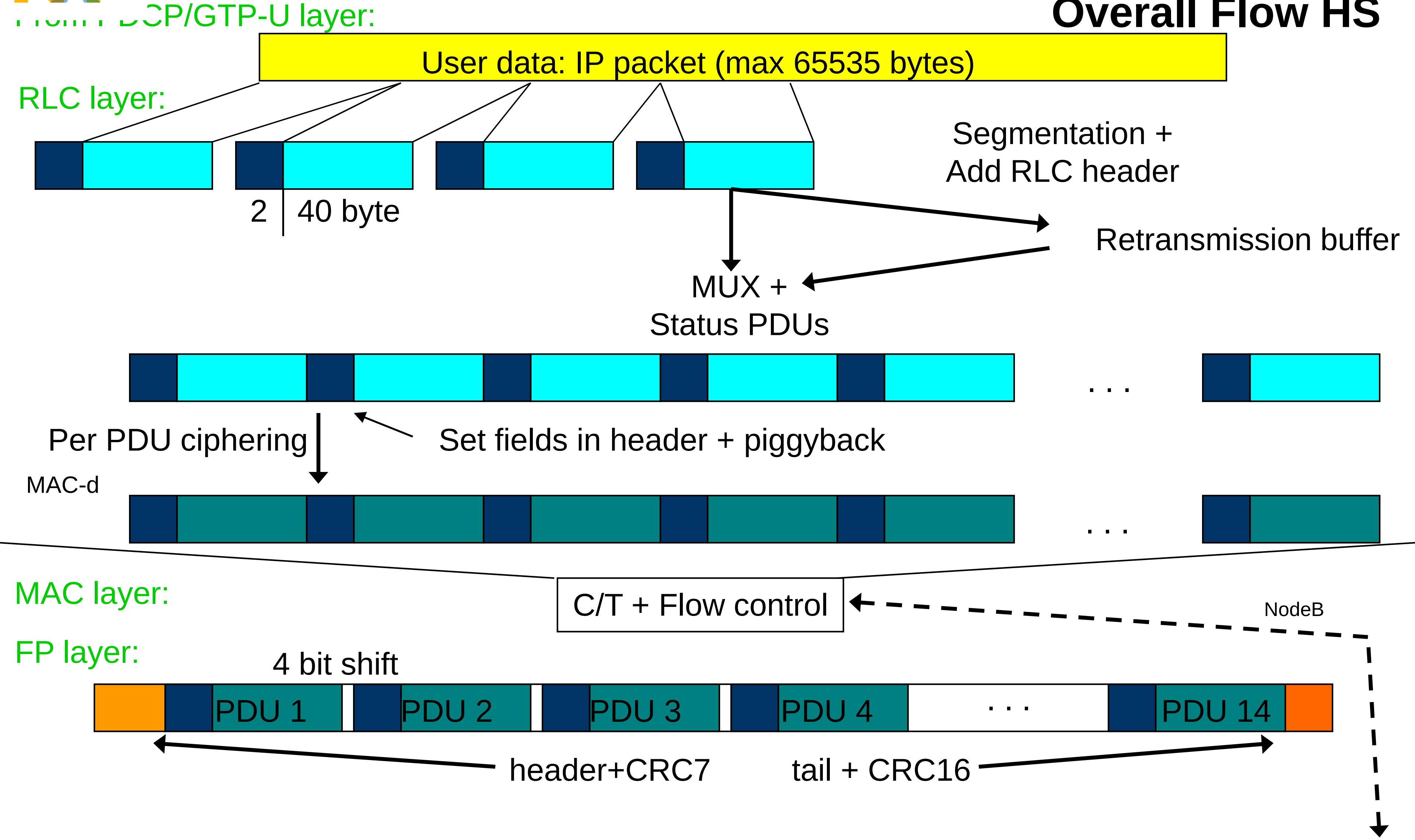
Overall Flow HS



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Frame Type 1 with MAC and RLC PDU – R7

Gray = Depends on configuration and version

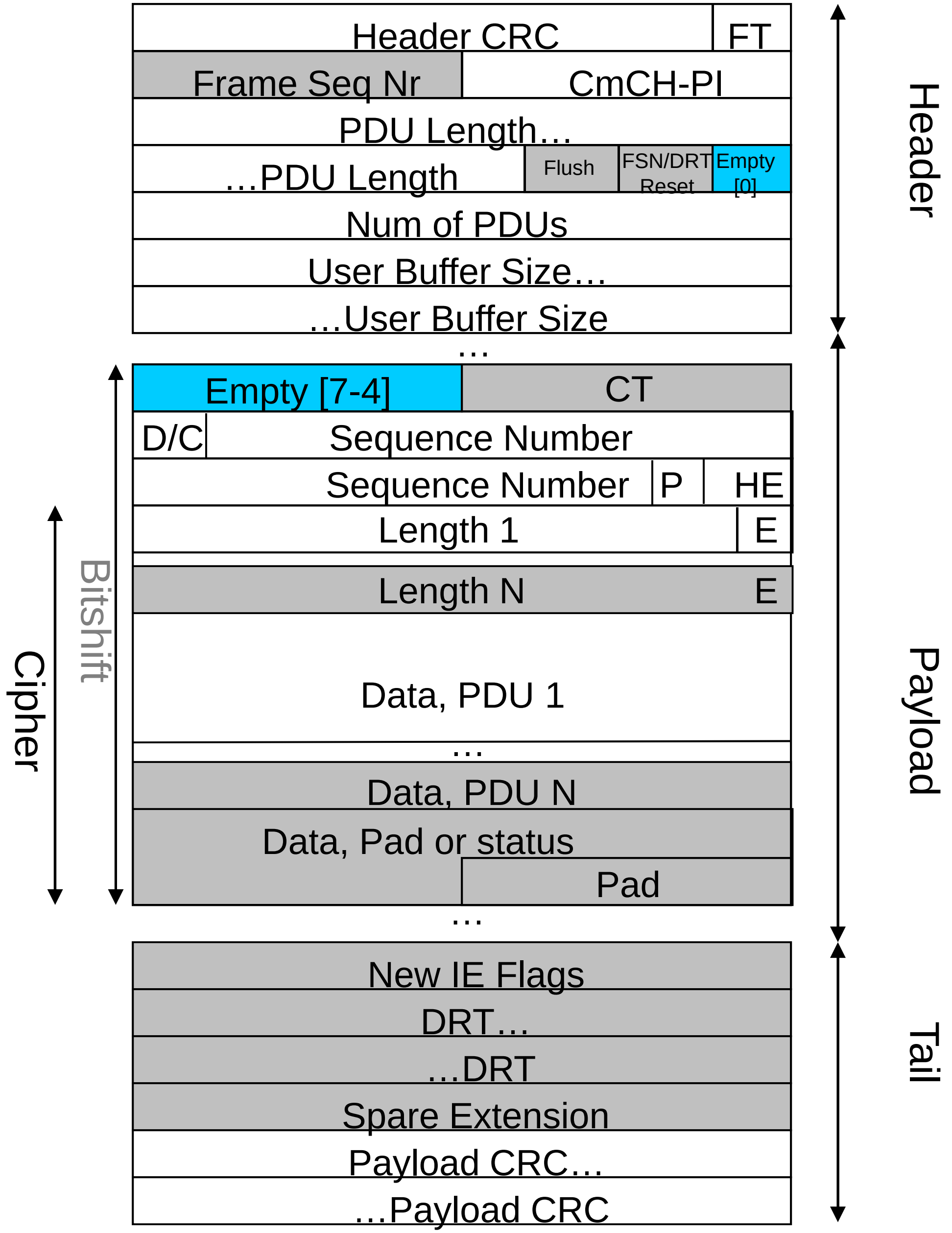
Blue = Empty

Example of special cases:

E bit can have “alternative interpretation”

HE valid values differs over revisions

Length field can be 7 or 15 bits



Header CRC | FT

Frame Seq Nr | CmCH-PI

PDU Length…

…PDU Length | Flush | FSN/DRT Reset | Empty [0]

Num of PDUs

User Buffer Size…

…User Buffer Size

…

Empty [7-4] | CT

D/C | Sequence Number

Sequence Number | P | HE

Length 1 | E

Length N | E

Data, PDU 1

…

Data, PDU N

Data, Pad or status

Pad

…

New IE Flags

DRT…

…DRT

Spare Extension

Payload CRC…

…Payload CRC

Header

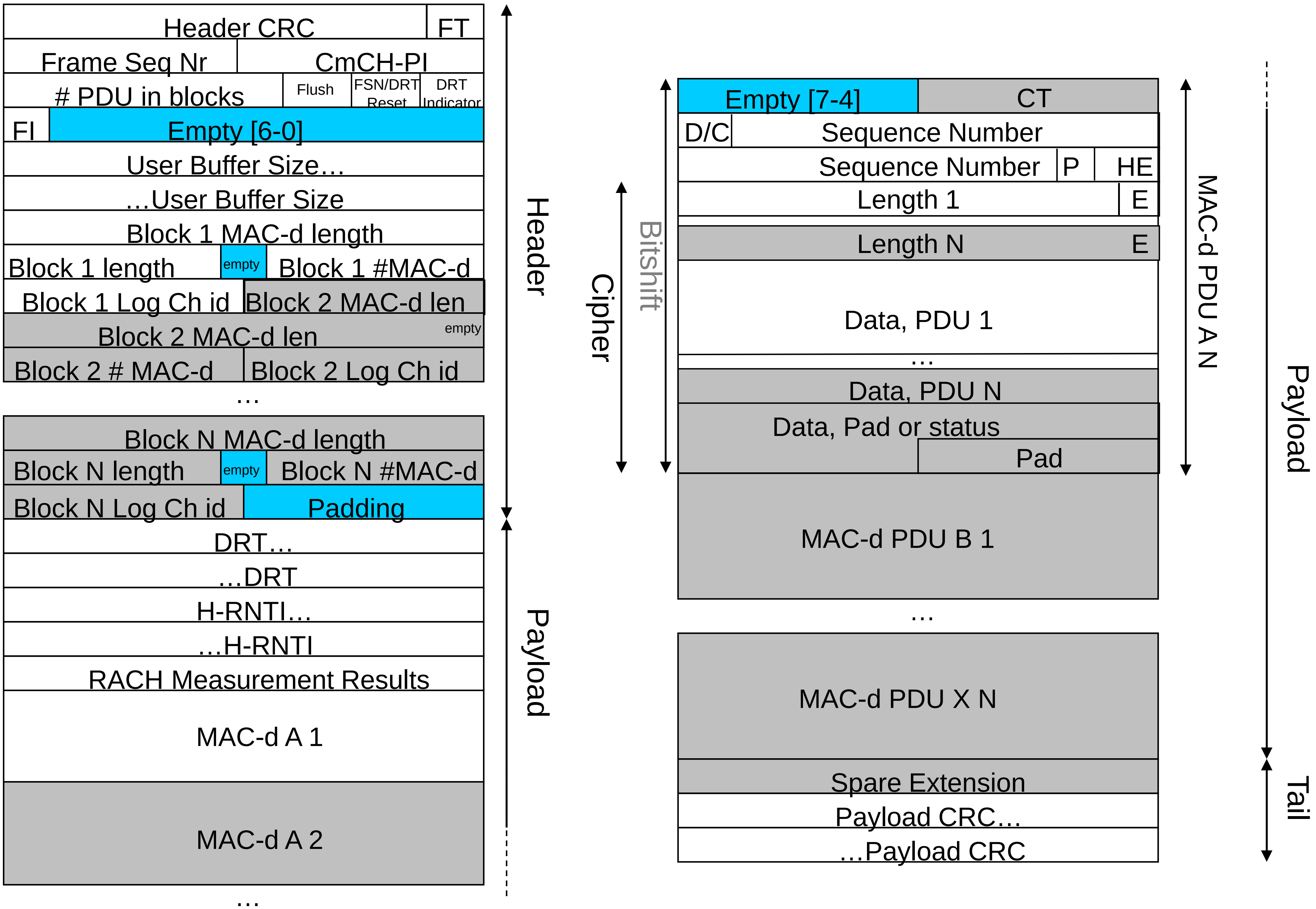
Payload

Tail

Cipher

Bitshift

Frame Type 2 with MAC and RLC PDU – R7



Header CRC | FT

Frame Seq Nr | CmCH-PI

# PDU in blocks | Flush | FSN/DRT Reset | DRT Indicator

FI | Empty [6-0]

User Buffer Size…

…User Buffer Size

Block 1 MAC-d length

Block 1 length | empty | Block 1 #MAC-d

Block 1 Log Ch id | Block 2 MAC-d len

Block 2 MAC-d len | empty

Block 2 # MAC-d | Block 2 Log Ch id

…

Block N MAC-d length

Block N length | empty | Block N #MAC-d

Block N Log Ch id | Padding

DRT…

…DRT

H-RNTI…

…H-RNTI

RACH Measurement Results

MAC-d A 1

MAC-d A 2

…

Header

Payload

Empty [7-4] | CT

D/C | Sequence Number

Sequence Number | P | HE

Length 1 | E

Length N | E

Data, PDU 1

…

Data, PDU N

Data, Pad or status

Pad

MAC-d PDU B 1

…

MAC-d PDU X N

Spare Extension

Payload CRC…

…Payload CRC

Cipher

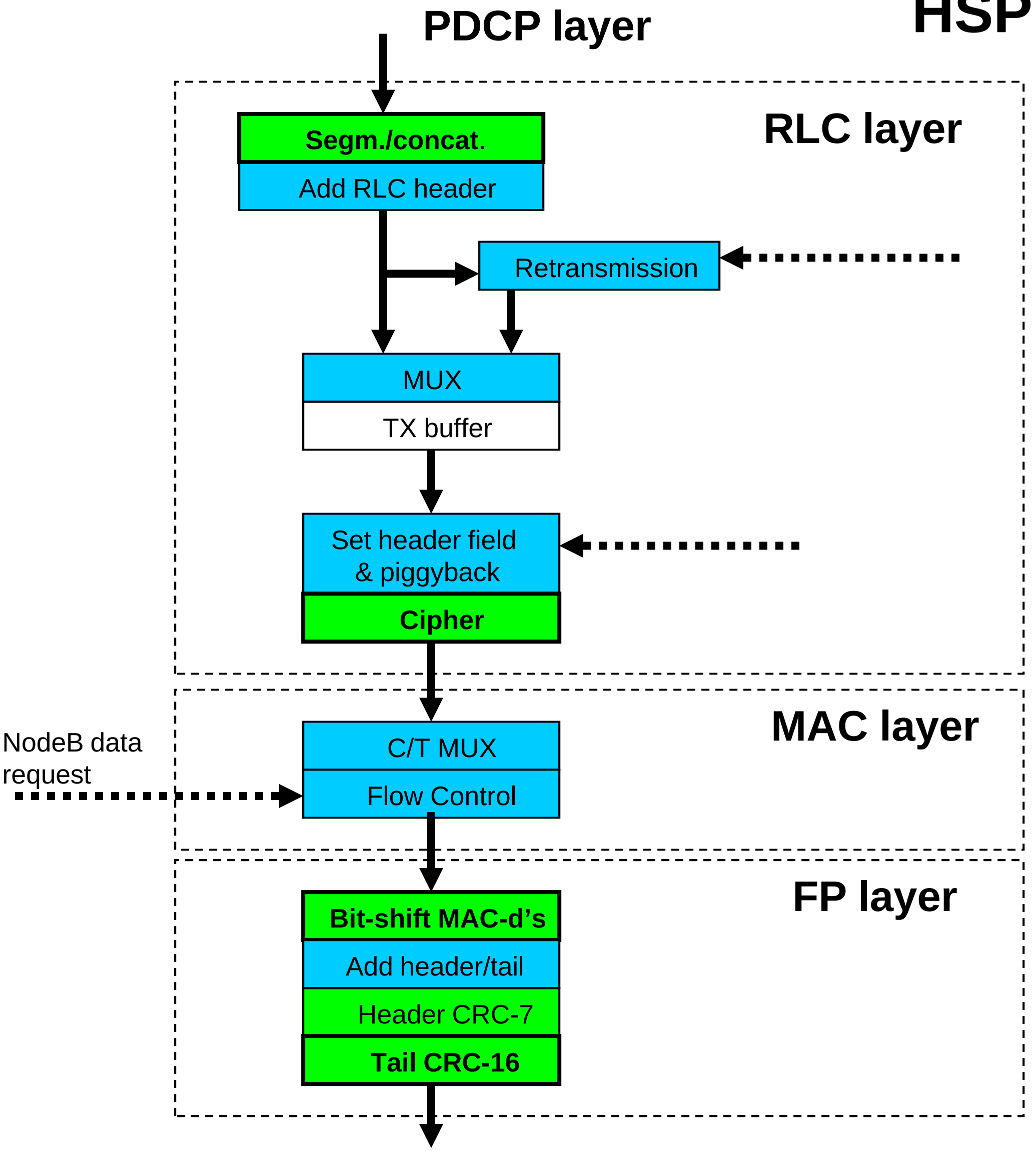
Bitshift

MAC-d PDU A N

Payload

Tail

HSPA: AM RLC/MAC/FP Downlink



Bold frame indicates intensive work.

Blue = Core

Green = Accelerator

Features for mobile broadband:

- Cipher blocks of packets
- Auto-update sequence number
- Bit-shifting
- CRC-7 / CRC-11 / CRC-16
- Dual CRC (header/payload)

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RLC / MAC / FP flow on P4080: Example A

- User data assembled in memory, from GTP-U.

- When MAC flow control indicates that we can send data:

Core:

1. Checks retransmission buffer.
2. Checks status transmission buffer.
3. Creates RLC headers with status.
4. Checks if C/T MUX is used.
5. Adds pointers to segments and RLC headers.
6. Concatenation/piggyback/pad. of last user-data packet
7. Saves pointers for retransmission buffer
8. Creates FP header/tail.

SEC: segments, adds header, bitshift and cipher. Adds FP header/tail and computes CRC-7 and CRC-16.

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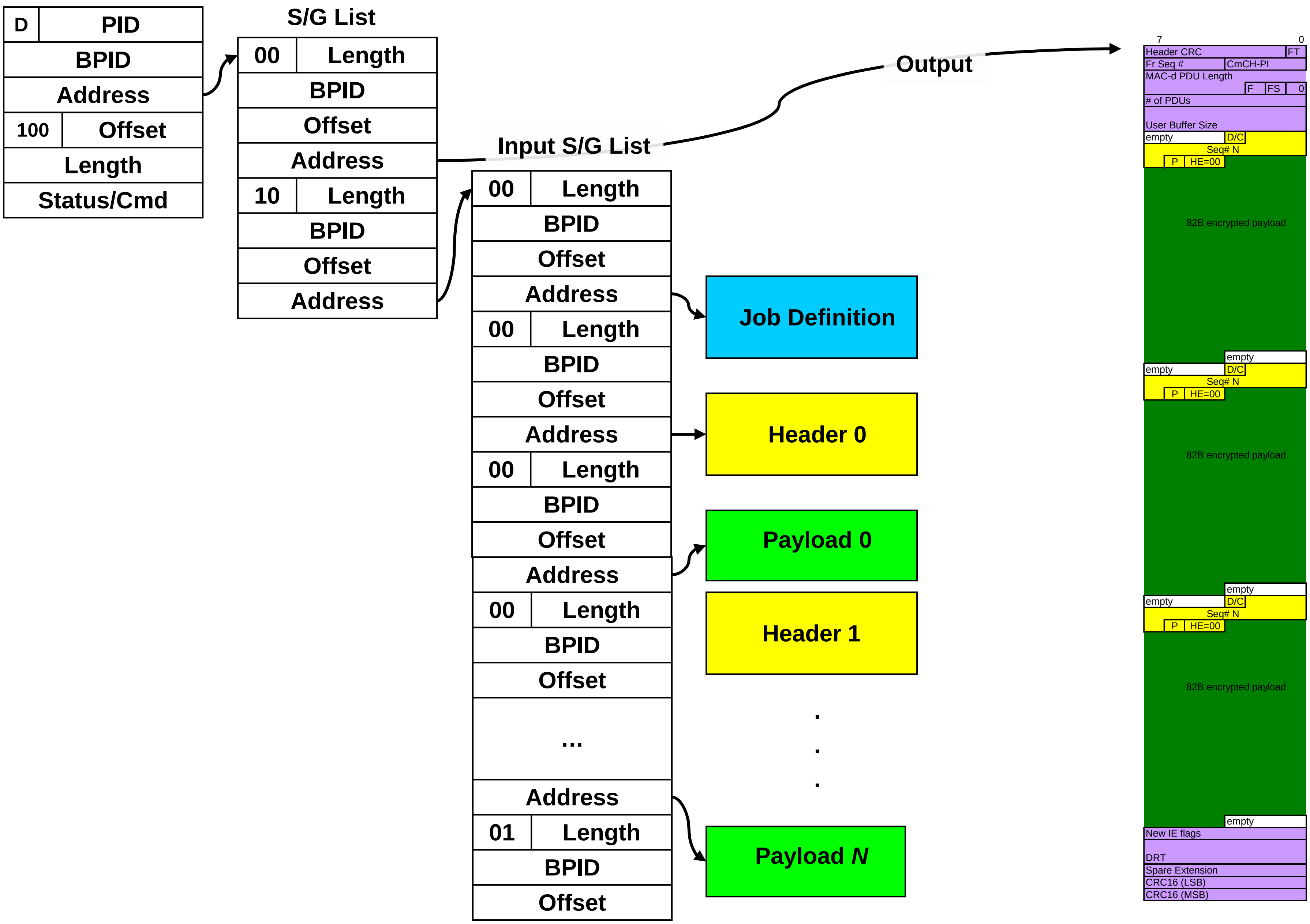
Type-1 MAC-d processing



Frame Descriptor

D	PID
BPID	
Address	
100	Offset
Length	
Status/Cmd	

S/G List

00	Length
BPID	
Offset	
Address	
10	Length
BPID	
Offset	
Address	

Input S/G List

00	Length
BPID	
Offset	
Address	
00	Length
BPID	
Offset	
Address	
00	Length
BPID	
Offset	
Address	
00	Length
BPID	
Offset	
…	
Address	
01	Length
BPID	
Offset	

Job Definition

Header 0

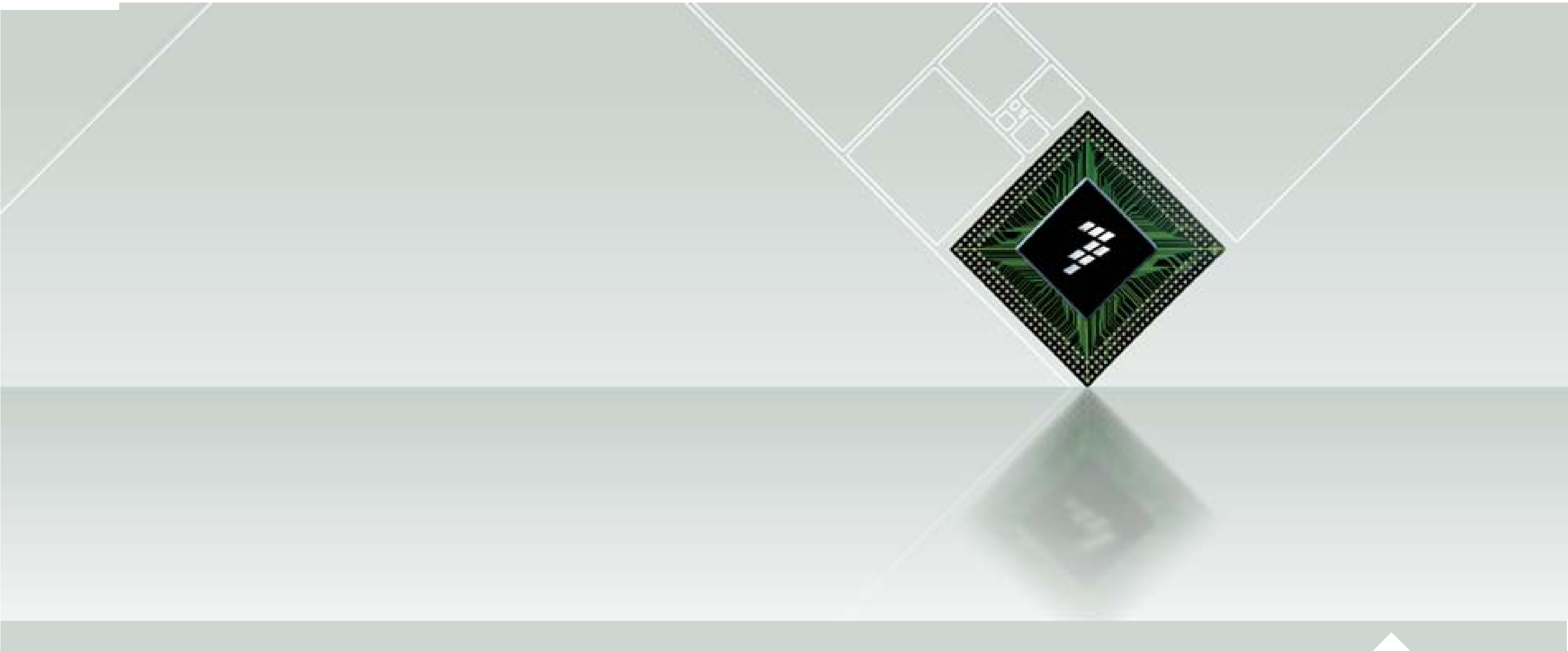
Payload 0

Header 1

.
.
.

Payload *N*

Output



DEMO

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