

NXP POWER MANAGEMENT SOLUTION FOR XILINX ULTRASCALE MPSOC

Aurelien Sanchez
JANUARY, 2023



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XILINX ULTRASCALE MPSOC FAMILY INTRODUCTION

	CG Devices	EG Devices	EV Devices
Application Processor	Dual-core ARM® Cortex™-A53 MPCore™ up to 1.3GHz	Quad-core ARM Cortex-A53 MPCore up to 1.5GHz	Quad-core ARM Cortex-A53 MPCore up to 1.5GHz
Real-Time Processor	Dual-core ARM Cortex-R5 MPCore up to 533MHz	Dual-core ARM Cortex-R5 MPCore up to 600MHz	Dual-core ARM Cortex-R5 MPCore up to 600MHz
Graphics Processor		Mali™-400 MP2	Mali™-400 MP2
Video Codec			H.264 / H.265
Programmable Logic	103K–600K System Logic Cells	103K–1143K System Logic Cells	192K–504K System Logic Cells
Applications	• Sensor Processing & Fusion • Motor Control • Low-cost Ultrasound • Traffic Engineering	• Flight Navigation • Missile & Munitions • Military Construction • Secure Solutions • Networking • Cloud Computing Security • Data Center • Machine Vision • Medical Endoscopy	• Situational Awareness • Surveillance/Reconnaissance • Smart Vision • Image Manipulation • Graphic Overlay • Human Machine Interface • Automotive ADAS • Video Processing • Interactive Display

XILINX ULTRASCALE MPSOC SPEED GRADES

	Device Name ⁽¹⁾																					
	Speed Grade	ZU2		ZU3		ZU4			ZU5			ZU6		ZU7			ZU9		ZU11	ZU15	ZU17	ZU19
		CG	EG	CG	EG	CG	EG	EV	CG	EG	EV	CG	EG	CG	EG	EV	CG	EG	EG	EG	EG	EG
Extended ⁽²⁾	-1	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	-2	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	-2L	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	-3	—	—	—	—	—	●	●	—	●	●	—	●	—	●	●	—	●	●	●	●	
Industrial	-1	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	-1L	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	-2	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	

Notes:
1. For full part number details, see the Ordering Information section in [DS891, Zynq UltraScale+ MPSoC Overview](#).
2. -2LE (Tj = 0°C to 110°C). For more details, see the Ordering Information section in [DS891, Zynq UltraScale+ MPSoC Overview](#).

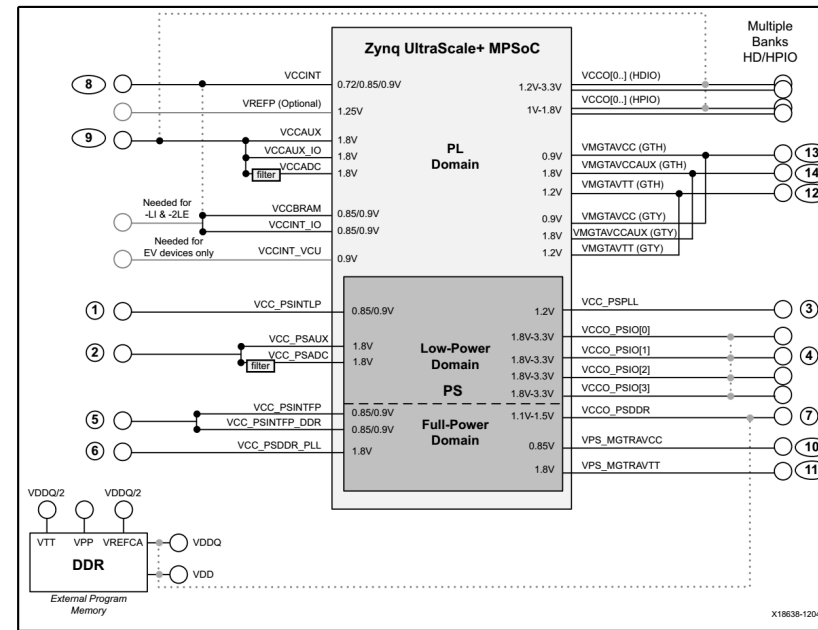
- :: available
- :: not offered



XILINX ULTRASCALE MPSOC POWER MANAGEMENT SOLUTION FROM ZU2 TO ZU19, CG / EG / EV, ALL SPEED GRADES

There are four identified use case to supply a Xilinx MPSOC:

- Always on: cost optimized (-1 and -2 devices)
- Always on: power/efficiency optimized (-1L and -2L devices)
- Always on: PL performance optimized (-3 devices)
- Full power management flexibility (all devices/speed grades)



Example: use case for full power management

XILINX ULTRASCALE MPSOC POWER MANAGEMENT SOLUTION FROM ZU2 TO ZU19, CG / EG / EV, ALL SPEED GRADES

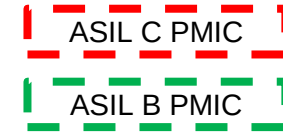
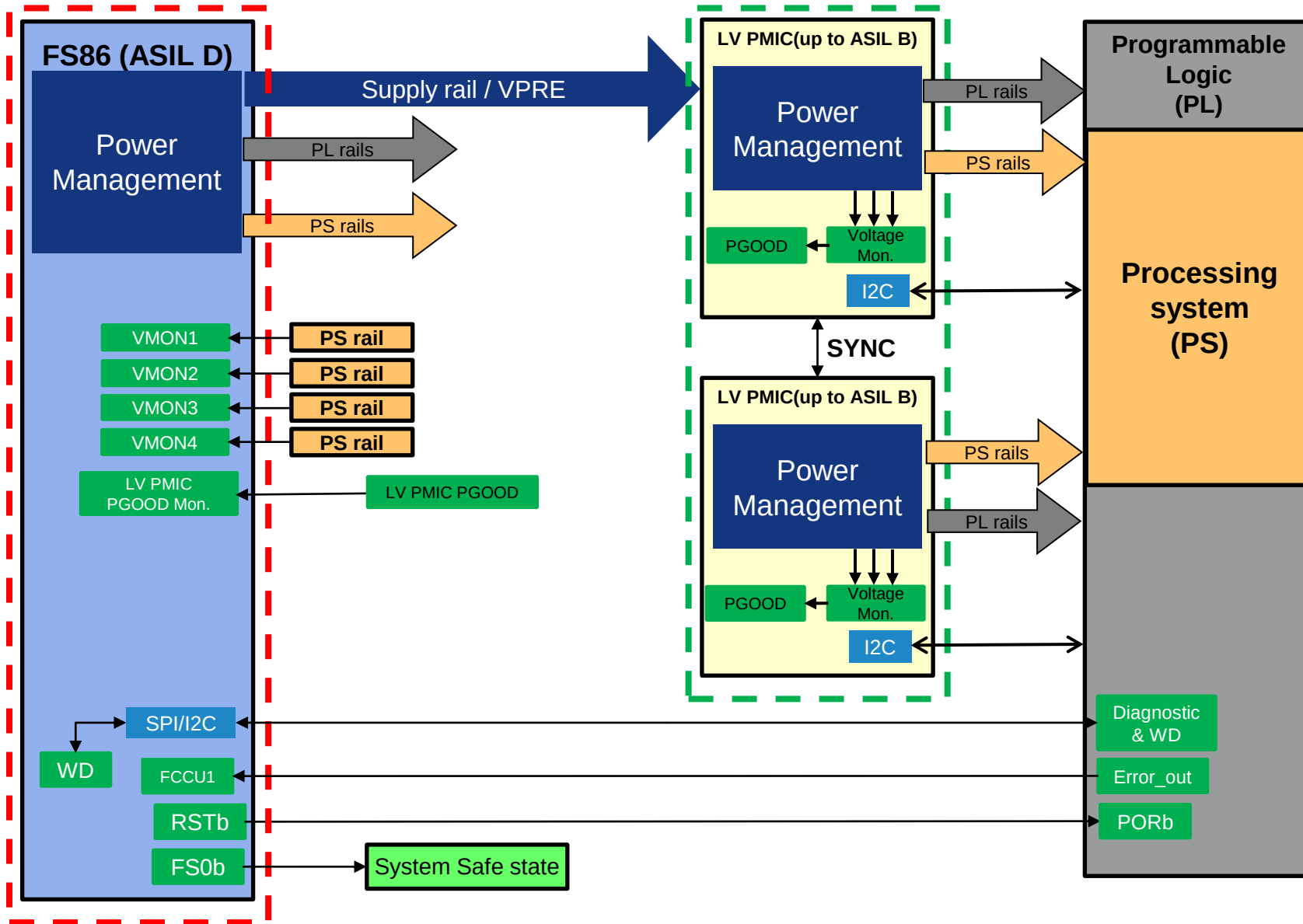
For all architecture, requirement are considered to be maximum for CG / EG / EV version, and for all speed grades:

- PS Domain, Low power domain and full-power domain rails are being monitored by ASIL-D PMIC (ASIL-C would be sufficient)
- For ZU4EV / 5EV / 7EV, VCCINT_VCU needs to be supplied independently (connected to ground otherwise)
- HDIO and HPIO (top right corner of bloc diagram) can be supplied independently, or attached to existing rail to save BOM cost if preferred (see dotted line)
- FS85xx can replace FS86xx if need only to monitor 6 supply rails with ASIL-D
- Power management solution are not unique, and differs depending processing and MPSOC features being used

	MPSOC	Device #1	Device #2	Device #3	Device #4	Device #5	Device #6
1. Cost optimized	ZU2-ZU3*	FS8500	PF7100				
	ZU2-ZU3	FS8632	PF5300	PF5024			
	ZU4-ZU5	FS8632	PF5300	PF7100	PF5023		
	ZU6-ZU9	FS8632	PF5200	PF7100	PF5023		
	ZU11-ZU19	FS8632	PF5200	PF5024	PF5024	PF5023	
2. Power and efficiency	ZU2-ZU3	FS8632	PF7100	PF5300			
	ZU4-ZU5	FS8632	PF7100	PF5300	PF5024		
	ZU6-ZU9	FS8632	PF7100	PF5200	PF5024		
	ZU11-ZU19	FS8632	PF7100	PF5200	PF5024	PF5023	
3. PL performance	ZU2-ZU3	FS8632	PF5300	PF5023	PF5023		
	ZU4-ZU5	FS8632	PF5300	PF5023	PF5023		
	ZU6-ZU9	FS8632	PF5200	PF5023	PF5023		
	ZU11-ZU19	FS8632	PF5200	PF5024	PF5024	PF5023	
4. Full power management	ZU2-ZU3	FS8633	PF7100	PF7100			
	ZU4-ZU5	FS8633	PF7100	PF5300	PF5020	PF5023	
	ZU6-ZU9	FS8633	PF7100	PF5200	PF5020	PF5023	
	ZU11-ZU19	FS8633	PF7100	PF5200	PF5020	PF5024	PF5024

*Minimum architecture possible for cost optimized solution

GENERIC ASIL C ARCHITECTURE WITH F86x.



- FS86x is an ASIL-D PMIC monitoring Processing System (PS) power rails
- FS86x acts as an independent monitoring of the PS including WD and error out
- LV PMIC is making ASIL B voltage monitoring of Programmable Logic (PL) rails
- LV PMIC PGOOD is feedback to PS and FS86x for common reaction at ASIL D domain if needed (system safe state)
- LV PMICs fully synchronized to ensure right power-up and power-down sequence whatever the number of LV PMICs

USE CASE 1

COST OPTIMIZED

MINIMUM SOLUTION

USE CASE 1: COST OPTIMIZED MINIMUM SOLUTION

This use case presents the minimum architecture possible to supply a **ZU2/ZU3 CG (-1,-2)** or **EG (-1,-2)** with the following configuration:

PS and PL DDR, 1.8V I/O, and 2.5V I/O or 3.3V I/O with no MGTs

On this power-tree:

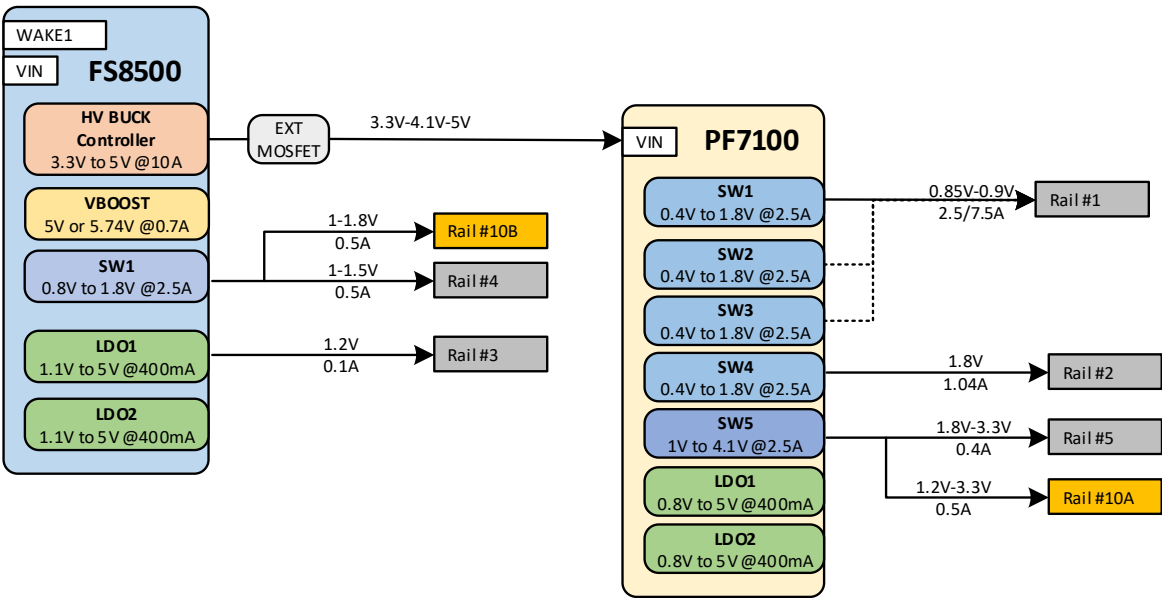
- FS8500 monitors all rails (5 rails with ASIL-D monitoring)
- Rail#1 can be supplied in single, dual or tri-phase to allow up to 7.5A depending processing needs
- FS8500 has 2 LDOs available for system or other rails
- PF7100 has 2 LDOs available for system or other rails

ZU2 – ZU3

Monitored by ASIL-B PMIC

Monitored by ASIL-D PMIC

PL-PS I/Os

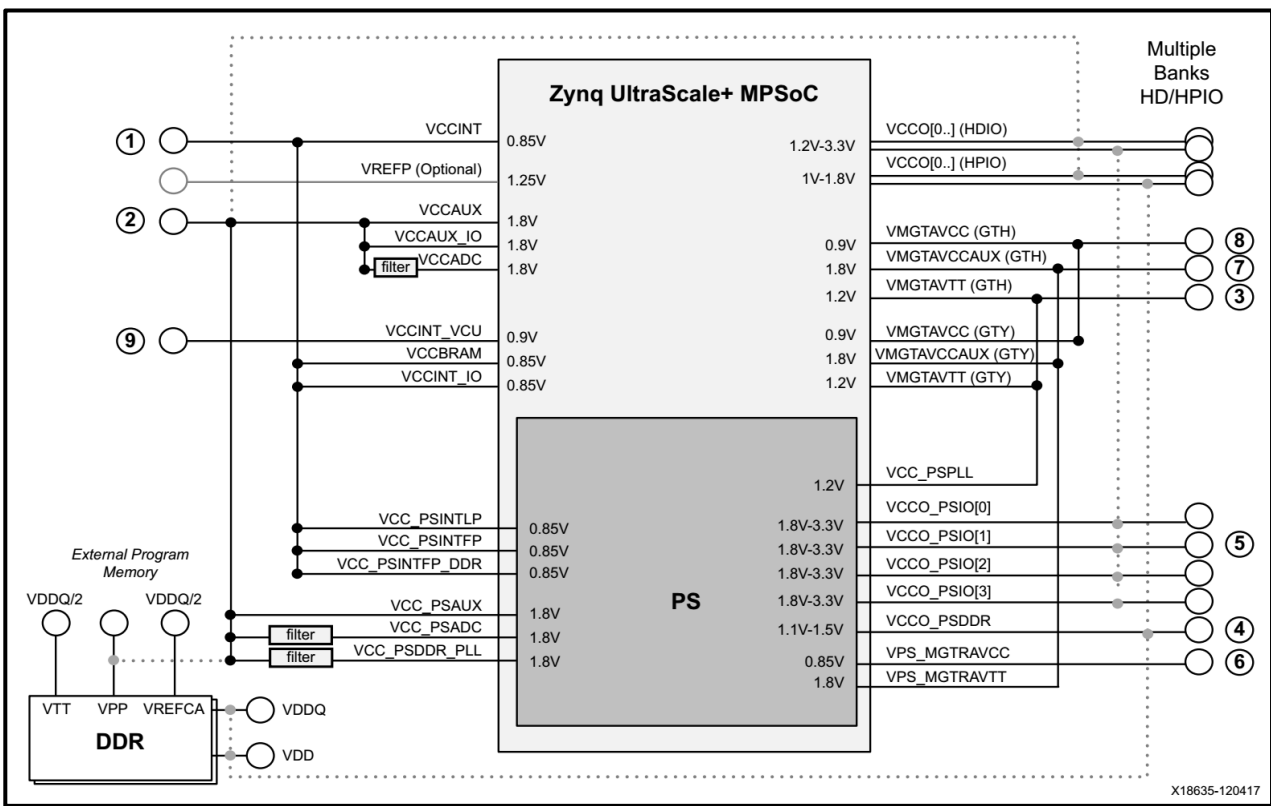


USE CASE 1

COST OPTIMIZED

USE CASE 1: COST OPTIMIZED

- HDIO/HPIO are connected to existing rails in this use case (see rail #10A and #10B)
- Rail #1/2/3/4/5/6/7/10 are all monitored by front PMIC FS8612 (up to ASIL-D)

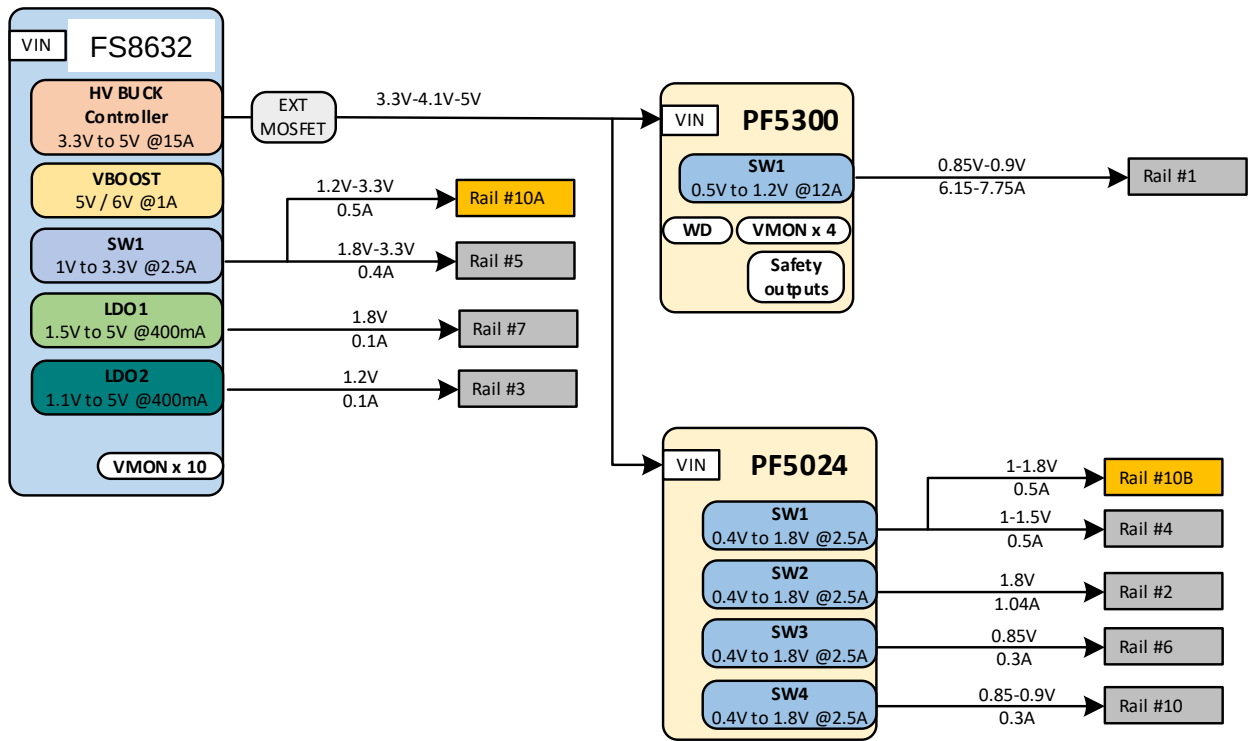


	Power Regulator	Sequence	Possible Power Rail Consolidation
Required	1	See <i>Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics</i> (DS925) [Ref 22]	VCCINT, VCC_PSINTFP, VCC_PSINTLP, VCC_PSINTFP_DDR, VCCINT_IO, VCCBRAM
	2		VCC_PSAUX, VCC_PSADC ⁽¹⁾ , VCC_PSDDR_PLL ⁽²⁾ , VCCAUX, VCCAUX_IO, and VCCADC ⁽¹⁾
	3		VCC_PSPLL, VMGTAVTT (GTH), and VMGTAVTT (GTY)
	4		VCCO_PSDDR
	5		VCCO_PSIO[0:3] assuming all PS I/Os run from same voltage
Required: EV -1 and -2	9		VCCINT_VCU
User-defined	6		VPS_MGTRAVCC
	7		VPS_MGTRAVTT, VMGTVCCAUX (GTH), and VMGTVCCAUX (GTY)
	8		VMGTAVCC (GTH) and VMGTAVCC (GTY)
	10		Optional PL and PS I/O voltages

USE CASE 1: COST OPTIMIZED, ZU2 – ZU3

ZU2 – ZU3

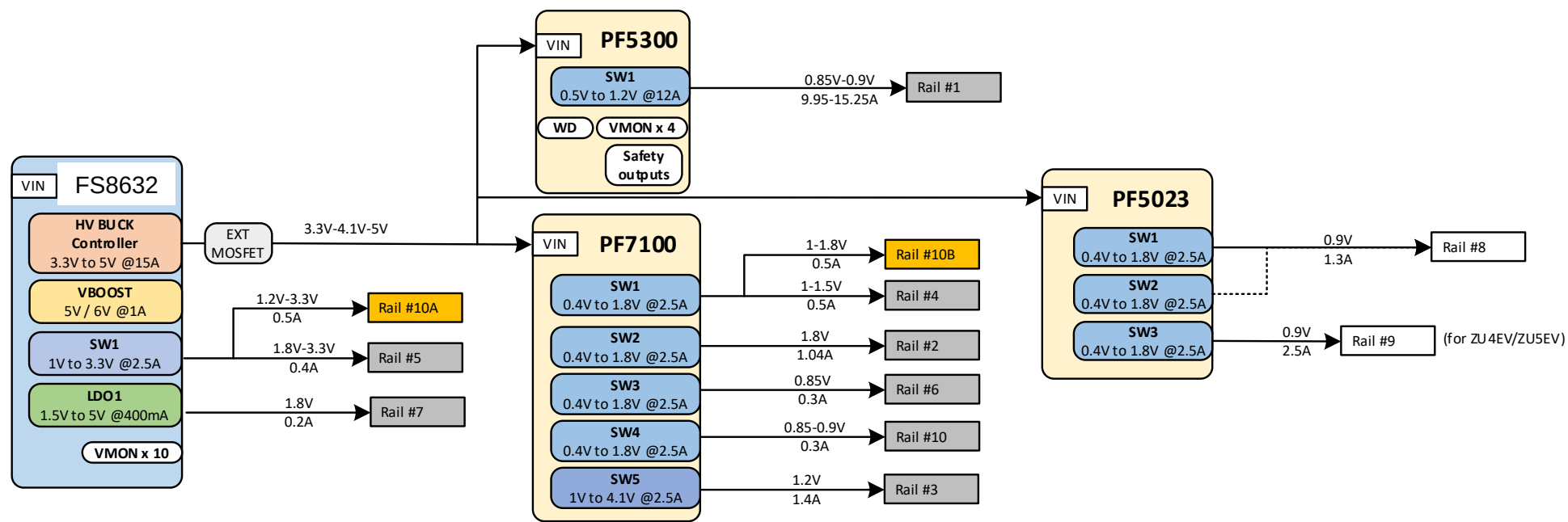
- Monitored by ASIL-B PMIC
- Monitored by ASIL-D PMIC
- PL-PS I/Os



USE CASE 1: COST OPTIMIZED, ZU4 – ZU5

ZU4 – ZU5

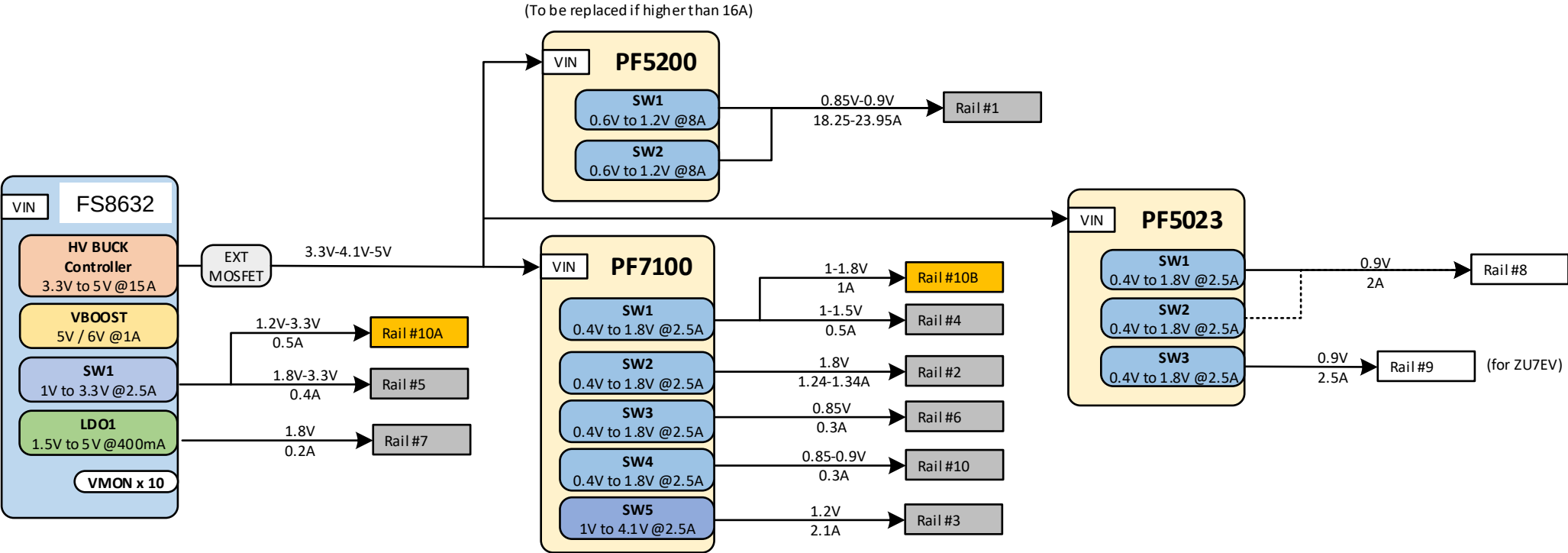
- Monitored by ASIL-B PMIC
- Monitored by ASIL-D PMIC
- PL-PS I/Os



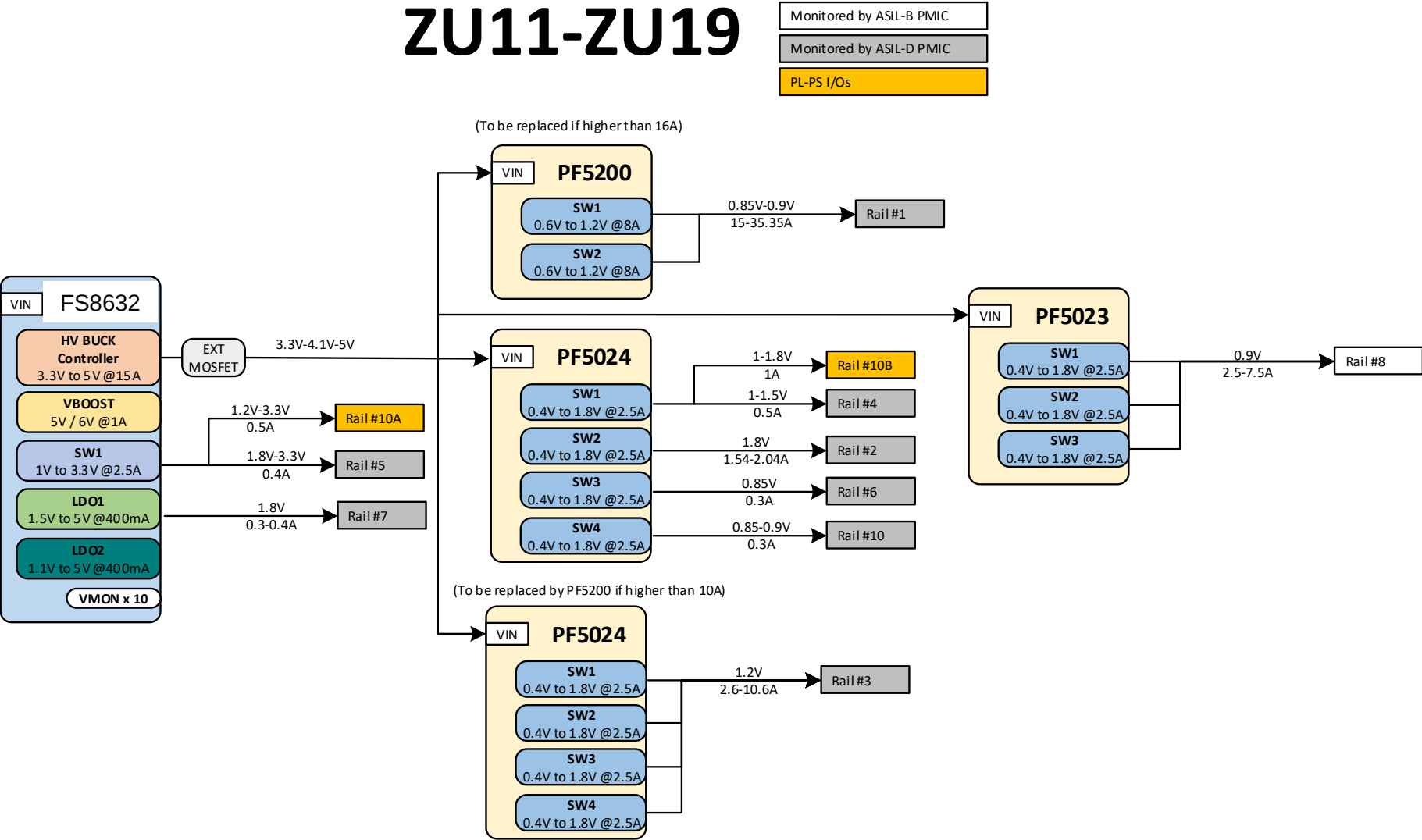
USE CASE 1: COST OPTIMIZED, ZU6 – ZU9

ZU6 – ZU9

- Monitored by ASIL-B PMIC
- Monitored by ASIL-D PMIC
- PL-PS I/Os



USE CASE 1: COST OPTIMIZED, ZU11 – ZU19

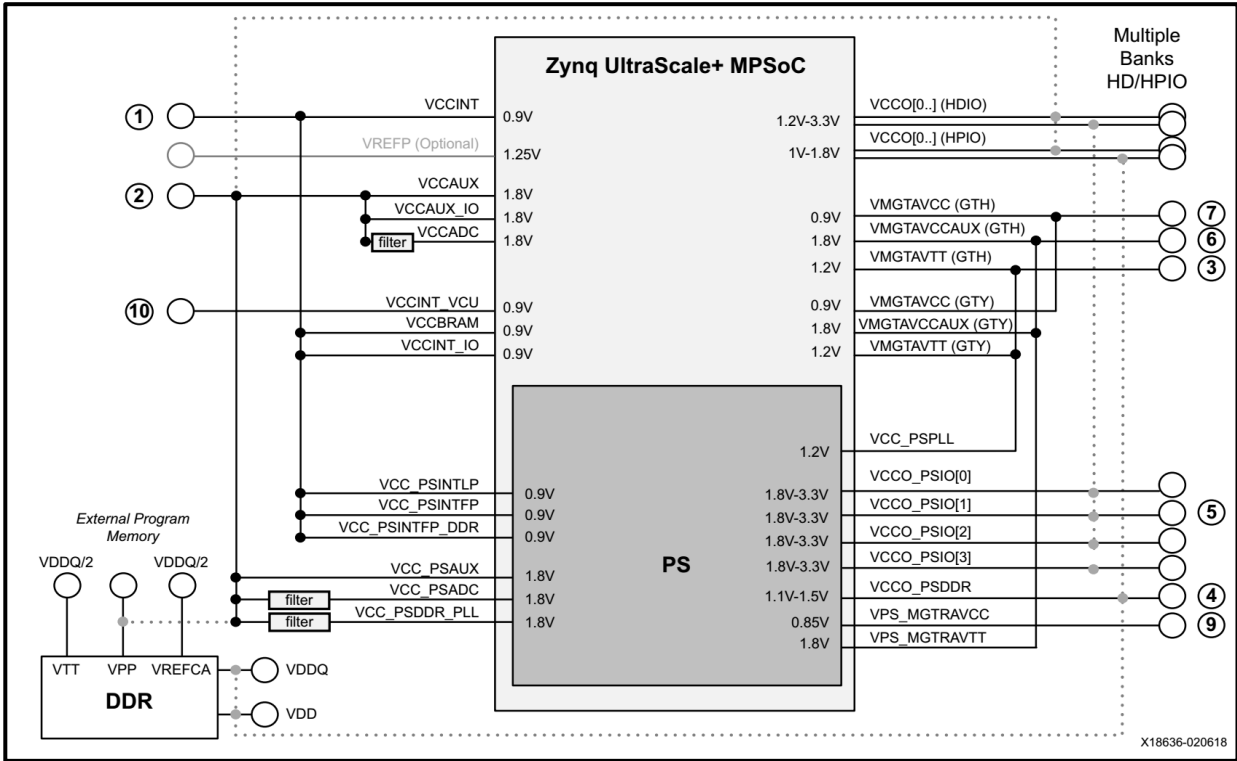


USE CASE 2

POWER AND EFFICIENCY

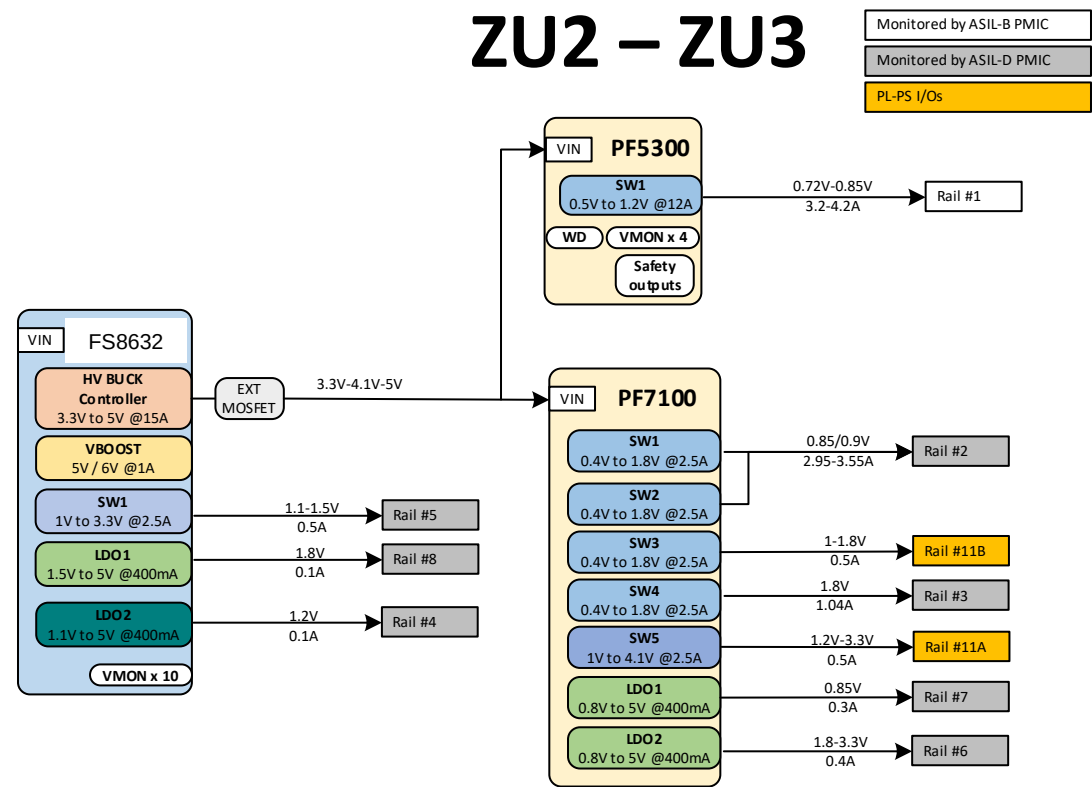
USE CASE 2: POWER AND EFFICIENCY OPTIMIZED

- HDIO/HPIO are either separated or connected to existing rails in this use case (see rail #11A and #11B)
- Rail #2/3/4/5/6/7/8 are all monitored by front PMIC FS8612 (up to ASIL-D)

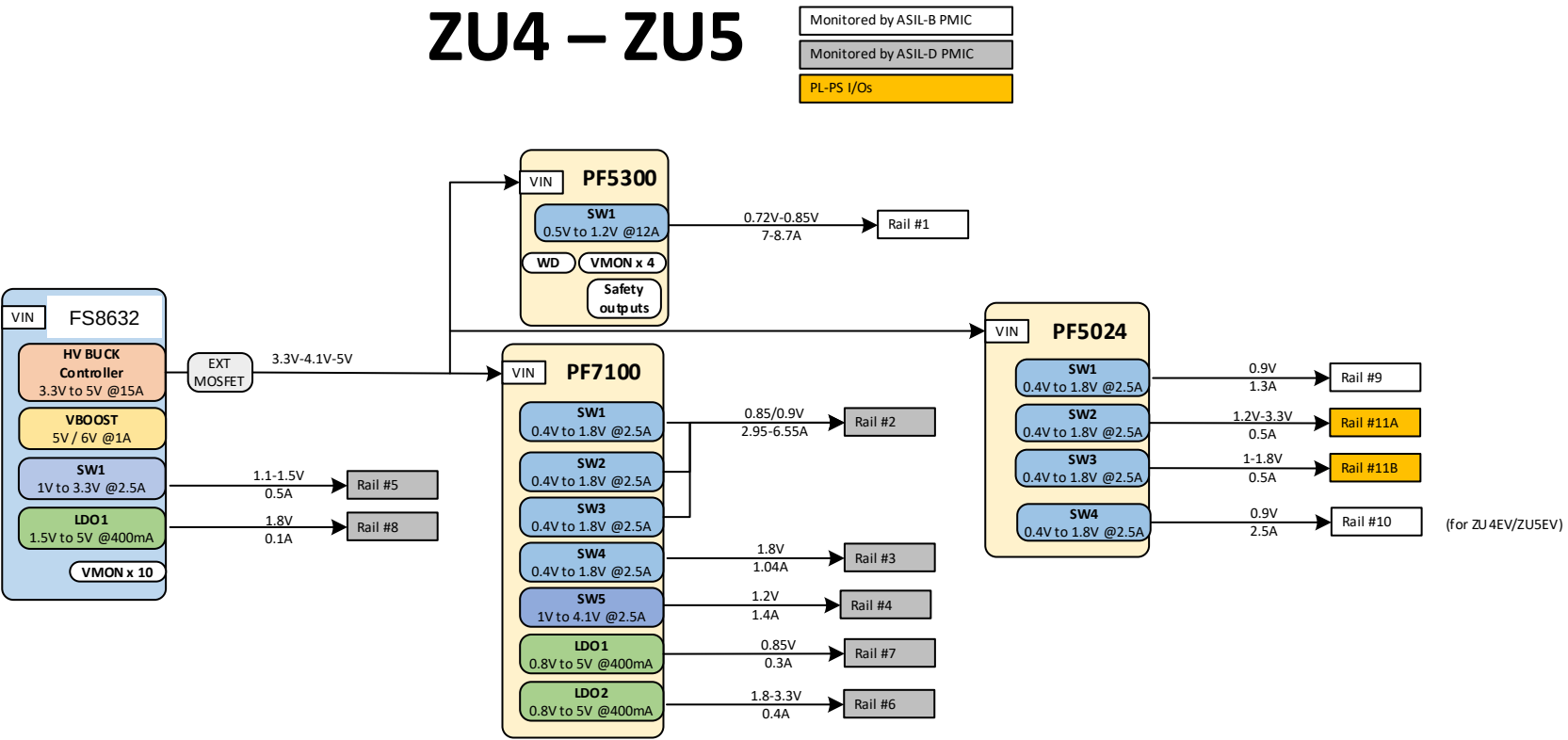


	Power Regulator	Sequence	Possible Power Rail Consolidation
Required	1	See Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics (DS925) [Ref 22]	VCCINT, VCC_PSINTFP, VCC_PSINTLP, VCC_PSINTFP_DDR, VCCINT_IO, VCCBRAM
	2		VCC_PSAUX, VCC_PSADC ⁽¹⁾ , VCC_PSDDR_PLL ⁽²⁾ , VCCAUX, VCCAUX_IO, and VCCADC ⁽¹⁾
	3		VCC_PSPLL, VMGTAVTT (GTH), and VMGTAVTT (GTY)
	4		VCCO_PSDDR
	5		VCCO_PSIQ[0:3] assuming all PS I/Os run from same voltage
	10		VCCINT_VCU (if used)
User-defined	6		VPS_MGTRAVTT, VMGTAVCCAUX (GTH), and VMGTAVCCAUX (GTY)
	7		VMGTAVCC (GTH), and VMGTAVCC (GTY)
	8		Additional PL and PS I/O voltages
	9		VPS_MGTRAVCC

USE CASE 2: POWER AND EFFICIENCY OPTIMIZED, ZU2 – ZU3



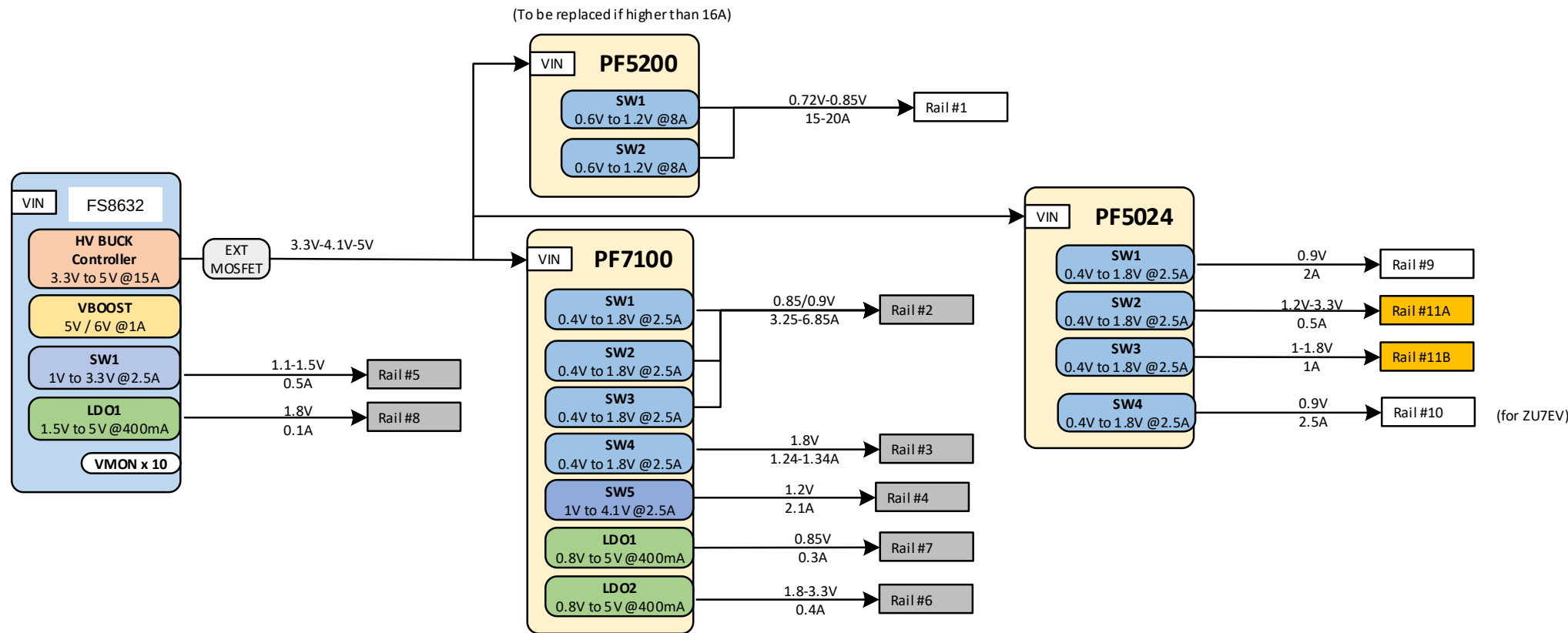
USE CASE 2: POWER AND EFFICIENCY OPTIMIZED, ZU4 – ZU5



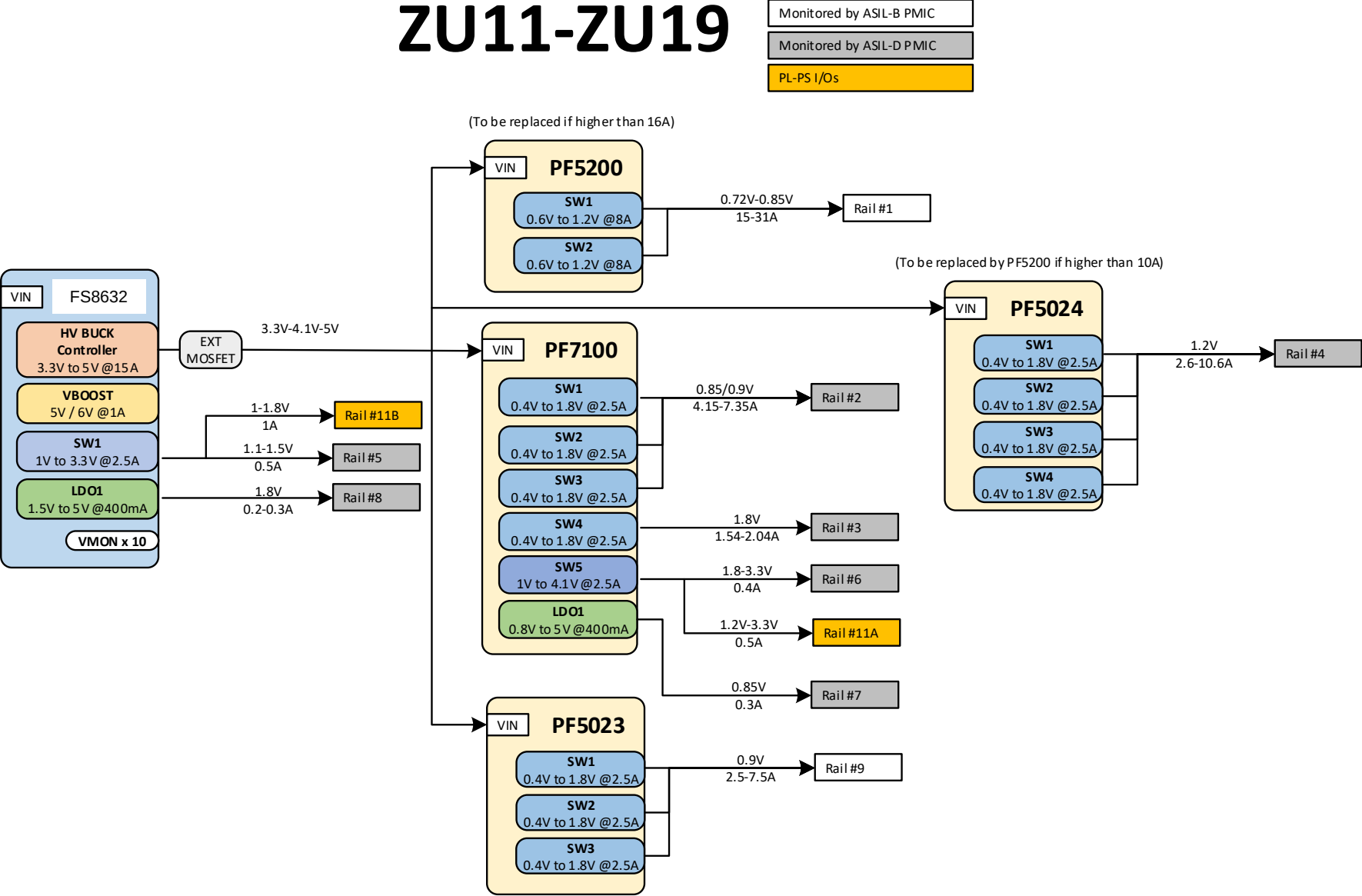
USE CASE 2: POWER AND EFFICIENCY OPTIMIZED, ZU6 – ZU9

ZU6 – ZU9

- Monitored by ASIL-B PMIC
- Monitored by ASIL-D PMIC
- PL-PS I/Os



USE CASE 2: POWER AND EFFICIENCY OPTIMIZED, ZU11 – ZU19

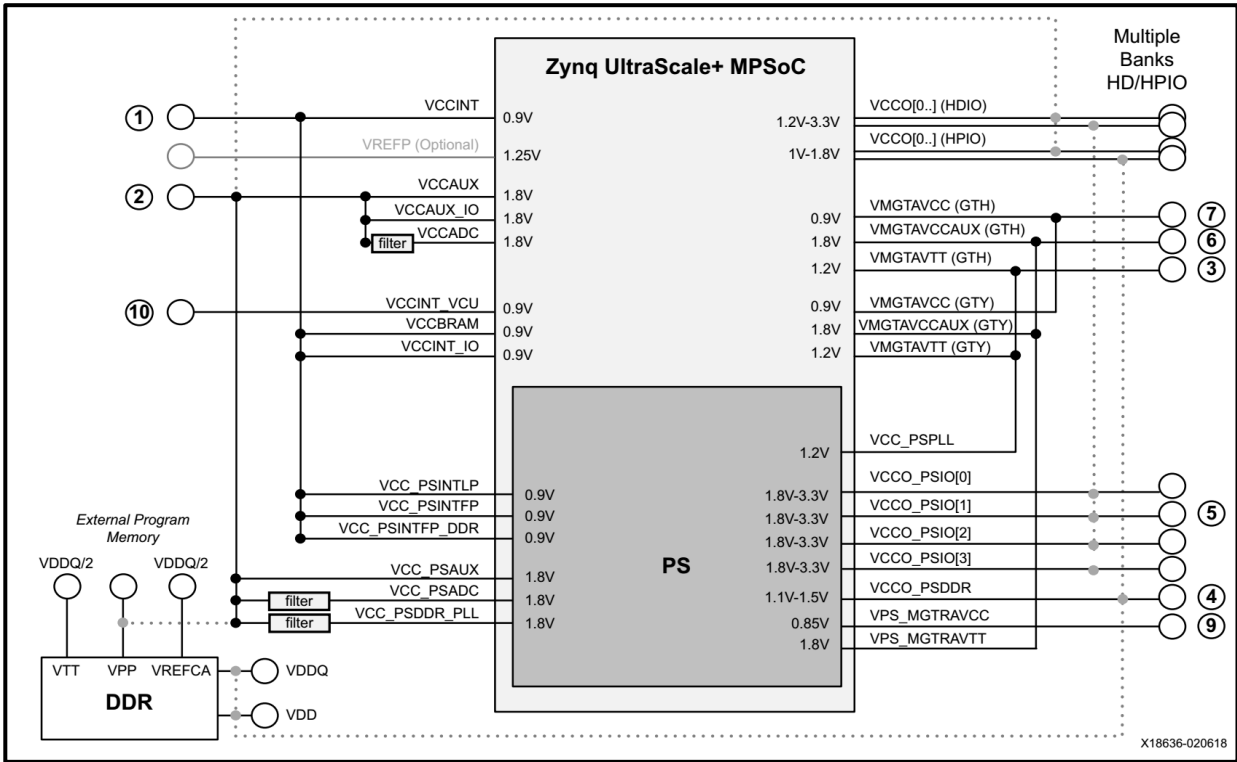


USE CASE 3

PL PERFORMANCE

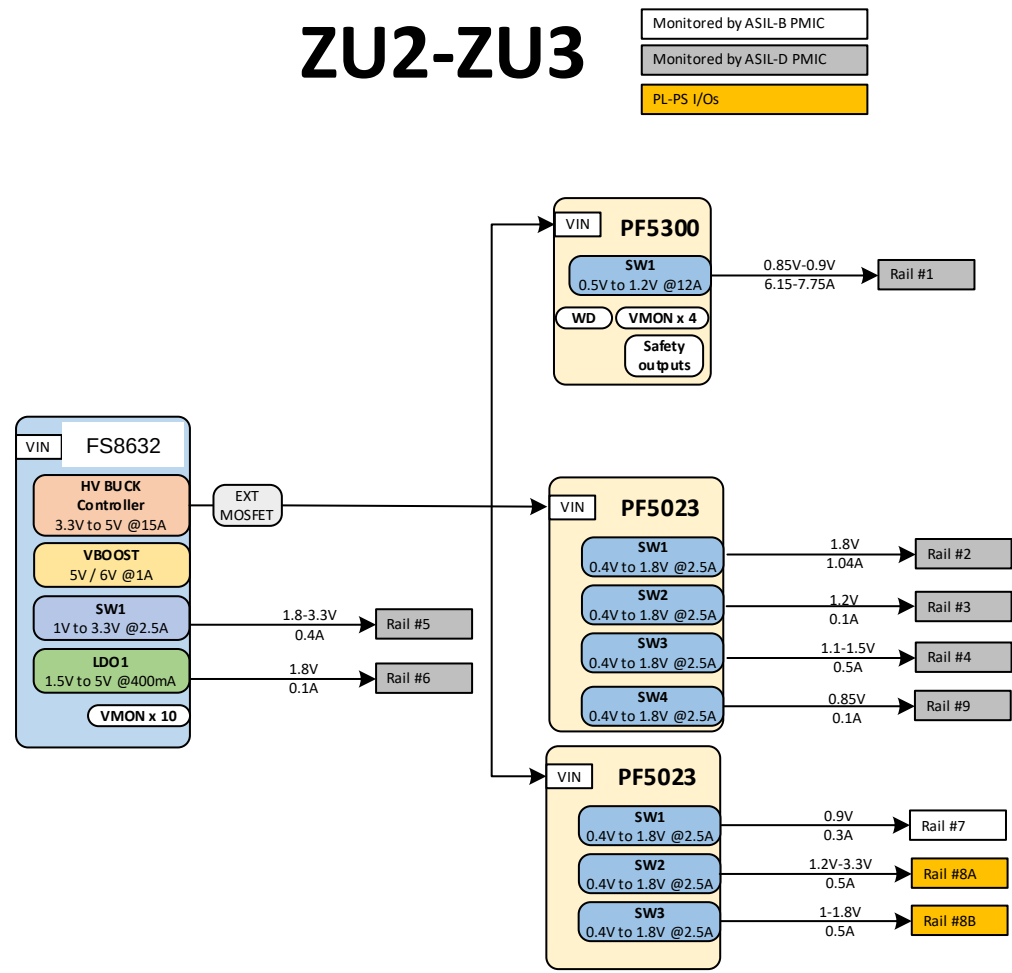
USE CASE 3: PL PERFORMANCE OPTIMIZED

- HDIO/HPIO are either connected to existing rails or supplied independently in this use case (see rail #8A and #8B)
- VCCBRAM and VCCINT_IO are supplied together with VCCINT (rail #8)
- Rail #1/2/3/4/5/6/9 are all monitored by front PMIC FS8612 (up to ASIL-D)

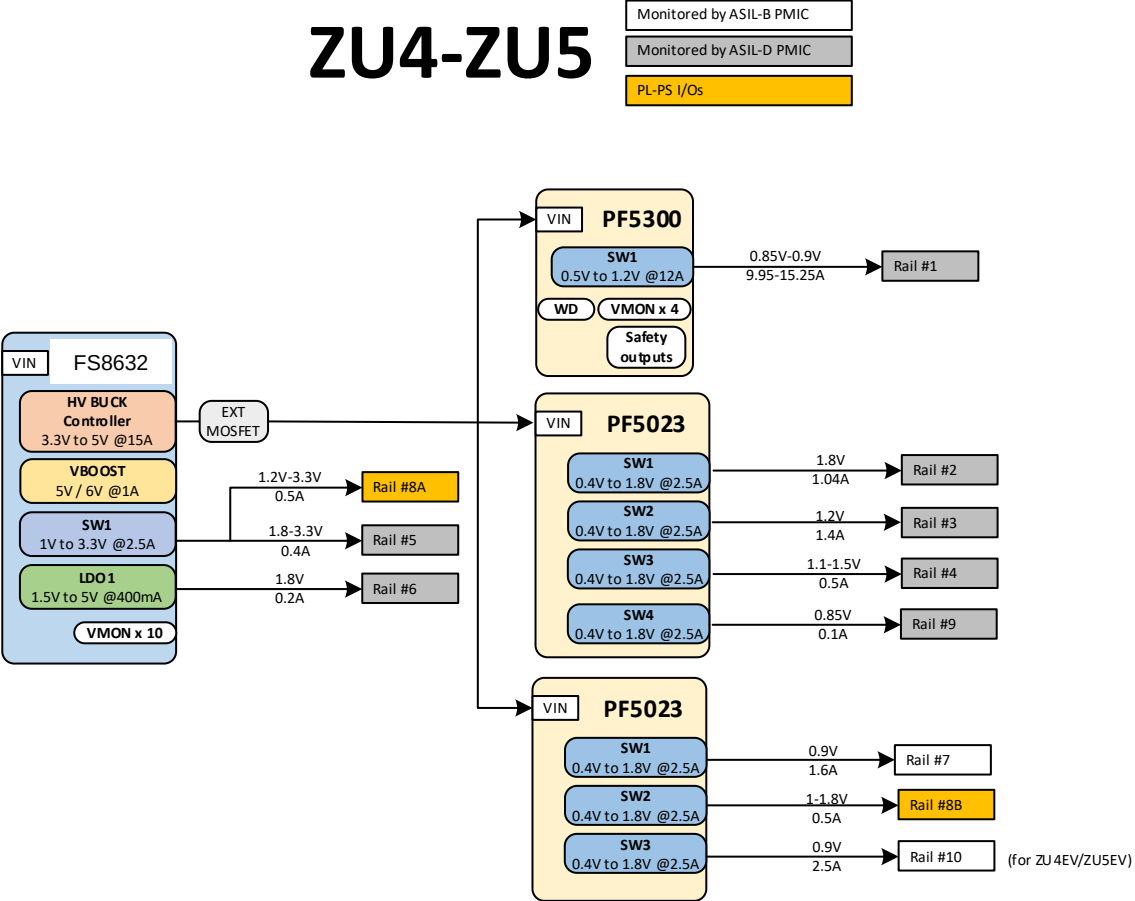


	Power Regulator	Sequence	Possible Power Rail Consolidation
Required	1	See Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics (DS925) [Ref 22]	VCCINT, VCC_PSINTFP, VCC_PSINTLP, VCC_PSINTFP_DDR, VCCINT_IO, VCCBRAM
	2		VCC_PSAUX, VCC_PSADC ⁽¹⁾ , VCC_PSDDR_PLL ⁽²⁾ , VCCAUX, VCCAUX_IO, and VCCADC ⁽¹⁾
	3		VCC_PSPLL, VMGTAVTT (GTH), and VMGTAVTT (GTY)
	4		VCCO_PSDDR
	5		VCCO_PSIQ[0:3] assuming all PS I/Os run from same voltage
	10		VCCINT_VCU (if used)
User-defined	6		VPS_MGTRAVTT, VMGTAVCCAUX (GTH), and VMGTAVCCAUX (GTY)
	7		VMGTAVCC (GTH), and VMGTAVCC (GTY)
	8		Additional PL and PS I/O voltages
	9		VPS_MGTRAVCC

USE CASE 3: PL PERFORMANCE OPTIMIZED, ZU2 – ZU3



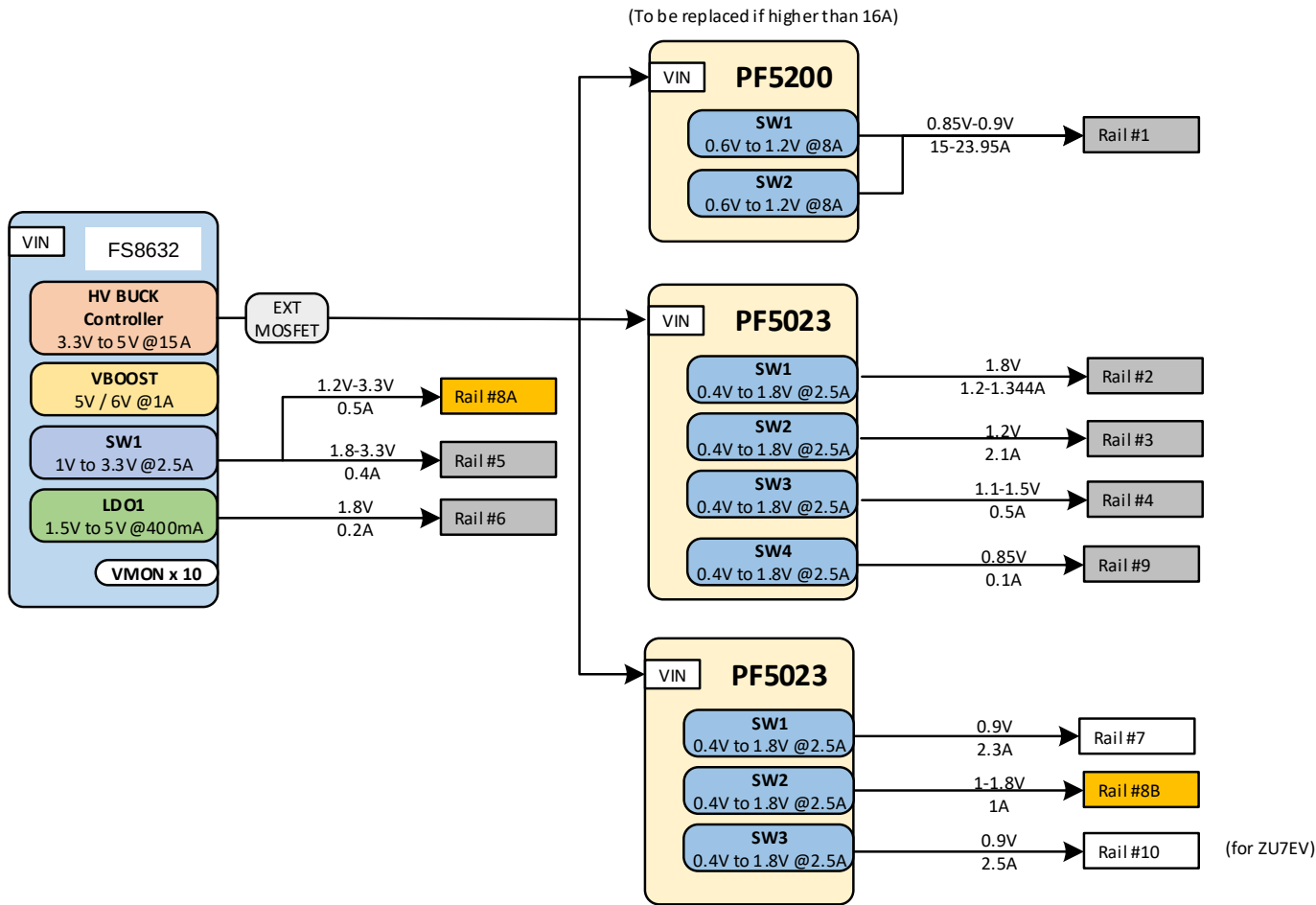
USE CASE 3: PL PERFORMANCE OPTIMIZED, ZU4 – ZU5



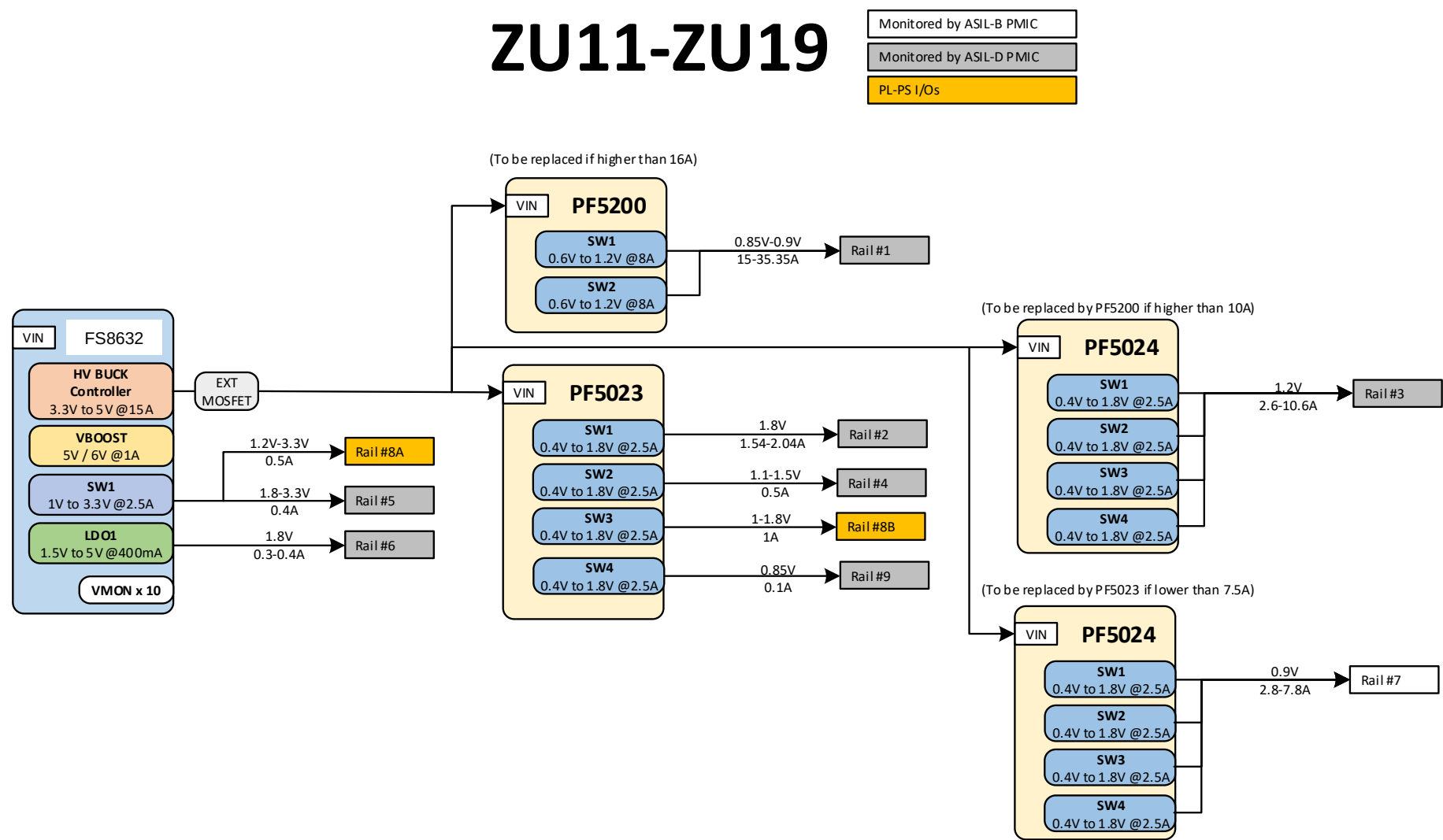
USE CASE 3: PL PERFORMANCE OPTIMIZED, ZU6 – ZU9

ZU6-ZU9

- Monitored by ASIL-B PMIC
- Monitored by ASIL-D PMIC
- PL-PS I/Os



USE CASE 3: PL PERFORMANCE OPTIMIZED, ZU11 – ZU19



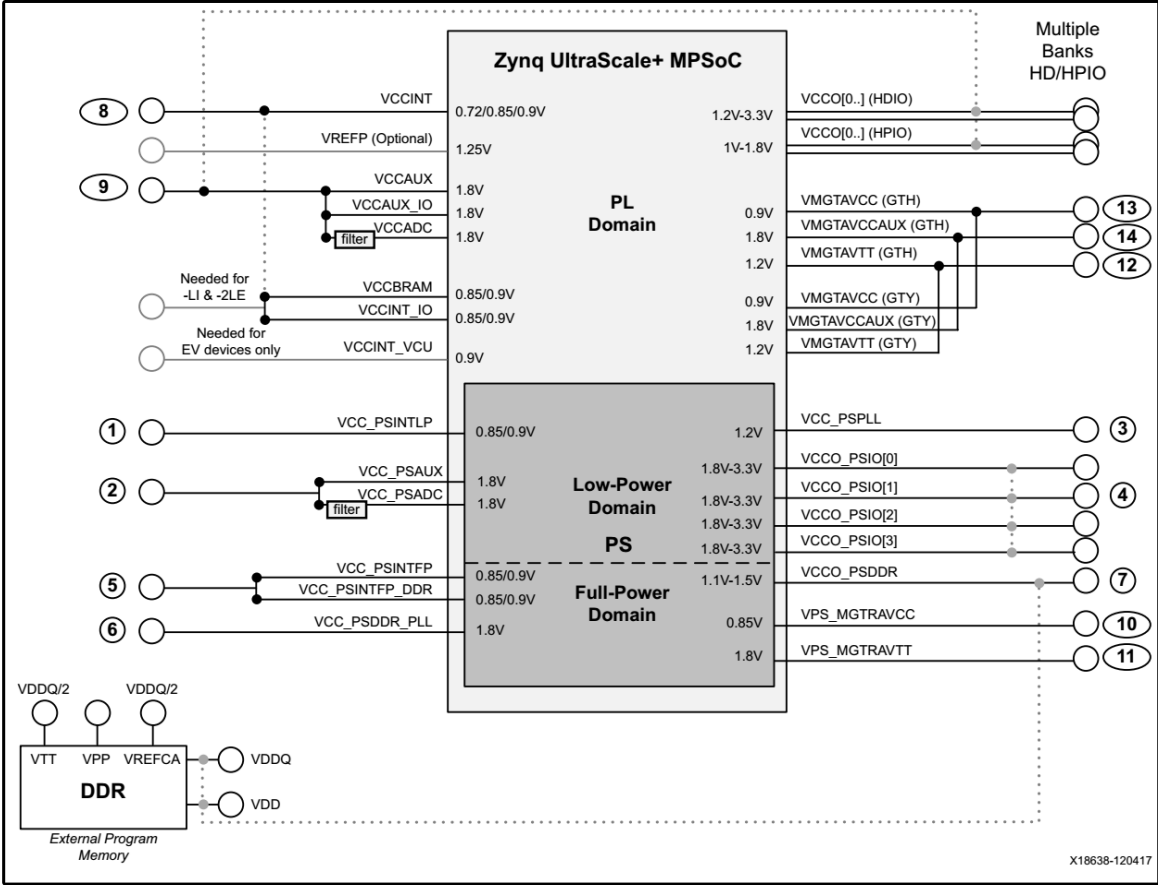
USE CASE 4

FULL POWER

MANAGEMENT

USE CASE 4: FULL POWER MANAGEMENT FLEXIBILITY

- HDIO/HPIO are supplied independently in this use case (see rail #16A and #16B)
- VCCBRAM and VCCINT_IO are supplied together with VCCINT (rail #8)
- Rail #1/2/3/4/5/6/7/10/11 are all monitored by front PMIC FS8616 (up to ASIL-D)

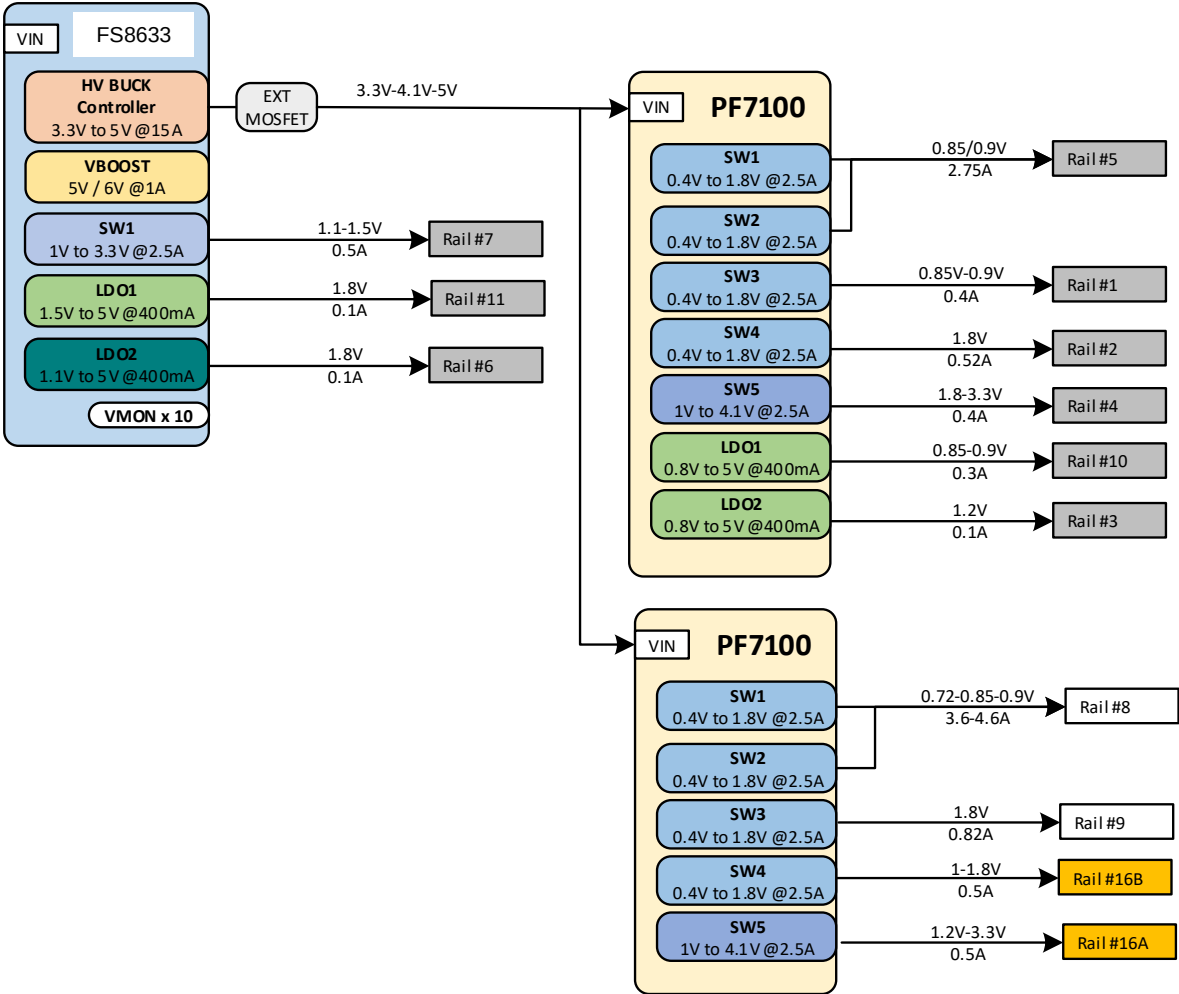


	Power Regulator	Sequence	Possible Power Rail Consolidation
Required	1	See Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics (DS925) [Ref 22]	VCC_PSINTLP
	2		VCC_PSAUX and VCC_PSADC ⁽¹⁾
	3		VCC_PSPLL
	4		VCCO_PSIO[0:3] assuming run off same voltage
	5		VCC_PSINTFP and VCC_PSINTFP_DDR
	6		VCC_PSDDR_PLL
	7		VCCO_PSDDR
	8		VCCINT ⁽²⁾ , VCCBRAM, and VCCINT_IO
	9		VCCAUX, VCCAUX_IO, VCCADC ⁽¹⁾
Required EV devices	15		VCCINT_VCU
User-defined	10		VPS_MGTRAVCC
	11		VPS_MGTRAVTT
	12		VMGTAVTT (GTH) and VMGTAVTT (GTY)
	13		VMGTAVCC (GTH) and VMGTAVCC (GTY)
	14		VMGTVCCAUX (GTH) and VMGTVCCAUX (GTY)
	16		Optional PL and PS I/O voltages

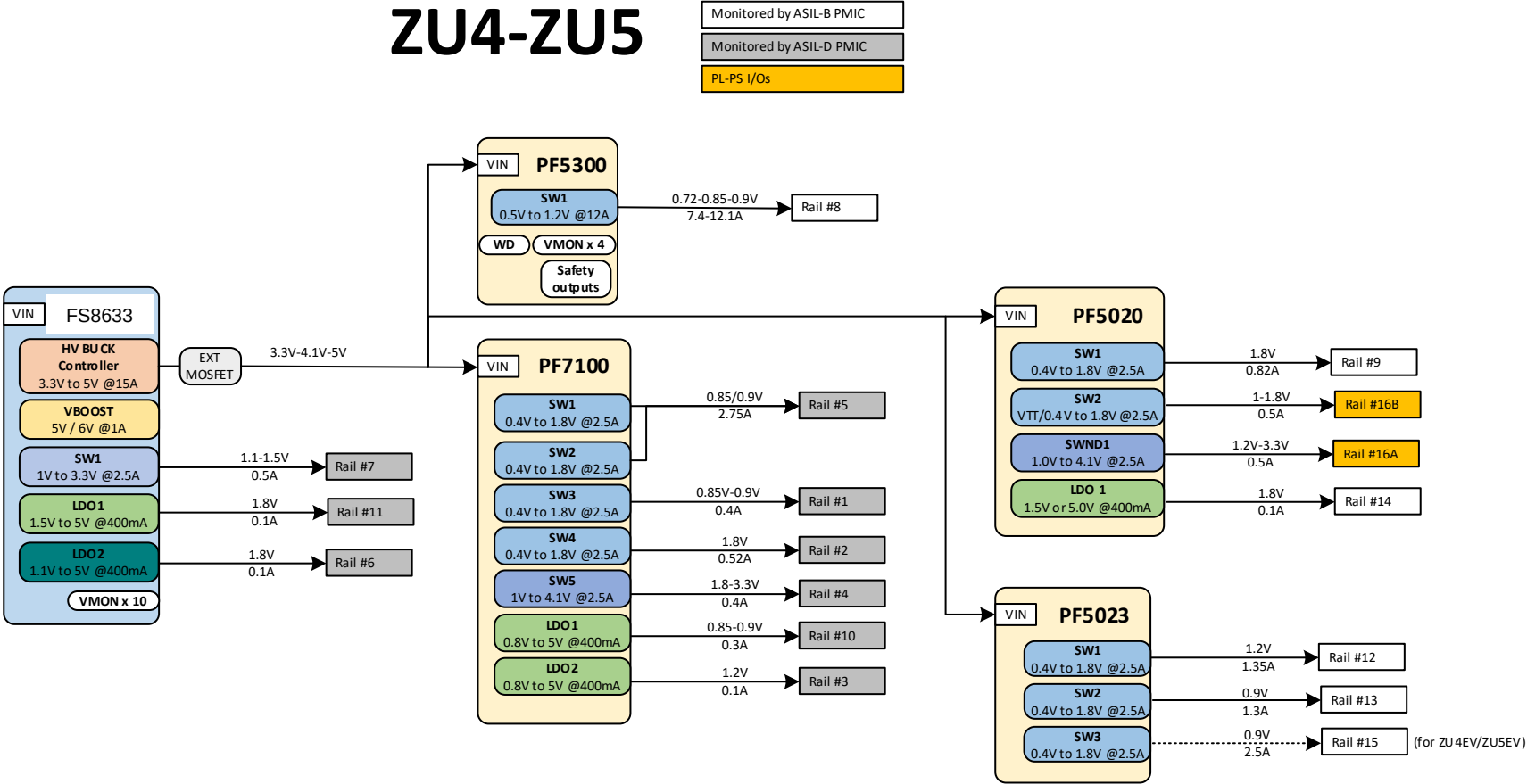
USE CASE 4: FULL POWER MANAGEMENT FLEXIBILITY, ZU2 – ZU3

ZU2-ZU3

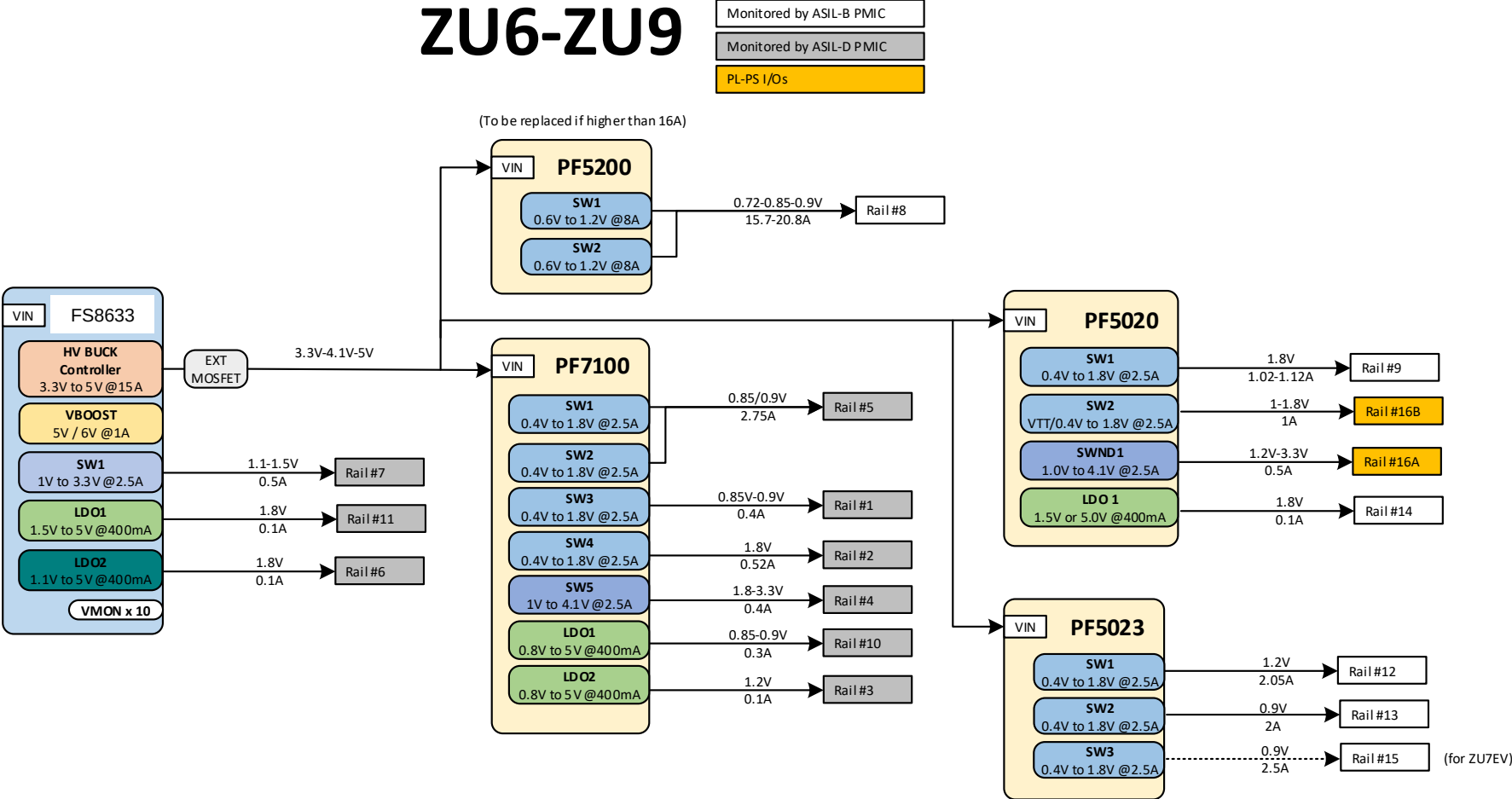
- Monitored by ASIL-B PMIC
- Monitored by ASIL-D PMIC
- PL-PS I/Os



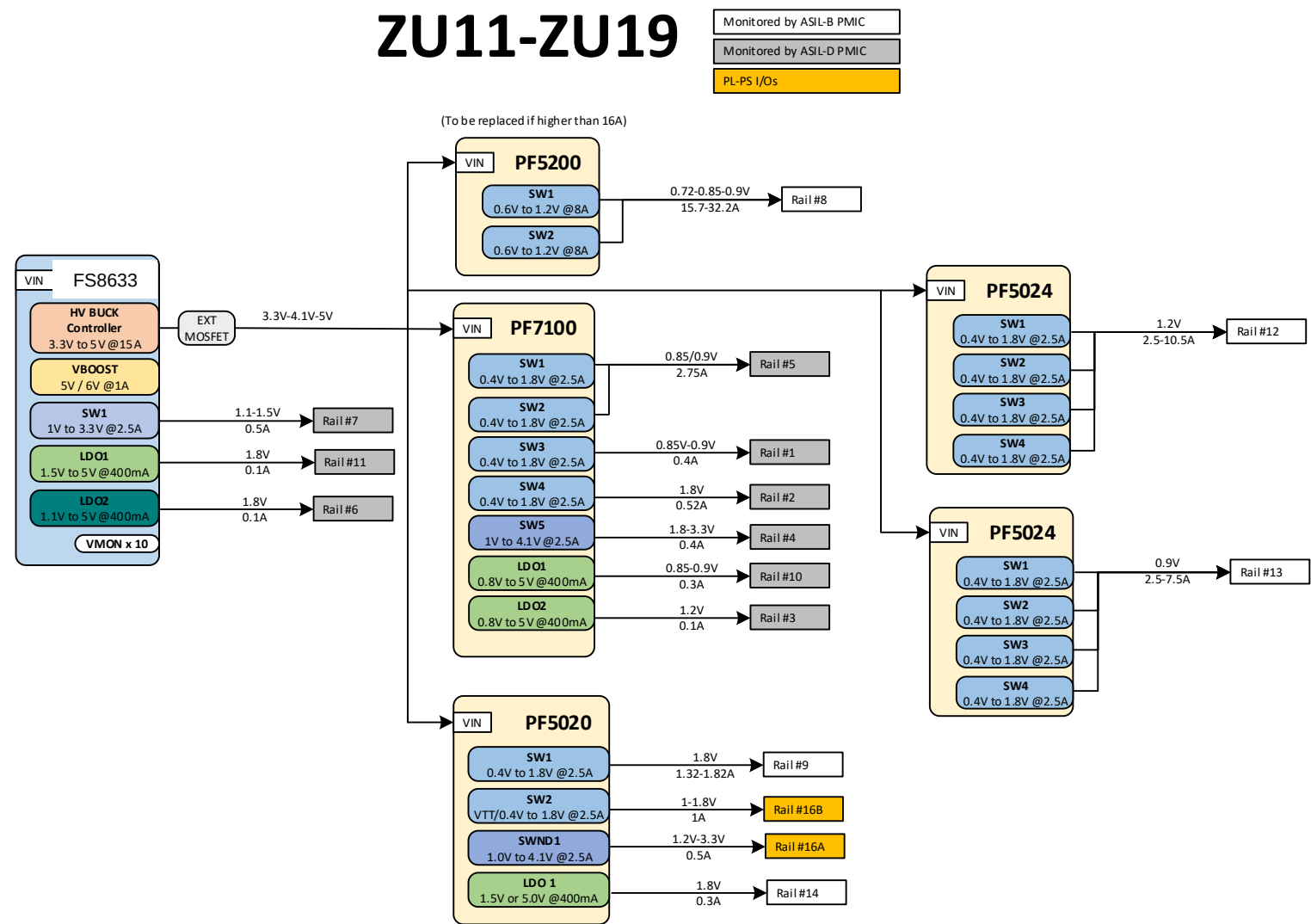
USE CASE 4: FULL POWER MANAGEMENT FLEXIBILITY, ZU4 – ZU5



USE CASE 4: FULL POWER MANAGEMENT FLEXIBILITY, ZU6 – ZU9



USE CASE 4: FULL POWER MANAGEMENT FLEXIBILITY, ZU11-ZU19

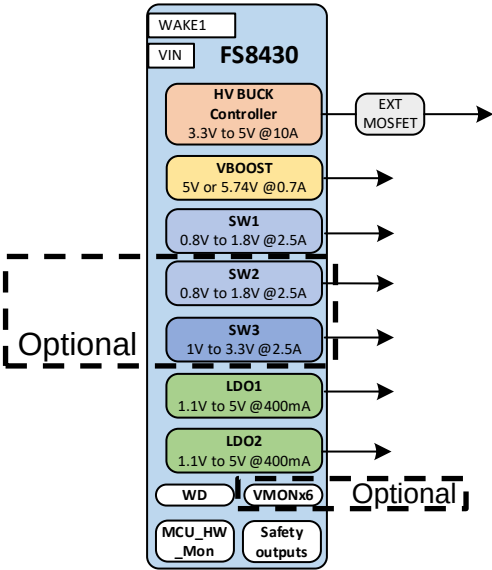


VALIDATION



NXP FS DEVICE PORTFOLIO

FS84 / FS85 – VPRE 10A
QM / ASIL B / ASIL D
QFN56



12V/24V compliant

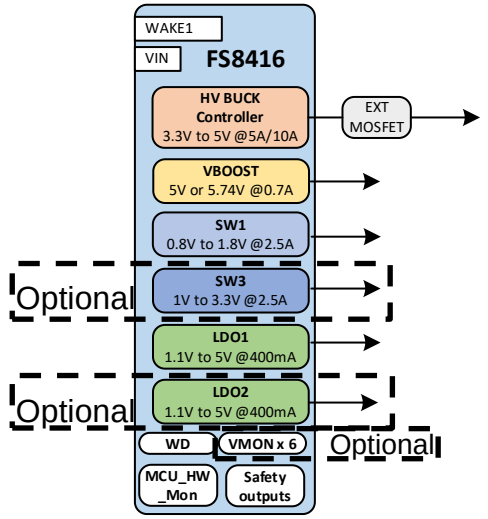
VMON accuracy +/-2%

OTP Flexibility : Power-up/down sequence configuration, settings, safety mechanisms

Safety : Safety Scalability / LBIST / ABIST / Watchdog / MCU HW error Mon / Voltage monitoring

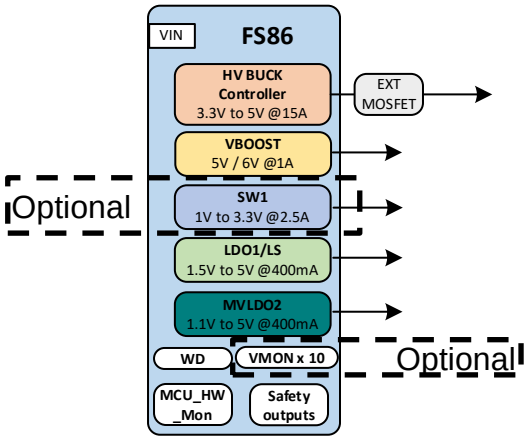
HV BUCK 450Khz/2.25Mhz / LVBUCK 2.25Mhz-2.5A

FS8416 – VPRE 5A/10A
QM / ASIL B
QFN48



12V Automotive systems

FS8600 – VPRE 15A
ASIL B/D
QFN48



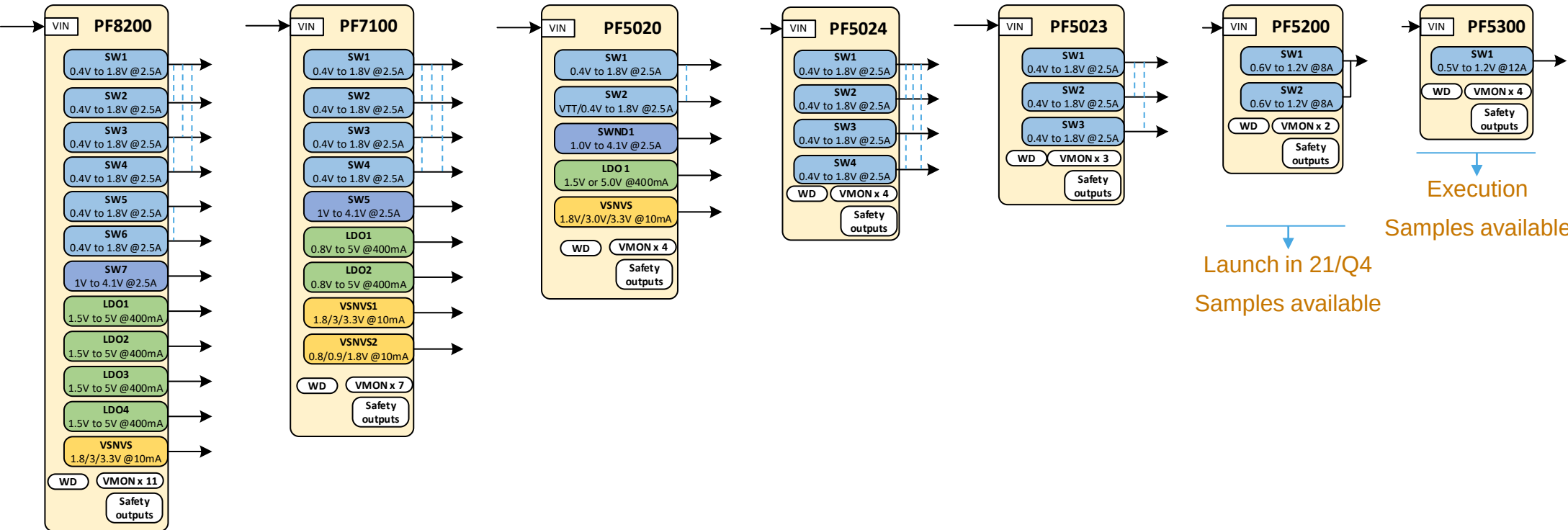
12V/24V compliant

VMON accuracy +/-1%





NXP PF DEVICE PORTFOLIO



High integration PMIC for SOC core supply (multiphase), IOs, and peripherals			High Power (SOC Core supply)	
Dynamic Voltage Scaling			AVP	
Safety : Safety Scalability (QM / ASIL B) / ABIST / Watchdog / Voltage monitoring			QM/ASIL B/ASIL D	
OTP Flexibility : Power-up/down sequence configuration, settings, safety mechanisms				
LVBUCK 2.25Mhz-2.5A				



RAIL ASSIGNMENT

Seq.	Rails	Total Tol.	Vout (V)	Transient (A/us)	Comment	NXP Block supply proposal (or equivalent IP)			
1	VCCINT, VCC_PSINTFP, VCC_PSINTLP, VCC_PSINTFP_DDR, VCCINT_IO, VCCBRAM	±3%	0.85	3.75	Up to 100A/us slew rate on VCCINT, 10A/us on other rails, allocate extra margin for supervision	PF5300/BUCK1	PF5200/BUCK12		
2	VCC_PSAUX, VCC_PSADC, VCC_PSDDR_PLL, VCCAUX, VCCAUX_IO, VCCADC, VPP(DDR)	±3%	1.8	0.9	VDD DDR power can be combined with other 1.8V	FS8500/BUCK1			
3	VCC_PSPLL, GTAVTT (GTH), VMGTAVTT (GTY)	±3%	1.2	0.5	<10mVpp steady state noise	FS8500/BUCK1	FS8500/BUCK3	FS8600/LDO2	FS8500/LDO1
4	VCCO_PSDDR	±3%	1.35	0.9		FS8500/BUCK1	FS8500/BUCK3		
5	VCCO_PSIO	±3%	1.8	0.09		FS8500/BUCK1	FS8500/BUCK3		
6	VCCINT_VCU	±3%	0.9	1.35		FS8500/BUCK1			
7	VPS_MGTRAVCC	±3%	0.85	0.125	<10mVpp steady state noise	FS8500/BUCK1	FS8500/LDO1		
8	VPS_MGTRAVTT, VMGTVCCAUX (GTH), VMGTVCCAUX (GTY)	±3%	1.8	0.3	<10mVpp steady state noise	FS8500/BUCK3	FS8500/LDO1		
9	VMGTAVCC (GTH) and VMGTAVCC (GTY)	±3%	0.9	0.125	<10mVpp steady state noise	FS8500/BUCK1	FS8500/LDO1		

NXP IP EQUIVALENCE

Rail #	Rail Block supply	Equivalent IP				
1	FS8500/BUCK1	FS8600/BUCK1	PF5024/BUCKx	PF5023/BUCKx	PF5020/BUCK12	PF7100/BUCK1234
2	FS8500/BUCK3	PF5020/BUCK3	PF7100/BUCK5			
3	FS8500/LDO1	FS8500/LDO2	FS8600/LDO1	PF7100/LDO12		
4	FS8600/LDO2					
5	PF5200/BUCK1					
6	PF5300/BUCK1					

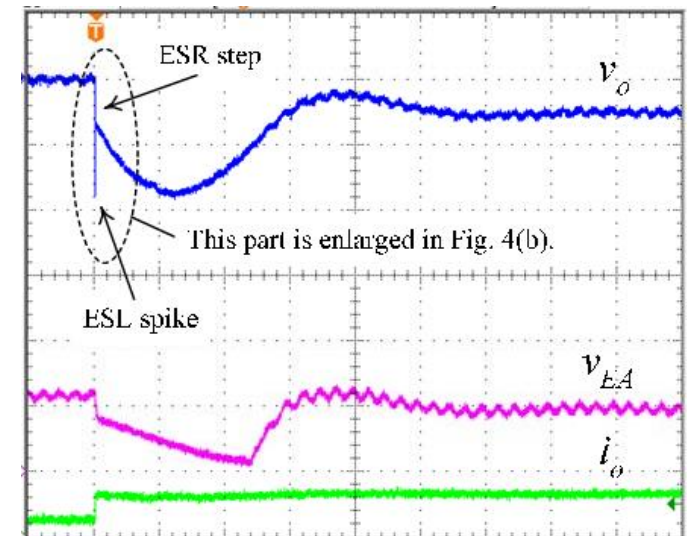
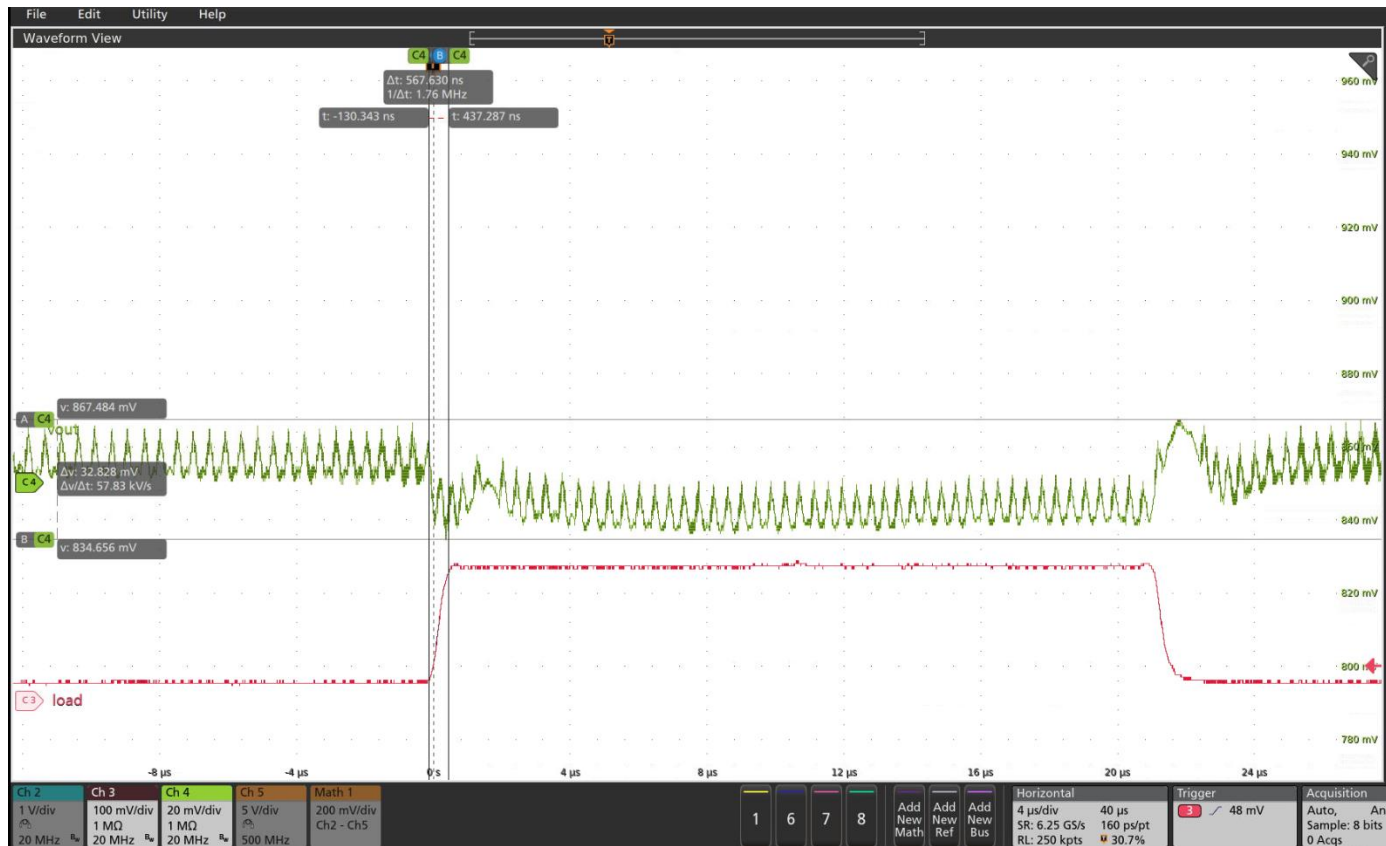
USE CASE LIST

Rail	Block	VOUT (V)	Transient (A/us)	Covered by
1	PF5300/BUCK1	0.85	4	Use Case 1
2	FS8500/BUCK1	1.8	0.9	Use Case 3
3	FS8500/BUCK1	1.2	0.5	Use Case 2
4	FS8500/BUCK1	1.35	0.9	Use Case 2
5	FS8500/BUCK1	1.8	0.09	Use Case 3
6	FS8500/BUCK1	0.9	1.35	Use Case 2
7	FS8500/BUCK1	0.85	0.125	Use Case 2
8	FS8500/BUCK3	1.8	0.3	Use Case 4
9	FS8500/BUCK1	0.9	0.125	Use Case 2

VALIDATED USE CASE

Use Case	Block	VOUT (V)	Transient (A/us)
1	PF5300/BUCK1	0.75	14
2	FS8500/BUCK1	0.8	2
3	FS8500/BUCK1	1.25	2
4	FS8500/BUCK3	1.8	2

Overall DC + AC + Ripple: 0.75V, 14A/us: 32mV (+/-2.1%)



PF5300 controlling 3rd droop

AVP and high bandwidth architecture result in <20mV peak-peak transient for a 14A/us load step with **8 x 22uF** capacitor inclusive of ripple.

For Faster speed, initial droop controlled by ESL and ESR of the caps in any case

FS8500 / BUCK1

AC Transient:

- A. 0.8V, 400mA to 1.2A, 2A/us: 19mV (2.3%)
- B. 1.25V, 400mA to 1.2A, 2A/us: 22mV (1.7%)

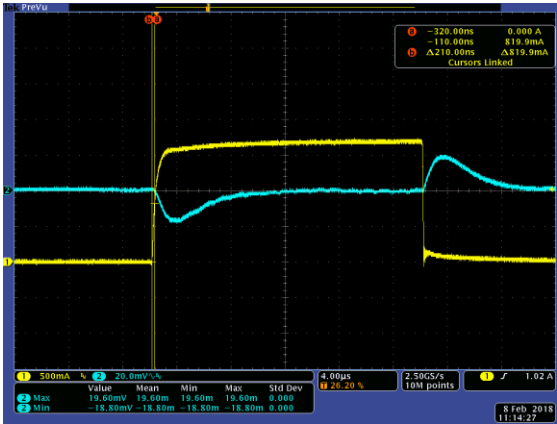
Ripple:

- C. 0.8V: 2.7mV (0.3%)

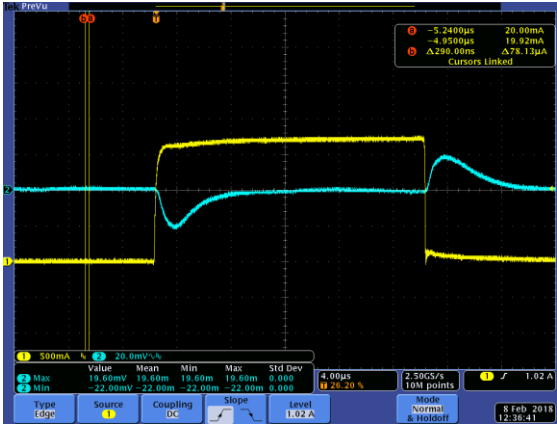
DC voltage:

Buck1 voltage (V)	BUCK1_FB (V)	error(mV)	error (%)	BUCK1_FB (V)	error(mV)	error (%)	voltage change vs load
0.4	0.4007	0.7	0.17	0.4007	0.7	0.17	0.00%
0.8	0.8004	0.4	0.05	0.8004	0.4	0.05	0.00%
1.1	1.1	0	0.00	1.0989	-1.1	-0.10	-0.10%
1.5	1.4971	-2.9	-0.19	1.4866	-13.4	-0.89	-0.70%
1.8	1.8	0	0.00	1.784	-16	-0.89	-0.89%

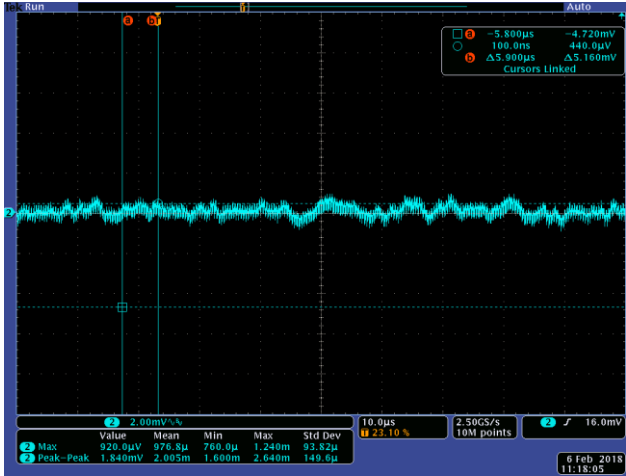
A



B



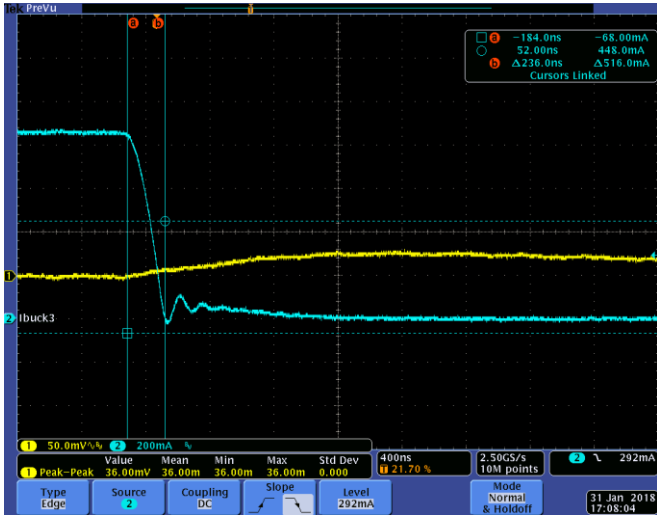
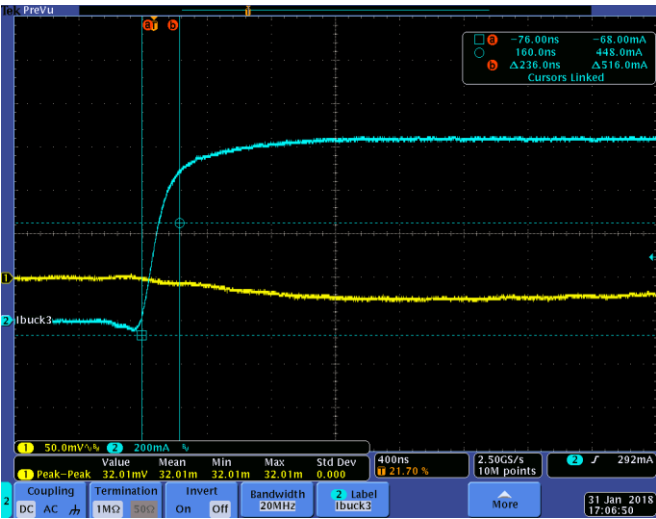
C



Summary: Worst case 2.6% at 0.8V, 2A/us. Pass

AC Transient:

1.8V, 400mA to 1.2A, 2A/us: 36mV (2%)



DC voltage:

Max 0.44%

VIN (V)	Iload(A)	VOUT (V)	%
5.5	0.1	1.1943	0.44%
5	0.1	1.1948	0.43%
4.5	0.1	1.1951	0.41%
4	0.1	1.1952	0.40%
3.5	0.1	1.1953	0.39%
3	0.1	1.1953	0.39%

Ripple:

Max 8.5mV (V: 2.7mV (0.47%))

Temp (°C)	Vout setting (V)	Vripple(mV)
25	1.2	6.00
25	2.3	6.48
25	3.3	6.08
-40	1.2	7.50
-40	2.3	8.44
-40	3.3	8.48
125	1.2	6.40
125	2.3	7.20
125	3.3	7.60

Summary: Worst case 2.9% at 1.8V, 2A/us. Pass

VALIDATION SUMMARY

Seq.	Rails	Total Tol.	Vout (V)	Transient (A/us)	Comment	NXP Block supply proposal (or equivalent IP)			
1	VCCINT, VCC_PSINTFP, VCC_PSINTLP, VCC_PSINTFP_DDR, VCCINT_IO, VCCBRAM	±3%	0.85	3.75	Up to 100A/us slew rate on VCCINT, 10A/us on other rails, allocate extra margin for supervision	PF5300/BUCK1	PF5200/BUCK12		
2	VCC_PSAUX, VCC_PSADC, VCC_PSDDR_PLL, VCCAUX, VCCAUX_IO, VCCADC, VPP(DDR)	±3%	1.8	0.9	VDD DDR power can be combined with other 1.8V	FS8500/BUCK1			
3	VCC_PSPLL, GTAVTT (GTH), VMGTAVTT (GTY)	±3%	1.2	0.5	<10mVpp steady state noise	FS8500/BUCK1	FS8500/BUCK3	FS8600/LDO2	FS8500/LDO1
4	VCCO_PSDDR	±3%	1.35	0.9		FS8500/BUCK1	FS8500/BUCK3		
5	VCCO_PSIO	±3%	1.8	0.09		FS8500/BUCK1	FS8500/BUCK3		
6	VCCINT_VCU	±3%	0.9	1.35		FS8500/BUCK1			
7	VPS_MGTRAVCC	±3%	0.85	0.125	<10mVpp steady state noise	FS8500/BUCK1	FS8500/LDO1		
8	VPS_MGTRAVTT, VMGTVCCAUX (GTH), VMGTVCCAUX (GTY)	±3%	1.8	0.3	<10mVpp steady state noise	FS8500/BUCK3	FS8500/LDO1		
9	VMGTAVCC (GTH) and VMGTAVCC (GTY)	±3%	0.9	0.125	<10mVpp steady state noise	FS8500/BUCK1	FS8500/LDO1		

- Validation shows above **Green** rails are within specification
- Above **Grey** rails can be used for specific use case less stringent

NXP PMIC ONE PAGER



FS8530 – 12/24V ASIL B/D SafetySBC

SafetySBC with Configurable Power and Safety Architecture



Power Management

- Input supply up to 60V – 12V and 24V systems
- **HVBUCK** , adjustable 3.3V to 5V, scalable output current up to 10A
 - Synchronous Buck, 455kHz or 2.22MHz, ext. MOS
- **BUCK1/2**, adjustable 0.8V to 1.8V, up to 2.5A DC – 3.6A peak
 - Synchronous Buck, up to 3MHz, int. MOS
 - Can operate in multi-phase delivering 5A
 - SVS capability on Buck1
- **BUCK3**, adjustable 1.0V to 3.3V, up to 2.5A DC – 3.6A peak
 - Synchronous Buck, up to 3MHz, int. MOS
- **BOOST** 5V or 5.74V, up to 800mA DC- 1.5A peak, int. MOS
- **LDO1/2**, configurable 1.1V to 5V, up to 400mA
- Synchronization signal for dual device operation / Power GOOD output
- Frequency Synchronization Fin/Fout.

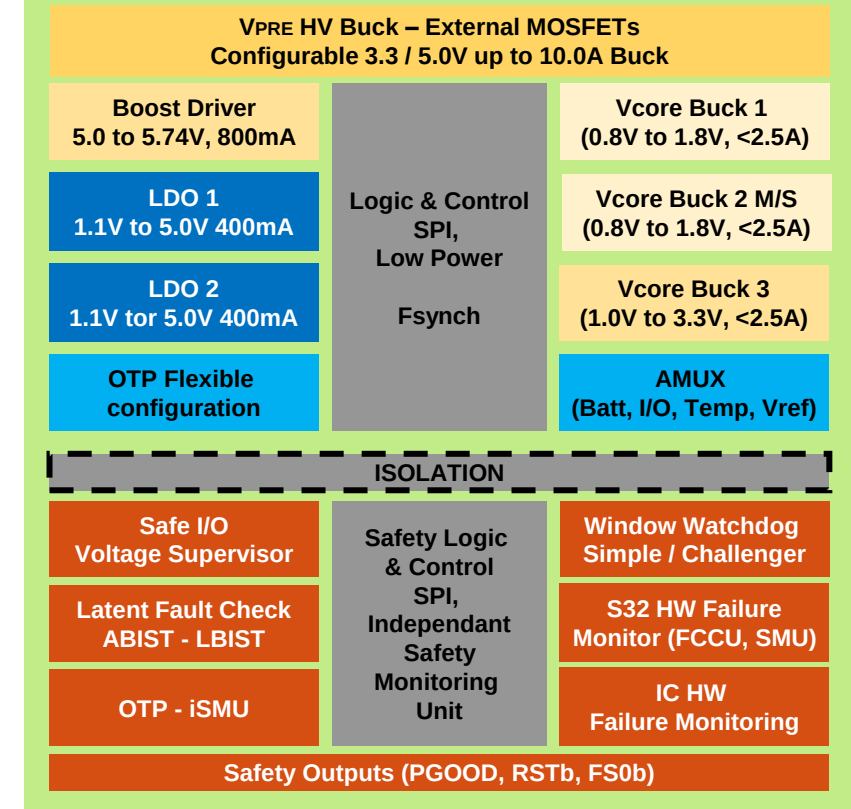
System Features

- Low Power Mode : 10µA in LPOFF, wake up via WAKE1/2 pins
- AMUX: Battery, Internal Safety critical voltages, Vref and Temperature
- Emulation and Programming capability offered in Engineering mode only : Voltage, Frequency, Phase shift, Power sequencing.
- EMC: Spread Spectrum, Freq. Synch., Vpre Slew Rate control, Freq. Tuning

Safety Features

- Independent Safety Monitoring Unit fit for ASIL D (FS85x) and fit for ASIL B (FS84x) architecture
- Control via 32 bits SPI and I2C (including CRC).

FS8530 Functional Block Diagram



Cocoon RADAR Ref Design available

FS8600 – FRONT ASIL D SBC FOR DOMAIN

ATTACH TO 12/24V BATTERY – ENHANCED FS/PF SYNC – EXTEND POWER & SAFETY SCALABILITY

Power Management

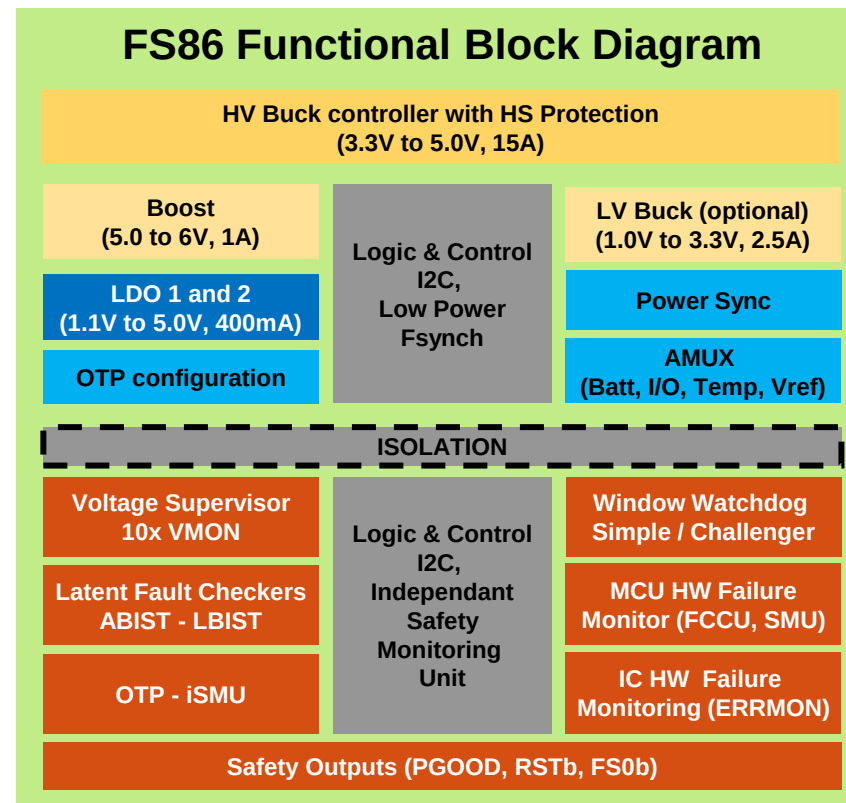
- **12V and 24V systemsv** – Input supply up to 60V
- **HVBUCK** controller, adjustable from 3.3V to 6.5V, scalable output current up to 15A DC
 - Synchronous Buck, 455kHz, **ext. MOS**
- **LVBUCK**, adjustable from 1.0V to 3.3V, up to 2.5A DC
 - Synchronous Buck, 2.25MHz, **int. MOS**
- **LVBOOST** converter, adjustable from 5V to 6V, 3% up to 1A DC, **int.MOS**
- **MVLDO**, configurable 1.1V to 5V, 3% up to 400mA
- **LDO**, load switch capable, configurable 1.5V to 5V, 3% up to 400mA
- **Meet LV124 normal cranking** specification (VBAT min = 4.5V)

System Management

- **Flexible Power Sequencing with Multi PMIC Synchronization**
- **RSTB delay** at power up
- **Low Power Mode OFF** : 15µA in LPOFF, wake up via WAKE1/2 pins compatible 3,3V
- **AMUX**: Battery, Internal Safety critical voltages, Vref and Temperature
- Emulation and Programming capability in Eng. Mode: Voltage, Freq. Phase shift, Power sequencing.
- **EMC optimized** : Spread Spectrum, Freq. Synch., Vpre Slew Rate control, Freq. Tuning

Safety Management

- Independent Safety Monitoring Unit to support ASIL D Applications
- **10 x Voltage Monitoring** configurable **2,5% to 10%**, **1% accuracy** at trim target
- I2C with CRC & Simple or Challenger Watchdog
- **MCU HW monitoring** (FCCU & SMU) with PWM capability
- EXT IC (ERRMON) monitoring



Package : QFN48eP

Samples : Now

PPAP : Q4 2021



Automotive Low Vin PMIC

PF5024 5.5V 4-Phase Buck Converter Point-of-Load

Differentiating Points

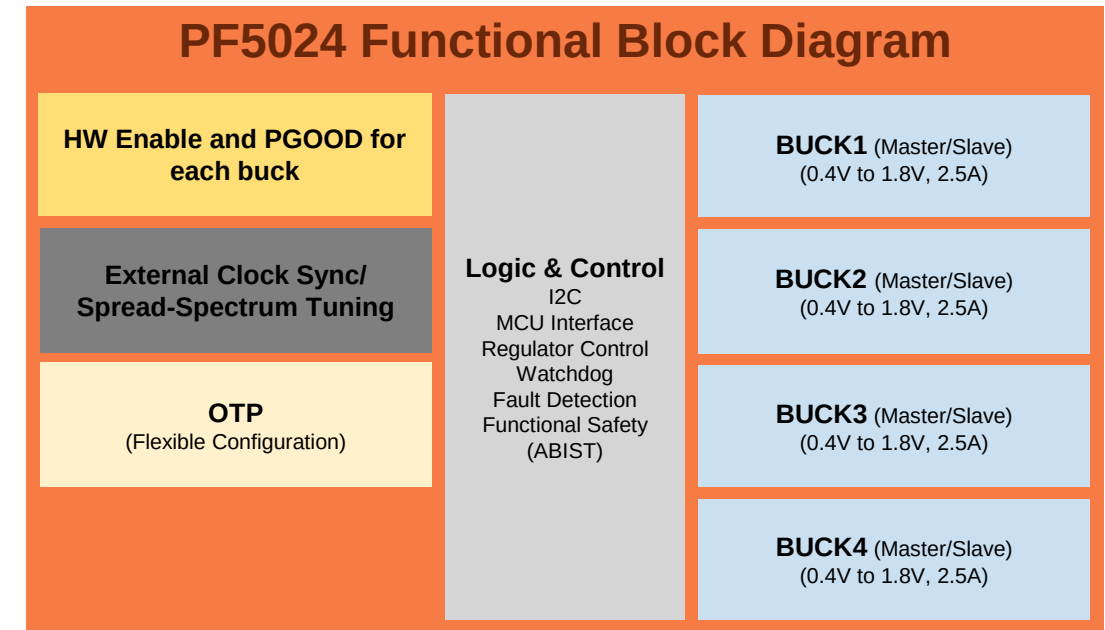
- ❑ Multiple-Phase Configurable buck regulator (Up to Four-Phase) with ASIL-B
- ❑ Hardware Control as well as I2C control
- ❑ Supports DVS, DVFS and SVS Operation
- ❑ Supports independent/dual-phase operation
- ❑ Used as companion regulator or as standalone regulator

Product Features

- ❑ Up to 10A Core/GPU supply and advanced thermal management
- ❑ Reduced noise: Spread spectrum, manual frequency tuning, frequency synchronization and dual-phase operation
- ❑ Reduced solution size through internal compensation, Total Component size of < 100mm²
- ❑ Fit for ASIL-B
- ❑ OTP configurability for scalable/flexible solutions
- ❑ -40°C to 125°C Operating Ambient Temperature
- ❑ 6mmx6mm 40LD QFN-EP Package
- ❑ Automotive and Industrial grades available

Applications

- ❑ Infotainment / Cluster / Driver Awareness
- ❑ Telematics
- ❑ V2X
- ❑ General Embedded Applications
- ❑ Point of Load Applications



Automotive Low Vin PMIC

PF5023 5.5V 4-Phase Buck Converter Point-of-Load

Differentiating Points

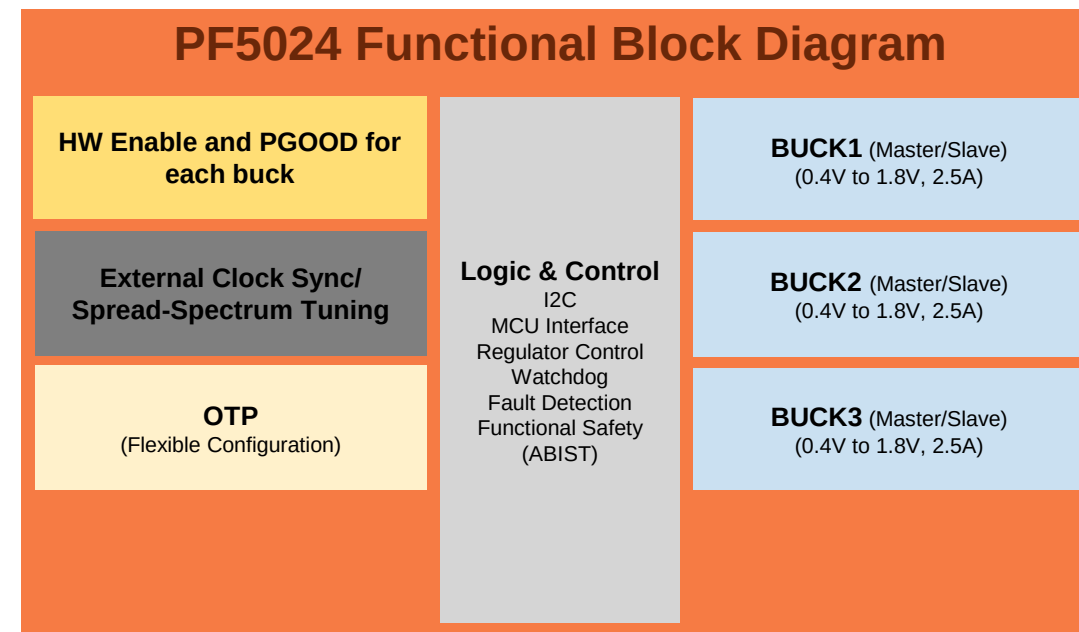
- ❑ Multiple-Phase Configurable buck regulator (Up to Three Phase) with ASIL-B
- ❑ Hardware Control as well as I2C control
- ❑ Supports DVS, DVFS and SVS Operation
- ❑ Supports independent/dual-phase operation
- ❑ Used as companion regulator or as standalone regulator

Product Features

- ❑ Up to 10A Core/GPU supply and advanced thermal management
- ❑ Reduced noise: Spread spectrum, manual frequency tuning, frequency synchronization and dual-phase operation
- ❑ Reduced solution size through internal compensation, Total Component size of < 100mm²
- ❑ Fit for ASIL-B
- ❑ OTP configurability for scalable/flexible solutions
- ❑ -40°C to 125°C Operating Ambient Temperature
- ❑ 6mmx6mm 40LD QFN-EP Package
- ❑ Automotive and Industrial grades available

Applications

- ❑ Infotainment / Cluster / Driver Awareness
- ❑ Telematics
- ❑ V2X
- ❑ General Embedded Applications
- ❑ Point of Load Applications



Automotive Low Vin PMIC

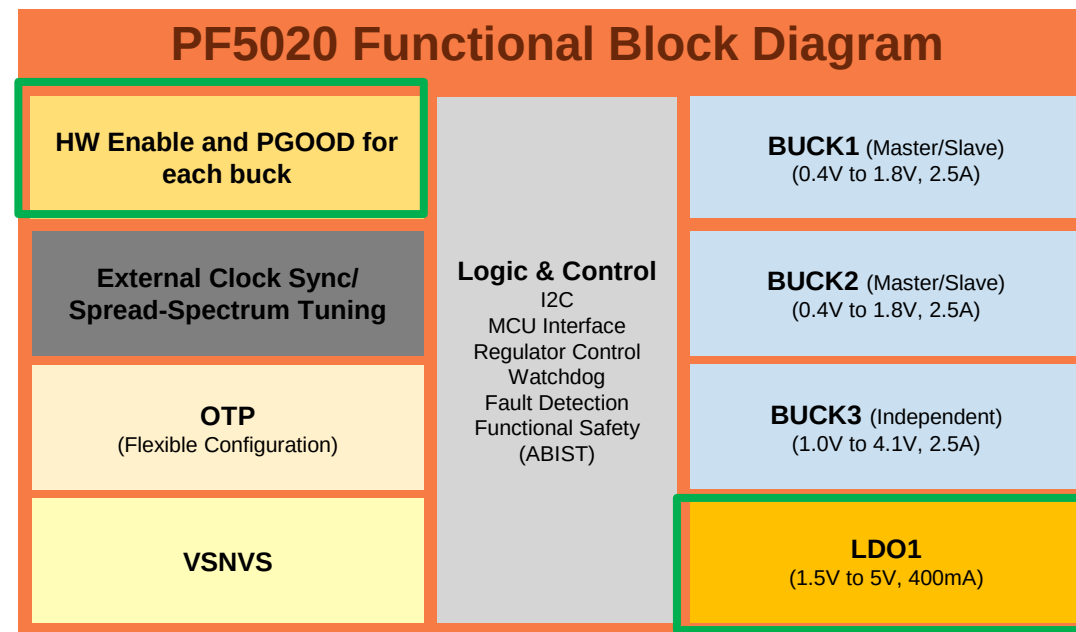
PF5020 5.5V Triple Buck Converter PMIC Companion

Differentiating Points

- ❑ Configurable Dual-Phase SOC regulator along with System regulator with ASIL-B
- ❑ Hardware Control as well as I2C control
- ❑ Supports DVS, DVFS and SVS Operation
- ❑ Supports independent/dual-phase operation
- ❑ Used as companion regulator or as standalone regulator

Product Features

- ❑ Up to 5A Core/GPU supply and advanced thermal management
- ❑ Reduced noise: Spread spectrum, manual frequency tuning, frequency synchronization and dual-phase operation
- ❑ Reduced solution size through internal compensation, Total Component size of < 80mm²
- ❑ Fit for ASIL-B
- ❑ OTP configurability for scalable/flexible solutions
- ❑ -40°C to 125°C Operating Ambient Temperature
- ❑ 6mmx6mm 40LD QFN-EP or 8mmx8mm 48LD LQFP-EP Package
- ❑ Automotive and Industrial grades available



Applications

- ❑ Infotainment / Cluster / Driver Awareness
- ❑ Telematics
- ❑ V2X
- ❑ General Embedded Applications
- ❑ Point of Load Applications

PF5200 HIGH CURRENT CORE SUPPLY

Differentiating Points

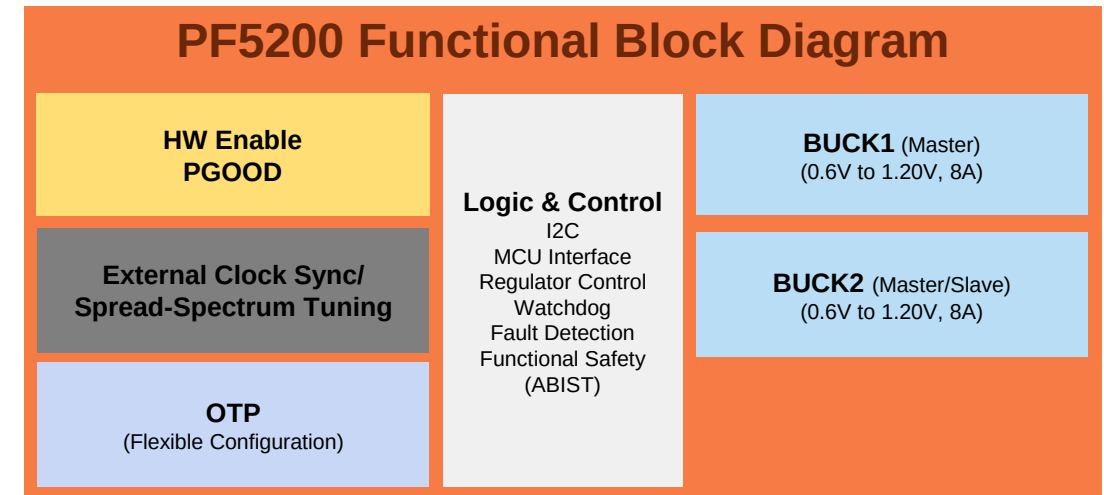
- Multiple-Phase Configurable buck regulator (Up to Dual-Phase) with ASIL-B
- Hardware Control as well as I2C control
- Supports DVS, DVFS and SVS Operation
- Supports independent phase operation
- Used as companion regulator

Product Features

- High current Core/GPU supply up to 16A and advanced thermal management
- Target efficiency >85% at 6.5A, 5V input , 0.8V output at RT
- Reduced noise: Spread spectrum, manual frequency tuning, frequency synchronization and dual-phase operation
- Fit for ASIL-B
- OTP configurability for scalable/flexible solutions
- -40°C to 125°C Operating Ambient Temperature
- 5mmx5mm 32pin FC-QFN with Wettable Flank package

Applications

- ADAS high end sensor module
- Domain controller
- General Embedded Applications
- Point of Load Applications



PF53 – 12A INTEGRATED FET CORE SUPPLY



Differentiating Points

- **Functional Safety** up to ASIL D
- **Low Shutdown Current:** 1.5 μ A
- **High Bandwidth** DC-DC with programmable AVP
- **Fast Start Up:** 500 μ s from Shutdown to Regulation
- **Proven & Robust** solution co-developed with MCU. BSP and reference designs provided.
- **Minimize EMC** with Spread spectrum, frequency tuning, frequency synchronization

Product Features

- Vin: 2.5 V to 5.5 V; Vout: 0.5 V to 1.2 V
- I2C with DVS capability can be offered as a variant
- **Programmable load-line (AVP)** with Up to 400kHz bandwidth for optimal transient response & reduced BOM cost (output capacitor reduced by 40%)
- **DC Accuracy:** +/- 1% with differential remote voltage sensing
- **Programmable OV/UV monitoring with 1% accuracy**
- Watchdog timer
- Integrated MOSFETs: 3 m Ω low side, 7.6 m Ω high side
- High Efficiency: 88% at 3.3 Vin, 0.8 Vout @10 A with > 90% peak
- -40 °C to 125 °C Operating Ambient Temperature (150°C Tj)
- Package: 3.5 mm x 4.5 mm FC-QFN package

Applications

- Gateway
- Infotainment / Cluster / Driver Awareness
- ADAS

PF53 - 12A Integrated FET Core Supply with AVP

Input Voltage: 2.5 V to 5.5 V
Output Voltage: 0.5 V to 1.2 V
Low Rdson High and Low Side MOSFETs
+/- 1% DC Accuracy
High-bandwidth loop with AVP

OV/UV Monitoring
Watchdog Timer

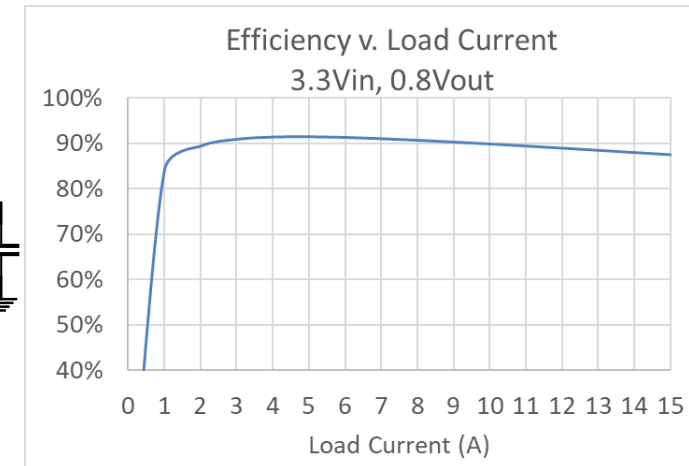
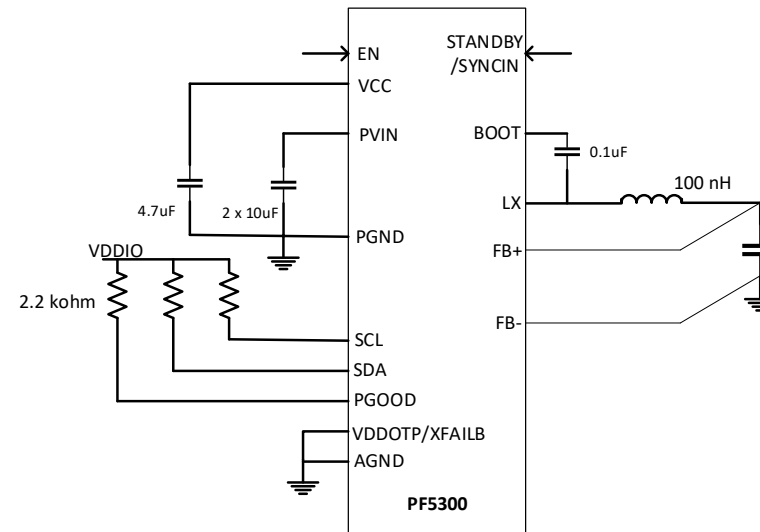
Temperature Protection

OTP Memory

ABIST

Current Limit Protection

Clock Synchronization
Spread Spectrum



3.5 mm x 4.5 mm FC-QFN package

PF7100 Automotive PMIC



Differentiating Points

- **High Power, High Efficiency** up to 5A Core supply with **tight accuracy** and advanced thermal management
- **Proven & Robust** solution co-developed with MCU. BSP and reference designs provided.
- **Scalable** supply for MCU family with OTP configurability options
- **Minimize EMC with** Spread spectrum, frequency tuning, frequency synchronization and multi-phase operation
- **Optimized Size** through advanced architecture, < 160mm² component area
- Fit for for **ASIL-B** Application

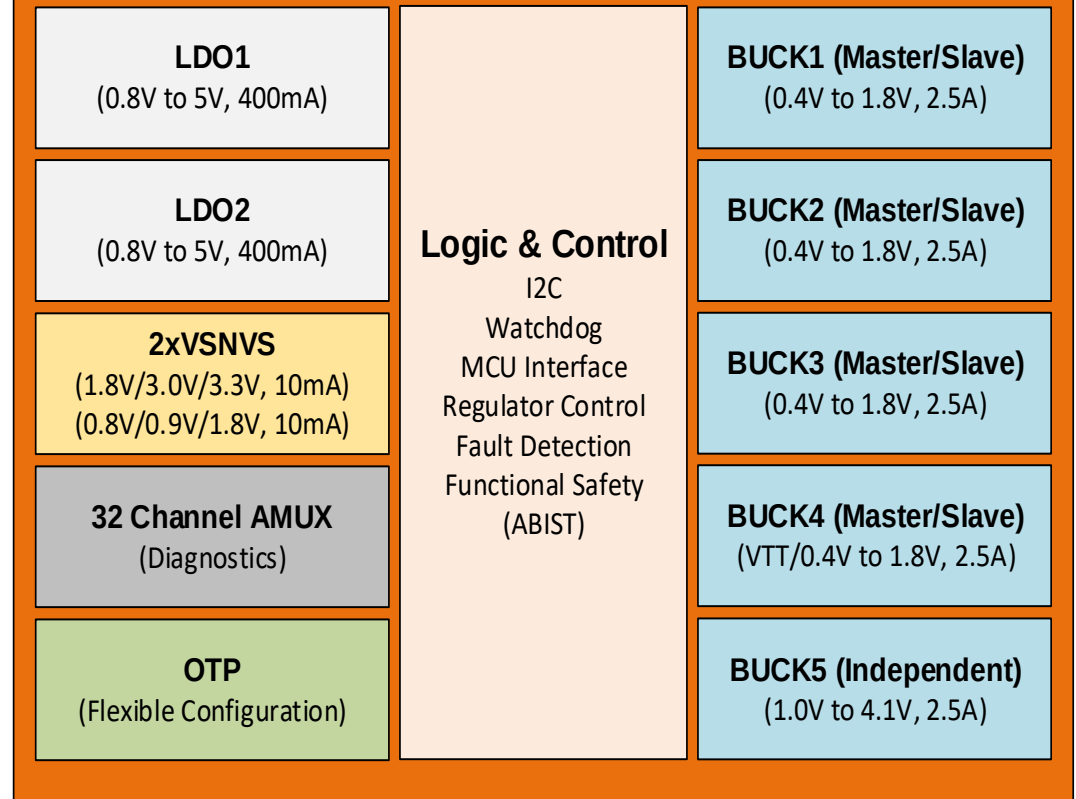
Product Features

- Vin 2.7 – 5.5 V
- 4 Buck 0.4- 1.8 V, 2.5A Master/Slave; 1 Buck 1.2- 4.5V Independent
- 2 LDO 0,8 - 5 V
- -40°C to 105°C Operating Ambient Temperature (150°C Tj)
- Prog Freq, Dynamic Freq Spread Spectrum , Ext Clock Synch
- 32 Channel AMUX, OV,UV
- Qualified for QM or ASIL-B Safety Level
- 7x7mm 48-LD QFN-EP
- Automotive and Industrial grades available (WF and non-WF Options)

Applications

- Telematics
- V2X
- SmartAntenna
- Industrial/Consumer

PF7100 Functional Block Diagram



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