DSI Bus Standard

Version 2.02

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****Implementation of the Bus Standard is governed by the terms of the Bus Standard Covenant, any changes to the specification must be agreed to by both TRW and Freescale ****

1 INTRODUCTION

1.1 Scope

This document defines the Distributed System Interface (DSI). It documents the bus topology and electrical and physical characteristics. It also defines the message protocol and classes, formats, bit transmission order, and the method of programming devices with programmable addresses. Individual device messages are defined in the documentation for those devices.

2 DSI OVERVIEW

2.1 General Overview

The DSI is a niche area network (NAN) designed to interconnect multiple remote sensor and actuator devices to a central control module. The initial target application for the network is automotive airbag systems. Some of the characteristics for this application are the need for a low cost, highly robust, moderate speed interconnection limited to two wires. In addition it must failsafe, be deterministic, and have good EMC characteristics. Even though devices with all levels of intelligence and programmability may connect to the network, remote devices must be realizable with simple state machines. Since module size is very important a minimum of components in both the central module and remote units is critical.

Airbag systems have many types of components that may be connected to the network. Typically, these components are delivered from suppliers directly to the vehicle assembly plant. Some may be embedded in instrument panels and steering columns, others in seats, potentially others in the wiring harness. The number of remote devices is typically in double digits. For these reasons it is highly desirable to allow network addressing to be self configuring at power-up. This minimizes the number of device types, and eliminates the need for special programming equipment at component suppliers and the vehicle assembly plant.

The above issues were paramount in the development of the DSI. To maintain determinism without sacrificing bus bandwidth and simplicity a single master /multiple slave configuration is used. Robustness is maintained through the use of message cyclic redundancy codes (CRC) and remote self diagnostics. High message density at moderate speeds and cost are facilitated by the simultaneous transmission of power, master commands, and slave responses. In a single ended configuration, one of the wires can be ground. An optional daisy chain interconnection method is defined which allows the assignment of network addresses at power-up with a priori device information stored in the central module.

There are two variations on this Bus Standard, Standard and Enhanced. Standard and Enhanced devices can be mixed on a bus and use Standard DSI operation. Enhanced DSI bus operation requires that all devices on the bus be compatible with the Enhanced DSI standard.

3 DSI NETWORK PHYSICAL LAYER

3.1 Introduction

The DSI is a single master multiple slave data communications bus implemented on two wires. The bus utilizes voltage mode signaling for messages sent from the master to the slaves and current mode signaling from the slaves to the master. The master may send messages to one or a combination of slaves on the bus. Slaves only transmit in response to messages sent from the master. The number of nodes on the bus is variable but is known a priori for a particular configuration. One or more DSI busses may be used in a system.

3.1.1 Network Configuration

The network is configured as a two wire multi-drop bus. Slaves may attach to the bus in daisy chain or parallel connections. The optional daisy chain connection allows the central module to establish the node addresses at power-up. The parallel configuration may be used for devices that have preprogrammed or fixed addresses. The two may be combined on one bus. Figure 3-1 shows an example network configuration.

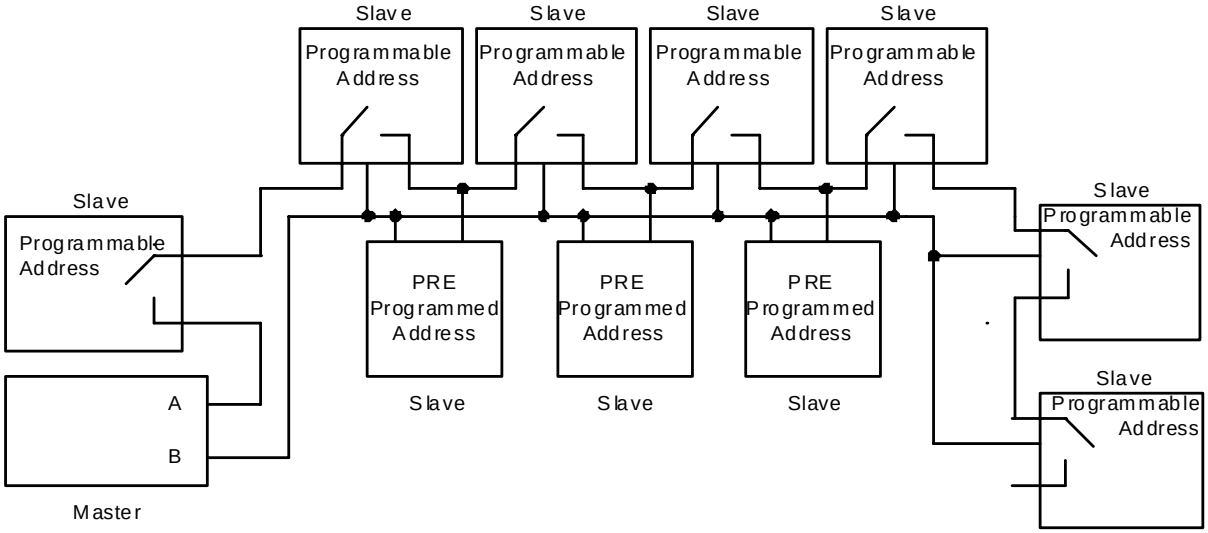

Figure 3-1 DSI Network Example

3.1.2 Number of nodes

The maximum number of nodes on a DSI bus is 16 (1 master and 15 slaves). The minimum number is 2 (1 master and 1 slave).

3.1.3 Number of DSI buses

There may be more than one DSI bus present in a system. There is no maximum limit to the number of busses allowed.

3.2 Data Bit Encoding

The DSI uses two methods of signaling - voltage mode for messages from the master to the slaves, and current mode for the responses from the slaves.

3.2.1 Voltage Mode Encoding

The voltage mode encoding uses a duty cycle modulated signal as shown in Figure 3-2.

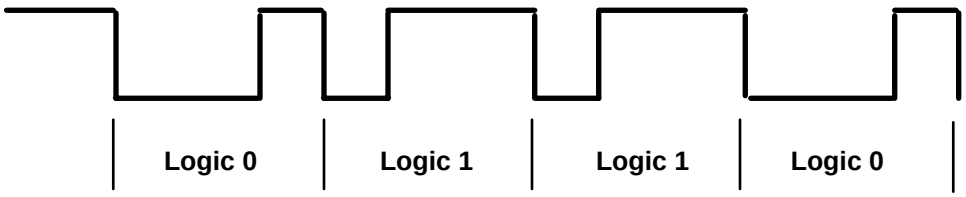

Figure 3-2 Voltage Mode Bit Encoding

Each bit time is broken up into thirds. For a logic zero the master produces a signal that is low for 2/3 of the bit time and high for the final 1/3. The reverse is true for a logic one. The slave interprets a signal that is low for more time than it is high as a logic zero, and a signal that is high for more time than it is low as a logic one.

3.2.2 Current Mode Encoding

Slave responses to commands are sent using a modulated current signal which is self synchronized to a falling edge voltage from the master. During the response time the master sends a pulse train of any combination of ones or zeros (note: this signal can be the next command message if desired, or it can be a “null” message). The current mode bits are sent during the bit time and sampled by the master at the falling edge of the voltage waveform. If a logic one is needed, the slave draws additional current from the source during the bit time. If a logic zero is needed the slave does not draw additional current during the bit time. Figure 3-3 shows a representation of the current waveform referenced to a voltage waveform.

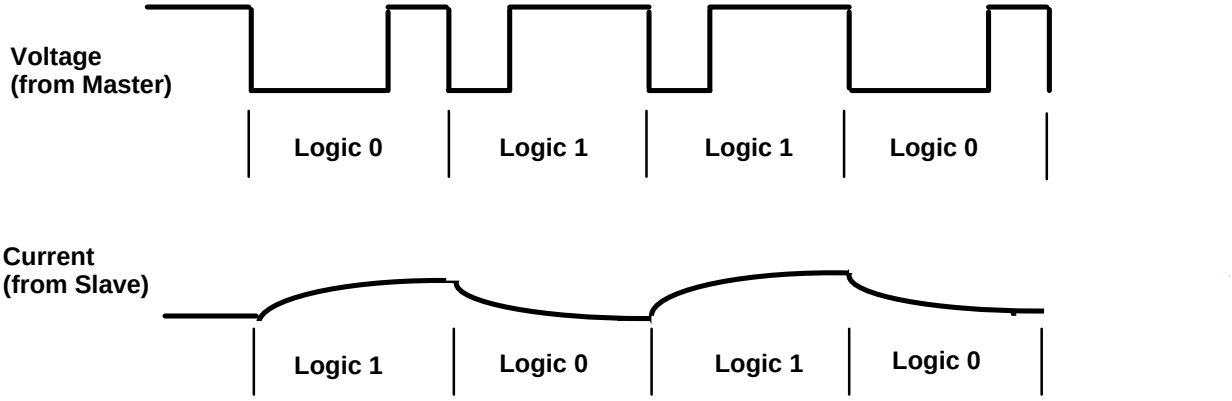

Figure 3-3 Current Waveform

3.3 Bus Voltage Levels

The voltage mode signaling uses a tri-level bus as shown in Figure 3-4. The bus idles at a voltage above the high threshold. In a single ended system, the voltage is on one of the wires. In a differential system, the voltage change may be shared between the two wires. The slave devices only detect the absolute difference in the voltage between the two wires. At the start of word time, the bus transitions below the high threshold followed by a transition below the low threshold. Data values are determined by the ratio of time spent above and below the low threshold. End of word and the end of the last bit is signaled by the voltage rising above the high threshold level. A “front porch” of approximately one bit time is added to the beginning of the word to allow the signal to transition from the idle voltage without degrading the low time of the first bit.

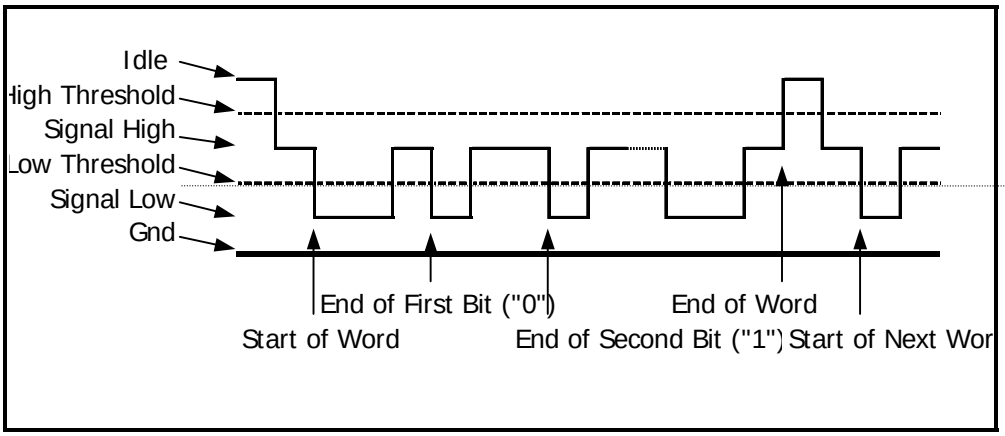

Figure 3-4 Tri-level bus

3.4 Bus Current Levels

There are two components to the bus current levels on the DSI related to signaling. The first is the quiescent current draw of the slaves (I_q) which is the sum of the quiescent currents of all of the slave devices connected to the bus. The second component is the current drawn by the slaves during signaling (I_{sig}).

3.5 Network Data Rates

The network data rate is variable within limits. The minimum data rate is 5 kbits/sec. The maximum data rate is not bound by this specification. In practice upper limits will be set by EMC and other considerations.

3.6 Electrical Characteristics

Characteristic	Min	Typ	Max	Units
Bus Current Limit Standard DSI Enhanced DSI			 150 250	 mA mA
Total Bus Equivalent Load Capacitance (C_{max})*			20	nF
Master Transceiver				
Bus Idle Voltage ($I_{out} \leq 125$ m)	7		26.5	V
Signal High Voltage (V_{outh})	4.175	4.5	4.825	V
Signal Low Voltage (V_{outl}) Single Ended Drive Differential Drive	 1.325 1.175	 1.5 1.5	 1.675 1.825	 V V
Signal Low Time for Logic Zero $T0_{lo}$	$0.9(2/3T_{bit})$		$1.1(2/3T_{bit})$	µs
Signal Low Time for Logic One $T1_{lo}$	$0.9(1/3T_{bit})$		$1.1(1/3T_{bit})$	µs
Voltage Slew Rate (V_{slew}) C < 2000 pF	0.10		8.00	Volts/µS
Received Logic Zero/One Trip Point (I_{th})	5.00	6.00	7.00	mA
Slave Transceiver				
Logic One Loading Current (I_{sig})	9.90	11	12.1	mA
Logic Zero Total Bus Loading Current (I_q)			1.6	mA
Current Slew Rate (I_{slew})	0.33		8.00	mA/µS
Bus High Threshold (V_{Th})	5.4	6.0	6.6	V
Bus Low Threshold (V_{Tl})	2.7	3.0	3.3	V
Message Characteristics				
Signal Bit Time (T_{bit})			200	µs
Start bit length (V_{th} < Vbus > V_{tl})	1/3		1	bit time
Inter Frame Separation (IFS)	4			Bits

* Equivalent capacitance for single ended drive is total capacitance from bus to return or circuit ground. Equivalent capacitance for differential drive is total capacitance from either drive line to circuit ground plus twice the capacitance between the bus drive lines.

4 DSI NETWORK DATA LINK LAYER

4.1 Message Format

DSI messages are composed of individual words separated by a minimum frame delay. Transfers are full duplex. Command messages from the master occur at the same time as responses from the slaves. Slave responses to commands occur during the next command message. This allows slaves time to decode the command, retrieve the information and prepare to send it to the master. A bus traffic example is shown in Figure 4-1.

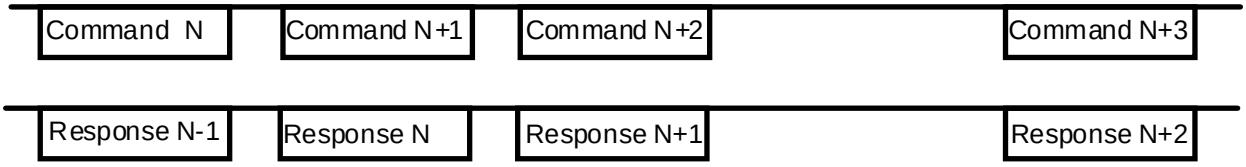

Figure 4-1 Bus Traffic Example

The example shows three commands separated by the minimum frame delay followed by a command after a longer delay. The minimum frame delay is present to allow recharge of energy storage devices in the slaves. This is necessary because the slave receives its power from the signal line. The minimum frame delay required is dependent upon several factors including the bus speed, the current consumption of the slaves and the amount of energy storage in the network.

4.2 Word Sizes

There are two word sizes, long and short. A standard DSI long word consists of 16-bits of information followed by a 4-bit cyclic redundancy check (CRC). A standard DSI short word is composed of 8-bits of information followed by the 4-bit CRC. For the target applications it is expected that most master/slave communications can be completed within one of these word sizes. However, longer messages can be composed of multiple words with an appropriately defined bit encoding.

Enhanced DSI components are capable of being set up to operate at a different short and long word sizes. At startup and after a “Clear” command has been sent on the bus, all devices will respond to standard DSI long and short word sizes. Enhanced mode devices can have the length of the CRC and non-CRC changed and by the Format Command described in 6.3.1.

4.3 Bit Order

All messages are sent with the message information bits first and the CRC last. The byte and bit transmission for the Standard DSI order is shown in Figures 4-2 and 4-3.

Enhanced DSI devices can have the length of the CRC changed in a long word.

Enhanced DSI devices can have the length of the Data and the length of the CRC changed in a short word.

The order will not be different between Standard DSI and Enhanced DSI. The byte and bit transmission for the Enhanced DSI order is shown in Figure 4-4 and Figure 4-5.

First Last

BYTE1								BYTE2								CRC			
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X3	X2	X1	X0

Figure 4-2 Standard DSI Long Command Bit Order

First Last

BYTE								CRC			
D7	D6	D5	D4	D3	D2	D1	D0	X3	X2	X1	X0

Figure 4-3 Standard DSI Short Command Bit Order

First Last

BYTE1								BYTE2								CRC
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0 to 8 Bits of CRC

Figure 4-4 Enhanced DSI Long Command Bit Order

First Last

BYTE	CRC
8 to 15 Bits of Data	0 to 8 Bits of CRC

Figure 4-5 Enhanced DSI Short Command Bit Order

4.4 CRC

At initialization the 4-bit CRC is calculated using a polynomial of X^4+1. The seed value is 1010.

The length, polynomial and seed can be changed in Enhanced DSI devices. The enhanced Long Command CRC can be changed to be between 0 and 8 bits in length. The Enhanced Short word can have the length of the data changed to be between 8 and 15 bits of data and the CRC changed to be between 0 and 8 bits. The method and structure for making this change is discussed in section 6.3.

4.5 Command Message Structure

Command messages are sent from the master to the slave.

4.5.1 Command Types

Messages from the master either follow the Standard DSI structure or the Enhanced DSI structure. They both come in two length types within these structures.

4.5.1.1 Standard DSI Long Command Structure

The Standard DSI long command structure is shown in Figure 4-6.

DATA								ADDRESS				COMMAND				CRC			
D7	D6	D5	D4	D3	D2	D1	D0	A3	A2	A1	A0	C3	C2	C1	C0	X3	X2	X1	X0

Figure 4-6 Standard DSI Long Command

The Standard DSI long commands consists of 8 bits of data, the encoded 4-bit address of the intended slave device, a 4-bit encoded command, and the calculated 4-bit CRC.

4.5.1.2 Standard DSI Short Command Structure

The Standard DSI short word command structure is shown in Figure 4-7.

ADDRESS				COMMAND				CRC			
A3	A2	A1	A0	C3	C2	C1	C0	X3	X2	X1	X0

Figure 4-7 Standard Short Command

The Standard DSI short command consists of the encoded 4-bit address of the intended slave device, a 4-bit encoded command, and the calculated 4-bit CRC.

4.5.1.3 Enhanced DSI Long Command Structure

The Enhanced DSI Long command contains the same number of non-CRC bits as the Standard DSI Long command. They are in the same order as the Standard DSI Long command. The length of the CRC can range from 0 to 8 bits and is at the end of the message. Figure 4-8 shows the Enhanced DSI Long Command structure.

DATA								ADDRESS				COMMAND				CRC
D7	D6	D5	D4	D3	D2	D1	D0	A3	A2	A1	A0	C3	C2	C1	C0	Length = 0 to 8 bits

Figure 4-8 Enhanced DSI Long Command

4.5.1.4 Enhanced DSI Short Command Structure

Enhanced DSI devices are allowed to change to a different number of data and CRC bits in the short command. The total length including CRC (if any) cannot be less than 8 bits. The non-CRC length must be at least 8 bits. If the non-CRC length is more than 8 bits, the first bits in excess of 8 are not defined by this specification. The number and use of these bits would be defined in individual device specifications. The first 4 bits after these will be the Address and the second 4 bits will be the Command. Figure 4-9 shows the Enhanced DSI Short Command structure.

Unassigned	ADDRESS				COMMAND				CRC
0 to 7 bits	D3	D2	D1	D0	D3	D2	D1	D0	Length = 0 to 8 bits

Figure 4-9 Enhanced DSI Short Command

4.6 Response Message Structure

Response messages are sent from the slaves to the master.

The length, polynomial and seed can be changed in Enhanced DSI devices. The method and structure for making this change is discussed in section 6.3.

Long responses are always sent in response to long commands and short responses are always sent in response to short commands. When the word format changes between successive commands the first response sent during the new format will be invalid since it will not have the proper number of bits.

4.6.1 Standard DSI Long Response Structure

A long response is sent from the slave to the master in response to a long command sent to the slave's address. The response is transmitted during the command following the one it is responding to. The Standard DSI long response structure is shown in Figure 4-10.

DATA BYTE1								DATA BYTE2								CRC			
D 15	D 14	D 13	D 12	D 11	D 10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X3	X2	X1	X0

Figure 4-10 Standard DSI Long Response Structure

The standard DSI long response consists of two 8-bit data bytes and the calculated 4-bit CRC.

4.6.2 Standard DSI Short Response Structure

A standard DSI short response is sent from the slave to the master in response to a short command from the master to the slave's address. The response is transmitted during the command following the one it is responding to. The short response encoding is shown in Figure 4-11.

DATA								CRC			
D7	D6	D5	D4	D3	D2	D1	D0	X3	X2	X1	X0

Figure 4-11 Standard DSI Short Response Structure

The Standard DSI response consists of one 8-bit data byte and the calculated 4-bit CRC.

4.6.3 Enhanced DSI Long Response Structure

The Enhanced DSI Long response contains the same number of non-CRC bits as the Standard DSI Long response. They are in the same order as the Standard DSI Long response. The length of the CRC can range from 0 to 8 bits and are at the end of the message. Figure 4-12 shows the Enhanced DSI Long response structure.

DATA																CRC
D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	0 to 8 bits (Same as command CRC bits)

Figure 4-12 Enhanced DSI Long Response Structure

4.6.4 Enhanced DSI Short Response Structure

Enhanced DSI devices are allowed to change to a different number of data and CRC bits in the short response. The overall number of bits will be the same as in the Enhanced DSI short command. The number of CRC bits is also the same as in the command. The non-CRC length must be at least 8 bits. Figure 4-13 shows the Enhanced DSI Short Response Structure.

Data	CRC
8 to 15 bits (Same as non-CRC command bits)	0 to 8 bits (Same as command CRC bits)

Figure 4-13 Enhanced DSI Short Response Structure

4.7 Error Checking

The master and slaves calculate a CRC on the information portion of their received messages. The message is valid only if the calculated CRC matches the CRC sent as part of the message. An error bit is set in the master when it receives an invalid message. The slaves discard and ignore all invalid received messages and in addition do not respond to them.

5 Section 5 DSI Addressing

5.1 Introduction

This section establishes a method for device addressing and programming slave addresses in the system.

5.2 Slave Device Addressing

Each slave device on the bus must be given a unique 4-bit address. The address may be pre-programmed into the device or it may be programmed using the technique described in section 5.3. When address 0 is used, it is called a global command and all devices are addressed at once. Generally, devices do not respond to global commands. The device address encoding is shown in Figure 5-1.

A3	A2	A1	A0	Slave Number
0	0	0	0	All Slaves
0	0	0	1	Slave 1
0	0	1	0	Slave 2
0	0	1	1	Slave 3
0	1	0	0	Slave 4
0	1	0	1	Slave 5
0	1	1	0	Slave 6
0	1	1	1	Slave 7
1	0	0	0	Slave 8
1	0	0	1	Slave 9
1	0	1	0	Slave 10
1	0	1	1	Slave 11
1	1	0	0	Slave 12
1	1	0	1	Slave 13
1	1	1	0	Slave 14
1	1	1	1	Slave 15

Figure 5-1 Slave Address Encoding

5.3 Programmable Devices

In the optional daisy chain programmed device, after system power up the master must set the address of daisy chain slave devices with addresses before network communications can commence. Programmable devices have a bus switch on the power/signal line. At power up programmable device bus switches must be open and remain open until an initialization or reverse-initialization message is received.

Since the first bus switch is open, the bus only goes as far as the first slave. When the master sends a slave initialization command the first slave device stores its address information and closes its bus switch. Now the second daisy chain slave is connected to the network. When the master initializes the second slave's address, the first device responds with an initialization response message. The response message echoes the programming information back to the master so that it knows that the address was successfully established. The initialization response message is sent only once by each slave after receiving a program address command message.

5.4 Pre-programmed Devices

Slaves that are pre-programmed do not require a bus switch. If they have a bus switch, it will be open following power-up. On power-up the stored pre-programmed address becomes the slave address. However, pre-programmed devices still must receive an Initialization or reverse-initialization command and reply with an initialization or reverse-initialization response before responding to any other bus commands. The Bus Switch (if included) will be controlled by the initialization or reverse-initialization command similar to a programmable command.

6 Section 6 Commands

6.1 Introduction

All DSI devices are required to decode and respond to certain commands which are used to configure and control the bus regardless of what type of part it is. This section covers those commands, their options and the required response if any.

6.2 Standard DSI Commands

6.2.1 Initialization Command (0000)

Initialization commands are used to activate the device on the bus. This command will be ignored if not applied to the bus switch input terminal. In the case of un-preprogrammed devices, this command will set the address for the part to use. Figure 6-1 shows the structure of the data portion of a long word command in an initialization command. This command will also control the bus-switch closure in Enhanced DSI devices which contain a bus-switch.

Initialization will use a global address for programmable devices and specific addresses for pre-programmed devices.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DD	BS	DD	DD	PA3	PA2	PA1	PA0

Figure 6-1 Initialization Command Structure

DD = Device Dependent. Value and function are not restricted or controlled by this standard.

BS = (Enhanced DSI devices with a bus-switch) A “1” will cause the bus switch to be closed. A “0” will cause it not to be closed. Actual bus-switch closure may be subject to fault checking in the device.

PAn = Address to set this device to if un-programmed. Address of programmed device if pre-programmed.

An un-programmed device will be addressed globally (address = 0). A pre-programmed device requires the use of its address when sending this command.

6.2.2 Reverse Initialization Command (1111)

Reverse Initialization commands are used to activate the device on the bus similar to Initialization commands. The difference is that it will be ignored if not applied to the bus switch output terminal. In the case of un-preprogrammed devices, this command will set the address for the part to use. Figure 6-1 shows the structure of the data portion of a long word command in a reverse initialization command. This command will also control the bus-switch closure in Enhanced DSI devices which contain a bus-switch.

Reverse-Initialization will use a global address for programmable devices and specific addresses for pre-programmed devices.

6.2.3 Clear Command (0111)

The clear command is used to reset the devices on the bus. This will cause them to go back to the state they are in following power-up and before initialization. Enhanced devices will return to standard DSI formatting following this command.

The clear command can use the global address to clear all of the devices on the bus with a single command.

6.3 Enhanced DSI Command

Enhanced DSI devices can allow the length of the short word, the length of the CRC, the seed of the CRC and the polynomial of the CRC to be changed.

The global address can be used to format all the devices at the same time and cause them to switch modes with a global write command changing the Format Selection register in all devices on the bus with a single command.

6.3.1 Format Control (1010)

On power-up or following a “Clear” command, the device will use the standard DSI word length and standard CRC length, polynomial and seed.

The registers associated with Format Control will default to values which correspond to Standard DSI operation upon power-up or at the issuance of a “Clear” command.

Changes made to the Format Control register will not become active until the 4 bits of the format selection register are set during a single write command. It will not switch back to Standard DSI settings unless all 4 bits of the format selection register are cleared by a single write.

The Format Control command is a Long Word Command and contains 8 bits of data which are used to determine read or write, the specific format control register, and the data to be written/read.

If the R/W bit is set, the value in the Data Bits will be written to the format control register pointed to by the 3 bit format register address. If the R/W bit is clear, the bits in the register pointed to by the format register address will not be changed, but the values in it will be returned in the following response from the device.

The response to this command will be the data that was written/read by the command.

The data bits for this command are defined as follows:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R/W	Addr 2	Addr 1	Addr 0	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0

Figure 6-2 Format Control Data Bits

R/W = Write when bit is “1”. Read when bit is “0” and it is not a global command.

Addr n = Address of register as defined in Figure 6-3.

Data Bit n = Data to be written to register when in Write mode.

Figure 6-3 shows the data field of the command for each of the Control Registers.

Format Control Register Address	Description
0	CRC Polynomial – Low Nibble
1	CRC Polynomial – High Nibble
2	Seed – Low Nibble
3	Seed – High Nibble
4	CRC Length (0 to 8)
5	Short Word Data Length
6	Reserved
7	Format Selection

Figure 6-3 Format Control Registers

6.3.1.1 CRC Polynomial

The CRC Taps control the feedback for the CRC Polynomial. The MSBit represents the $X^{7.}$ The LSBit represents X^0 or the value 1 if set or 0 if not set. The standard DSI CRCof X^4+1 would be obtained by loading ‘0001’ into Format register 0 and ‘0001’ into Format Control register 1. On a reset or clear, the standard DSI CRC taps are loaded into these registers.

6.3.1.2 Seed

The Seed is the starting value loaded into the CRC checking registers before each transaction starts. The default DSI seed of ‘1010’ would be selected by loading ‘1010’ into control register 2 and ‘0000’ into control register 3. On reset or clear, the standard DSI seed is loaded into these registers.

6.3.1.3 CRC Length

The CRC length value can range from 0 (no CRC checking performed) to 8 (8 bits of CRC checking. On a reset or clear, the value in this register defaults to 4. Attempting to write a value higher than 8 to this register will cause the write to be ignored. The standard DSI CRC length would be set by loading ‘0100’ into this register.

6.3.1.4 Short Word Data Length

The Short Word Data Length controls the number of bits of data in a short word. This can be set from 8 to 15. On a reset or clear, the value in this register defaults to 8. If a number less than 8 is written to the register, it is ignored and the contents of the register are not changed. The standard DSI short word data length would be set by loading ‘1000’ into this register.

6.3.1.5 Format Selection

The Format selection determines whether the standard DSI values will be used or the values in the Format register. The switch to the values in the format registers occurs when ‘1111’ is successfully written to control register 7in a single command. If the register is currently cleared, and one of the data bits is not received as a “1”, the data in the register will remain all zeroes and the device will not use the Format register settings. A switch back to standard DSI occurs when a ‘0000’ is successfully written to control register 7. If the registers bits are all set, and one of the bits is received as a “1”, the value of the bits in the register will remain ‘1111’ and the switch back to Standard DSI values will not occur. This is done to reduce the possibility of switching operation modes due to a corrupted command.