FTF FREESCALE TECHNOLOGY FORUM 2015

Driving Efficiency with the S32V Vision Accelerators

FTF ACC-F1178

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J U N E . 2 0 1 5

freescale™

External Use

Agenda

- Freescale S32V Family
  - Target Applications
  - Block Diagram
  - Accelerator Architectures
- Neusoft Overview
- Challenges and Difficulties
- S32V Based Solution
- Lab Demo Introduction
- Roadmap Based on S32V
- Summary

S32V: Target Applications

ADAS applications are increasingly deployed in Co-Piloted functions:

For Example:

- Autonomous Emergency Brake (AEB)
- Lane Departure Correction (LDC)
- Pedestrian Protection (PD)
- Sensor Fusion

- **Freescale's S32V234:**

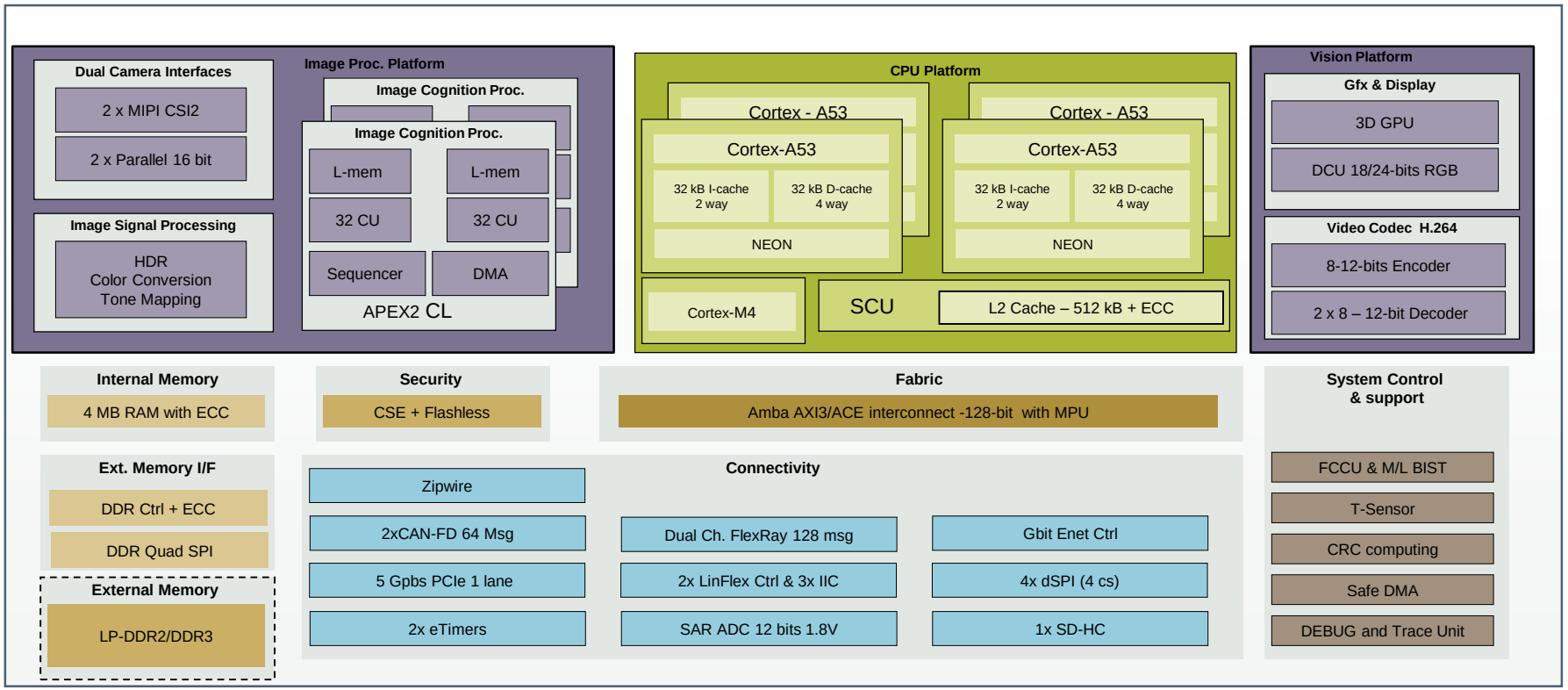
✓ Fully targeted at ISO 26262 ASIL B

✓ Hardware security encryption to protect against malicious hacking

✓ Designed to exacting automotive requirements

✓ Manufactured for robustness and long term automotive reliability

S32V234 – ADAS MCU



Specifications:

- **CPU1-4:** ARM® Cortex®-A53 @ 1 GHz, L1/L2 cache with ECC & Neon
- **CPU5:** Cortex-M4 for IO control with I/D Cache and ECC
- **ICP:** 2 x APEX2 CL (MIMD APU-64 CU each) at 400 MHz
- **GPU:** GC3000 from Vivante
- **Package:** 17x17**FC-BGA**
- **Temp Range (Ta):** -40 to 105 °C, 125 °C Tj, AEC-Q100 Grade 2
- **Main Supply:** 3.3 V IO and 0.94 V Core - external PMU + DDR rails

Key Features:

- **F. Safety:** developed as per ISO 26262 with target ASILB
- **SW Enablement:** OpenCL Tools for ICP, GPU, NEON.
- **Video Codec:** H.264 Encoder (8–2-bit) + Decoder (8–12-bit)
- **DRAM:** External LPDDR2 & DDR3 supported
- **Security:** SHE compliant Crypto Security Engine
- **Surround 3D**: 3D unified architecture. 19/38 Gflops at 600 MHz
- **Video dist. Network**: 2X MIPI CIS2 – 4 Virtual channels each
- **Connectivity**: Gbit Ethernet, PCIe, FD-Can & Flexray

S32 V230 Family – Options

Automated Drive
Sensor Fusion
Many Core
ASIL B – D

Surround View
Surround Sense and stitching
Many Core
ASIL B – C

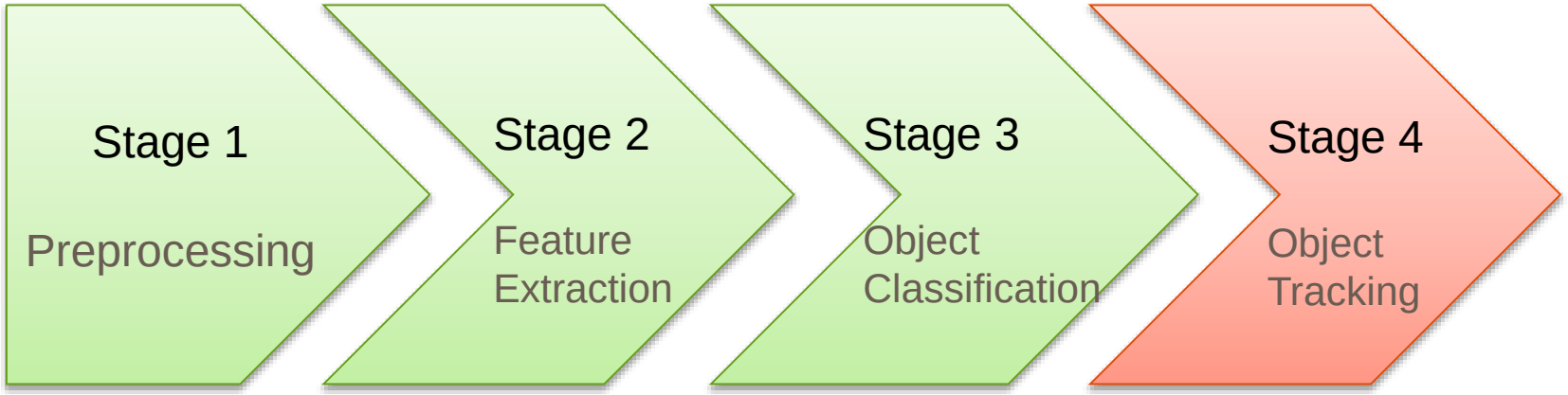
Front / Rear Vision
Vision NCAP
Many Core
ASIL B – C

ASIL B	Dual Core	Quad Core	3D GPU	ISP	APEX	Security
✓	✓	✓	Optional	N/A	Optional	✓
✓	✓	✓	✓	Optional	✓	✓
✓	✓	✓	N/A	Optional	✓	✓

Vision Accelerators on S32V

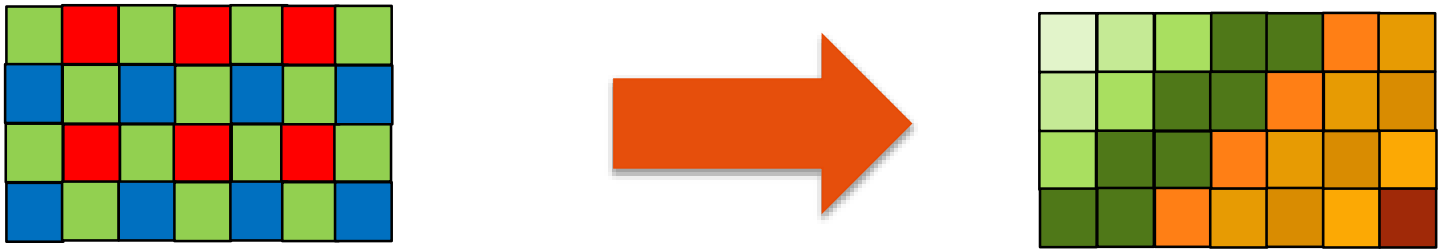
Processing steps of a typical Vision Pipeline

Processing Steps



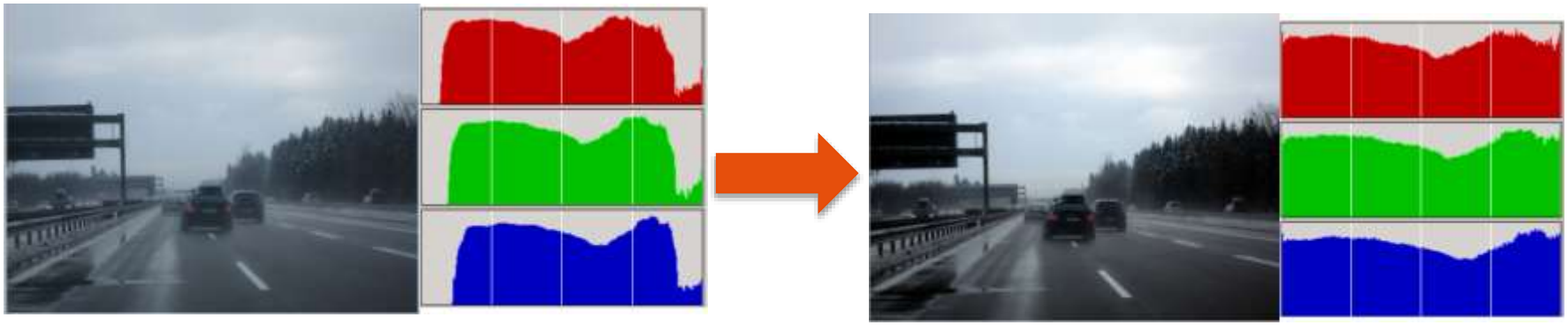
Step 1: Preprocessing

- **De-Bayer**

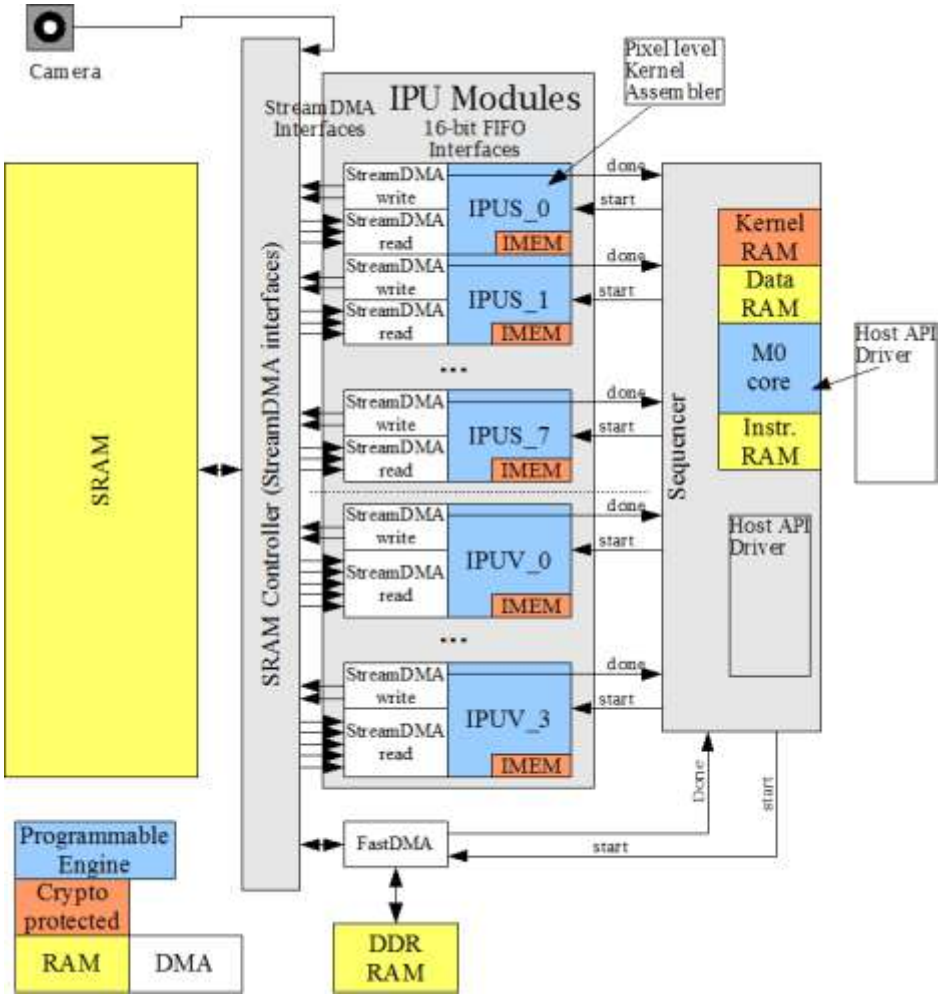


Sensor pixel array

- **White balance, Contrast equalization**



Step 1+2: Preprocessing + Feature Extraction ISP



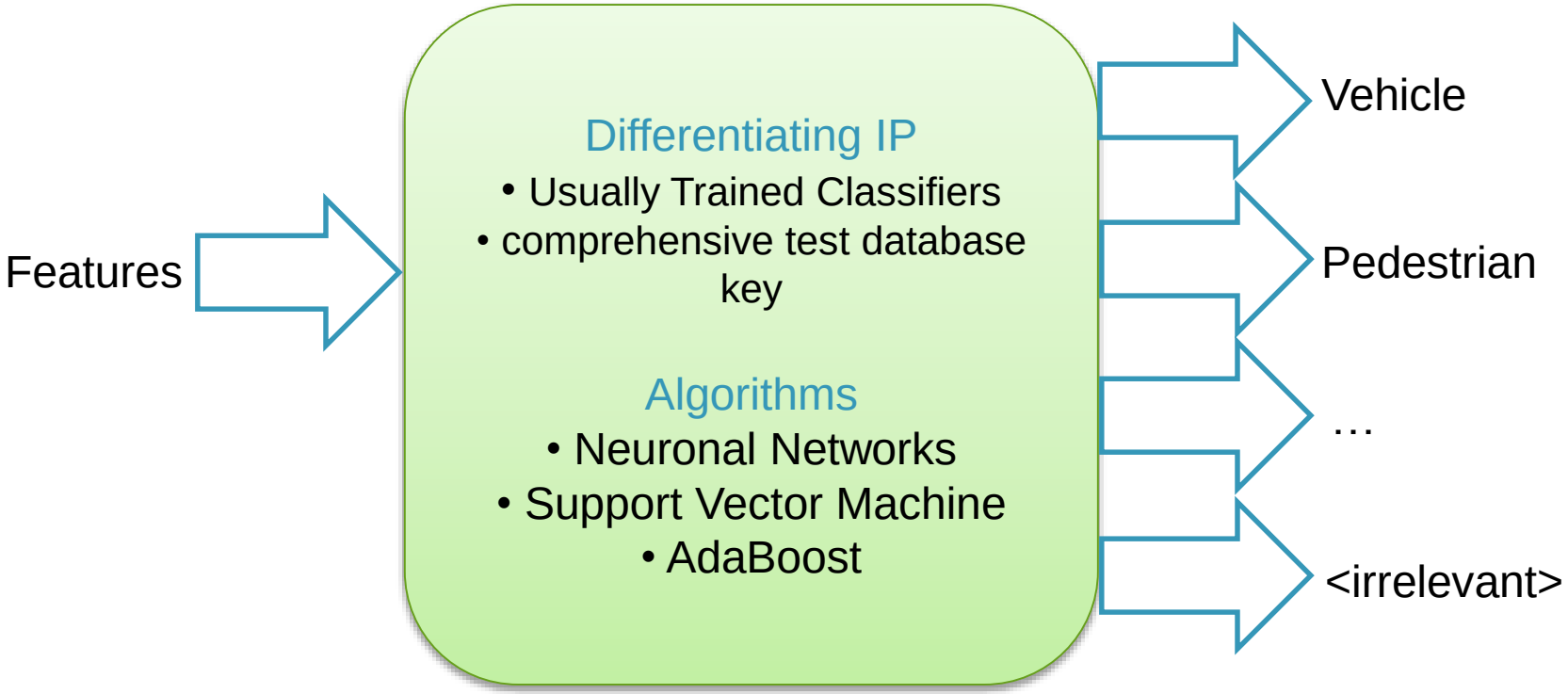
Step 2: Feature Extraction

Source Picture

Harris Corner (Corner Detector)

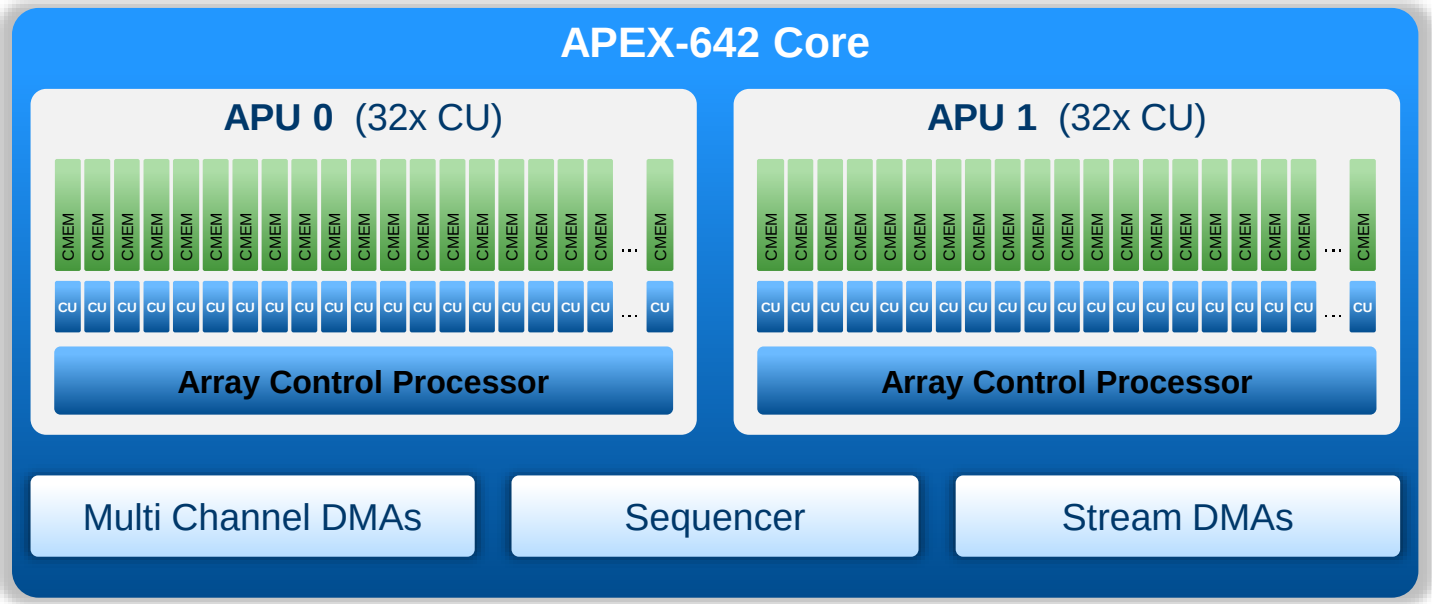
M.Staudenmaier

Step 3: Classification



Step 2+3: Feature Extraction + Classification APEX2

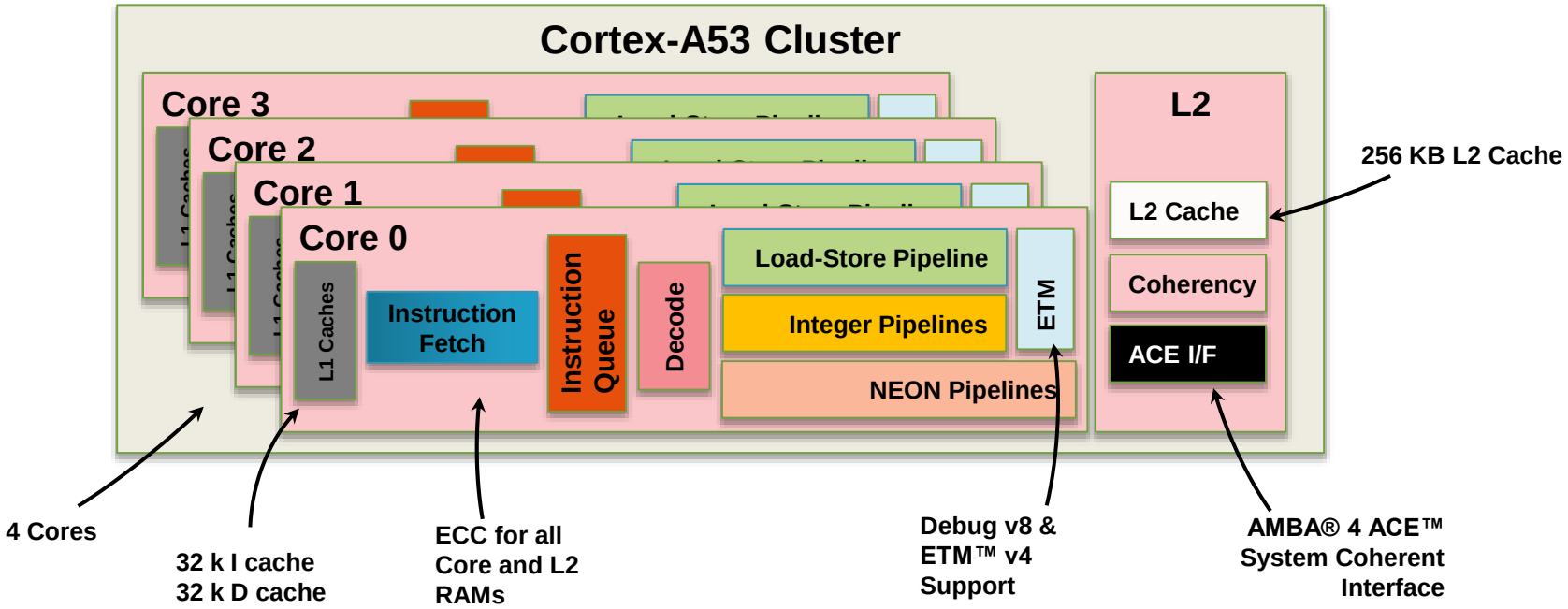
- **Features**
  - Massively Parallel SIMD for vector processing (CU's + 4 KB CMEM per CU
  - Array Control Processor (ACP) for scalar processing, access to external and internal memory
  - MC-DMA for efficient instruction and data movement
  - Stream DMA for pixel data in/out of CMEM
  - Sequencer off-loads ACP for data and instruction and sequencing



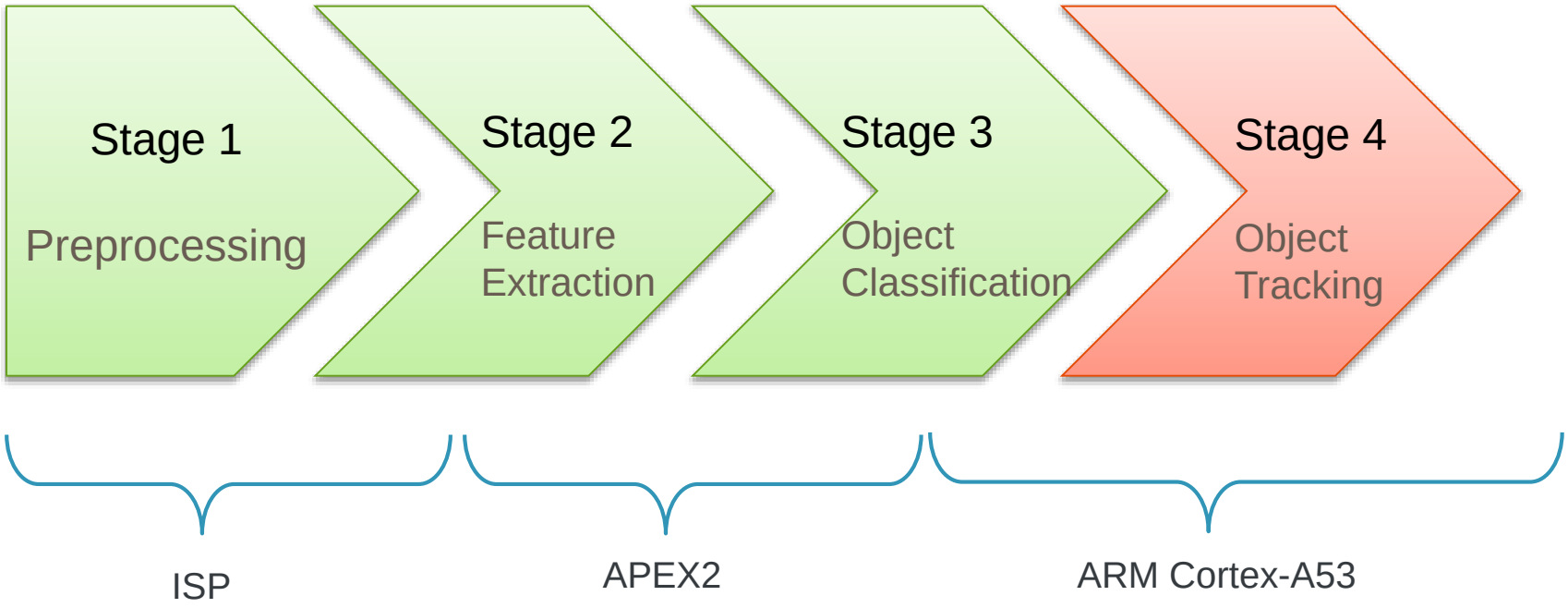
Step 4: Object Tracking

Step 3+4: Classification + Object Tracking

- Up to 4 * ARM Cortex-A53 @ 1 GHz
  - Cortex-A53 8-Stage in-order LITTLE pipeline
    - 2.3 DMIPS/MHz
    - Target Frequency – 1 GHz
    - Total Performance - 9200 DMIPS

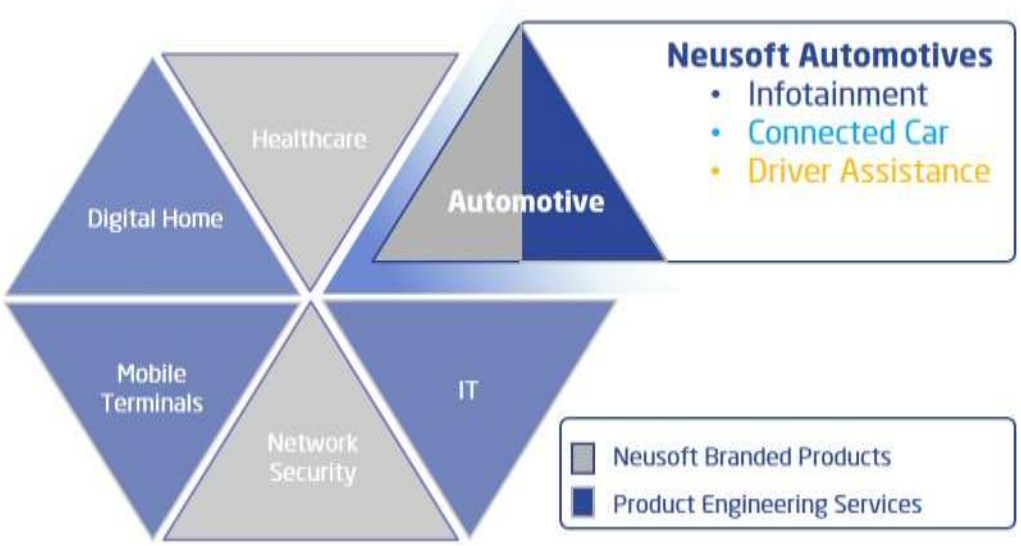


Processing Steps



Neusoft Overview

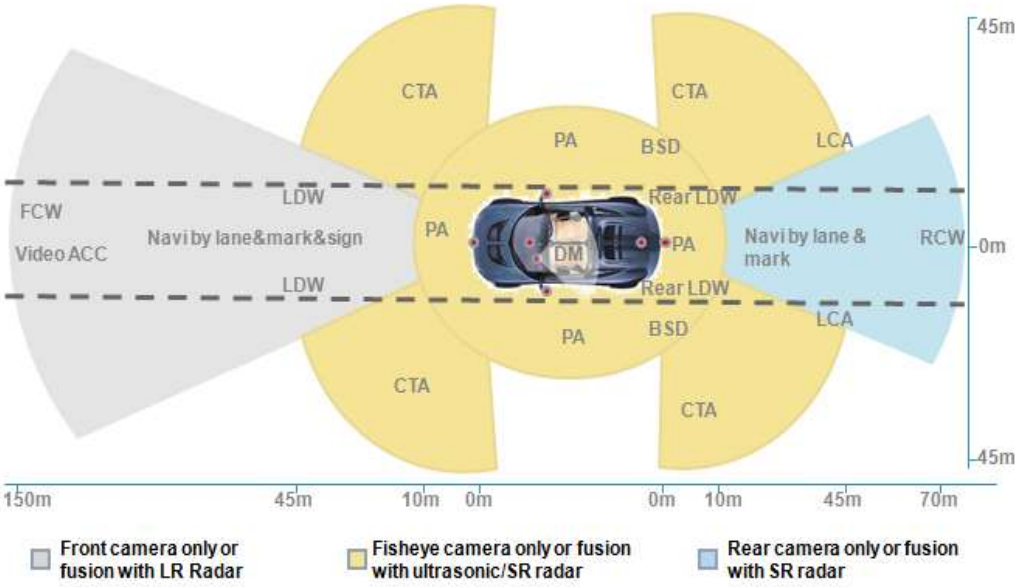
Neusoft Corporation Overview – Who We Are



Highlights

- Founded 1991 at North Eastern University (NEU) in Shenyang, China
- More than 24,000 employees
- International subsidiaries in Europe, USA, Middle East and Japan
- First CMMI 5-appraised software company in China in 2004
- Publicly listed since 1996 (600718.SS)
- Largest IT solutions and service provider in China with more than 20 years of experience with international customers and partners.

Neusoft Automotives Overview – What We Do



- More than 20 years of experience in developing automotive software for the global market
- More than 10 years experiences on ADAS
- 50+ patents on computer vision
- Covering a wide range of infotainment solutions and engineering services
- ISO/TC204 member, ADAS representative of China
- CMMI L5 and Automotive SPICE L3 certified

Neusoft Overview – What Role Do We Play

- In May 2014 Freescale Semiconductor announced a partnership with Neusoft Automotive
- Freescale：delivering high quality automotive microcontrollers
- Neusoft： development of cutting edge automotive vision software
- Green Hills：provides the safety certified INTEGRITY® real-time operating system (RTOS) for the Freescale platform
- Cognivue： IP provider for APEX2 engine

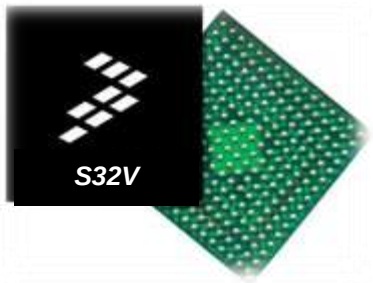
►*Key Freescale Eco-system partnerships:*

IP	RTOS Tools	Soft-ware
►Partnership to deliver image processing IP and software ►Enabled by OpenCL	►Partnership to deliver RTOS and Toolchain for S32V ►Dependable, Reliable, Predictable	►Partnership to deliver algorithms, demo's and full vision applications

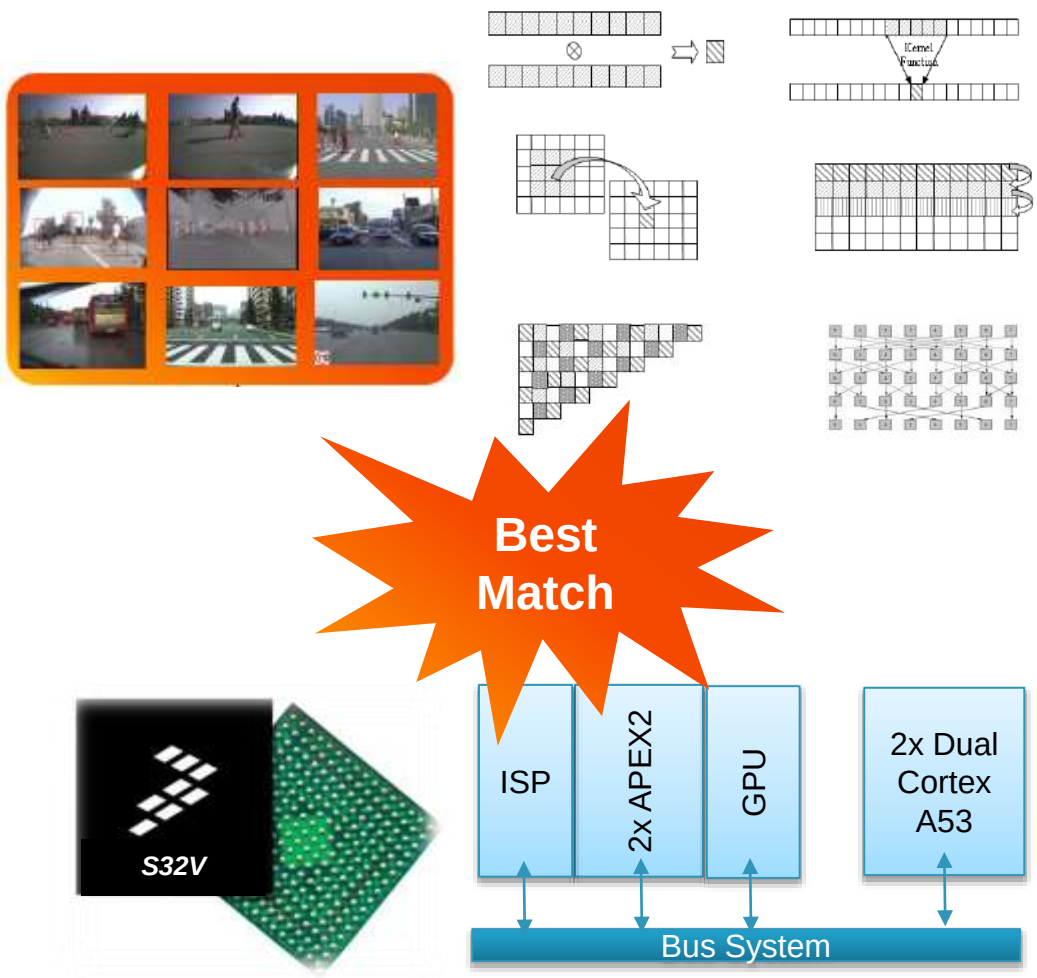
Challenges and Difficulties

Challenge and Difficulties: Complexity *vs* Performance

- ADAS Functions should support
  - Various traffic environments
  - Various weather and light conditions
- By Introduce
  - more advanced vision sensors
  - More complicated Artificial Intelligent algorithm
- Which will Bring Out
  - More complicated computation patterns
  - More computation workloads



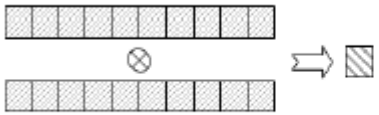
Challenge and Difficulties: Complexity *vs* Performance



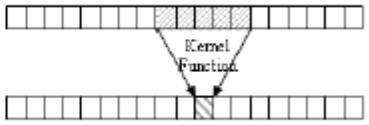
- The Key Point: How to Best Matching between software and hardware
  - Hardware designers should be aware of the workload characters of the key algorithms so as to provide custom and effective hardware speedups
  - Software designer should be aware of the characters of different computation units (including CPU, GPU, APU and ISP) to best utilized the computation power of hardware

S32V based Solution

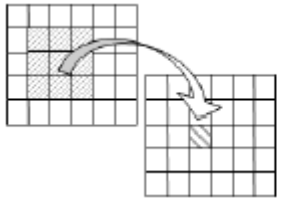
Computation Patterns Identify & Hardware Mapping



1. elementwise

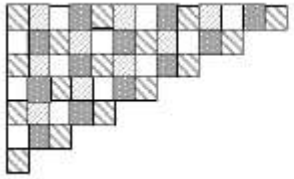


2. 1D LNO
(local Neighbored Operation)

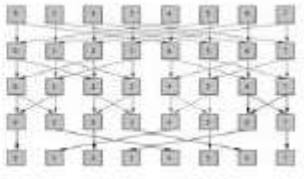


3. 2D LNO

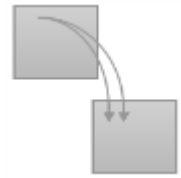
4. 2D line-dependent LNO



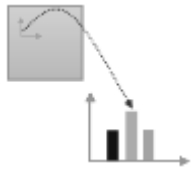
5. 2D waveline impendent LNO



6. Global dependent



7. Scatter



8. Random Access

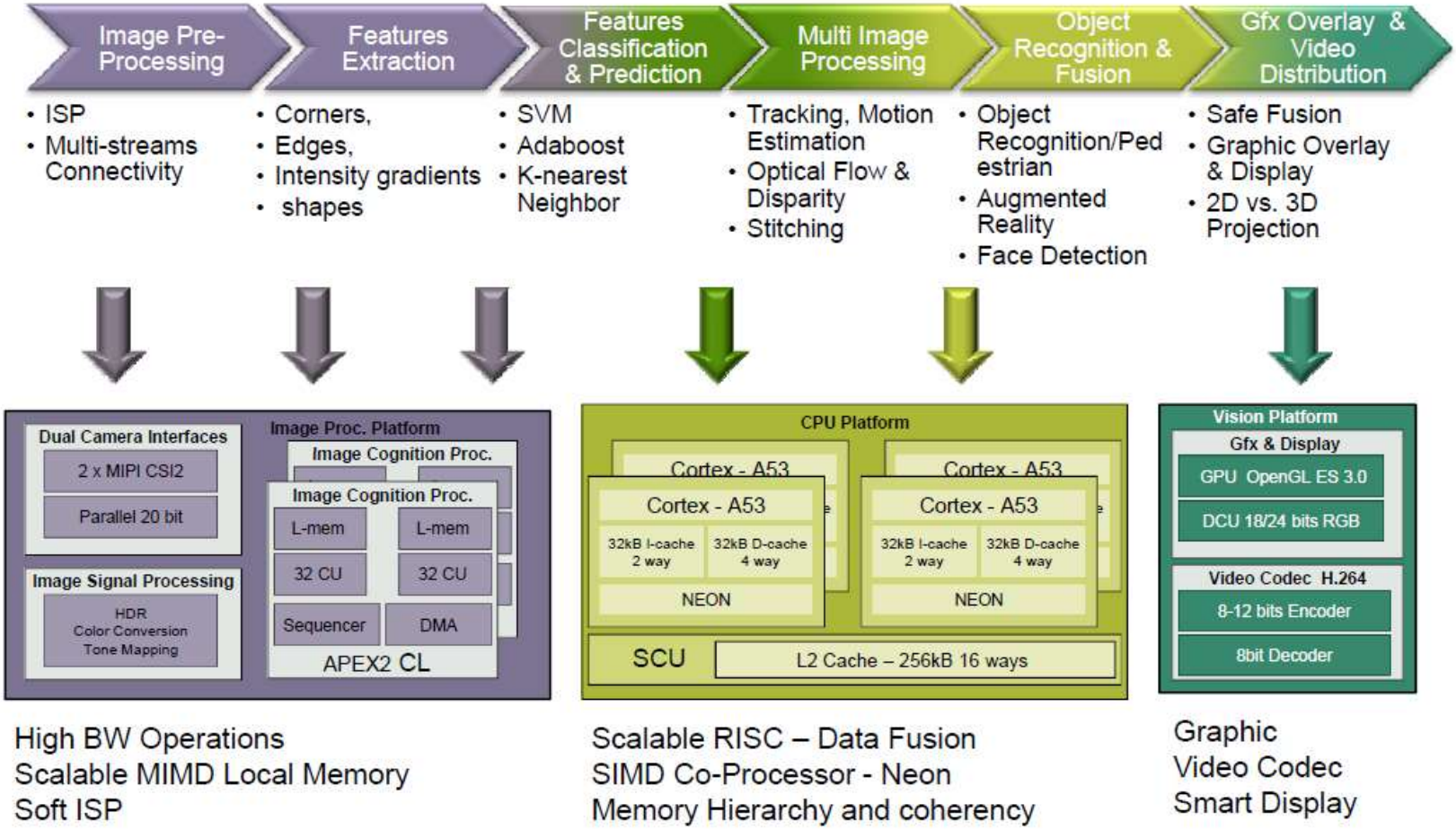
Low level vision
ISP/APEX

Middle level vision
ISP/APEX

High level vision
APEX/CPU

Parallelism Exploitation

Low level vision Middle Level vision High Level vision



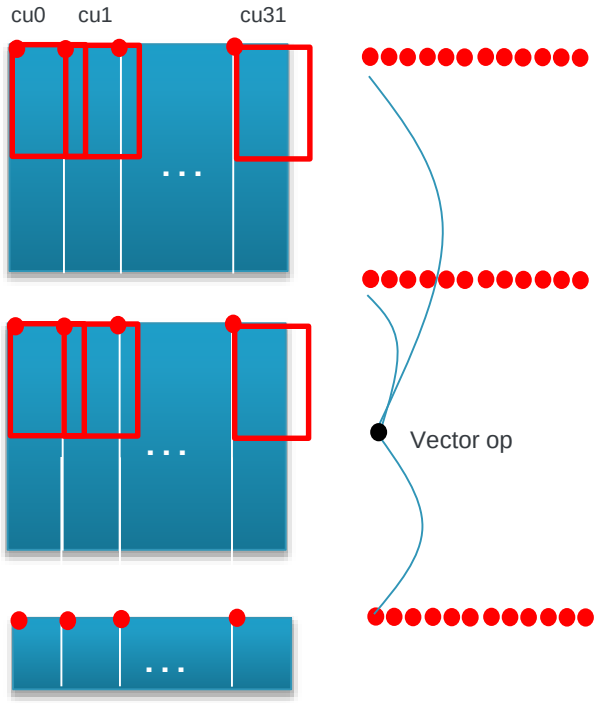
High BW Operations
Scalable MIMD Local Memory
Soft ISP

Scalable RISC – Data Fusion
SIMD Co-Processor - Neon
Memory Hierarchy and coherency

Graphic
Video Codec
Smart Display

Parallelism Exploitation

- Data Parallelism



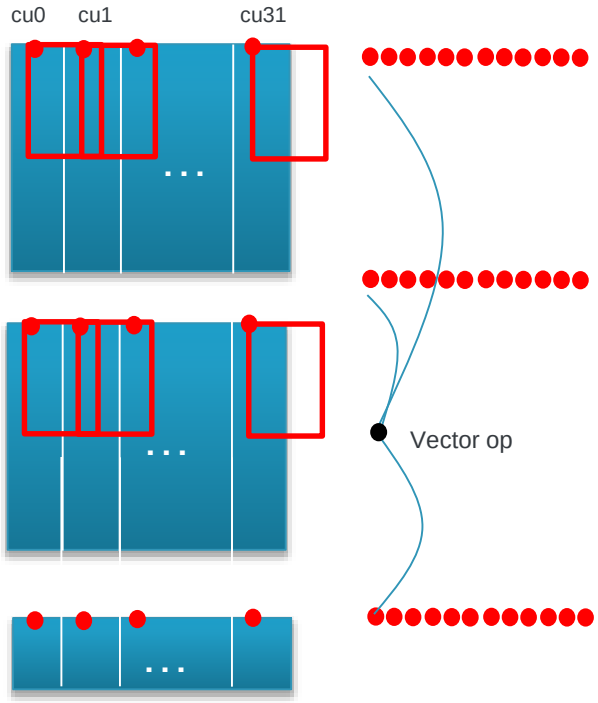
Algorithm	APEX kernel for object classification data-parallelism exploration
Param	intImg, intImg45 (integral image, rotated integral image)
	bw (block width for each CU)
	flag(output flag)

void apex_kernel_classification (vec32u* intImg, vec32u* intImg45, int bw, vec08u* flag)

```
1   {
2       ....
3       for (i=0; i<bw; i++)
4       {
5           vbool vRet = apex_vec_adaboost(intImg, intImg45, bw, iLine);
6           vif( vRet)
7           {
8               flag[i] = (vec08u)1;
9             } velse {
10              flag[i]=(vec08u)0;
11            }
12        }
13  }
```

Parallelism Exploitation

- Data Parallelism



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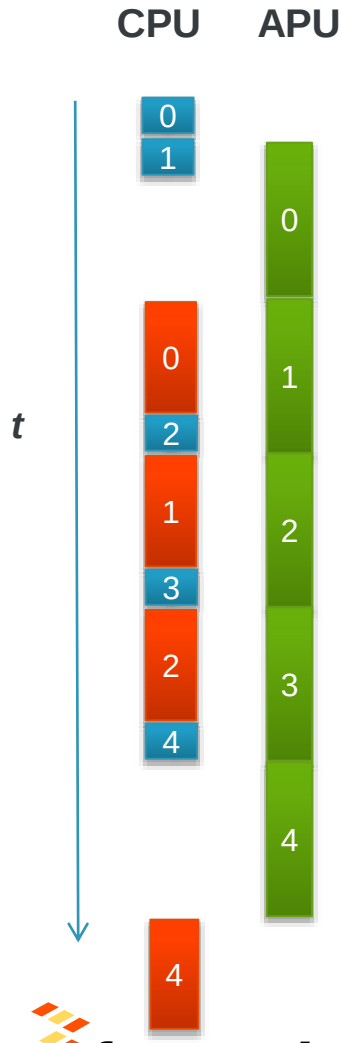
```

Parallelism Exploitation

- Pipeline Parallelism



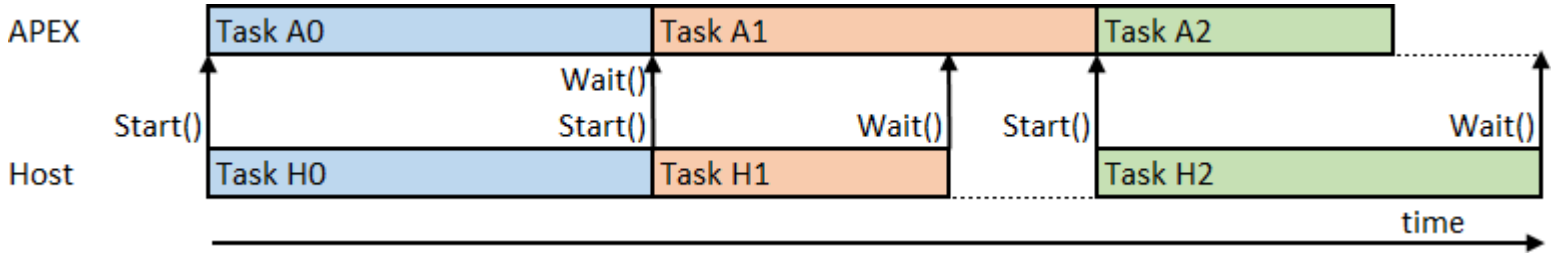
Algorithm	Pedestrian Detection CPU/APU collaboration for pipeline/data-parallelism exploration
Param	img (Input grayscale image)
	process(APU_HAAR_DETECTION process)
	list(output detected pedestrian list)

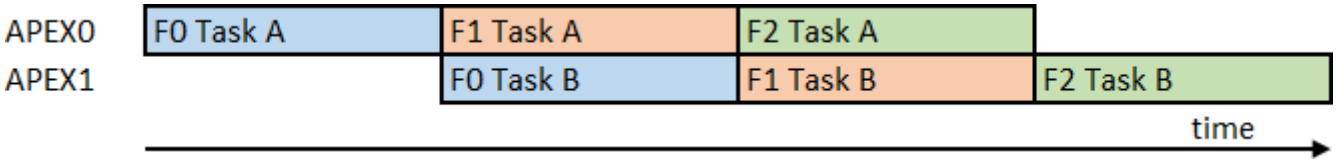
apex_process_detection (img, process, list)

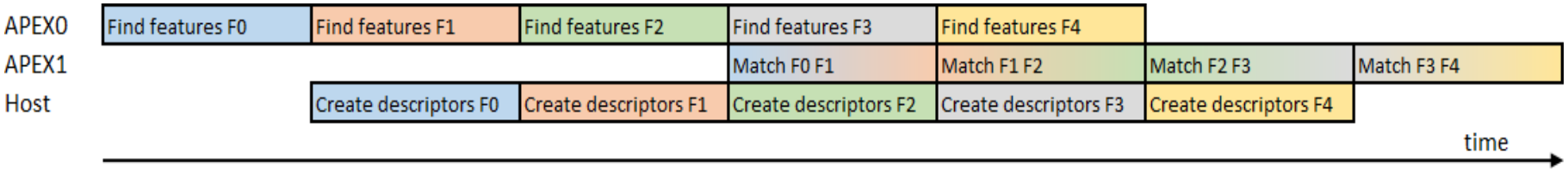
```
1   {
2       iROINum ← apex_process_getROINum(width, height, CU_NUM, CU_BLKW)
3       rx, rw, ry, rh ← apex_process_getROIInfo(iROINum, 0)
4       preprocess(img,0)
5       apex_process_connectIO_ROI(process, rx, rw, ry, rh)
6       process.start()
7       for (k=1; k<iROINum; k++) {
8           preprocess(img, k)
9           process.wait()
10          rx, rw, ry, rh ← apex_process_getROIInfo(iROINum, k)
11          apex_process_connectIO_ROI(process, rx, rw, ry, rh)
12          process.start()
13          postprocess(k-1, list)
14      }
15      process.wait()
16      postprocess(k, list)
17  }
```

Parallelism Exploitation

- Pipeline Parallelism(cont.)

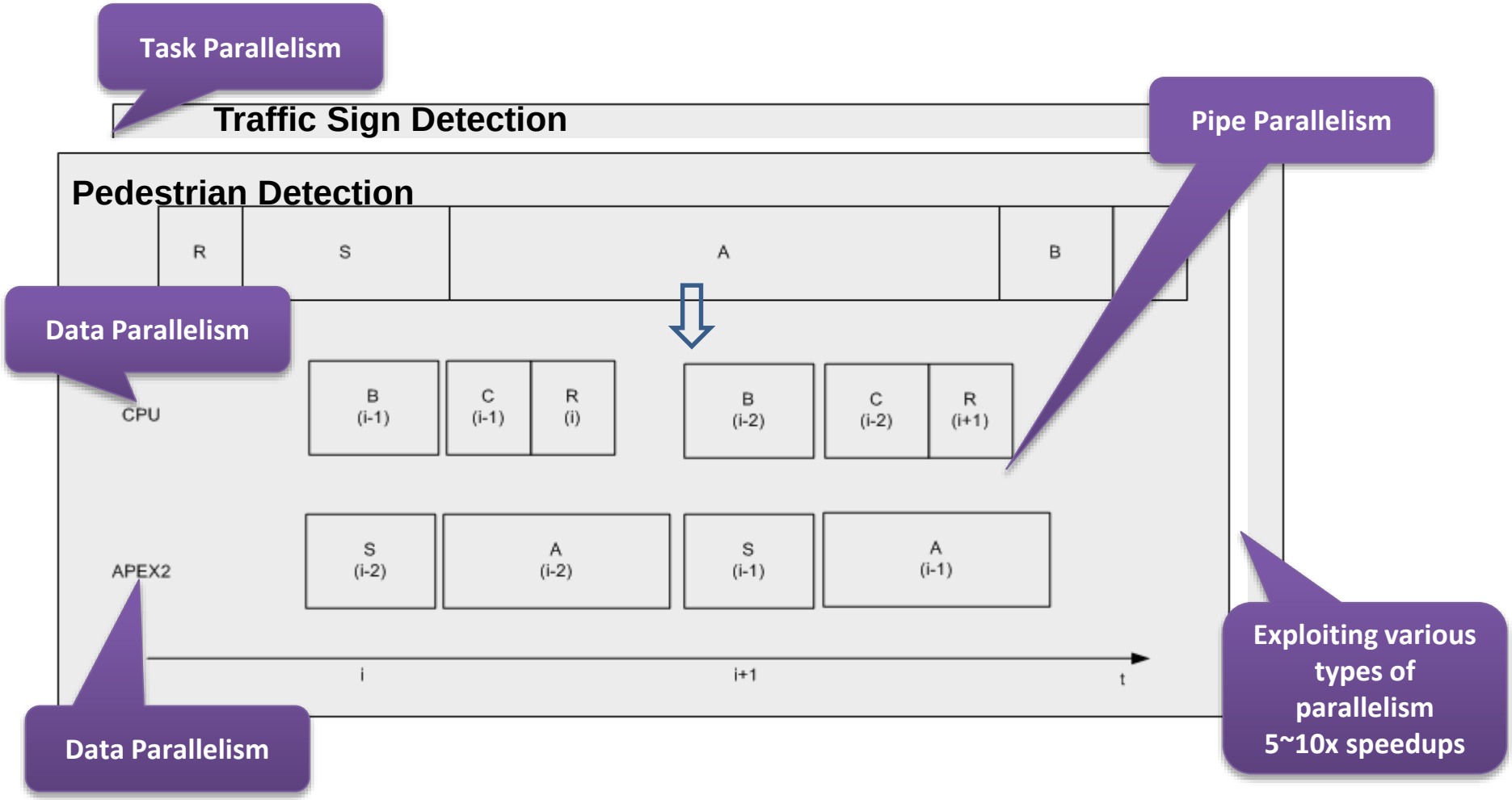






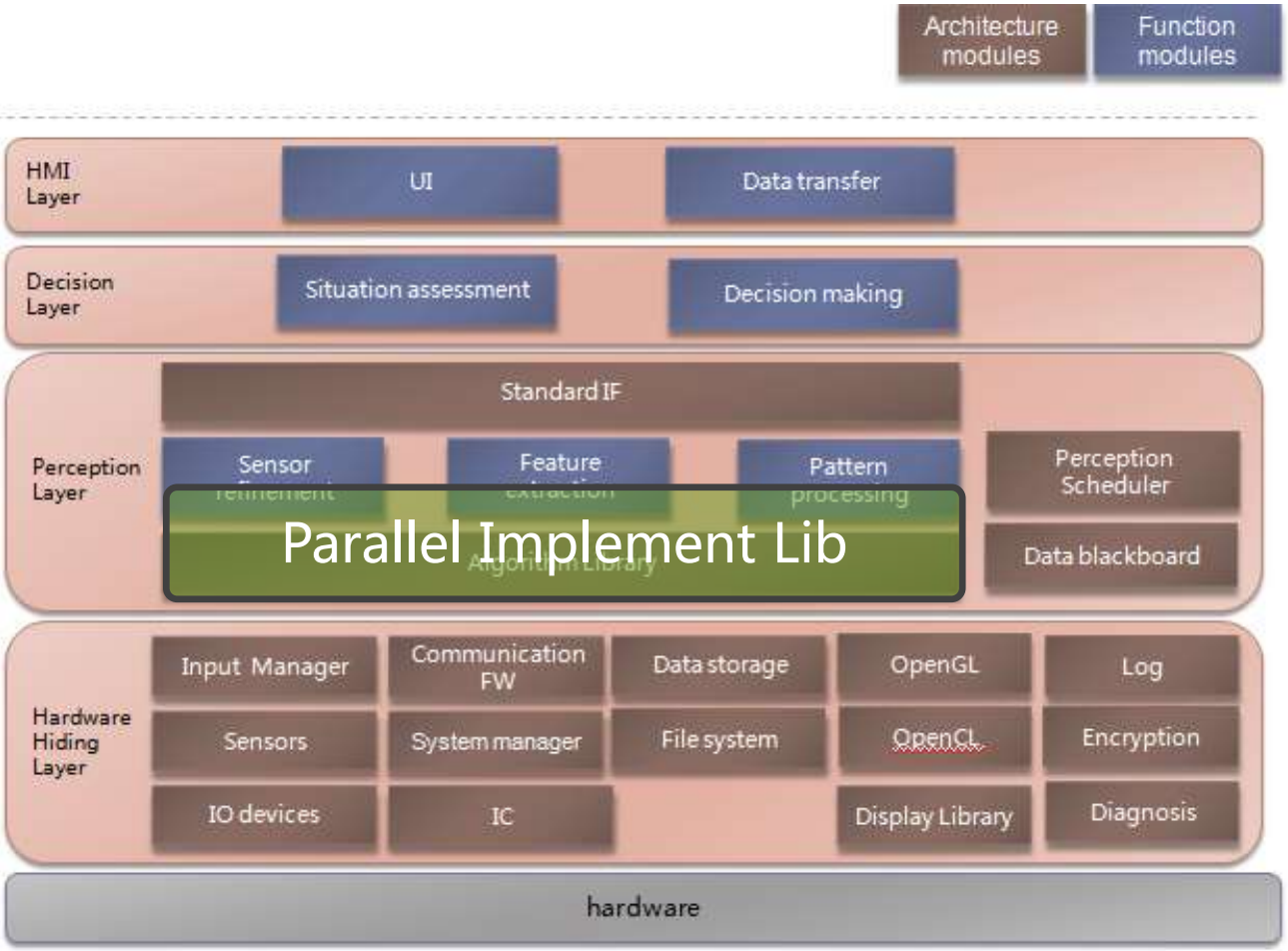
Parallelism Exploitation

- Data/Pipe/Task Parallelism



Parallelism Exploitation

- Function List (ported to S32V) and Speedups



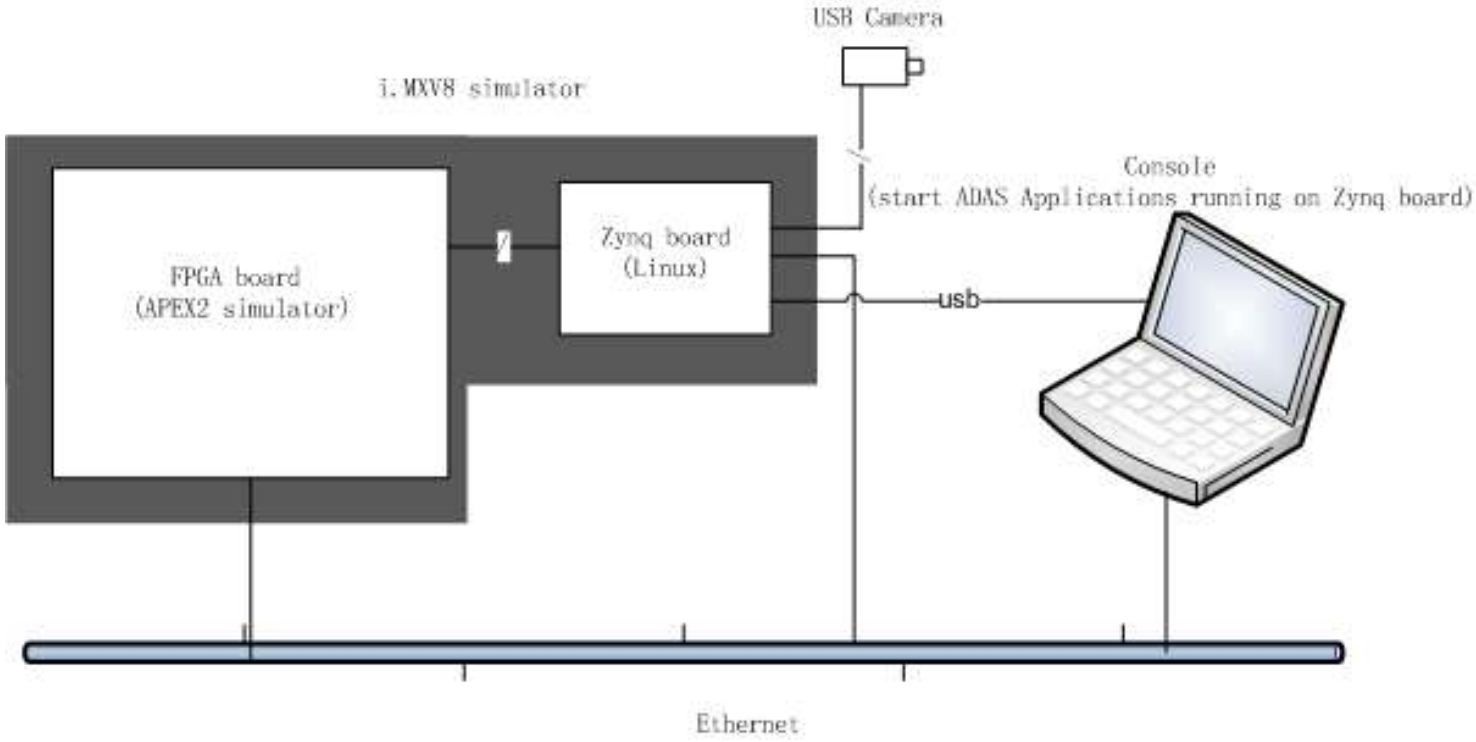
Parallelism Exploitation

- Function List (ported to S32V) and Speedups

		Function Name	Average Speedups
APEX Kernels	Preprocess	CvtColor	10~19x
		Resize	
		Gauss filter	
		Sobel filter	
		…	
	Feature Extraction	HOG	8~12x
		LBP	
		Texton	
		Wavelet	
		FFT	
		SSD	
		SAT	
		…	
	Classification	Adaboost	4~10x
		ELM	
		SVM	
	Tracking	Optical Flow	

Lab Demo

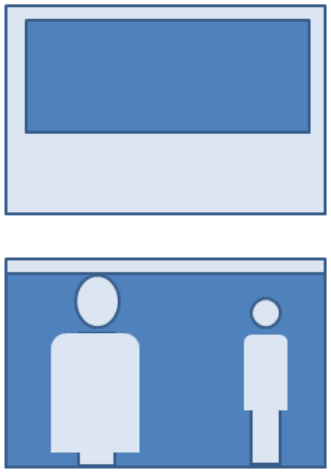
Demo Setup



Demo Setup Environment:

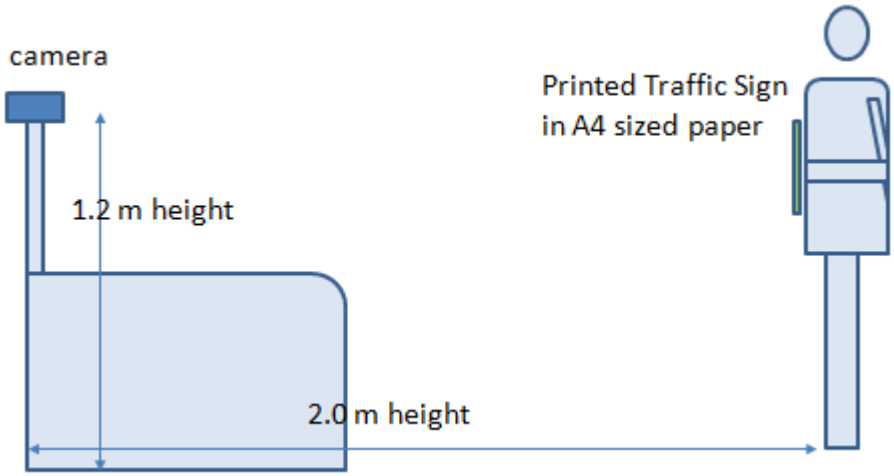
- S32V simulator part
  - Zynq board, Daul Cortex-A9, 677MHz, simulating ARM core on future S32V
  - FPGA board, APEX2 simulator, 64PE, 50MHz, simulating APEX2
  - USB camera, maximum 720P

Demo Setup



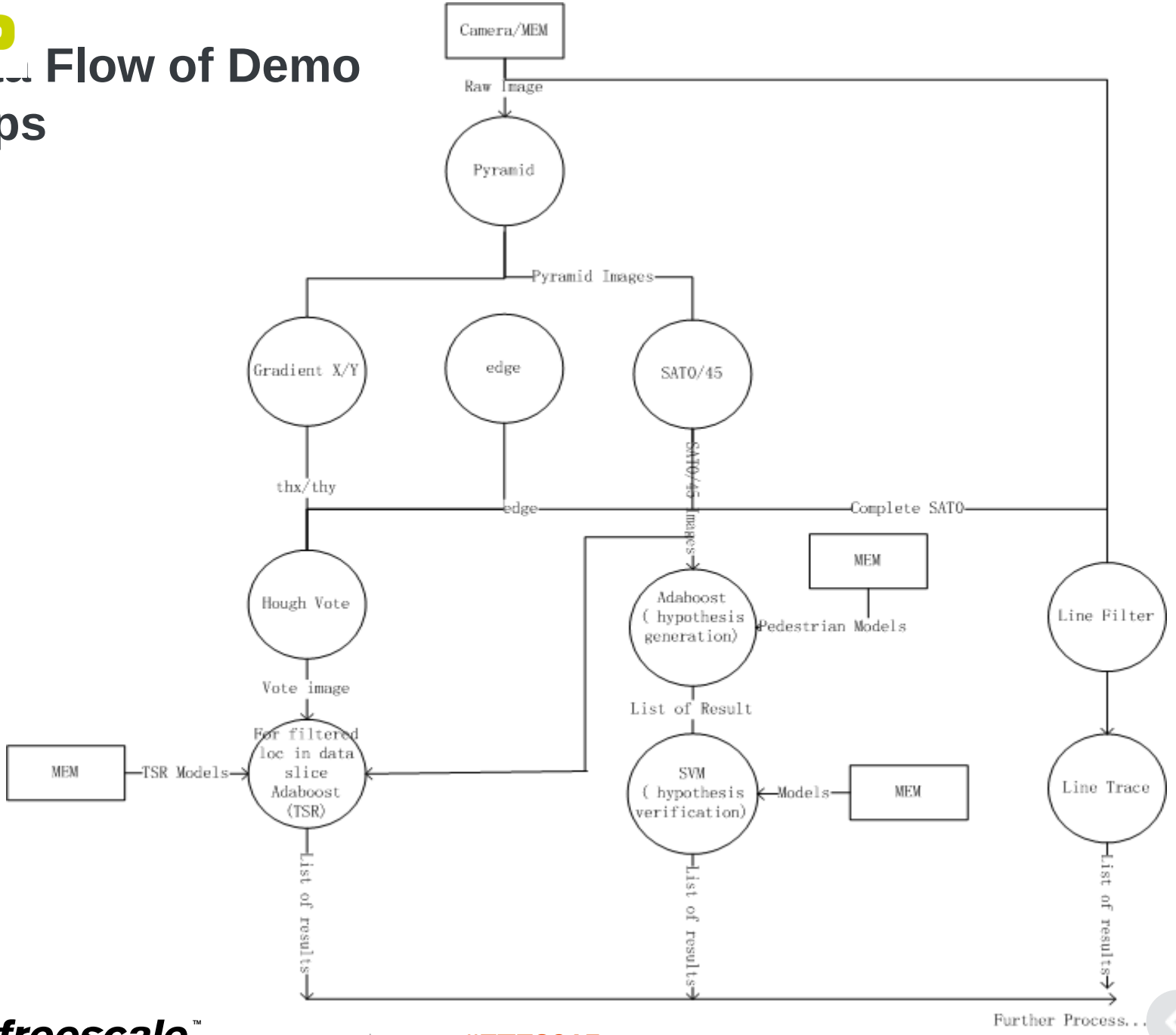
Detection Rage of Traffic Sign

Approximately Detection Rage of PD



- **Demo Setup Environment:**
  - App Algorithm part
    - PD and TSR are running parallel
    - The range of the detection has been adjusted, to adapt the indoor environment
    - The algorithm is a clipper version from Neusoft's real product algorithm library, the demo apps indicates exactly the same workload as real product in the future.

Data Flow of Demo Apps



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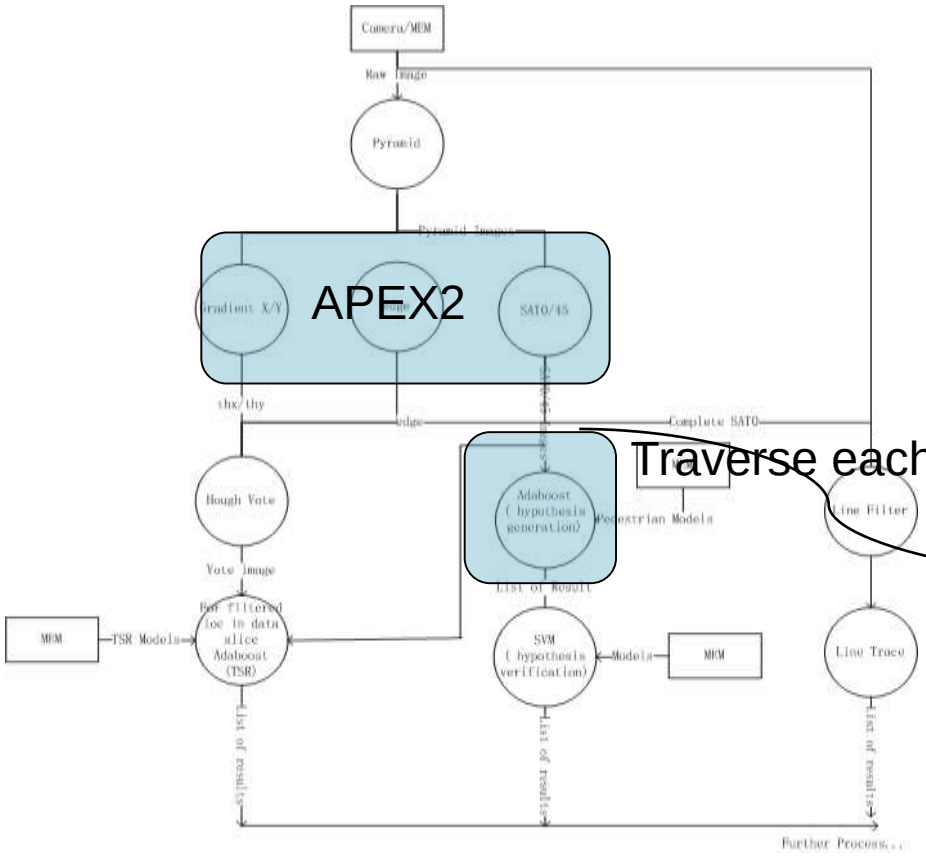
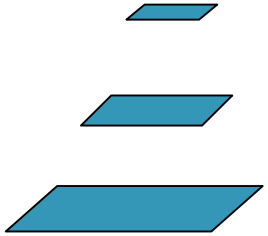
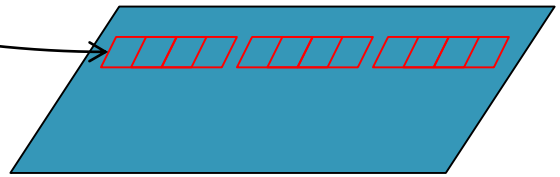


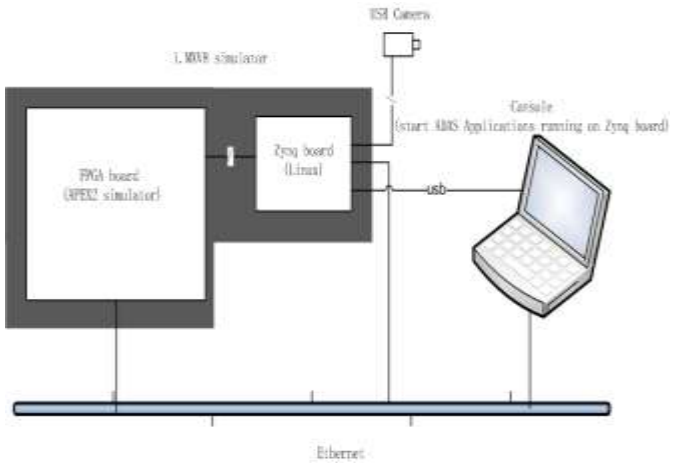


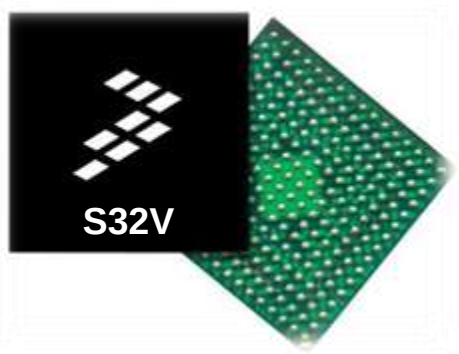
Traverse each possible position for hypothesis generation



Serials Exec Time of PD (for example)

Performance





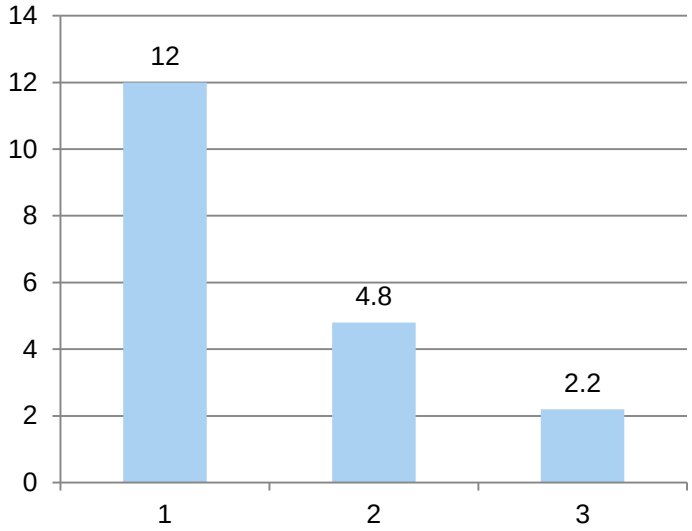
Performance on FPGA (measured):

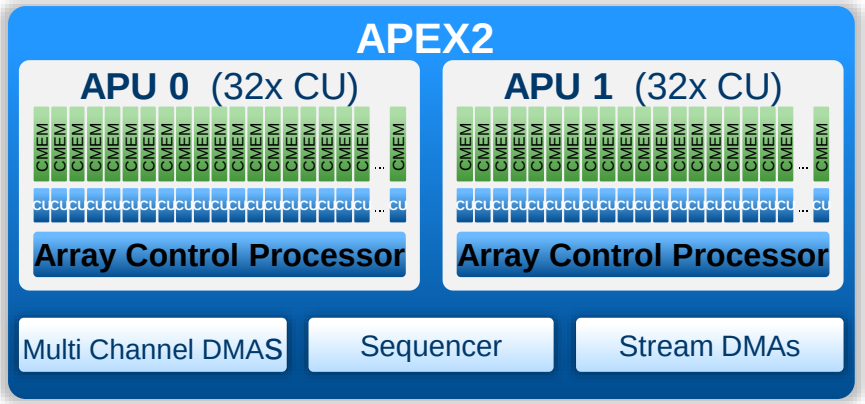
- PD (2fps)
  - 140ms, hypothesis generation(APEX2)
  - 40ms, hypothesis verification(ARM)
  - 450ms, Image capture/copy between 2 board, display and framework (ARM)
- TSR(2fps) ARM+APEX2
- LDW (15fps) ARM+APEX2

Performance on IC(estimated):

- PD (15fps)
  - 25ms , hypothesis generation(APEX2)
  - 40ms, hypothesis verification(ARM) ARM
  - 10ms, image data transfer(ISP/GPU)
- TSR (15fps+) ARM+APEX2
- LDW(30fps) ARM + APEx2

APEX2 Capability



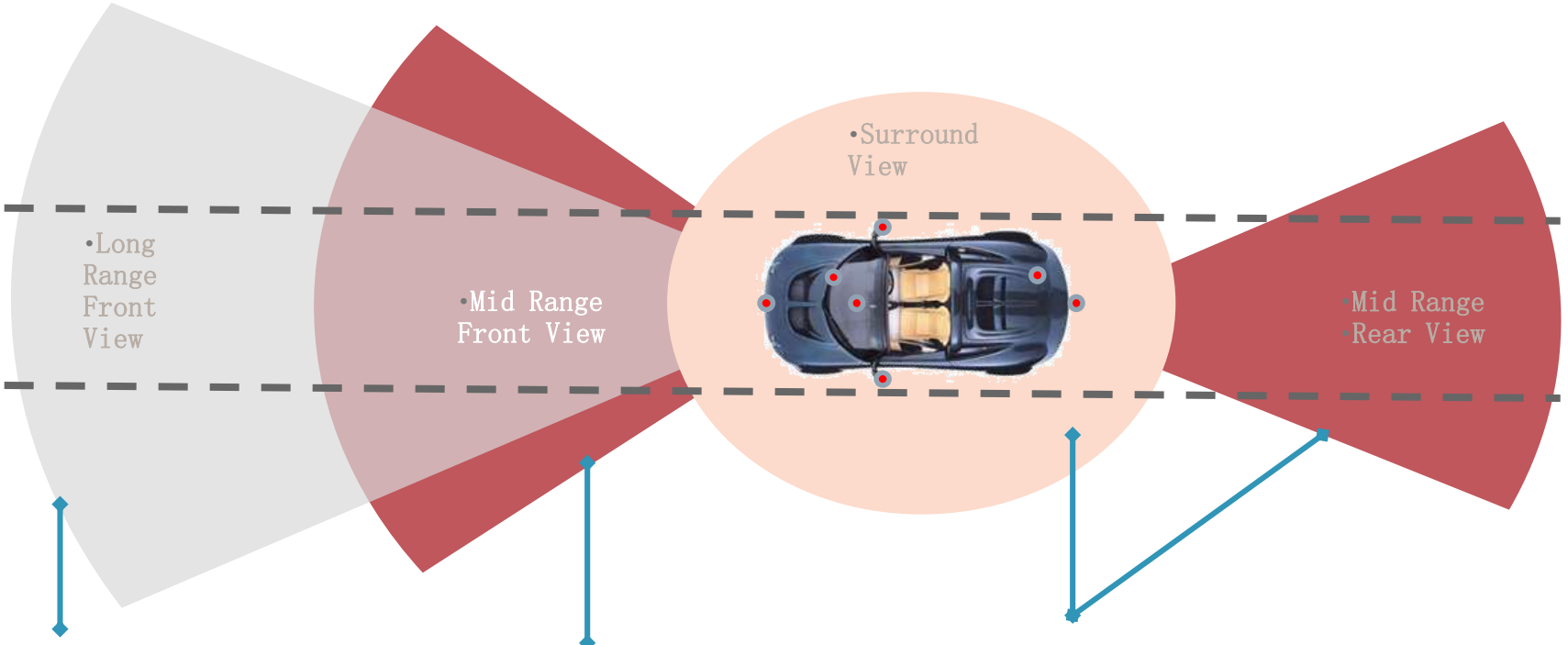


- **Speedups on S32V (estimated based on data collected on FPGA): PD as example**
  1. Adaboost Kernel speedups running on APEX2 : 12 x
  2. Complete Adaboost Algorithm for hypothesis generation (APEX2+ARM): 4.8 x
  3. Complete PD algorithm speedups: 2.2 x

Roadmap based S32V

Function Planning for ADAS and Autonomous Driving

Front camera: 3, side camera: 2



TLR: Traffic Light Recognize
TSR: Traffic Sign Recognize
VD: Vehicle Detect

LD: Lane Detect
PD: Pedestrian Detect
VD: Vehicle Detect

R-LD: Rear Lane Detect
LCA: Lane Change Assist
VD: Vehicle Detect
360: Surround View
BSD: Blind Spot Detect
OD: Obstacle Detect

Function Planning for ADAS and Autonomous Driving

All listed vision functions are running in parallel

S32V	Camera	Function	2 Dual Core A53	2*APEX	GPU	ISP
Configure #1	Long Range Front	TLD				
		TSR				
		VD				
Configure #2	Mid Range Front	LDW				
		PD				
		VD				
Configure #3	Surround	360				
	Mid Rear	R-LDW				
		BSD				

25% CU reserved

50% CU reserved

100% CU reserved

Summary

Summary

- Neusoft's deep understanding of ADAS algorithm helps Freescale understand the hardware requirement of ADAS product and optimize the SOC design

- Freescale's safe, secure, reliable hardware give Neusoft's ADAS key advantages in the intense market competition.

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