i.MX RT SERIES

INDUSTRY'S FIRST CROSSOVER PROCESSOR

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arm TechCon

i.MX RT 1050 Agenda

- Introduction to i.MX RT1050
- Product Overview
- Key Peripherals
- Wrap up

The edge is getting smarter

Essentials for the connected world

- Edge Computing and Data Management
- Reliable Security and Assured Privacy
- Graphics and Display support
- Seamless Connectivity

For the thousands of IoT applications, these next-gen features have not been…

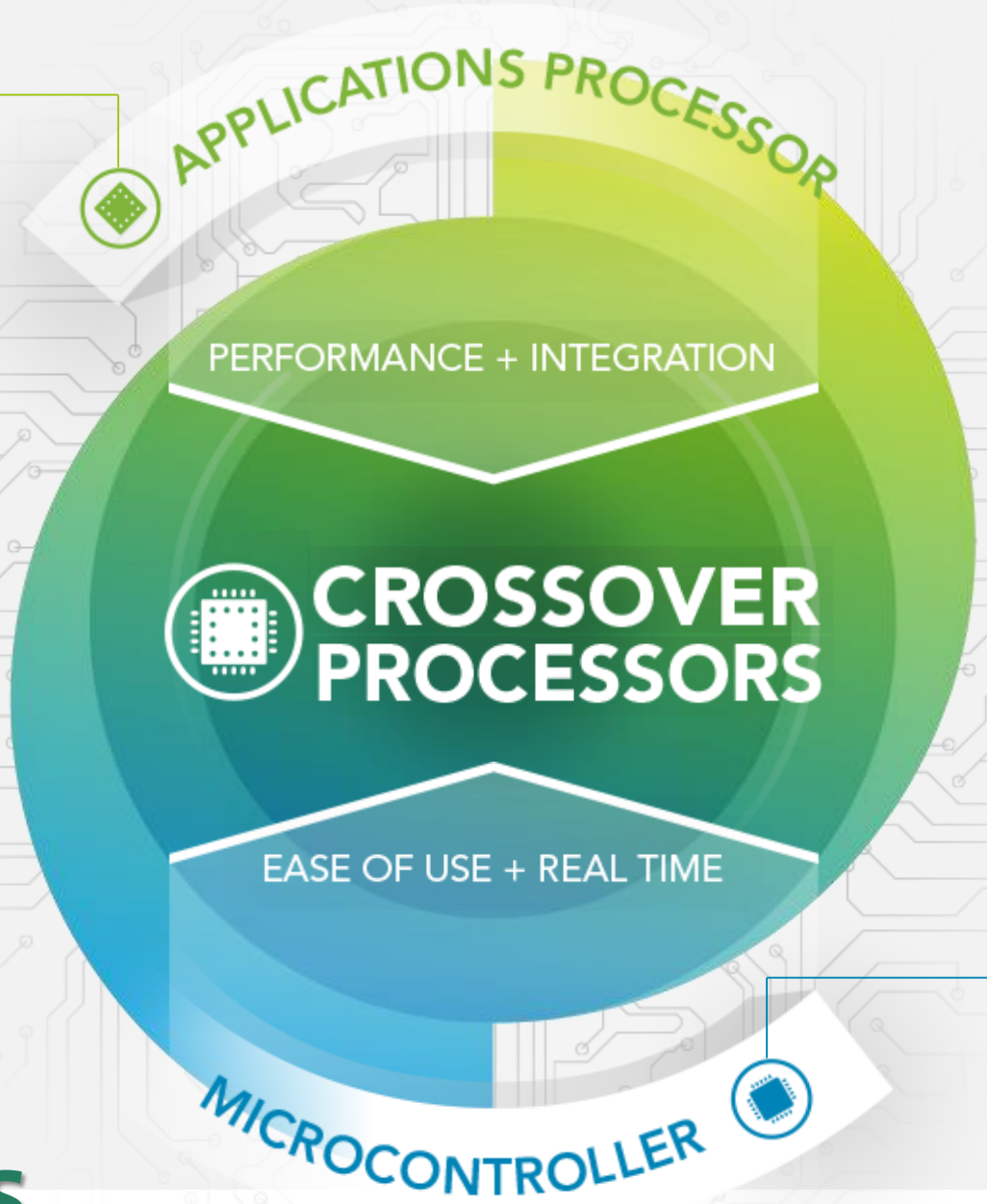
- Addressable by traditional MCUs or the system level complexities of Advanced Application Processors


Microcontrollers
(MCUs)
Applications
Processors
nest
IN 20 MIN
68
amazon
SONOS
CHAPTER I
kindle

i.MX
APPLICATIONS PROCESSORS

- ARM Cortex-A class and Cortex-M cores
- 600 MHz to 2 GHz performance
- Rich HMI experience
- Full open-source OS platforms

Linux android



- ARM Cortex-M cores
- Performance up to 300 MHz
- Embedded memory
- Easy to use tools
- RTOS support

IAR SYSTEMS KEIL Tools by ARM

MCUXpresso RTOS

KINETIS & LPC
MCUs

Best Of Both Worlds

i.MX RT1050 Key Highlights

High Performance Real-time Processing

- Cortex-M7 up to 600MHz (50% faster than current M7 products)
- 20ns interrupt latency
- Up to 512KB Tightly Coupled Memory

High Level of Integration

- High Security enabled by AES-128, HAB and On-the-fly QSPI Flash Decryption
- 2D graphics acceleration engine
- Parallel camera sensor interface
- LCD display controller up to WXGA (1366x768)
- Audio interface with three I2S for multichannel high performance audio

Low BOM Cost

- Competitive Pricing – starting @ $2.98 10k RSL
- Fully integrated PMIC with DC-DC
- Low cost package, 10x10 BGA, enabling 4 Layer PCB design
- Memory interfaces

Easy to Use

- MCU customers can leveraging their current toolchain (MCUXpresso, IAR, Keil)
- Rapid and easy prototyping and development with NXP FreeRTOS, SDK, Arm mbed and the global Arm ecosystem
- Single voltage input simplifies power circuit design
- Scalability to Kinetis & i.MX products

Reduced Systems-level Costs for Customers with i.MX RT Series

Lower Bill-of-Materials cost

- Large internal SRAM removes the need for external DRAM
- Low cost package options enable 4-layer PCB designs
- Integrated PMIC with DC-DC
  - Lowest active power consumption among all Cortex-M7 based processors

Lower cost of programming with off-chip memories

- Faster programming speeds with external serial flash due to simplicity of direct programming
  - 2MB external NOR **can be up to 60% faster** to program than MCUs with 2MB embedded flash
- Lower set-up and handling costs with i.MX RT
  - Lower pin count and homogeneity of external flash suppliers simplifies programming house logistics
  - Eliminates set-up & handling costs of complex high-pin count MCUs & vendor variability of MCUs
- Secure external storage enabled by On-the-fly decryption (AES-128)

i.MX RT1050 Target Applications

Audio Subsystem

High-end, consumer audio devices, including specialty equipment such as

Professional microphone

Guitar pedals

Consumer & Healthcare

Smart appliances

Cameras & LCDs

Mobile patient care, e.g. infusion pump or respirator

Blood pressure monitor

Activity and wellness monitor

Exercise equipment with display

Home & Building Automation

HVAC climate control

Security

Lighting control panels

IoT gateways

Industrial Computing

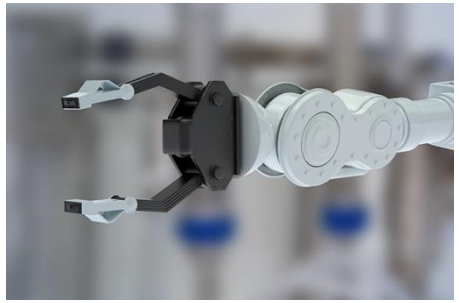
EBS

PLCs

Factory automation

Test and measurement

HMI control assembly line robotics



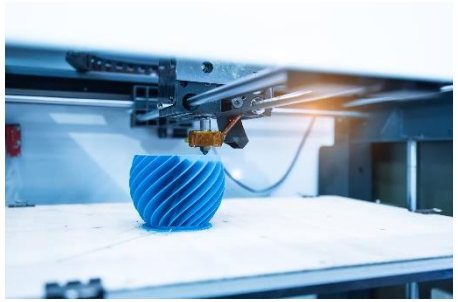
Motor Control & Power Conversion

3D printers

Thermal printers

Unmanned autonomous vehicles

Robotic vacuum cleaners



i.MX RT Enablement Overview

Runtime Software

NXP Solutions:

RTOS, Middleware Partners:

FreeRTOS, Crank software inc., Embedded Access Inc, SEGGER www.segger.com, MICROEJ, DRAUPNER GRAPHICS, RT-Thread 启动下一代实时操作系统演化, TouchGFX, wolfSSL, Embedded Wizard

Software Development Tools

IDE / Toolchains:

IAR SYSTEMS, ARM KEIL Microcontroller Tools, ARM mbed, SEGGER www.segger.com

Hardware Development Tools

Evaluation Kits:

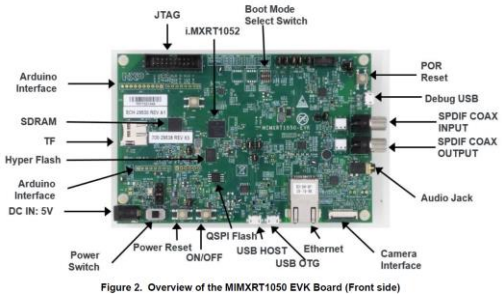


Figure 2. Overview of the MIMXRT1050 EVK Board (Front side)

Partner Solutions

Embedded Artists, EmCraft systems, FDI FUTURE DESIGNS, INC

Application Specific

- Graphics
- Touch HMI
- Camera interface
- Motor Control
- Voice activation
- Audio
- Sensor Fusion
- Cloud Connectivity

Connectivity Solutions

Bluetooth SMART, Wi Fi, EtherNet, 802.15.4, USB, CAN

Support

Broad Market:

- NXP Community
- Solution Designs
- Application Notes
- Schematics

High Touch:

- Professional Support
- Professional Services

Comprehensive frameworks and solutions for low-power, connected, and secure embedded systems

Industry leading IDE support and intuitive software configuration tools to accelerate application development

Low cost hardware platforms for evaluation and application development. Partner solutions for hardware debugging solutions

Software frameworks and development tools for targeted applications and certified connectivity solutions

Get started quickly and get the support you need, when you need it

i.MX RT1050 Block Diagram

Specifications

- Package: MAPBGA196 | 10x10mm^2, 0.65mm pitch (130 GPIOs)
- Temp / Qual: -40 to 105°C (Tj) Industrial / 0 to 95°C (Tj) Consumer

High Performance Real Time system

- Cortex-M7 up to 600MHz , 50% faster than any other existing M7 products
- 20ns interrupt latency, a TRUE Real time processor
- 512KB SRAM, configurable to 512KB TCM

Rich Peripheral

- Motor Control: Flex PWM X 4, Quad Timer X 4, ENC X 4
- 2x USB, 2x SDIO, 2x CAN, 1x ENET with 1588, 8xUART, 4x SPI, 4X I2C
- 8/16-bit CSI interface and 8/16/24-bit LCD interface
- Qual-SPI interface, with Bus Encryption Engine
- Audio interface: 3x SAI/ SPDIF RX & TX

Security

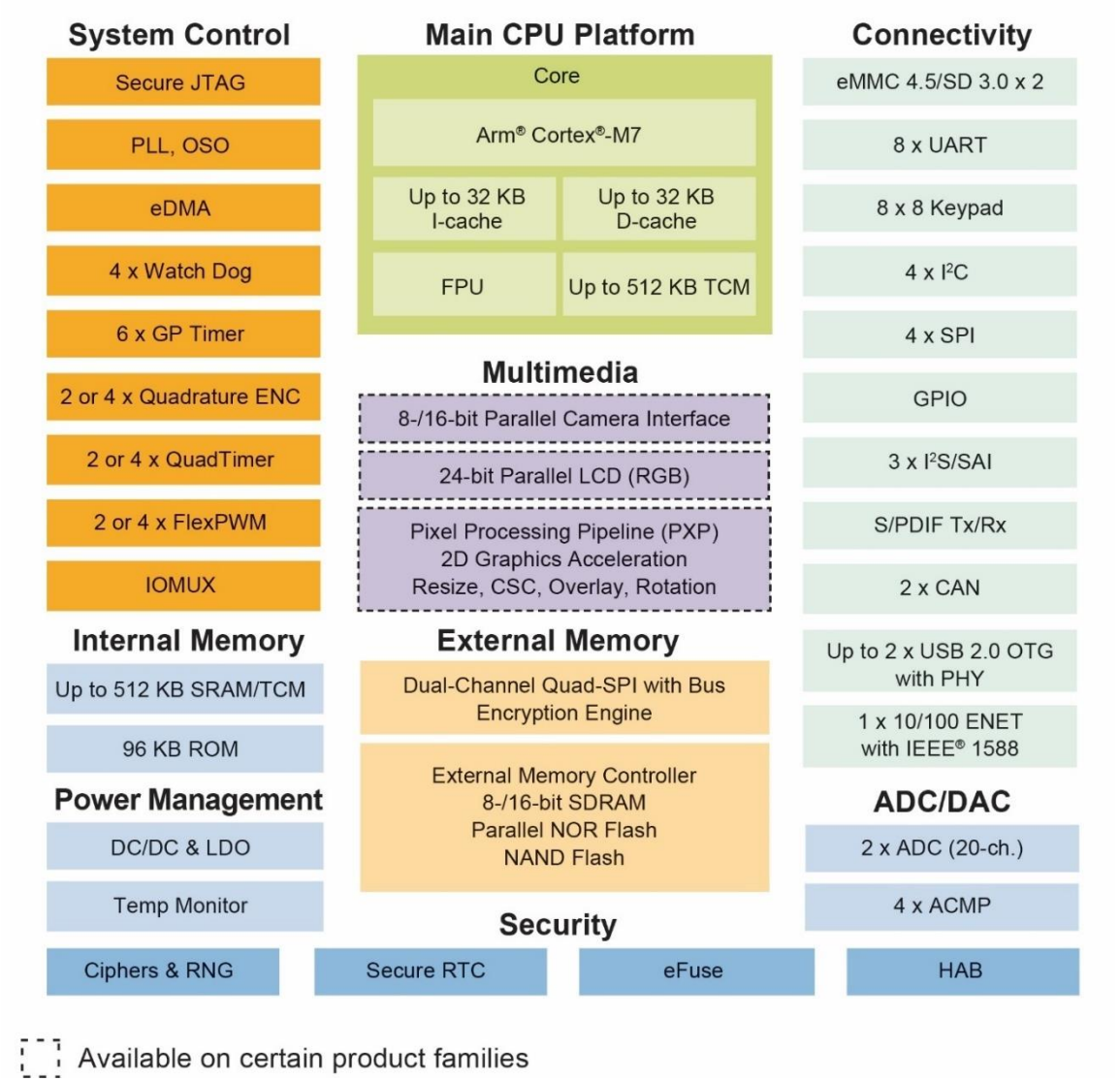
- TRNG&PRNG(NIST SP 800-90 Certified)
- 128-AES cryptography
- Bus Encryption Engine: Protect QSPI Flash Content

Ease of Use

- MCUXpresso with SDK
- FreeRTOS
- Comprehensive ecosystem

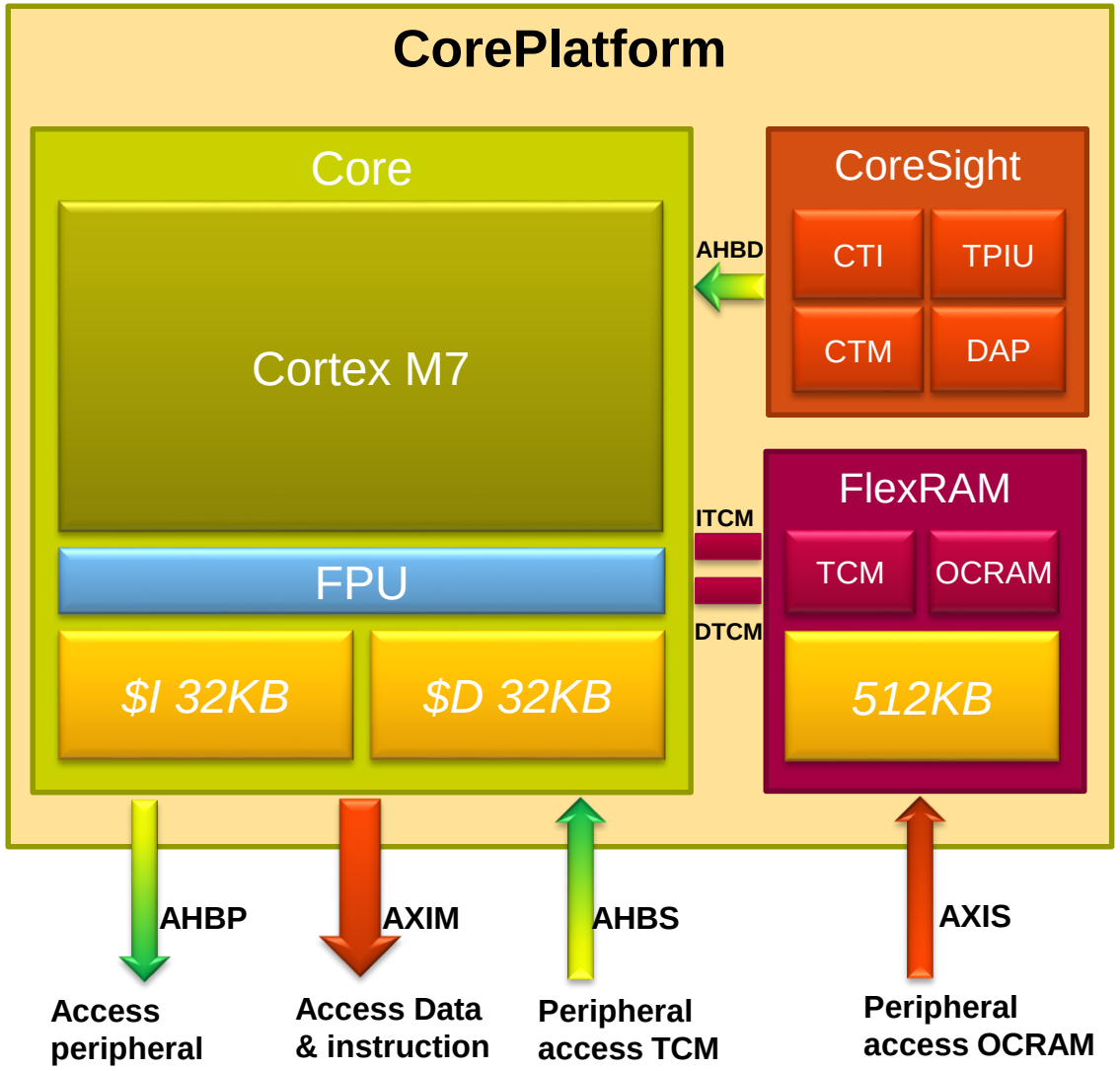
Low BOM Cost

- Competitive Price
- Fully integrated PMIC with DC-DC
- Low cost package, 10x10 BGA with 0.65mm Pitch
- SDRAM interface



CPU Platform

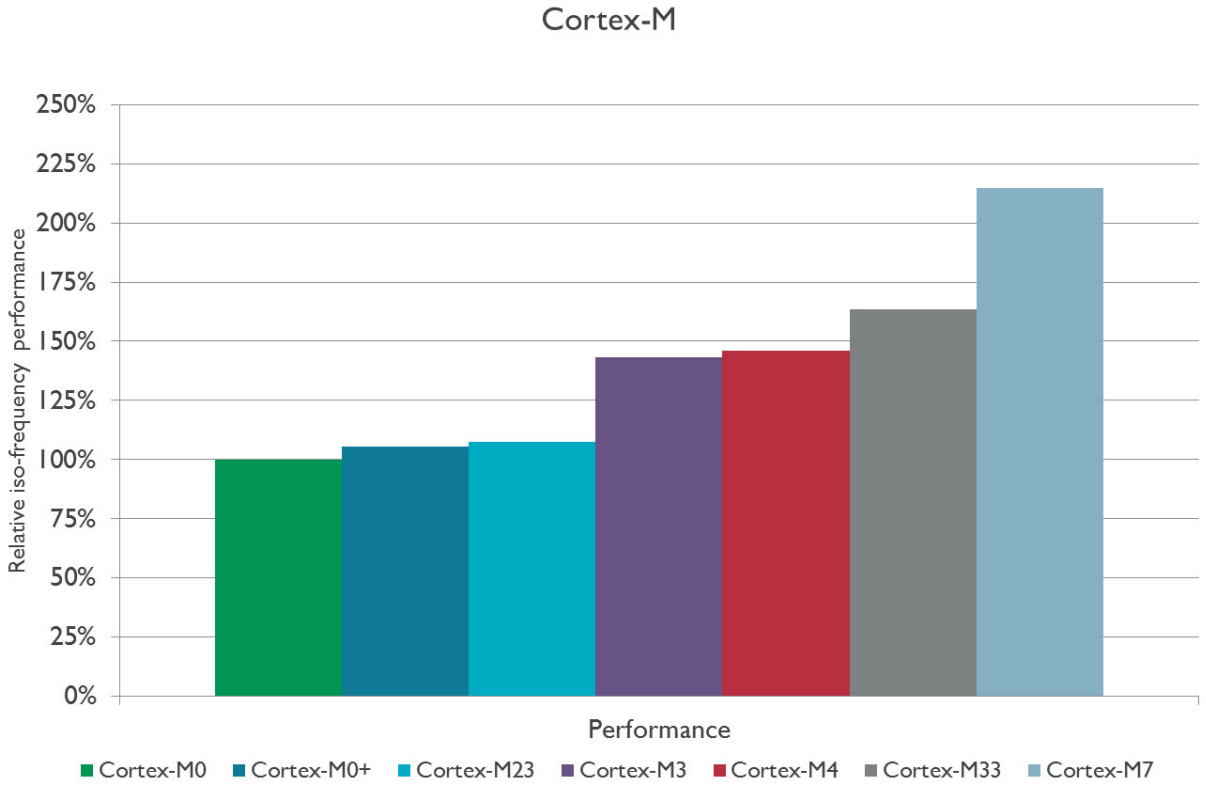
Cortex-M7 CPU Platform



- 32 KB L1 Instruction Cache
- 32 KB L1 Data Cache
- 512KB TCM and OCRAM shared SRAM
- Floating Point Unit (FPU) with support of the VFPv5 architecture
- Integrated Nested Vector Interrupt Controller (NVIC)
- Separate AMBA AXI/AHB bus connection architecture – high efficiency & low latency
- Cortex M7 debug architecture that complies with the CoreSight debug/trace architecture

Cortex-M7

Highest Performance Microcontroller



http://www.arm.com/-/media/arm-com/products/processors/Cortex-M-series-performance-graph.jpg?la=en

Low Power Features for CPU Platform on i.MX RT1050

Dynamic Voltage Frequency Switch (DVFS) Support

- 600MHz in Overdrive mode (High speed at high voltage)
- 528MHz in Nominal mode (Full speed at nominal voltage)
- 24MHz in Underdrive mode (Low speed at low voltage)

Statue Retention Power Gate (SRPG) Support

- CPU can save its state into internal RAM with SW
- When exiting from low power mode, CPU can restore the state by SW, and continue executing the program

Power Gating Support

- Power gating for CPU core
- Power gating for TCM Memories
- Support TCM memory power on while CPU power gated to allow fast wakeup while still maintain lower power

Memory

Internal Memory

- L1 Cache 32KB + 32KB
  - L1 I-Cache memory in M7 Core
  - L1 D-Cache memory in M7 Core

- TCM and OCRAM
  - Total 512KB tightly coupled SRAM which can be flexibly allocated to ITCM, DTCM or OCRAM on 32KB granularity
    - High Speed: working at ARM core frequency
    - Low latency: tightly coupled, zero access latency

- ROM 96KB
  - Used to store the boot ROM, including code for boot device support, HAB, etc

External Mass Storage

- QSPI NOR/NAND FLASH
  - Supports industry Standard Single, Dual and Quad mode serial flashes, Octal/Hyper RAM/Flash;
  - Supports Double Data Rate (DDR) serial flash for high performance;
  - Maximum serial clock frequency 132MHz SDR Mode, 66MHz DDR Mode; SDR and DDR 166MHz with DQS input
  - Dual channel architecture enables simultaneous access to two external flashes;

- SD/eMMC x2
  - Conforms to the SD Host Controller Standard Specification version 3.0;
  - Compatible with the MMC System Specification version 4.5;
  - Card bus clock frequency up to 192 MHz;

- RawNAND
  - 8/16-bit SLC NAND FLASH, ECC handled in SW;
  - ONFI 2.x complain
  - Support ONFI NAND for Micron and Hynix and Toggle NAND for Toshiba and Samsung;
  - Async mode

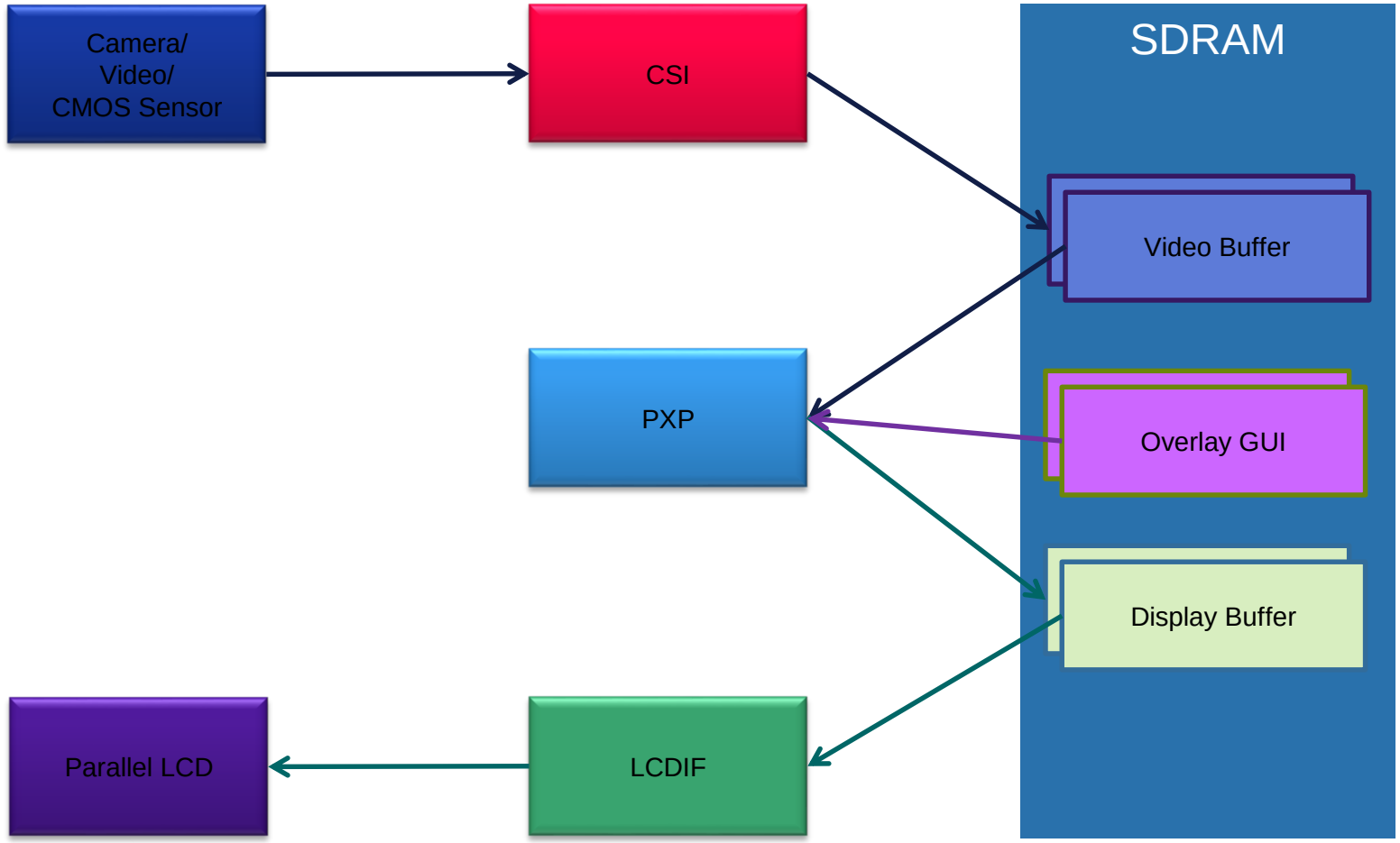
- Parallel NOR FLASH/SRAM
  - Support 8/16-bit parallel NOR FLASH/SRAM;
  - Async mode;

SDRAM Interface

- Key Features
  - 8/16-bit SDRAM
  - Support single x16 DRAM chip or dual x8 DRAM chip
  - Clock up to 166MHz (166MT/s), 332MB/s theoretical bandwidth
  - Support up to 4 CS
  - Total Address space: 1.5GB, configurable per CS
- Performance
  - Support Real-Time priority via QoS
  - Access Latency hiding
  - Bank interleaving
  - Consecutive read/write access optimizations
  - Enabling access priority to open memory pages
  - Deep queues for read and write requests
- Low Power
  - Support of Dynamic Frequency Scaling
  - Self Refresh and Power Down support

Multimedia

Camera & Display Subsystem



CMOS Sensor Interface (CSI)

- Provides direct connectivity to relevant image sensors and connectivity bridges: camera, cmos sensor, HDMI receiver, TV decoder …
- Data bus
  - Up to 24-bit
  - Also support 8-bit, 10-bit and 16-bit
- Variety of data formats YUV 4:2:2/4:4:4
  - RGB 16/24 bpp
  - CCIR656
  - Other: as generic data, including compressed streams
- Frame resolution
  - Essentially unlimited (up to 65535 x 65535 pixels)
- Input rate
  - 75 MPixel/s peak
- Additional features
  - Configurable master clock frequency output to sensor
  - Statistic data generation for Auto Exposure (AE) and Auto White Balance (AWB) control
  - Supports simple de-interlacing of interlaced input

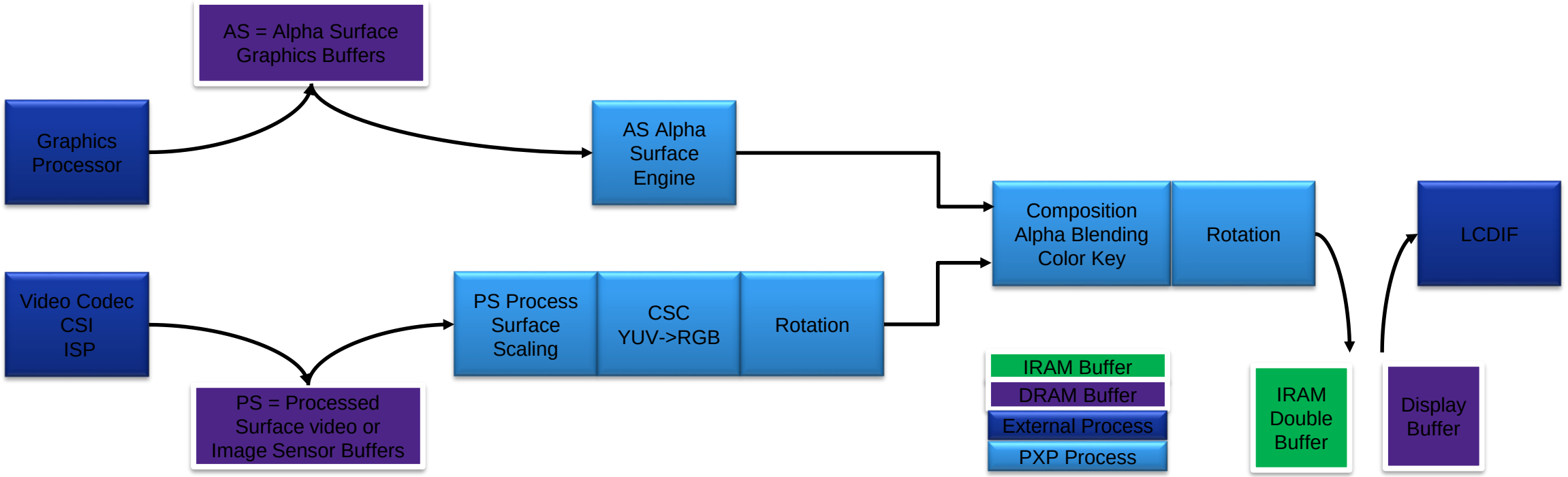
LCD Interface (LCDIF)

- Operation Mode
  - DOTCLK Mode (sync mode for dumb display)
  - MPU Mode (async mode for smart display)
- Display Data Bus
  - Up to 24-bit
  - Also support 8-bit / 16-bit / 18-bit
- Display Resolution
  - Support up to WVGA@60fps with rich UI & application
  - Typical pixel rate: 27~74.25 MP/sec

Name	Resolution			
	Width	x	Height	Total [MP]
VGA	640	x	480	0.31
PAL	720	x	480	0.35
WVGA	800	x	480	0.38
NTSC	720	x	576	0.41
SVGA	800	x	600	0.48
WSVGA	1024	x	600	0.61
XGA	1024	x	768	0.79
HD720	1280	x	720	0.92
WXGA	1366	x	768	1.05

Pixel Pipeline (PXP)

- High-efficiency graphics 2D and image processing engine:
  - BitBlit
  - Flexible image composition options (alpha, color key, Porter-Duff blending)
  - Color space conversion from YUV to RGB for PS;
  - Single-pass processing for Resize, CSC, Overlay and Rotation (90º, 180º, 270º);
  - Support data pipeline mode with LCDIF to for DRAM bandwidth saving;



Audio Subsystem

- Audio subsystem of i.MX RT1050 is composed of:
  - 1x Multi-channel SAI/I2S
  - 2x Single-channel SAI/I2S
  - 1x SPDIF TX & RX
  - 1x MQS
- Audio PLL
  - Fractional PLL which can generate very accurate audio clock
  - Support on-the-fly frequency change
- Audio Master clock synchronization
  - Flexible master clock synchronization between each SAIs and SPDIF
  - Independent master clock option for RX and TX
  - MQS is tightly coupled with SAI-3 block

Synchronous Audio Interface (SAI)

- Key Features
  - Supports I2S, AC97, TDM, and codec/DSP interfaces
  - 32x32-bit for each TX and RX channel (SSI FIFOs are 15x32-bit)
  - Graceful restart after FIFO error (enhancement over SSI)
  - TX with independent bit clock and frame sync to support 1 data channel
  - RX with independent bit clock and frame sync to support 1 data channel
  - Maximum frame size of 32 words
  - Word sizes from 8-32 bits

- DMA Support
  - Dedicated eDMA channel for each TX/RX

- Clock
  - Support both clock source from Audio PLL or external master clock input

- Multi-channel Support
  - SAI-1 supports 1x Dedicate TX, 1x Dedicate RX and 3x TX/RX multiplexed data lanes
  - SAI-2 and SAI-3 support 1x TX and 1x RX data lane

Security

Security

Cipher Engine (DCP)

- Encryption/Decryption - AES-128
- Hash algorithm – SHA1/SHA256
- CRC
- Secured AES key management

Bus Encryption Engine (BEE)

- On-the-fly FlexSPI (QSPI/Octal Flash) decryption
- Support AES-128 ECB and CTR modes
- 2 independent memory regions cipher policy management

Central Security management Unit (CSU)

- Access permission assignment for system Masters (such as eDMA, DCP, ENET, USB, etc.)
- Security level assignment for system Peripherals (such as register space of each module, OCRAM, TCM)

TRNG

- Pseudo Random Number Generator
- True Random Number Generator

On Chip OTP Controller (OCOTP)

- On chip fuse block operation control
- Fuse permission control, including read-protect, write-protect and program-protect

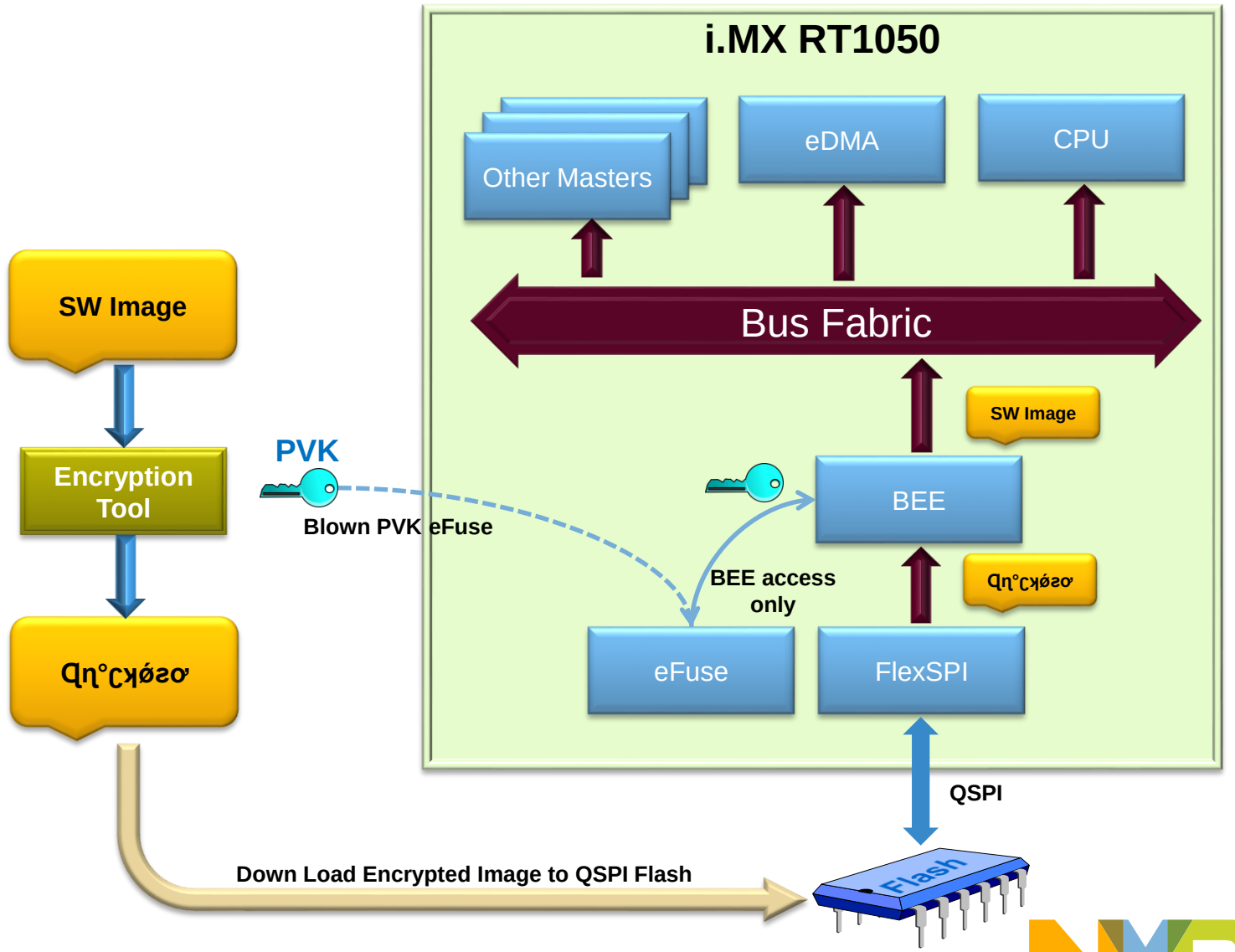
Image Protection – Encrypted XiP

Image generation

- Entire or partial SW image is encrypted with customized private secret key (PVK)
- The secret key is then burned to on chip eFuse block (OCOTP) and limited to be BEE access only
- Each chip could use a unique secret key to encrypt the SW image, so each image can only boot on the chip with the right secret key, “image clone” can be prevented

Image decryption

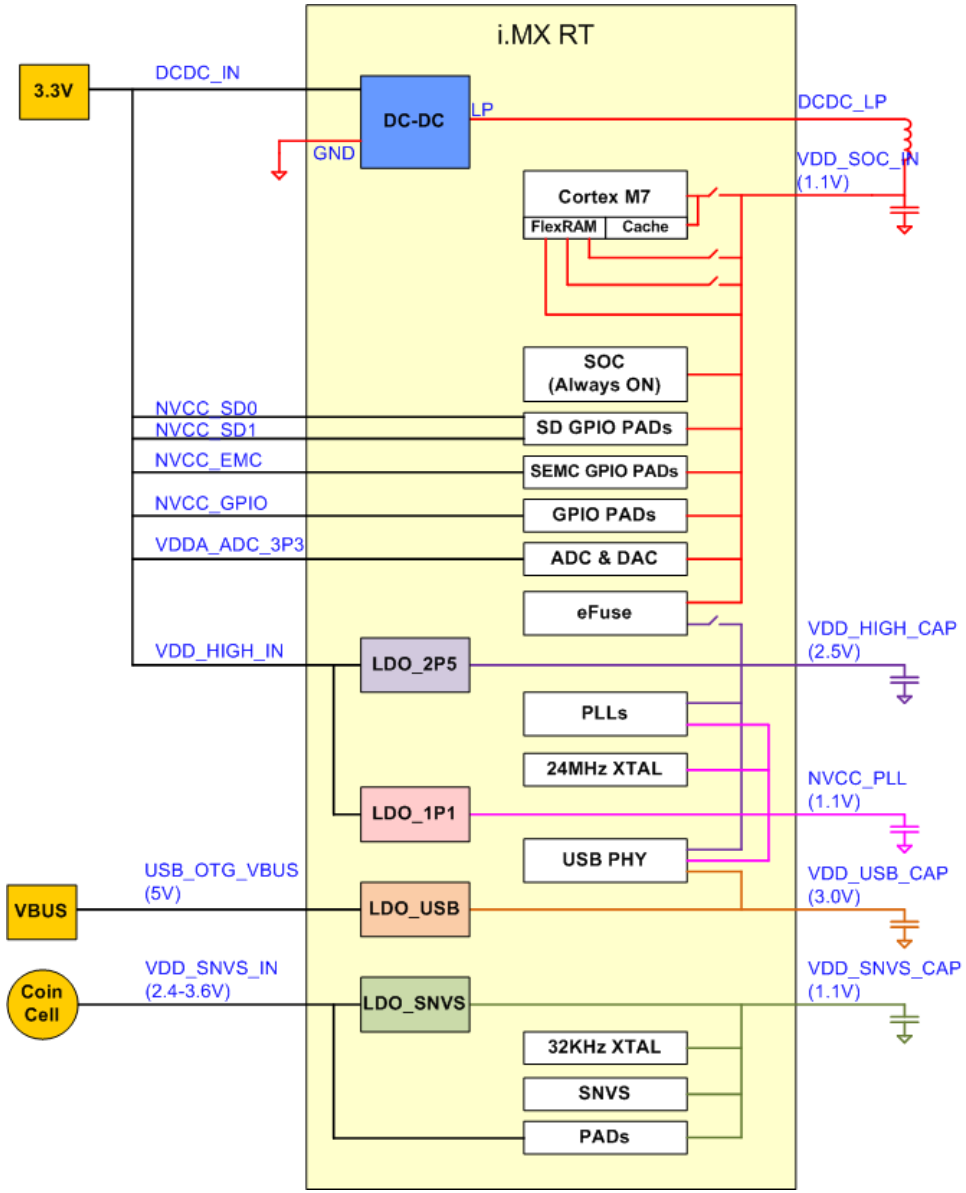
- During boot, ROM code initializes BEE based on boot image layout
- And then system master like CPU and eDMA can then get access to the plaint text on-the-fly



Power Management

Power architecture

- Full PMIC integration
  - Single 3.3v Power supply
  - Integrated high efficiency DC-DC for core power supply
  - Integrated LDO to reduce external power supply rails
- Smart Power management
  - SoC DVFS for dynamic power saving
  - Integrated Power Switch for effective power saving in low power mode
  - Simplified power on/off sequence



Run Mode Definition

Over Drive	• CPU runs at 600MHz, full loading • Internal bus frequency at full speed • All the peripheral is enable and runs at target frequency
Full Speed Run	• CPU runs at 528MHz, full loading • Internal bus frequency at full speed • All the peripheral is enable and runs at target frequency
Low Speed Run	• CPU runs at 132MHz • Internal bus frequency at quarter speed • Some PLL are powered down • Only necessary peripherals are active, others are in low power mode
Low Power Run	• CPU runs at 24MHz, lower core voltage • Internal bus frequency at 12MHz • All PLLs are powered down • High-speed peripherals are power down

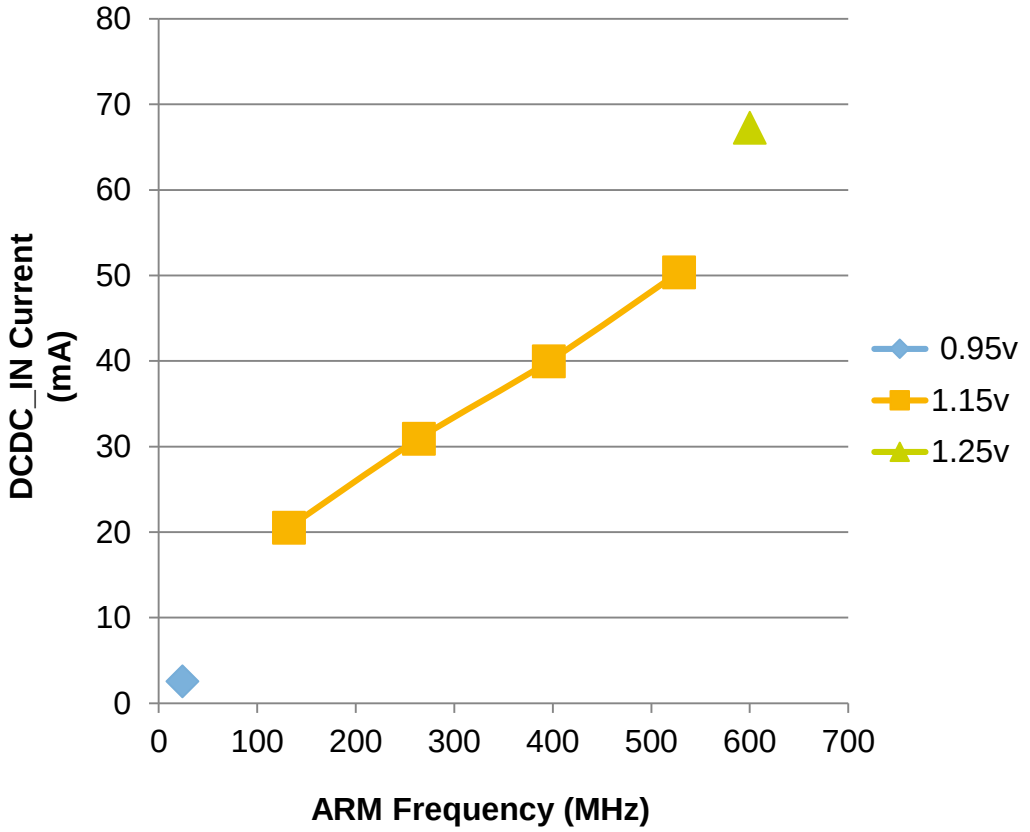
Low Power Mode Definition

System Idle	• CPU can automatically enter this mode when no thread running • All the peripheral can remain active • CPU only enter WFI mode, it will have its state retained so the interrupt response can be very short • SDRAM put into self-refresh by SW
Low Power Idle	• Much lower power than System Idle mode, with longer exit time • All PLLs are shut off, analog modules running in low power mode • All high-speed peripheral are power gated, low speed peripherals can remain running at low frequency • SDRAM put into self-refresh by SW
Suspend	• The most power saving mode with longest exit time • All PLLs are shut off, XTAL are off, all clocks are shut off except 32K clock • All peripherals are clock gated • SDRAM put into self-refresh by SW
SNVS	• All SOC digital logic, analog module are shut off only except SNVS domain • 32KHz RTC is alive

CoreMark with DVFS – All Peripheral On

VDD_SOC_IN	Frequency	DCDC_IN Current
(V)	(MHz)	(mA)
0.95	24	2.57
1.15	132	20.53
1.15	264	30.91
1.15	396	39.96
1.15	528	50.36
1.25	600	67.28

- **112.1 uA/MHz** at 600MHz

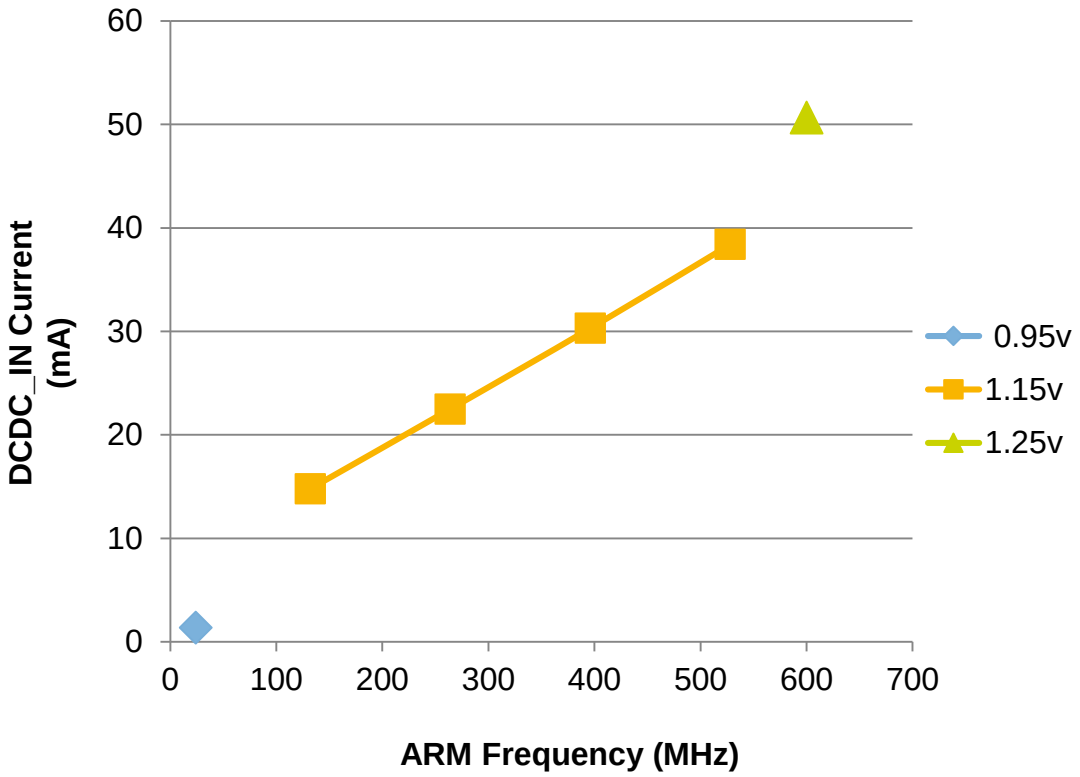


- All peripherals are clock enabled
- All power numbers are typical silicon at 25C
- Not include power on VDD_HIGH_IN, VDD_SNVS_IN and NVCC

CoreMark with DVFS – All Peripheral Off

VDD_SOC_IN	Frequency	DCDC_IN Current
(V)	(MHz)	(mA)
0.95	24	2.32
1.15	132	12.86
1.15	264	20.72
1.15	396	28.49
1.15	528	36.43
1.25	600	48.07

- **80.1 uA/MHz** at 600MHz



- All peripherals are clock gated
- All power numbers are typical silicon at 25C
- Not include power on VDD_HIGH_IN, VDD_SNVS_IN and NVCC

Run Mode

Power Rail	Overdrive (600MHz)			Full Speed Run (528MHz)			Low Speed Run (132MHz)			Low Power Run (24MHz)		
	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)
DCDC_IN	3.3	67.280	222.024	3.3	50.770	167.541	3.3	13.210	43.593	3.3	2.320	7.656
VDD_HIGH_IN	3.3	19.840	65.472	3.3	19.280	63.624	3.3	10.060	33.198	3.3	0.310	1.023
VDD_SNVS_IN	3.3	0.068	0.224	3.3	0.055	0.182	3.3	0.024	0.079	3.3	0.015	0.050
Total Current (mA)			**87.188**			**70.105**			**23.294**			**2.645**

- Overdrive: CPU runs at 600MHz, all peripheral enabled and running at target frequency.
- Full Speed Run: CPU runs at 528MHz, all peripheral enabled and running at target frequency.
- Low Speed Run: CPU runs at 132MHz, 20% peripheral active.
- Low Speed Run: CPU runs at 24MHz, only low speed peripherals active, such as UART/I2C.
- All power numbers are typical silicon at 25C

Low Power Mode

Power Rail	System Idle			Low Power Idle			Suspend			SNVS		
	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)
DCDC_IN	3.3	2.860	9.438	3.3	0.990	3.267	3.3	0.170	0.561	0	0	0
VDD_HIGH_IN	3.3	6.720	22.180	3.3	0.260	0.924	3.3	0.016	0.033	0	0	0
VDD_SNVS_IN	3.3	0.024	0.080	3.3	0.038	0.125	3.3	0.015	0.05	3.3	0.015	0.050
Total Current (mA)			**9.604**			**1.288**			**0.201**			**0.015**

* All power numbers are typical silicon at 25C.

i.MX RT1050: Orderable Part Numbers Overview

Description	Production Part #	Qualification Tier	Package	CPU Frequency	Features
i.MXRT1050 Industrial 10x10	MIMXRT1052CVL5A	Industrial	196MAPBGA 10mm X 10mm 0.65pitch	500M	500Mhz, Industrial Grade for general purpose - basic security, with LCD/CSI , PXP, CAN x2, Ethernet , EMMC 4.5/sd 3.0 x2,USB OTG x2, UART x8, SAI x3, Timer x4, PWM x4, I2C x4, SPI x4
i.MXRT1050 Industrial 10x10	MIMXRT1051CVL5A	Industrial	196MAPBGA 10mm X 10mm 0.65pitch	500M	500Mhz, Industrial Grade for general purpose - basic security, no LCD/CSI, PXP , CAN x2, Ethernet , EMMC 4.5/sd 3.0 x2,USB OTG x2, UART x8, SAI x3, Timer x4, PWM x4, I2C x4, SPI x4
i.MXRT1050 Commercial 10x10	MIMXRT1052DVL6A	Commercial	196MAPBGA 10mm X 10mm 0.65pitch	600M	600Mhz,Commercial Grade for general purpose - basic security, with LCD/ CSI , PXP, CAN x2, Ethernet , EMMC 4.5/sd 3.0 x2,USB OTG x2, UART x8, SAI x3, Timer x4, PWM x4, I2C x4, SPI x4
i.MXRT1050 Commercial 10x10	MIMXRT1051DVL6A	Commercial	196MAPBGA 10mm X 10mm 0.65pitch	600M	600Mhz, Commercial Grade for general purpose - basic security, no LCD/CSI, PXP , CAN x2, Ethernet , EMMC 4.5/sd 3.0 x2,USB OTG x2, UART x8, SAI x3, Timer x4, PWM x4, I2C x4, SPI x4
MIMXRT1050 Development Platform	MIMXRT1050-EVK			600M	Micro USB Host connector, Micro USB OTG connector, Ethernet (10/100T) connector, CAN Transceivers, ARDUINO interface, Parallel LCD connector, Camera Connector, 6-Axis Ecompass (3-Axis Mag, 3-Axis Accel) sensor FXOS8700CQ, Audio Codec, 4-pole Audio Headphone Jack, External speaker connection, Microphone, SPDIF Connector
4.3” Display	RK043FN02H-CT			-	4.3” LCD Display

MIMXRT1050 Development Platform Key Features

Part Numbers: MIMXRT1050-EVK ($79)
Display (4.3”): RK043FN02H-CT ($29)

Processor
- NXP Semiconductors MIMXRT1052DVL6A 600MHz ARM Cortex-M7

Memory
- 256 Mbit SDRAM memory
- 512Mbit Hyper Flash
- Footprint for QSPI Flash
- TF socket for SD card

Display
- Parallel LCD connector
- Camera Connector

Audio
- Audio Codec
- 4-pole Audio Headphone Jack
- External speaker connection
- Microphone
- SPDIF Connector

Connectivity
- Micro USB Host connector
- Micro USB OTG connector
- Ethernet (10/100T) connector
- CAN Transceivers
- ARDUINO interface

Debug
- JTAG connector
- On board DAP-Link debugger

Sensor
- 6-Axis Ecompass (3-Axis Mag, 3-Axis Accel) sensor FXOS8700CQ

Tools & OS Support
- IAR, MDK
- SDK with FreeRTOS

Others
- All in one board design
- 4 layer through hole PCB

IAR SYSTEMS KEIL Tools by ARM

MCUXpresso RTOS

i.MX RT Series

196BGA, 10x10

Cortex-M7 up to 600MHz
32KB/32KB I/D Cache
512KB SRAM / TCM
4x Flex PWM, 4x Quad Timer, 4x ENC
2x HS USB, 2x SDIO, 2x CAN, 1x ENET
8x UART, 4x SPI, 4x I2C
Qual-SPI interface
External Memory Controller (SDRAM, NOR, NAND)
3x SAI/ SPDIF RX & TX/ 1x ESAI
2x ADC, 4x ACMP
PxP for 2D acceleration
Parallel Camera Interface
Parallel LCD Interface
TRNG&PRNG
128-AES cryptography
Bus Encryption Engine
Integrated PMIC

Package:
- 196BGA, 10x10, 0.65 pitch

144LQFP, 20x20
100LQFP, 14x14

Cortex-M7 up to 500MHz
16KB/16KB I/D Cache
256KB SRAM / TCM
2x Flex PWM, 2x Quad Timer, 2x ENC
1x HS USB, 2x SDIO, 2x CAN, 1x ENET
8x UART, 4x SPI, 4x I2C
Qual-SPI interface
External Memory Controller (SDRAM, NOR, NAND)
3x SAI/ SPDIF RX & TX/ 1x ESAI
2x ADC, 4x ACMP
-n/a-
-n/a-
-n/a-
TRNG&PRNG
128-AES cryptography
Bus Encryption Engine
Integrated PMIC

Package:
- 144LQFP, 20x20, 0.5 pitch
- 100LQFP, 14x14, 0.5 pitch

Changes from RT1050

i.MX RT – Helpful links

- i.MX RT web page: www.nxp.com/imxrt
  - Introduction and Fact Sheet
  - Datasheet and Reference Manual
  - White paper Crossover processing
  - i.MX RT blog
  - Videos

- i.MX RT + TouchGFX webinar: Unbeatable UI Performance on New NXP Crossover Processor
  - i.MX RT webpage under Training and Support
  - https://register.gotowebinar.com/rt/1949795142102802433?source=NXP

i.MX RT Crossover Processor

Unprecedented performance and usability never before seen in the embedded market

2 FAMILIES FOR MAX FLEXIBILITY

i.MX RT1050 is available now starting at $2.98 USD for 10K quantity
i.MX RT1020 will be available Q2 2018 and priced at $2.18 USD for 10K quantity

SIGNIFICANTLY LOWER SYSTEM LEVEL COST

Higher performance than other products on the market at a FRACTION of the cost
Lower bill-of-materials cost and lower cost of programming with off-chip memories

arm TechCon

WED OCT 25 11:30am-12:20pm | Rob Cosaro, NXP Fellow
The Convergence of Applications Processors and Microcontrollers Unfolds with the Advent of High Performance Arm Cortex-M7 Based Devices

Audio playback demo at NXP Booth (#500)

www.nxp.com/iMXRT

THANK YOU

SECURE CONNECTIONS
FOR A SMARTER WORLD