S32K3 | Safe and Secure Family of Automotive General Purpose MCUs

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Automotive FAE
May 2024

LEADING AUTOMOTIVE SEMICONDUCTOR SYSTEM SOLUTIONS
IS HOW WE HELP OUR CUSTOMERS ACCELERATE BREAKTHROUGHS

Headquarters in The Netherlands
~34,500
employees

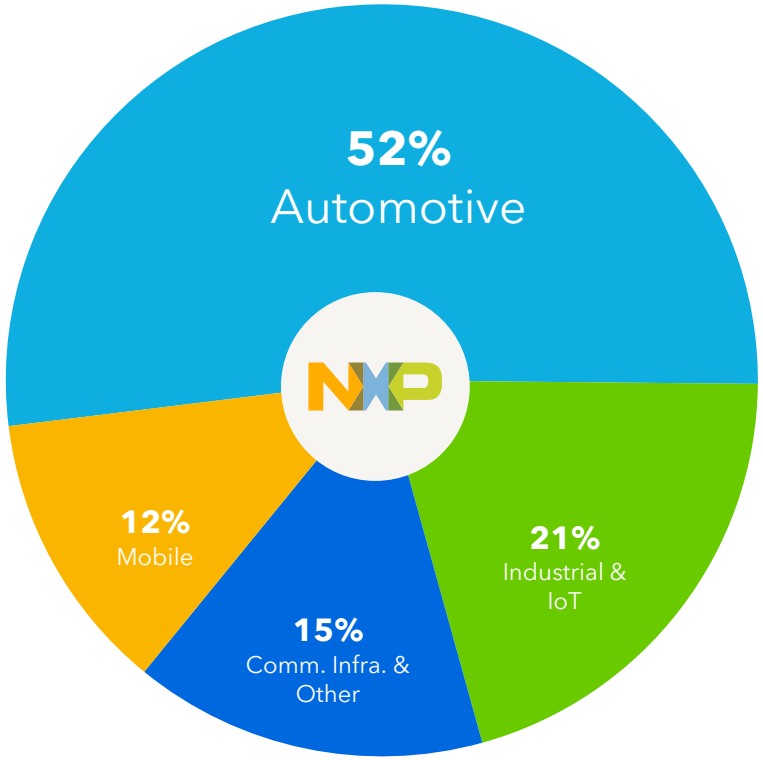
11,000
R&D Engineers

9,500
Patents

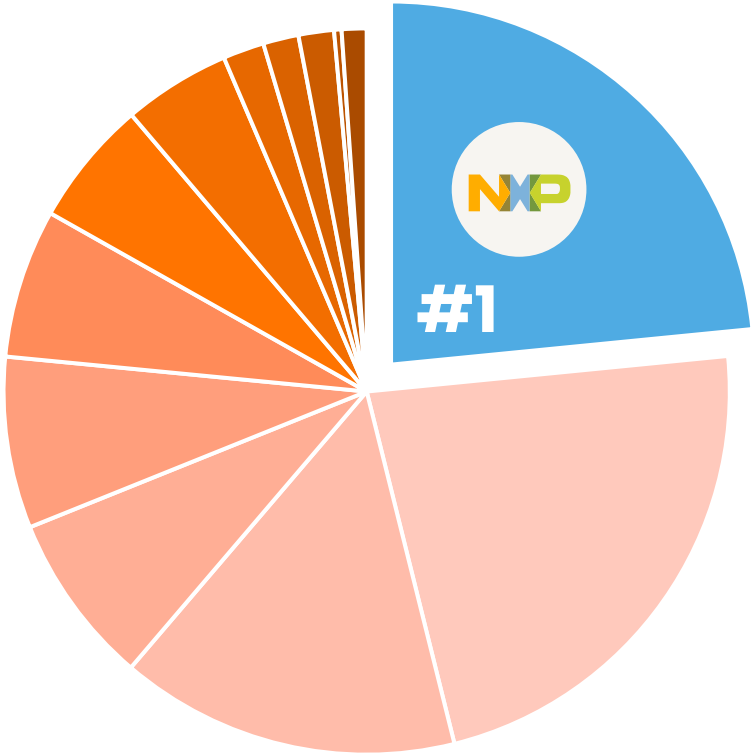
2022 Revenue
$13.2B

Capacity committed for growth to
~$15B in 2024
(+8-12% p.a.)

2022 REVENUE
BY END-MARKET EXPOSURE



2022 AUTO PROCESSOR MARKET SHARE



~**725MU** shipped in 2023 (~**2MU** per day)
S32K1: over **440MU** shipped, **<50PPB**

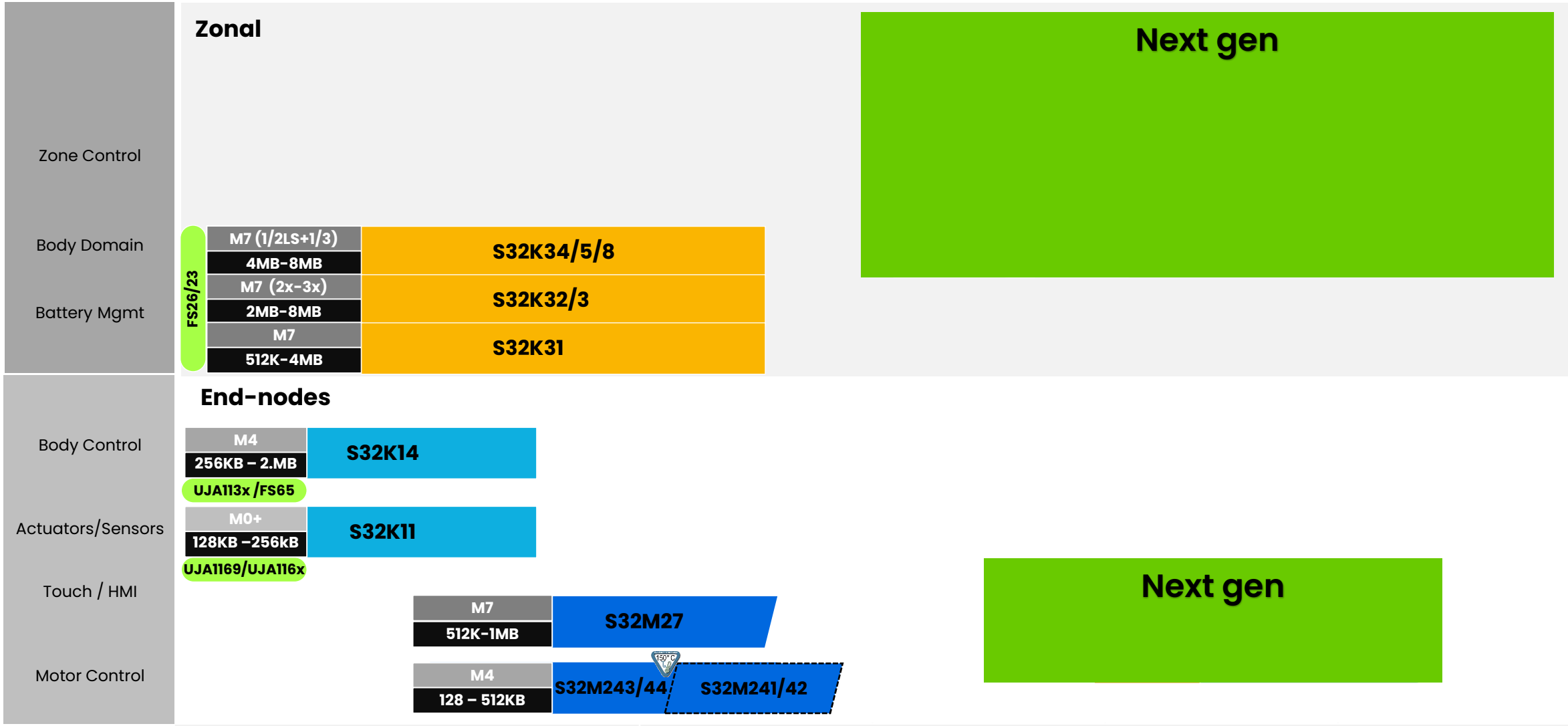
Source: TechInsight / Strategy Analytics (Mar 2023)

Agenda

- S32K3 Family overview
- A word about safety
- A word about security
- Application specific peripherals
- Software offering

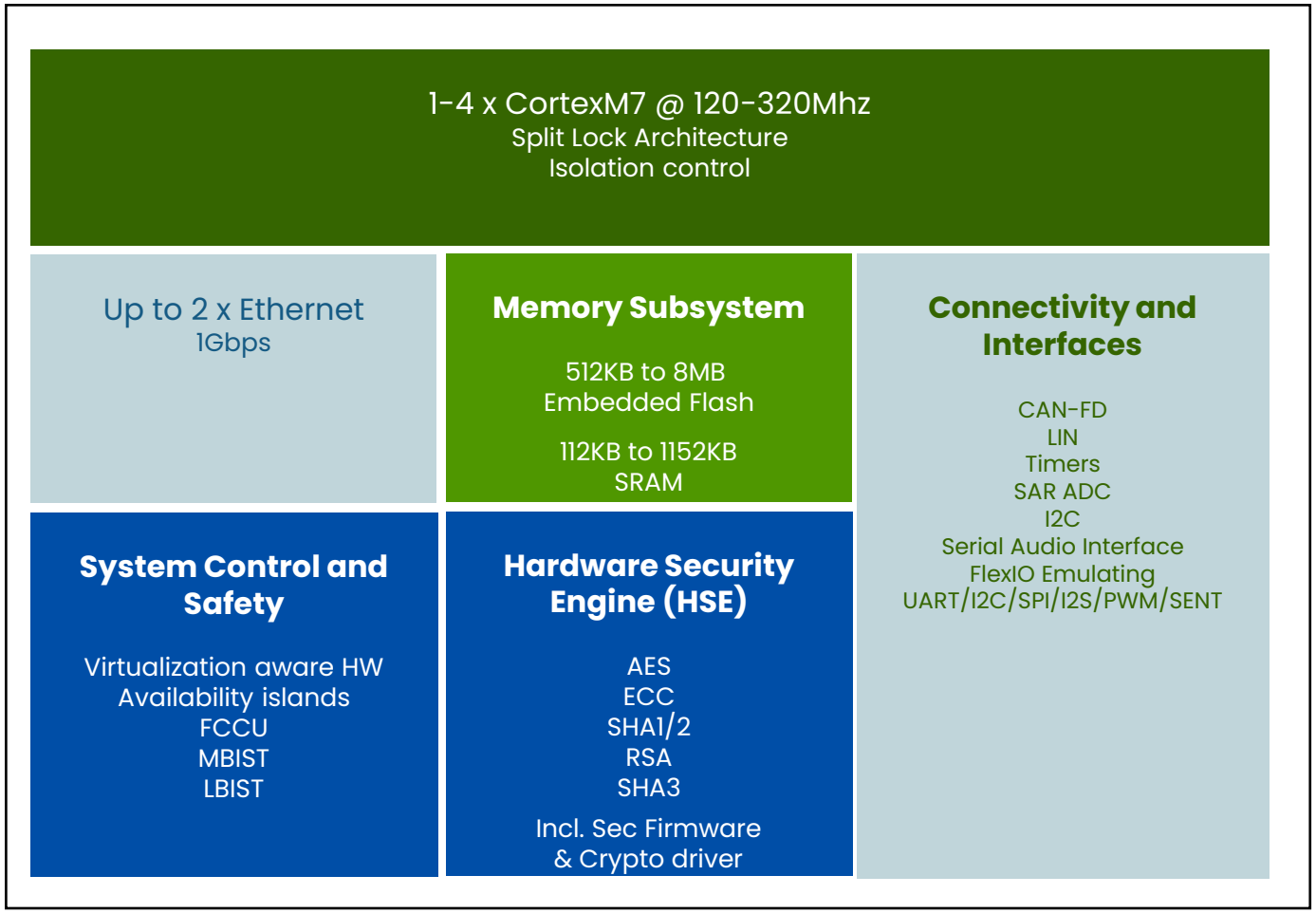
Last update: April 17th, 2024

Automotive Microcontrollers Roadmap

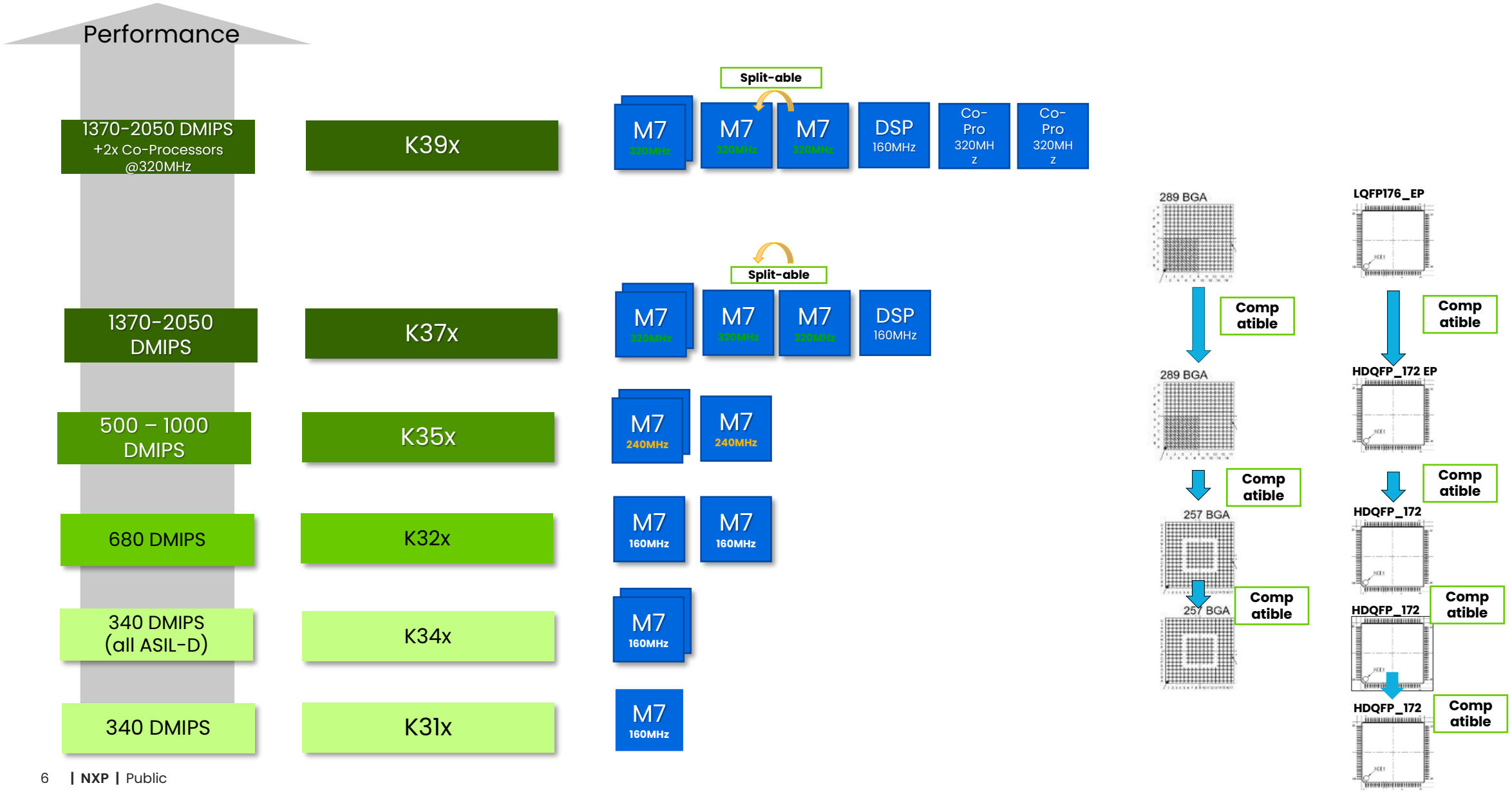


LS: Lock Step, SL= Split Lock Step

S32K3 – Scalable, Low Power, 512KB-8MB Flash MCU

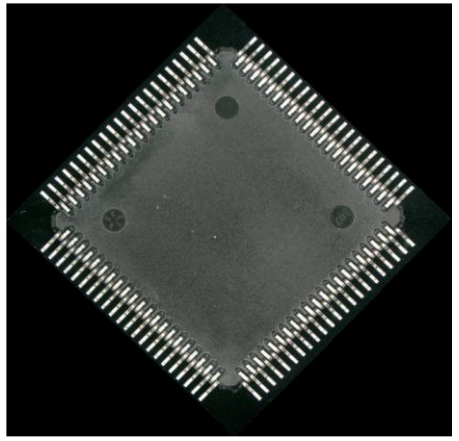


S32K3xx– Performance scalability & pin-to-pin compatibility

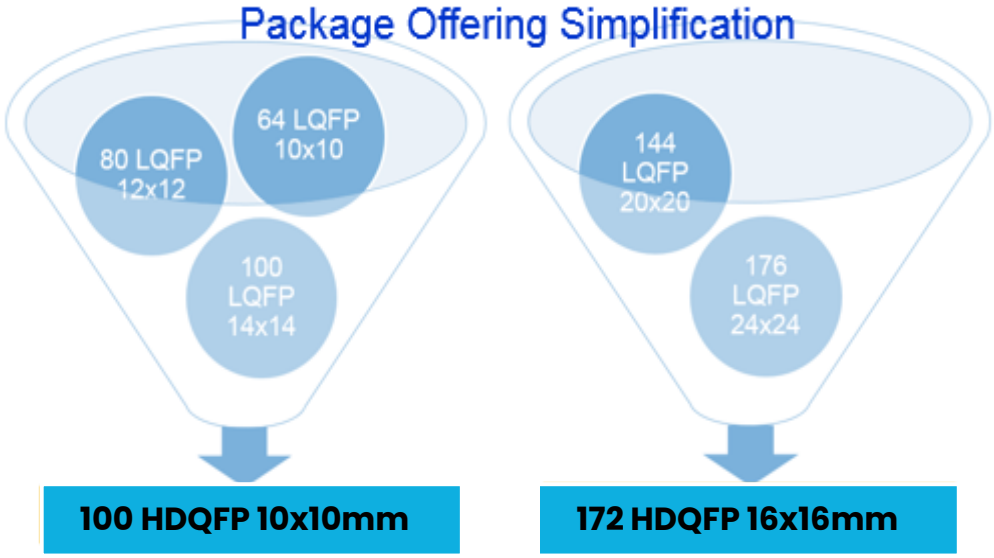


S32K3 Platform – Unmatched Scalability

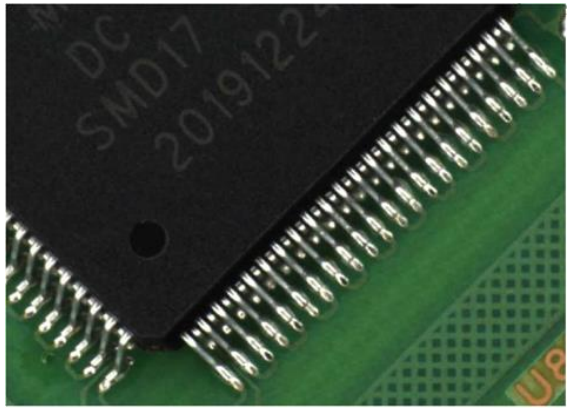
- Core & Platform: Same Arm Cortex M7 core across S32K3 family for SW reuse
- Security: HSE B across S32K3 family
- Safety: ASIL D and ASIL B fully compatible in S32K3 family
- Memory: 512K-8MB in S32K3, scalable down to 128KB in S32K1
- Package: BGA / HDQFP pin compatible in S32K3 family

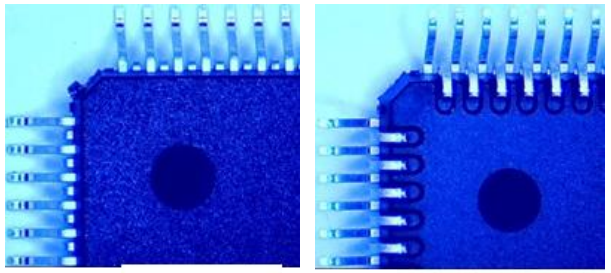


K3 Flash	K3 Package				
	48 LQFP	100 HDQFP	172 HDQFP	257 BGA	289 BGA
	7 x 7 mm	10 x 10 mm	16 x 16 mm	14 x 14 mm	14 x 14 mm
8M			**K358/48/38/28 with Exposed Pad**		**K388 K358/48/38/28* ***
6M					**K376/K396****
4M			**K344/24/14**	**K344/24/14**	**K374/K394****
2M		**K342/22/12**	**K342/22/12**		
1M	**K311**	**K311**	**K341**		
512K	**K310**	**K310**			



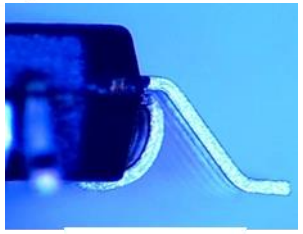
HDQFP – Summary





Top view

Bottom view



Side view

Disruptive leadframe package:

- Combining QFP 'gull-wing' + PLCC 'J-lead'
- Significant NXP IP: innovation with patents

Benefits:

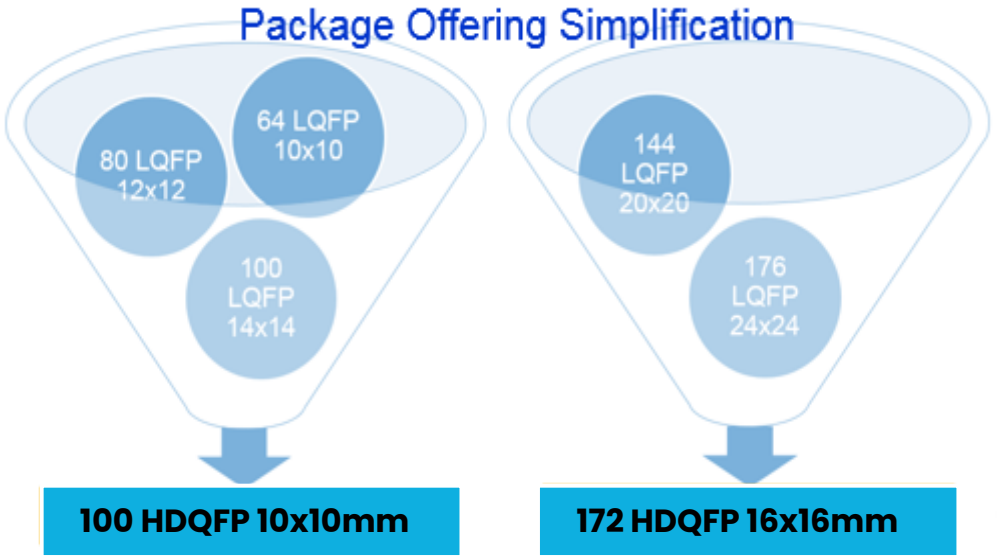
- ~2x IO count in similar size or ½ package size with similar IO count
- Package portfolio simplification
- No extra cost
- Same PCB design rules as 0.5mm pitch QFP - No additional PCB Cost
- Solder joint inspectable with 3D automatic optical inspection

Package options on S32K3:

- 100 HDQFP (10 x 10 mm)
- 172 HDQFP (16 x 16 mm)

Package status:

- Package Qualification: AEC Q100 Grade1 completed



S32K3xx 512K-4MB Device Feature Overview

S32K310	S32K311	S32K312	S32K314	S32K322	S32K324	S32K341	S32K342	S32K344	S32K374	S32K394
1x Cortex-M7 @ 120MHz			1x Cortex-M7 @ 160MHz	2x Cortex-M7 @ 160MHz		1x LS Cortex-M7 @ 160MHz			1x LS Cortex-M7 + 2x Cortex-M7 @ 320MHz Or 2x LS Cortex-M7 @320MHz + 1x DSP (CoolFlux) @ 160MHz	1x LS Cortex-M7+2x Cortex-M7 @ 320MHz Or 2x LS Cortex-M7 @320MHz + 1x DSP (CoolFlux) @ 160MHz + 2x I/O Co-Processors @ 320MHz
ASIL B	ASIL B	ASIL B	ASIL B	ASIL B	ASIL B	ASIL D	ASIL D	ASIL D	ASIL D	ASIL D
HSE B	HSE B	HSE B	HSE B	HSE B	HSE B	HSE B	HSE B	HSE B	HSE B	
512KB Flash	1MB Flash	2MB Flash	4MB Flash	2MB Flash	4MB Flash	1MB Flash	2MB Flash	4MB Flash	4MB Flash	
112K SRAM incl. 96K TCM	128K SRAM incl. 96K TCM	192K SRAM incl. 96K TCM	512K SRAM incl. 96K TCM	256K SRAM incl. 192K TCM	512K SRAM incl. 192K TCM	256K SRAM incl. 192K TCM	256K SRAM incl. 192K TCM	512K SRAM incl. 192K TCM	800K SRAM incl. 288K TCM	
up to 84 I/Os	up to 84 I/Os	up to 145 I/Os	up to 218 I/Os	up to 142 I/Os	up to 218 I/Os	up to 142 I/Os	up to 142 I/Os	up to 218 I/Os	up to 218 I/Os	
12 channel eDMA			32ch eDMA	32 channel eDMA					2x 32 channel eDMA (1 w/ Lockstep)	
3x FlexCAN w/ CAN-FD		6x FlexCAN w/ CAN-FD		4x FlexCAN w/ CAN-FD	6x FlexCAN w/ CAN-FD	4xFlexCAN w/ CAN-FD	4x FlexCAN w/ CAN-FD	6x FlexCAN w/ CAN-FD	6x FlexCAN w/ CAN-FD	
			No Ethernet / 1x 100Mbps Ethernet (TSN)	No Ethernet / 1x 100Mbps Ethernet (TSN)						
2x I2C			2x I2C	2x I2C	2x I2C	2x I2C	2x I2C	2x I2C	2x I2C	
4x SPI**			6x SPI**	4x SPI**	6x SPI**	4x SPI**	4x SPI**	6x SPI**	6x SPI**	
2x 24ch 12-bit ADC			3x 24ch 12-bit ADC	2x 24ch 12-bit ADC	3x 24ch 12-bit ADC	2x 24ch 12-bit ADC	2x 24ch 12-bit ADC	3x 24ch 12-bit ADC	7x 12-bit ADC 4x SD-ADC 2x 12-bit DAC	
			2 x SAI (I2S)	2x SAI (I2S)					-	
			Quad SPI	Quad SPI					Quad SPI	
									ZipWire	
LQFP-48		HDQFP-172		HDQFP-172					LQFP-176EP	
HDQFP-100				HDQFP-100		HDQFP-100	HDQFP-100			
			MAPBGA-257		MAPBGA-257			MAPBGA-257	MAPBGA-289	

Common HW: LPUART, FlexIO, eMIOS Timers, ACMP, LCU, BCTU, TRGMUX
Common SW: Real Time Driver, Security FM, Safety Framework SW & Core Self Test

S32K3xx 6M-12MB Device Feature Overview

S32K376	S32K396	S32K328	S32K338	S32K348	S32K358	S32K388	S32K389*
1x LS Cortex-M7+2x Cortex-M7 @ 320MHz Or 2x LS Cortex-M7 @320MHz + 1x DSP (CoolFlux) @ 160MHz	1x LS Cortex-M7+2x Cortex-M7 @ 320MHz Or 2x LS Cortex-M7 @320MHz + 1x DSP (CoolFlux) @ 160MHz + 2x I/O Co-Processors @ 320MHz	2x Cortex-M7 @ 240MHz	3x Cortex-M7 @ 240MHz	1x LS Cortex-M7 @ 240MHz	1x LS Cortex-M7 + 1x Cortex-M7 @ 240MHz	1x LS Cortex-M7 + 3xCortex-M7 @ 320MHz or 2x LS Cortex-M7 + 1xCortex-M7 @ 320MHz	1x LS Cortex-M7 + 3xCortex-M7 @ 300MHz or 2x LS Cortex-M7 + 1xCortex-M7 @ 300MHz
ASIL D	ASIL D	ASIL B	ASIL B	ASIL D	ASIL D	ASIL D	ASIL D
HSE B	HSE B	HSE B	HSE B	HSE B	HSE B	HSE-B	HSE-B
6MB Flash		8MB Flash					12MB Flash
800K SRAM incl. 288K TCM		1152K SRAM Incl 192K TCM for K328,348. Incl 384K TCM for K338,358, 388					~2.3MB SRAM
up to 218 I/Os		up to 218 I/Os			Up to 235 I/Os		up to 330 I/Os
2x 32 channel eDMA (1 w/ Lockstep)		32 channel eDMA					32 channel eDMA
6x FlexCAN w/ CAN-FD		8x FlexCAN w/ CAN-FD					12x FlexCAN w/ CAN-FD
No Ethernet / 1x 100Mbps Ethernet (TSN)		No Ethernet / 1x 1Gbps Ethernet (TSN)				2x 1Gbps Ethernet (TSN)	2x 1Gbps Ethernet (TSN)
2x I2C	2x I2C	2x I2C					
6x SPI**	6x SPI**	6x SPI**					
7x 12-bit ADC, 4x SD-ADC, 2x 12-bit DAC		3x 24ch 12-bit ADC					
		2x SAI (I2S)					
Quad SPI							
		SDHC(SDIO)					
ZipWire							
		HDQFP-172 EP					
LQFP-176 EP							
MAPBGA-289							MAPBGA-437

*K389 feature is preliminary and subject to change, last update on 21st Feb 2024

S32K3 Communication Interfaces

- **Ethernet MAC (10/100/1000Mbps): MII/RMII interface, AVB and TSN support**
  - TSN Enhancement to Scheduled Traffic Standard 802.1Qbv-2015, Frame Preemption Standard 802.1Qbu-2016Standard 802.1br
  - Support IEEE 1722 Layer 2 Transport Protocol, IEEE 802.1AS Timing and Synchronization, IEEE 802.1Qav
  - Compliant with 3 Industrial Ethernet Protocols

- **Ethernet 10BaseT1S**
  - Supported by SPI + external MAC&PHY

- **CAN FD**
  - FlexCAN modules with ISOCAN-FD and DMA support
  - Support 5Mbps using 16 time quanta

- **Enhanced FlexIO configurable as different communication peripherals**
  - SENT, I2C, I2S, UART, SPI, entry level TFT LCD driver

- **Synchronous Audio Interface (SAI)**
  - Supports full duplex serial interfaces with frame synchronization such as I2S, AC97, TDM, and codec/DSP interfaces

S32K3 Power Management

- Flexible Voltage Level: 5V, 3.3V, or 5V & 3.3V split I/O domains
- Simplified Power Modes:

Standby	Run
• Main cores / Platform / Flash memory, PLL, etc, all power gated off; large parts of SoC inactive • Fixed amount of 32KB SRAM • Up to 60 wake-up pins supported via padkeeping • Wakeup logic, API / RTC • Analogue comparator sub-system • Clocks (FIRC, SIRC, SXOSC, FXOSC). CLKOUT available	• All modules + FLASH powered • All modules can be clock-gated to reduce power • Default exit from reset with all peripherals clock gated • Full support for max speed / max Idd mode • Default to operate from 48MHz FIRC

- Low power in Standby Mode
  - Typ current consumption ~60uA(K344) and ~50uA(K312)
  - All 60 wake up pins enabled to monitor IO, optimized power
- consumption in typical body/zone periodic wakeup use cc
- Power Estimation Tool with GUI

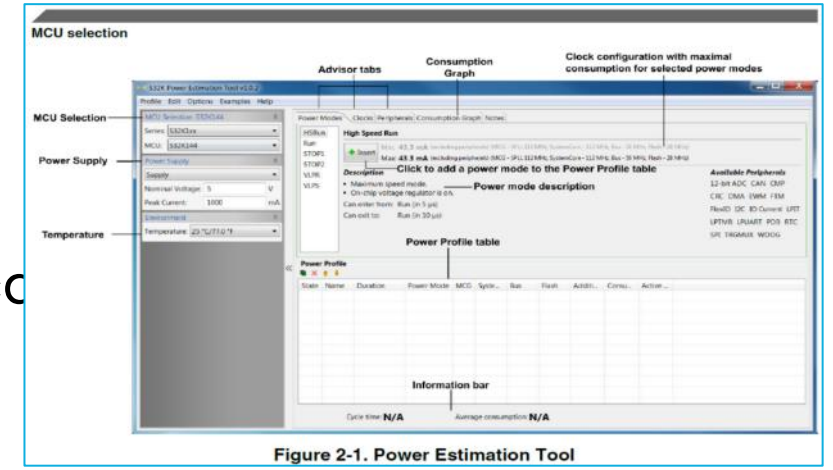
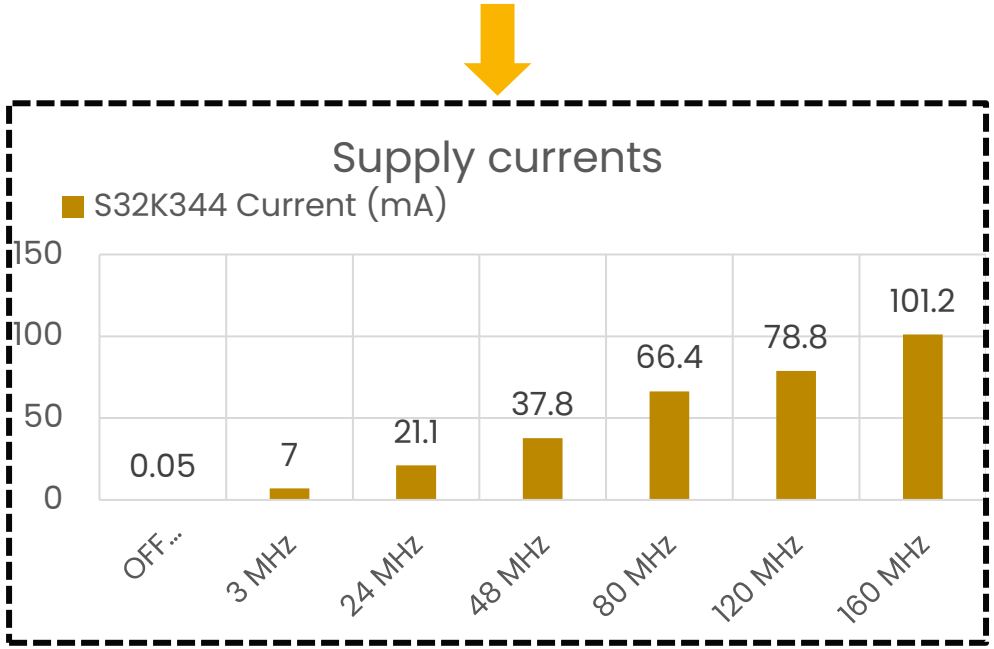


Figure 2-1. Power Estimation Tool

S32K3 Optimized for Low Current Consumption

RUN mode

- Scalable current consumption based on the application requirements.
- All modules + FLASH are powered.
- All modules can be clock-gated to reduce power.
- Full support for max speed. Up to 160MHz.



Standby mode

- Main cores / Platform / Flash / PLL are power gated off. Large parts of SoC inactive.
- STANDBY-RAM (32KB Content retention).
- WAKE-UP from up to **60** digital inputs.
- WAKE-UP from up to **24** analog inputs **(3 x LPCMP).**
- WAKE-UP from on-chip timers **(PIT0, SWT0, RTC).**
- Pad-keeping.
- Configurable secure and un-secure wake-up routes.

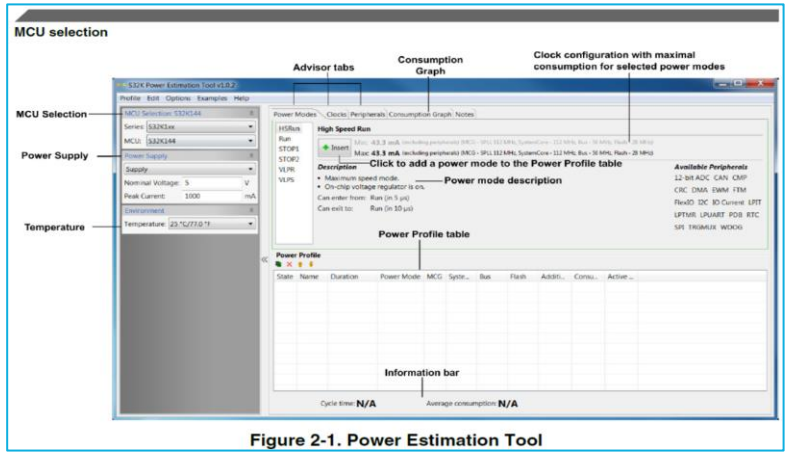


Figure 2-1. Power Estimation Tool

S32K3xx OTA Solution

Seamless update

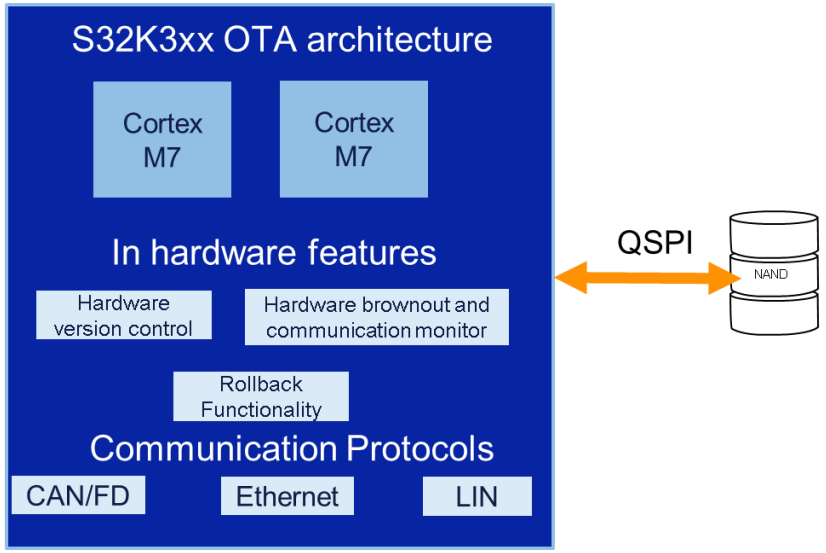
- Zero downtime - download while application running with ***Read while write between flash banks.***

No compiler/linker restrictions

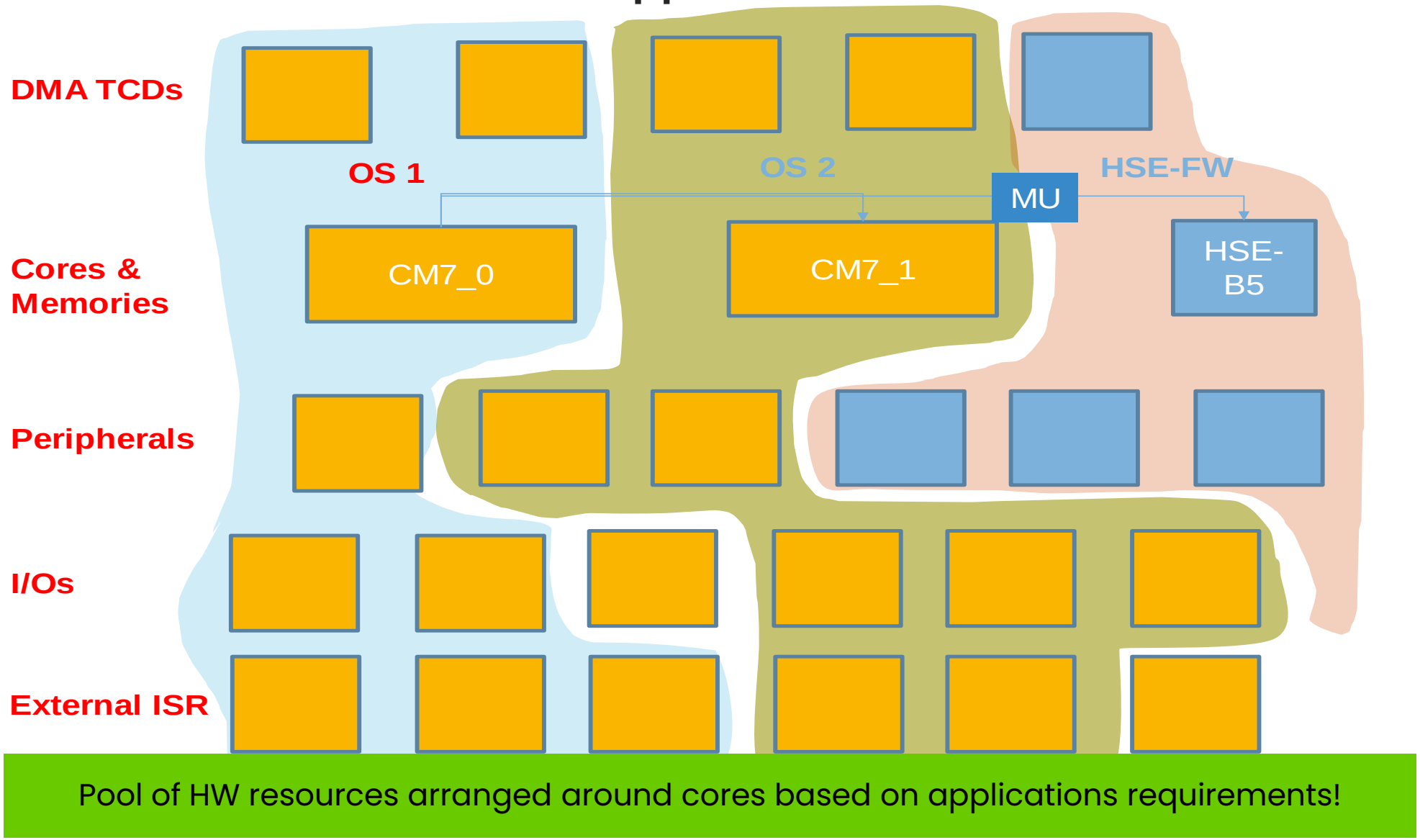
- Automatic firmware ***address translation.***

Reliable and Robust update

- ***Rollback functionality*** to backup firmware controlled by HSE .
- Secure firmware version control In HW
- Contains incremental and bitwise-complement sections to indicate firmware revision and firmware validity
- Managed by HSE
- brownout and communication monitor in HW by ***Firmware indicator validation***



S32K3xx Freedom of Interferences Support



Security

S32K3 Security offer is simpler

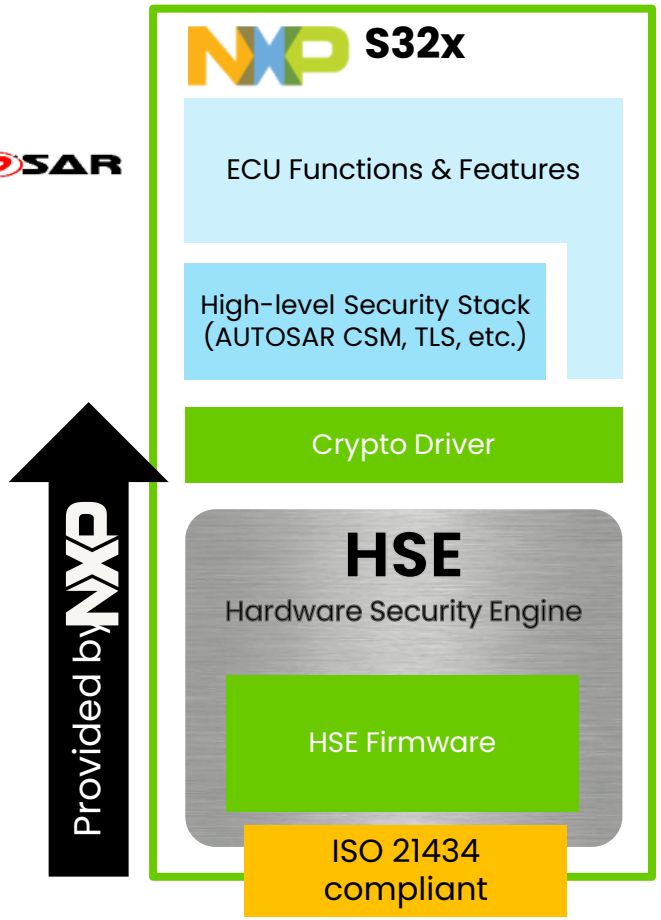
Comprehensive service offer

- FAE support
- FQE analysis
- PSIRT
- Standard crypto-driver: MCAL

No extra costs

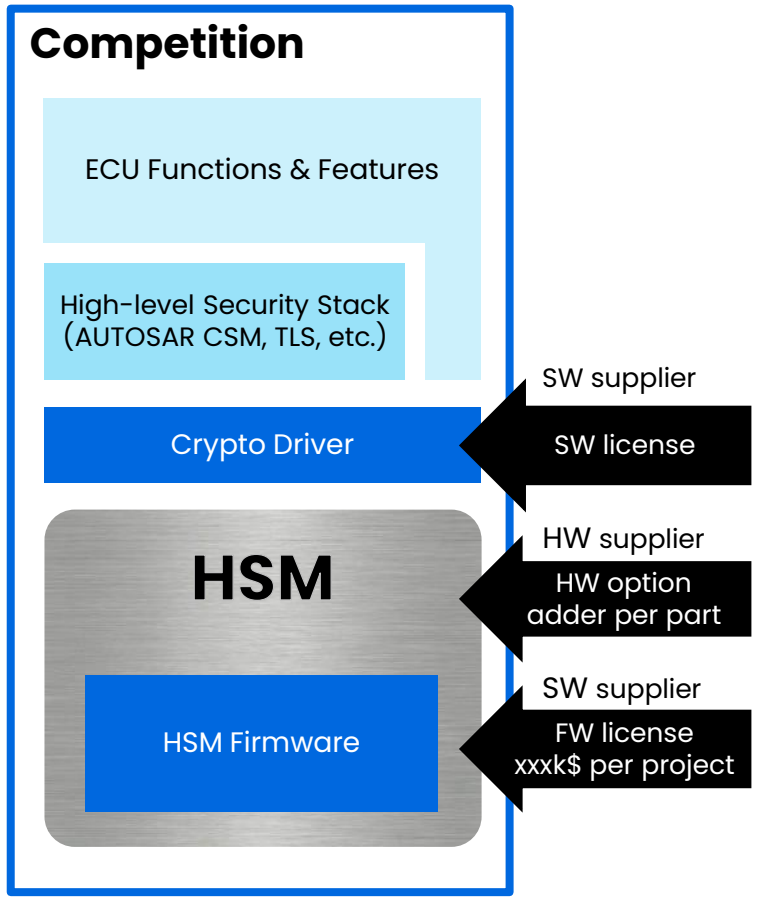
- No license fees
- No maintenance fees
- Solution cost covered by device price

One-stop-shop (HW + FW)
Cost-optimized solution

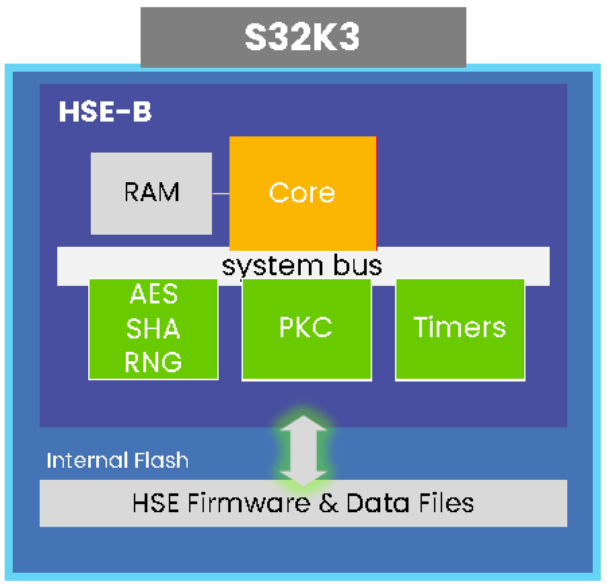


VS

Two suppliers (HW / FW)
Higher solution cost & complexity



HSE – Security services



KEY MANAGEMENT

- KEY IMPORT
- KEY EXPORT
- KEY GENERATION
- KEY DERIVATION
- KEY EXCHANGE
- KEY FILE MANAGEMENT

AES 256 BITS / RSA 4096 BITS
ECC ON PRIME CURVES

CRYPTO OPERATIONS

- AES
  ENCRYPTION & DECRYPTION
- CMAC / HMAC
  GENERATION & VERIFICATION
- HASHING (SHA2 & SHA3)
- RSA / ECC SIGNATURE
  GENERATION & VERIFICATION
- RSA OAEP / ECIES
  ENCRYPTION & DECRYPTION
- RANDOM GENERATION
  TRNG & PRNG

ALL OPERATIONS
HARDWARE ACCELERATED

PLATFORM SECURITY

- STRICT SECURE BOOT
  VERIFY-THEN-START
- PARALLEL SECURE BOOT
  VERIFY-AND-START
- ON-DEMAND VERIFICATION
  SECURE BOOT CONTROL IN APP.
- CONFIGURABLE SANCTIONS
  E.G. KEY USAGE RESTRICTIONS

SECURE BOOT
OPTIMIZED FOR SPEED

S32 HSE : one stop shop for security

NXP is committed to be a “one-stop shop” for its HSE solution

HSE solution = HW (HSE subsystem) + FW (HSE services)

Key Benefits

Best Performances
Best Security Assurance Level
Faster Time-to-Market
Low ASP

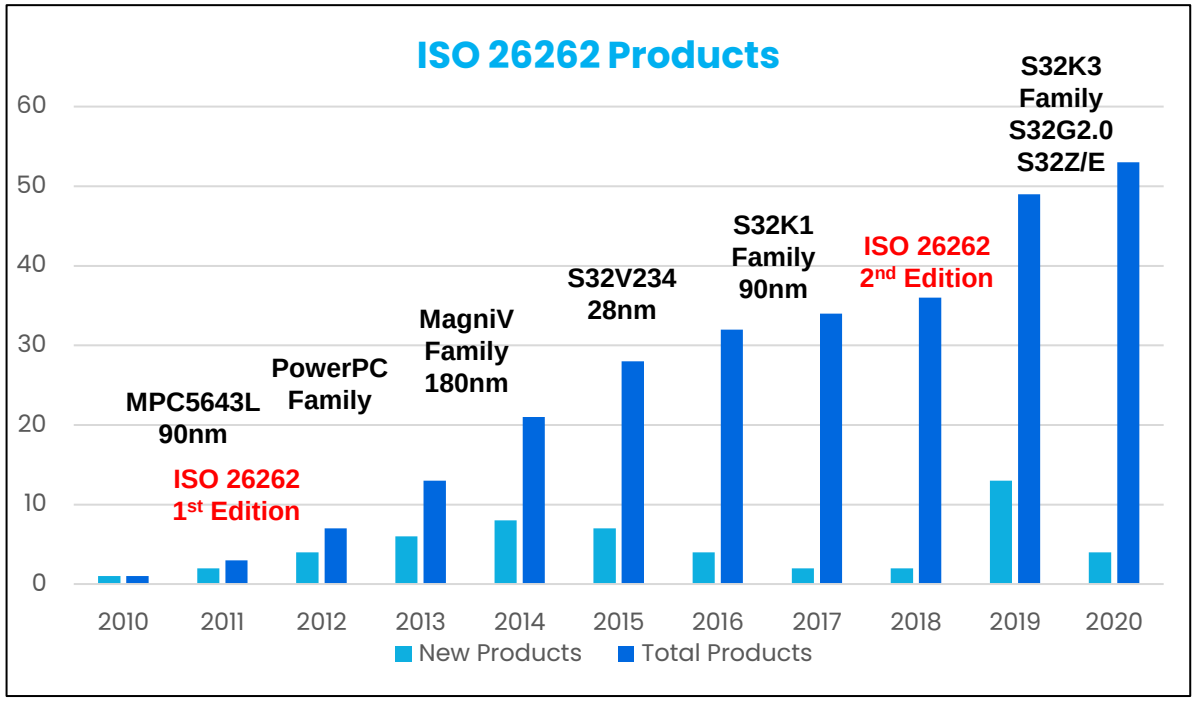
Extras

Seamless Integration
(Standard SW Stacks)
Custom Extensions When Necessary
In-Field Updatable

Safety

ISO 26262 Products in Automotive Processing (AP)

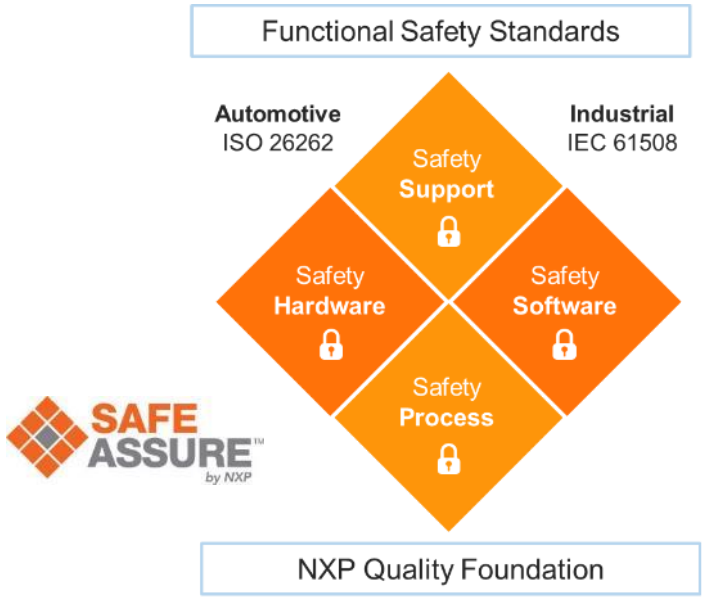
- 20+ years of safety MCU/MPU development.
- Safety Collaterals (FMEDA, Manual, etc.) provided with products before 2010.
- Rapid growth of safety products since 2010.
- MPC5643L is the industry's first semiconductor product to achieve the ISO26262 certification from an independent accredited assessor in 2012.
- BCAM7 development process certified by TUV for ISO26262 compliance in 2017.
- Certification updated to comply with ISO26262:2018 in 2019.

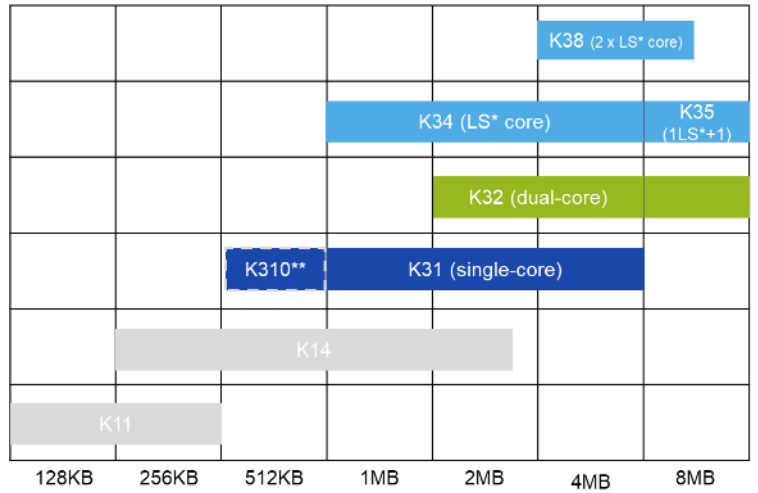



Certificate / Certificat
Zertifikat / 合格証
FREESCALE 1108067 P0026 C001
exida Certification S.A. hereby confirms that the:
MICROCONTROLLER MPC5643L
FREESCALE Halbleiter Deutschland GmbH
Munich, Germany
Has been assessed per the relevant requirements regarding µC development and verification & validation of:
ISO 26262 : 2011 Parts 2, 4, 5, 7, 8, 9 and 10 (to the extent applicable)
and meets requirements providing:
Systematic Integrity: ASIL D
Safety related function:
The µC supports the execution of safety-related software by a dual-core lock-step architecture with memory protection and centralized fault collection and control unit.
Application restrictions:
The microcontroller shall be used per the Safety Application Guide requirements.
Reports:
Freescale 11/08-067-C R009 V1 R0
Results of the ISO 26262 Functional Safety Assessment
Validity:
This assessment is valid for Microcontroller MPC5643L
This assessment is valid until August 31, 2015.
V1 R1 September, 2012


CERTIFICATE
No. Q4B 003346 0002 Rev. 01
Holder of Certificate: NXP Semiconductors Germany GmbH
Factory(ies):
Certification Mark:
Scope of Certificate: Business Creation and Management (BCaM) Process
Applied Standard(s):

S32K3 Safety





Complete Safety Solution

- Documentation incl safety manual, ASIL confirmation report, MCU + SBC safety guide
- BMS application reference design with system level safety manual (MCU + SBC + BCC)
- HW, SW designed with safety process
- Safety framework and core self test SW

Comprehensive Safety Measure

- Redundant hardware
- XRDC for memory access protection
- Program flow monitor
- Data integrity (ECC on flash and RAM)
- Clock, power, temperature monitoring
- Self test and error reporting
- Latent fault detection (LBIST)

ASIL B/D Scalability

- Single/Dual Core for ASIL B, Lock Step Core for ASIL D
- Pin compatible
- HW, SW and Tool reuse

S32K3xx Safety Measures (ASIL D)

Redundant Hardware
- M7 delayed core lockstep
- Arm® INTC, L1 Controller memories
- Redundant check control unit (RCCU)

Protection against storage interference
- Arm MPU: controls master access rights
- XRDC memory protection
- XRDC peripheral protection
- AIPS peripheral protect, trusted master-slave connection
- Register protection mechanism
- Triple voting flip flops on critical registers

Program flow monitor
- Internal SW Watchdog
- External SW Watchdog
- Windowed watchdog with independent clock source

Data integrity
- SRAM: ECC (data error correction and detection, address detection)
- SRAM: Column multiplexing to mitigate multi bit errors
- Cache memories: ECC and column multiplexing
- TCMs memories: ECC and column multiplexing
- NVM: ECC (data error correction)
- NVM: address encode (parallel address path check)
- NVM: EDC after ECC
- SRAMs: MBIST (RAMs)
- NVM: Array Integrity
- Data path
  - EDC gaskets (data and address buses)
  - XBIC monitor for AHB control signals attached to XBARs)
  - HW CRC

Clock Monitor
- Clock Monitoring (analog and system clocks at the end of clock tree generation)
- PLL loss of lock detection

Power supply monitoring
- LVDs (redundant Full and Reduce Mode)
- HVDs (Full Mode and ADC channel)
- Monitoring of internal supplies with reset reaction

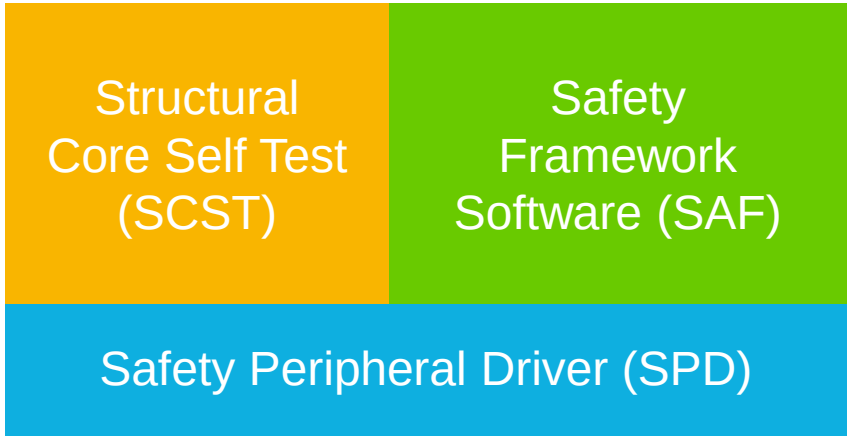
Temperature monitoring
- ETS and route the output (temperature translated to Voltage) to the ADC channel
- Application SW reads converted temperature values once within FTTI

Self Test
- Self Test Control Unit
- SW Core Self Test
- ADC Self TEST

Error reporting
- Error reporting module
- Error injection module
- Fault Collection module with programmable reaction type (alarm, interrupt, functional reset)

Latent fault detection
- MBIST for all volatile memories
- LBIST: CMU, XRDC, FLASHC, PRAMCs, XBARS& XBICs, Platform and EDC gaskets, CMUs, XBICs, EDS gaskets, CRC, SWTs, EIM, ERM

S32K3 safety software overview



- ✓ Common solution across S32 processors
- ✓ Developed according to an ISO26262 compliant process
- ✓ Supporting all safety integrity levels (up to ASIL D)
- ✓ Fast time to market

Safety Peripheral Driver (SPD):

- Incl. two drivers for safety peripherals - BIST Manager (Bist), Extended Microcontroller Error Manager (eMcem)
- Same architecture as Real Time Drivers
- Applicable for both AUTOSAR and non-AUTOSAR environment

Structural Core Self Test (SCST):

- For runtime detection of permanent HW faults in processor cores, with 90% diagnostic coverage
- SCST for Arm Cortex®-M7

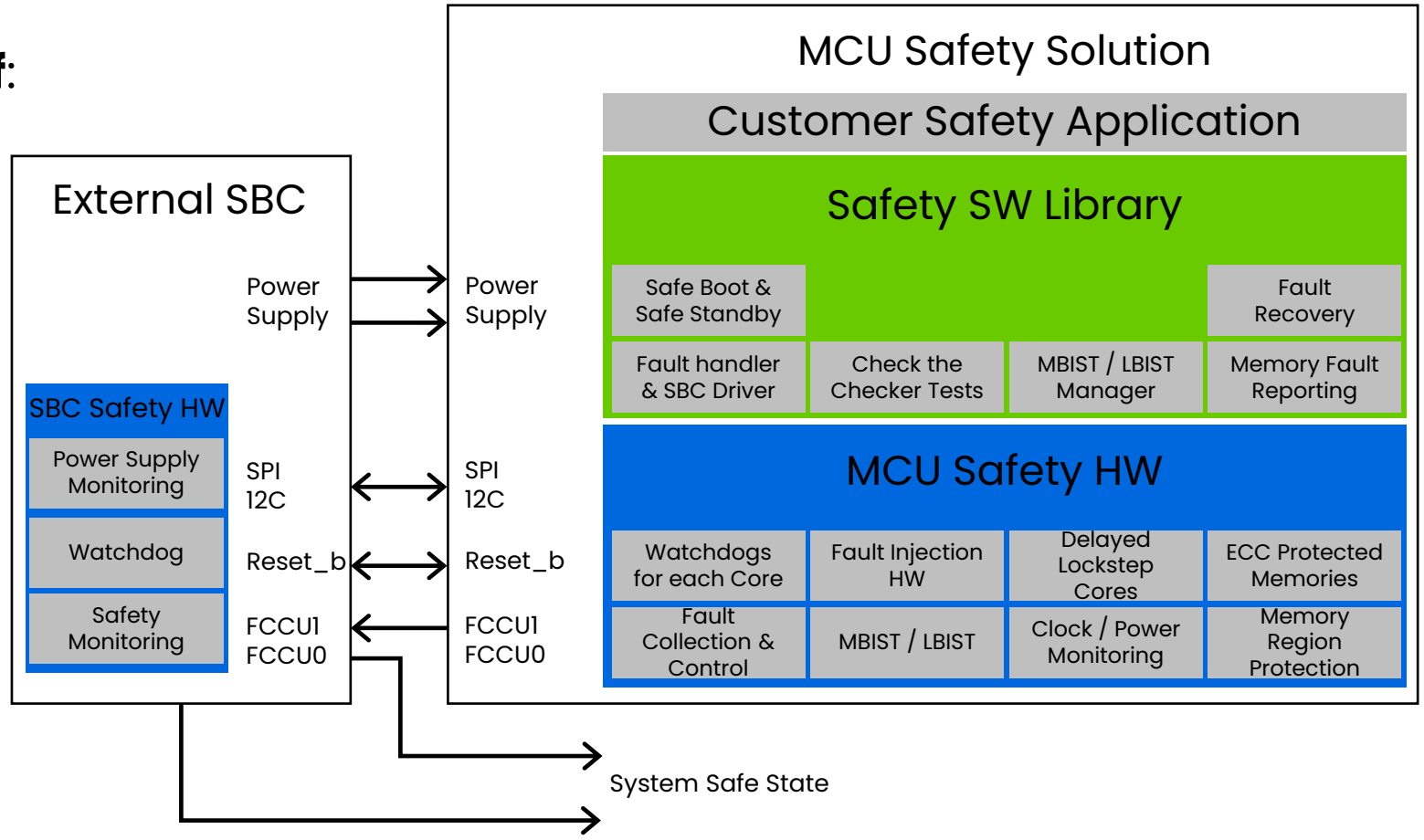
Safety Framework Software (SAF):

- Provide detection and reaction mechanism for single-point and latent HW faults w/ 6 SW components - Bist, eMcem, Mode Selector (mSel), Safe Boot (sBoot), Square Check (sCheck) and software Recovery(sReco)
- Recommended solution for many assumptions in the S32K3xx Safety Manual
- Full coverage of Software safety mechanisms within the MCU in S32K3xx Safety Manual
- Documentation available for integrating S32 SAF into applications that conform to the ISO26262 standard

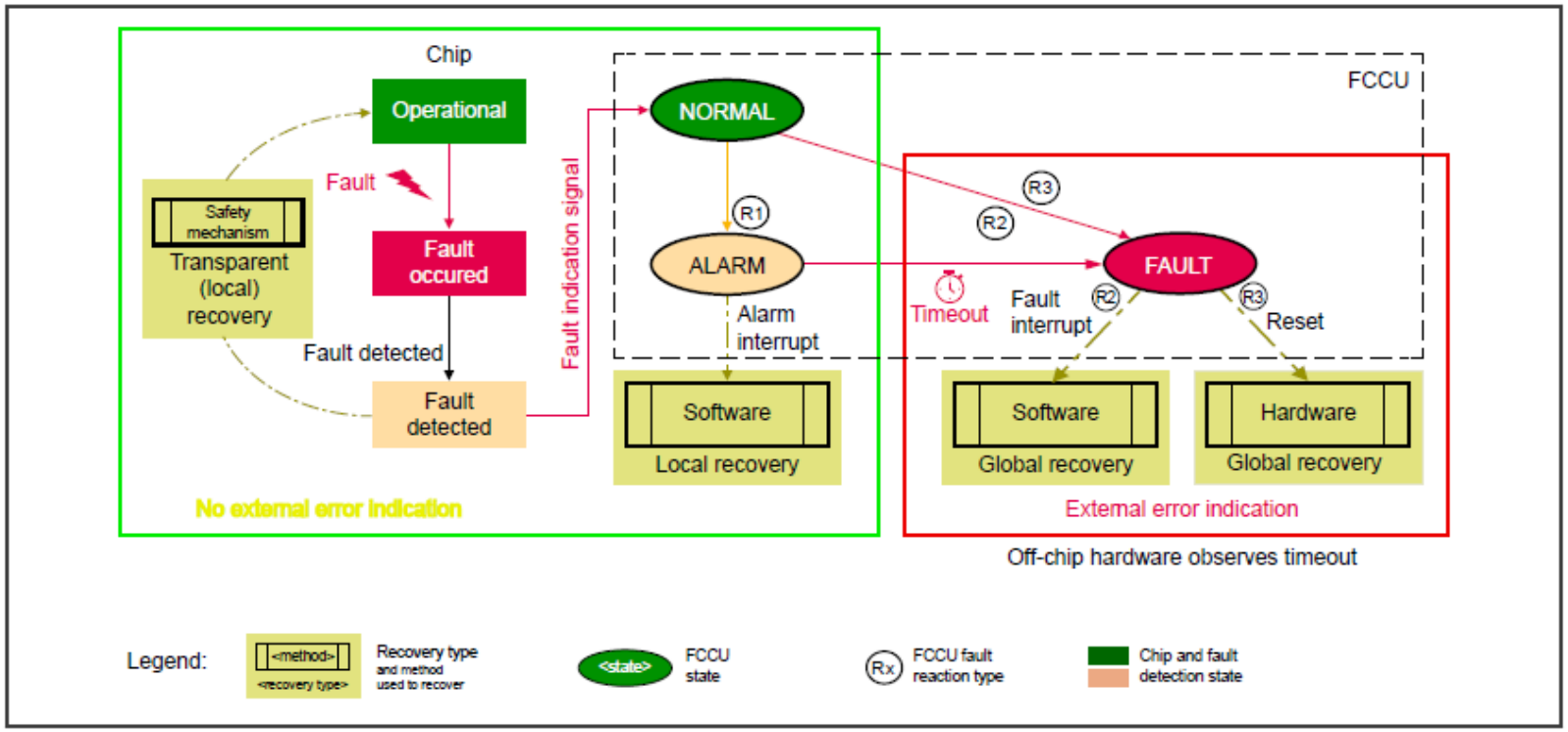
S32K3xx & FS26xx: Safety System Solution Overview

- **MCU System Solution consist of**:
  - MCU safety HW
  - Customer safety application
  - SW safety library (Interface to customer application)

- **External SBC (FS26xx)**
  - MCU power supplies monitoring
  - MCU HW monitoring
  - MCU SW monitoring
  - Safety output(s) to set the system in a safe state



Fault HANDLING AND Recovery

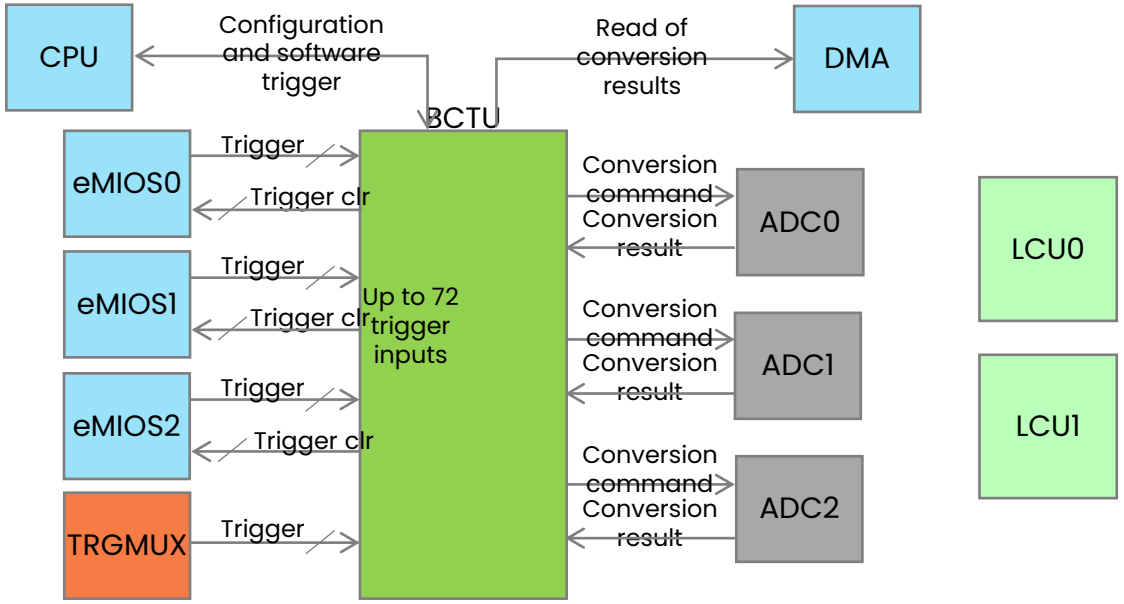


- Following recovery mechanisms are used in different scenarios:
- **Transparent recovery** : ECC single-bit error correction
- **Local (software) recovery** : ECC error in communication packet, where application retransmits the packet.
- **Global software recovery** : If another attempt for software recovery would take more time than then alarm timeout in local (software) recovery permits, then this recovery should be used. Here recovery happens after achieving chip safe state.
- **Global hardware recovery** : Faults in master safety core that cannot be recovered by software. E.g., Lockstep error indicated to the FCCU. Here recovery happens after achieving chip safe state.

Power conversion and Motor-control peripheral subsystem

S32K3 Motor Control Subsystem lowering the CPU loading: ADC, eMIOS, BCTU, TRGMUX, LCU HW + AMMC lib SW

Typical Application: Pump, Fan, Door, Window lift or Sunroof, Power lift gate, xEV inverter



- **eMIOS** timers generate PWM signals with arbitrary pulse width and frequency
- **LCU** generates complementary signals, insert dead-time and also performs fault processing (combinatorial path)
- **BCTU** serves for ADC triggering
- **TRGMUX** interconnects input and output trigger pulses of motor control peripherals and others

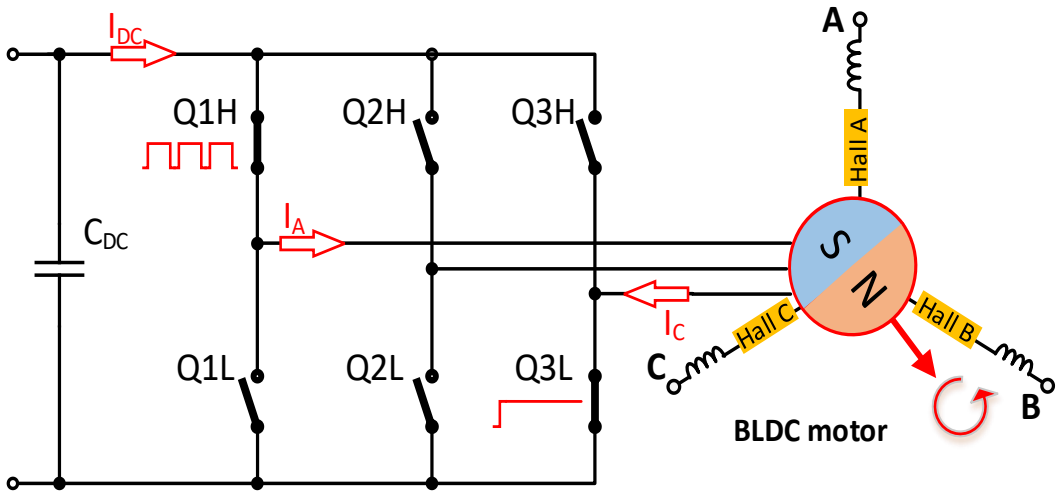
Automotive Math & Motor Control Library

- Accelerate the motor control SW development, supported by model based design tool

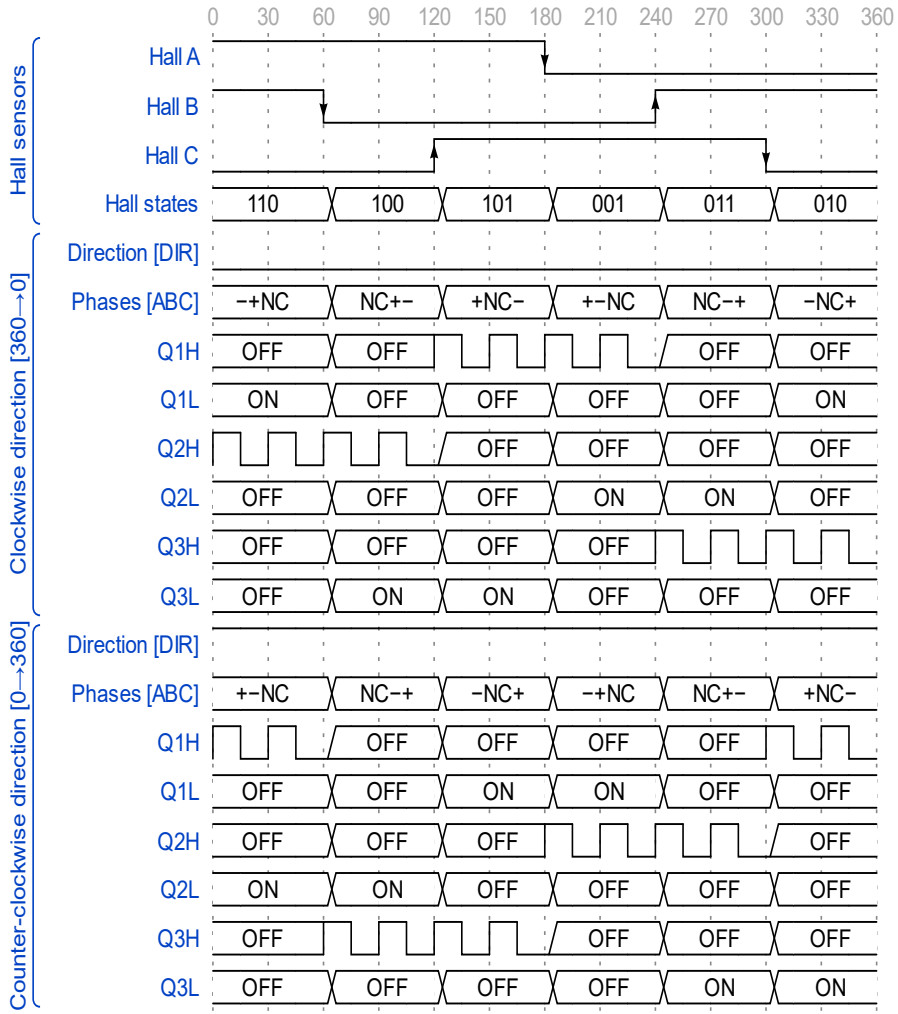
Example : implementing a BLDC Motor PWM Controller

- LCU can be configured to replace software commutator in BLDC motor control application with hall sensors position measurement.

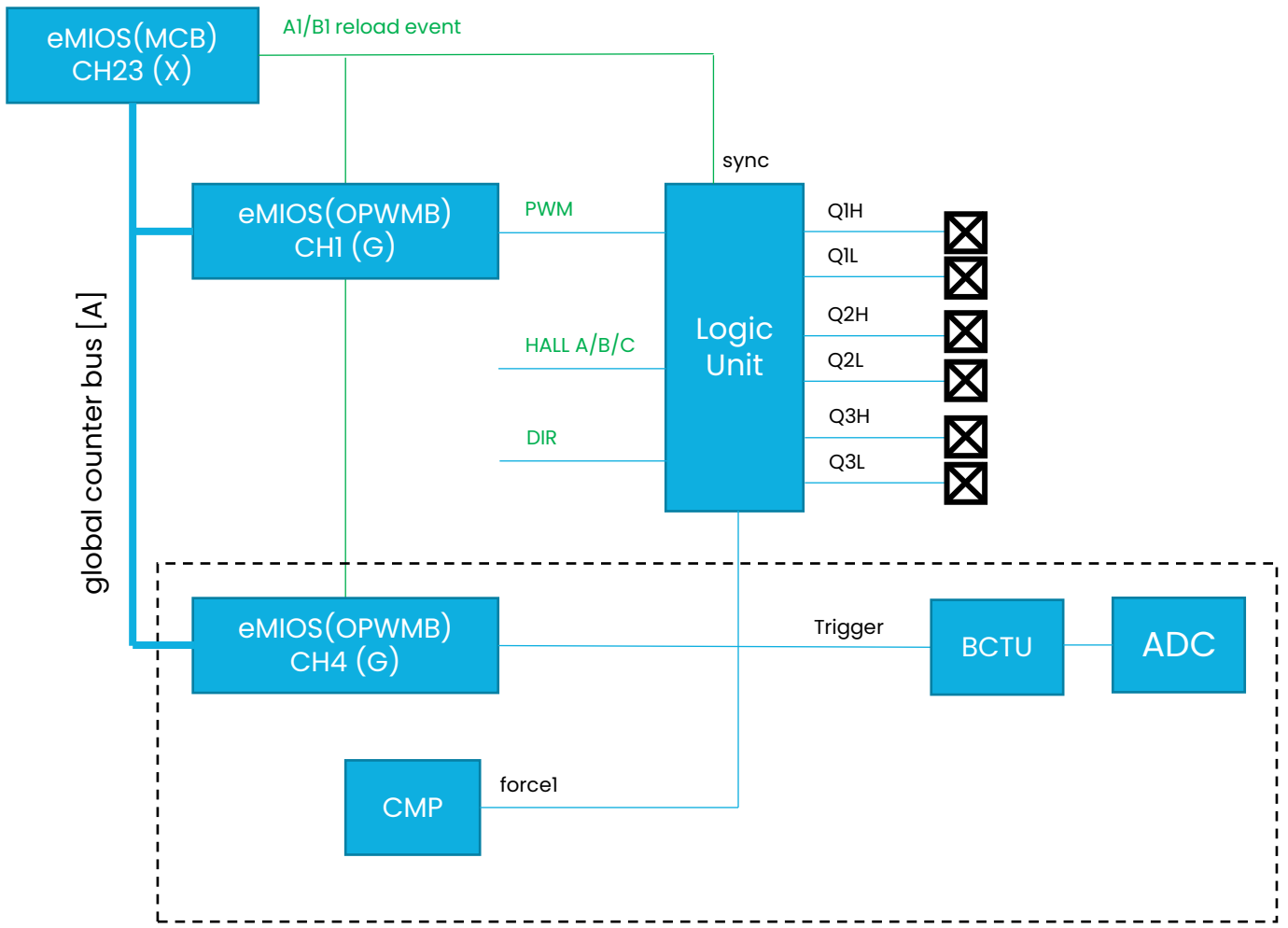
BLDC motor power stage



BLDC motor control waveforms



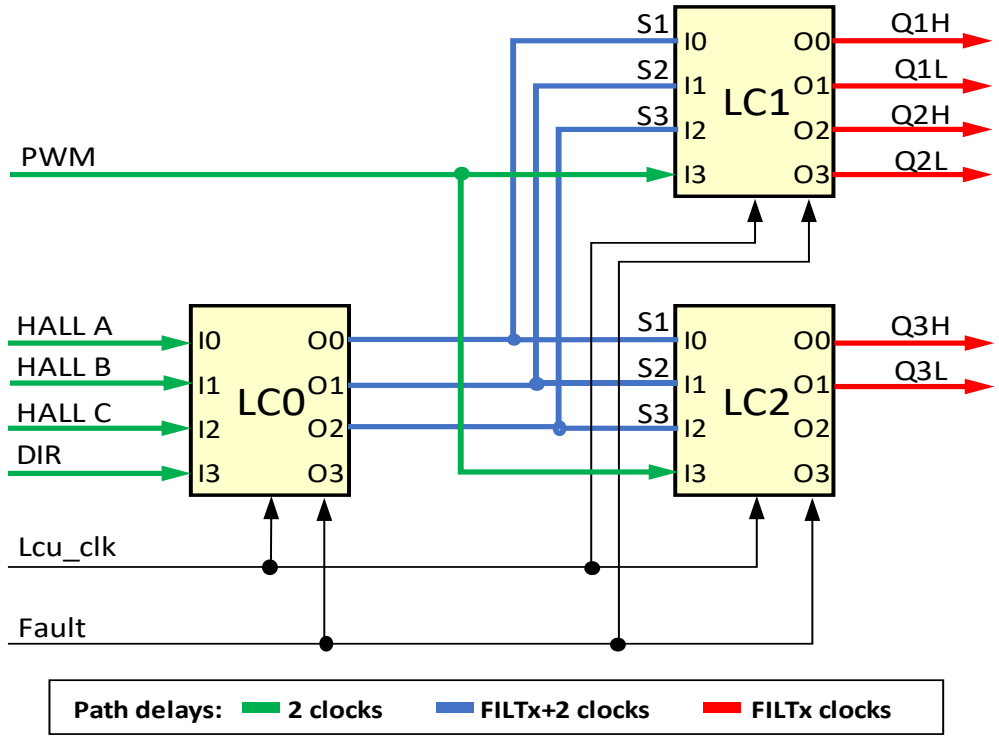
Example - Implementation



BLDC Motor PWM Controller – Cont'd

- First logic cell takes direction DIR and Hall A, Hall B and Hall C output states to generate switching states S1, S2, and S3. Second and third logic cells convert switching states to PWM or ON/OFF signals for controlling power switches.

BLDC Motor PWM Controller Implementation



BLDC Motor PWM Controller Truth Tables

LC1

PWM	S3	S2	S1	Q1_H	Q1_L	Q2_H	Q2_L	Comment
0	0	0	0	0	0	0	0	Not used
0	0	0	1	0	0	0	0	
0	0	1	0	0	1	0	0	
0	0	1	1	0	1	0	0	
0	1	0	0	0	0	0	1	
0	1	0	1	0	0	0	0	
0	1	1	0	0	0	0	1	
0	1	1	1	0	0	0	0	Not used
1	0	0	0	0	0	0	0	Not used
1	0	0	1	0	0	1	0	
1	0	1	0	0	1	0	0	
1	0	1	1	0	1	1	0	
1	1	0	0	1	0	0	1	
1	1	0	1	1	0	0	0	
1	1	1	0	0	0	0	1	
1	1	1	1	0	0	0	0	Not used

LC0

DIR	Hall C	Hall B	Hall A	S1	S2	S3	Comment
0	0	0	0	0	0	0	Not used
0	0	0	1	1	0	0	Hall states
0	0	1	0	0	1	0	Hall states
0	0	1	1	1	1	0	Hall states
0	1	0	0	0	0	1	Hall states
0	1	0	1	1	0	1	Hall states
0	1	1	0	0	1	1	Hall states
0	1	1	1	0	0	0	Not used
1	0	0	0	0	0	0	Not used
1	0	0	1	0	1	1	~Hall states
1	0	1	0	1	0	1	~Hall states
1	0	1	1	0	0	1	~Hall states
1	1	0	0	1	1	0	~Hall states
1	1	0	1	0	1	0	~Hall states
1	1	1	0	1	0	0	~Hall states
1	1	1	1	0	0	0	Not used

LC2

PWM	S3	S2	S1	Q3_H	Q3_L	Comment
0	0	0	0	0	0	Not used
0	0	0	1	0	1	
0	0	1	0	0	0	
0	0	1	1	0	0	
0	1	0	0	0	0	
0	1	0	1	0	1	
0	1	1	0	0	0	
0	1	1	1	0	0	Not used
1	0	0	0	0	0	Not used
1	0	0	1	0	1	
1	0	1	0	1	0	
1	0	1	1	0	0	
1	1	0	0	0	0	
1	1	0	1	0	1	
1	1	1	0	1	0	
1	1	1	1	0	0	Not used

Software

Real Time Drivers

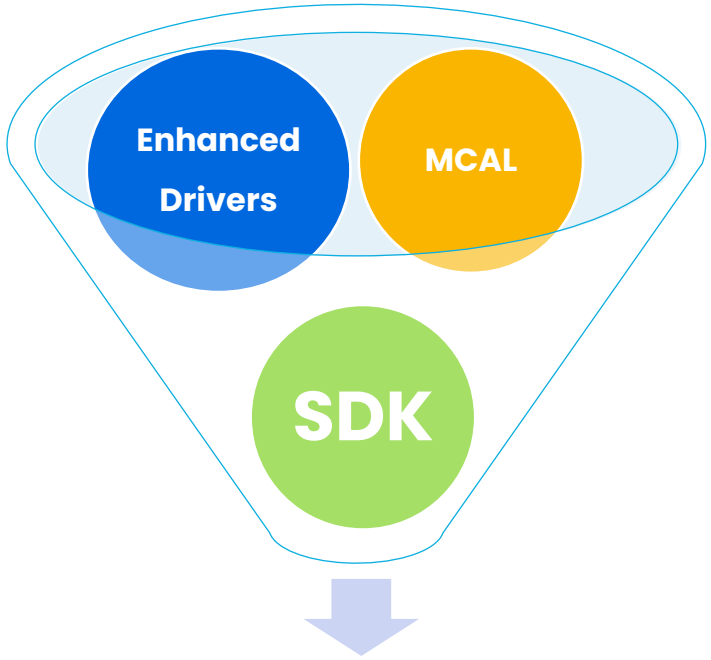
New and Innovative Drivers Set for AUTOSAR and Non-AUTOSAR Solutions

- Specifically focused on **Real Time Software**
- Targeted for MCUs based **on ARM Cortex M-cores**
- **Single package for each** S32 MCU or Processor

For **ASR** and **non-ASR** systems

Enhancements

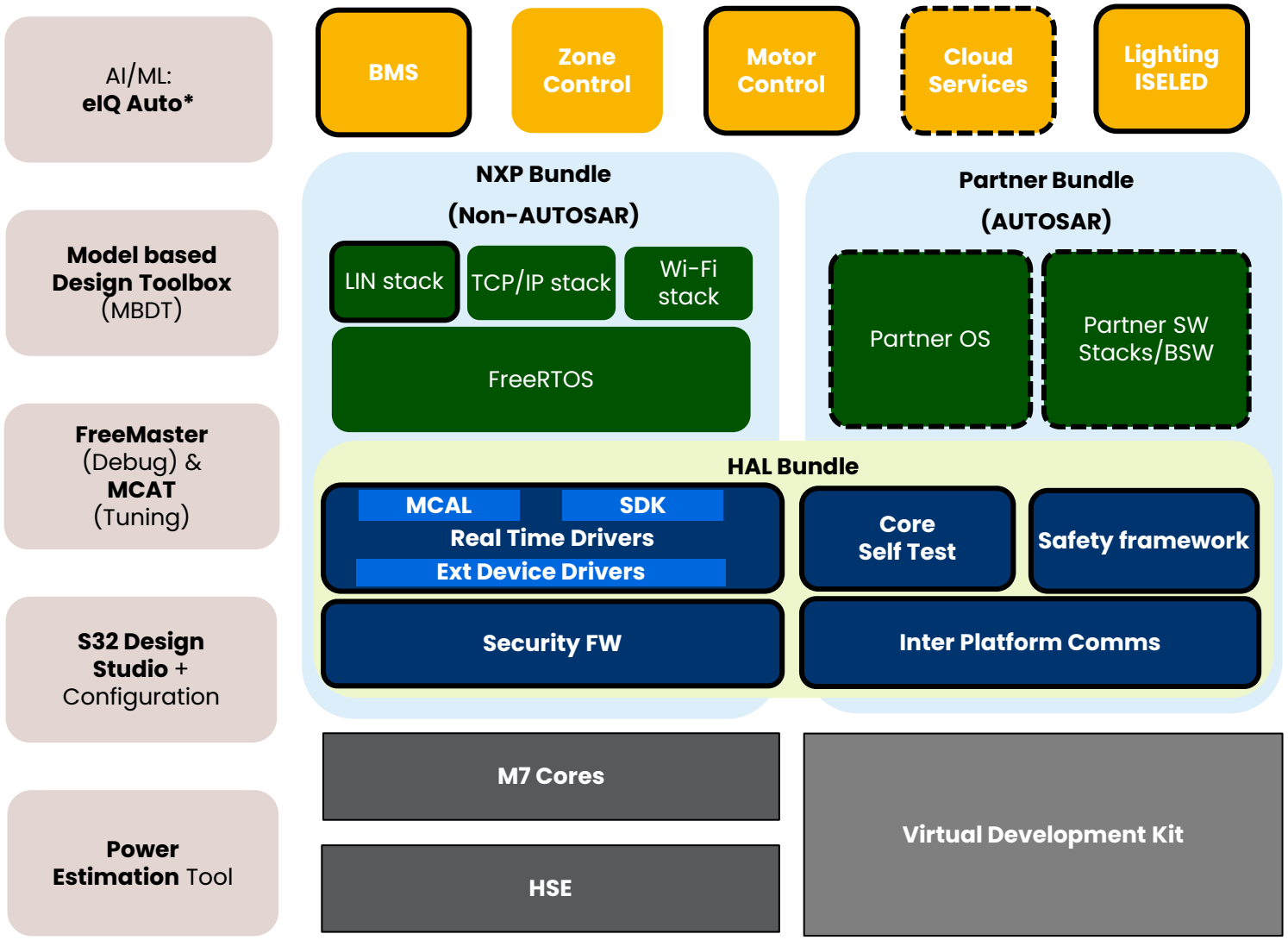
- ISO26262 Compliance for all SW layers
- AUTOSAR functionalities (e.g. multicore, user mode) are expanded also to non-ASR environment (previously only available for ASR)
- Full IP and features coverage for both ASR and non-ASR
- Possible integration on platform level of middlewares (FATFS for EEP, FEE for FLS *derived from MCAL*) and stacks (LIN, NFC, TCIP, ..)
- Driver examples with default configurations



Real Time Drivers

AUTOSAR & Non-AUTOSAR

S32K3 Software and Tools Overview



Application Solutions

- Broad offering of application enablement software
- Accelerate application focused SW development

Execution Layer

- Complete middleware for AUTOSAR and Non-AUTOSAR environment
- FreeRTOS with NXP com stacks for Non-AUTOSAR
- Partner SW from EB, Vector and ETAS for AUTOSAR

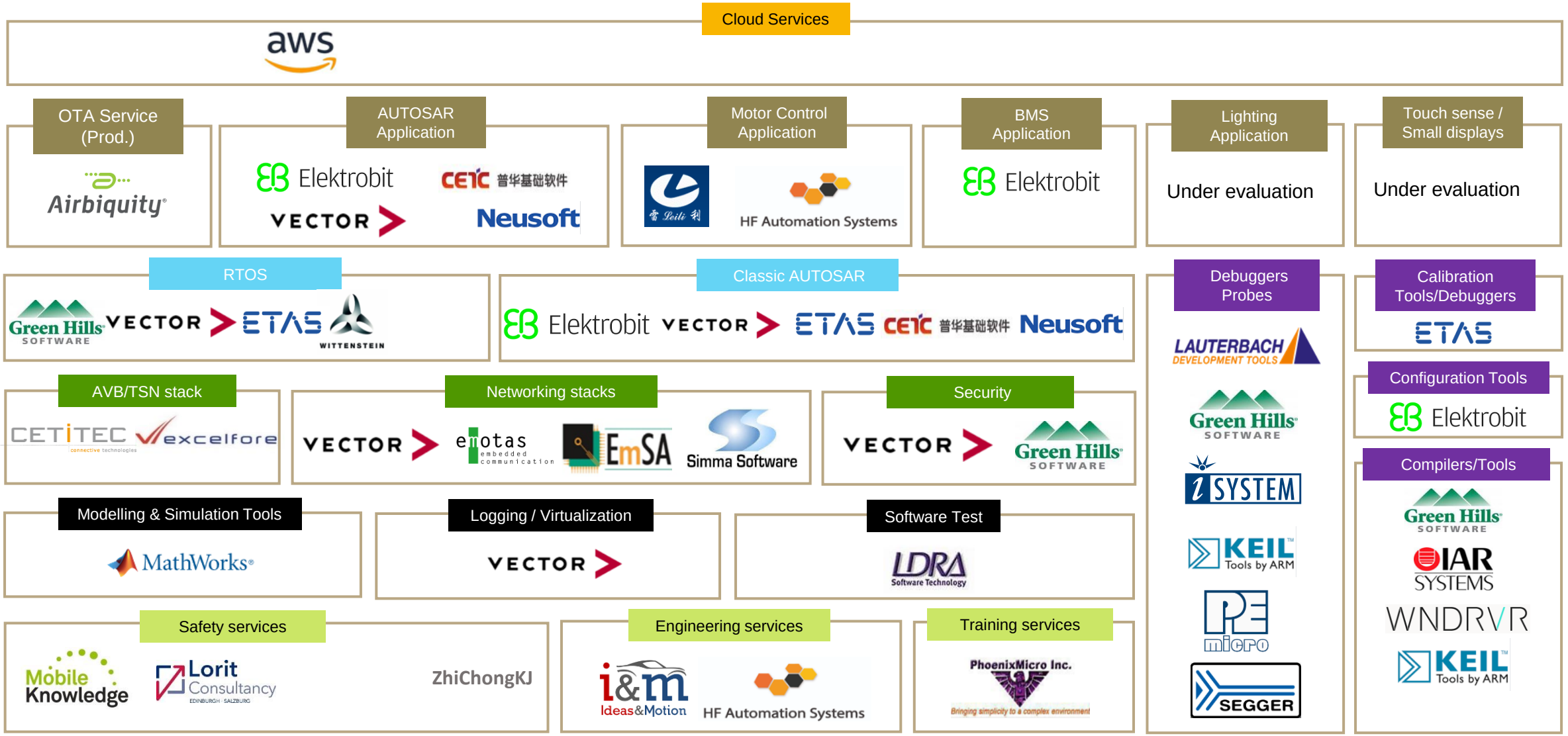
Hardware Abstraction Layer (HAL)

- Production ready software for hardware abstraction
- Drivers, Firmware, Safety, multi-core commn

Partner/3rd party

Production Grade

S32K Partner Ecosystem



Rev. September 2023

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Technical Session Survey

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