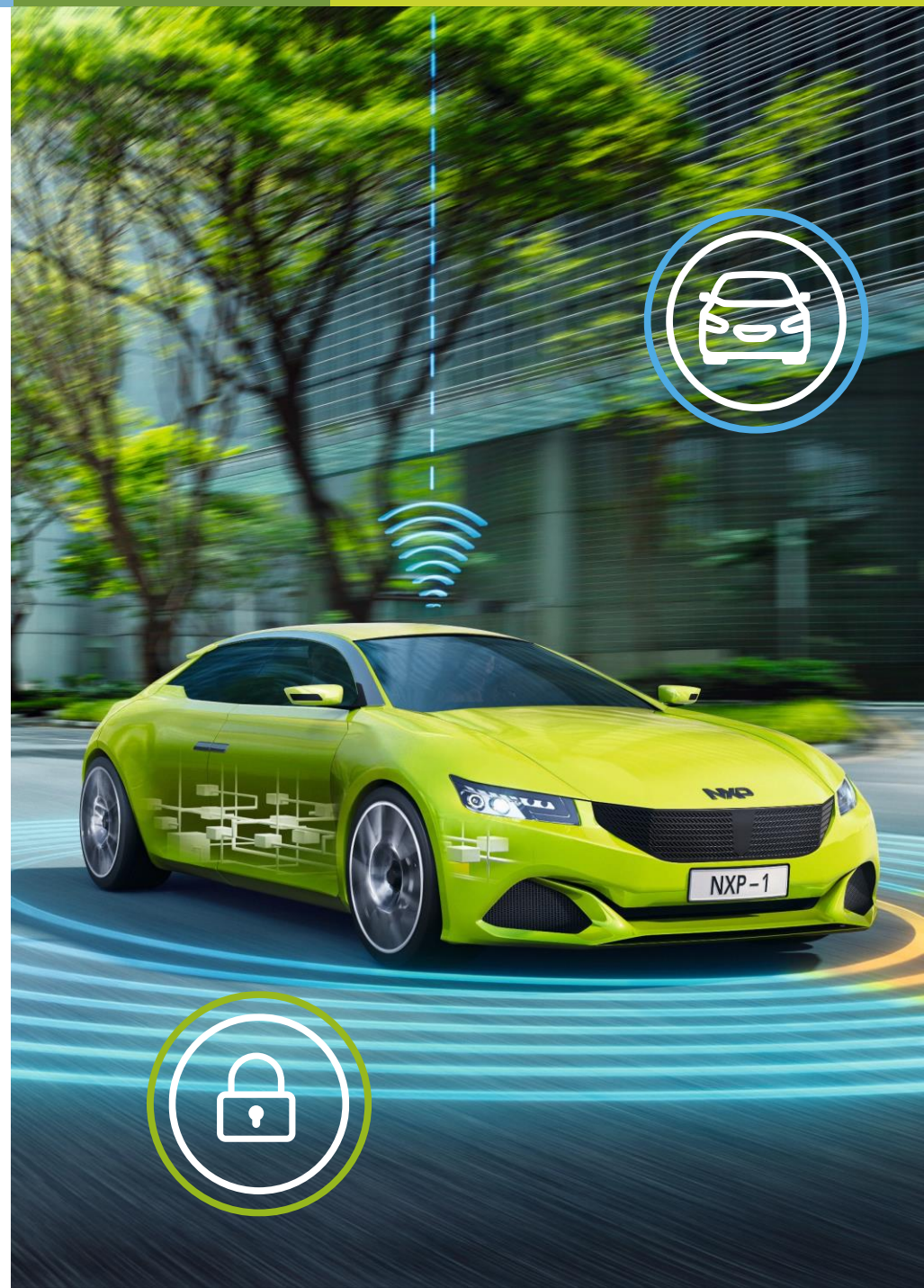
EXPLORING THE ROLE OF LIN NETWORKS IN ZONAL ARCHITECTURES

Tony Adamson

NOVEMBER 2023

SECURE CONNECTIONS FOR A SMARTER WORLD

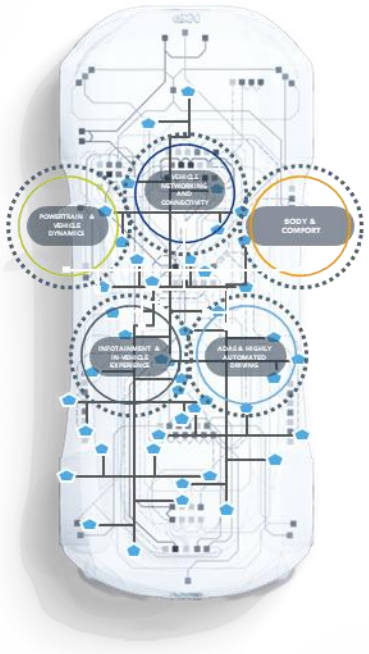


AGENDA

- Vehicle Architecture Evolution
- Role of LIN in the Future SDV
- NXP’s LIN Portfolio
- Focus: TJA1124
- Focus: SJA1124

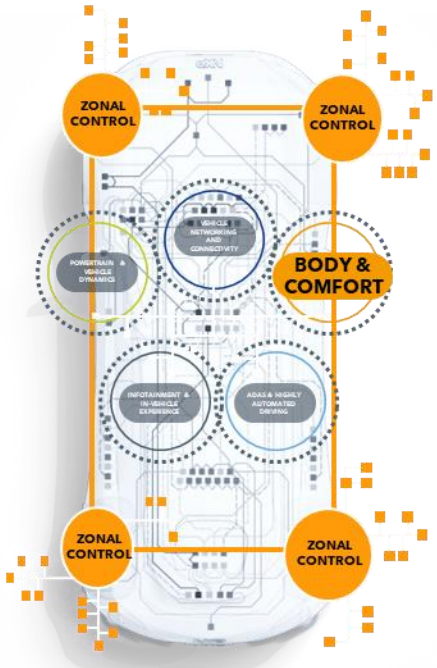
VEHICLE ARCHITECTURE EVOLVING ACROSS DOMAIN AND ZONE AXIS

DOMAIN ARCHITECTURES IN RAMP



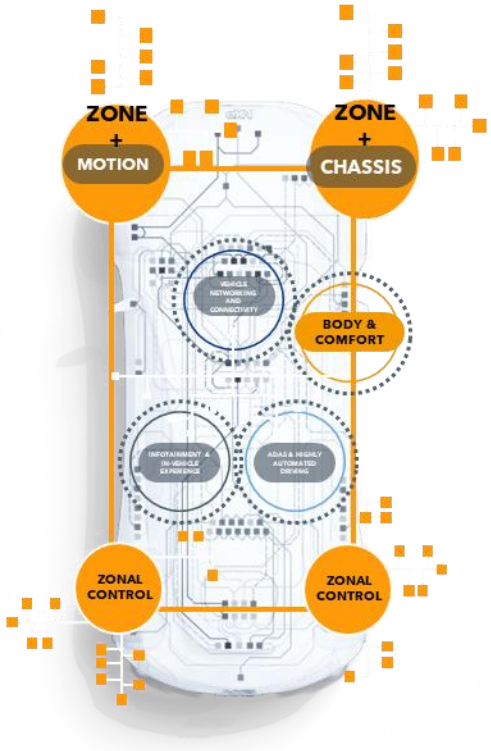
SCALABLE AND CENTRALIZED SOFTWARE DEVELOPMENT

DOMAIN PLUS ZONALIZATION: BODY ZONES



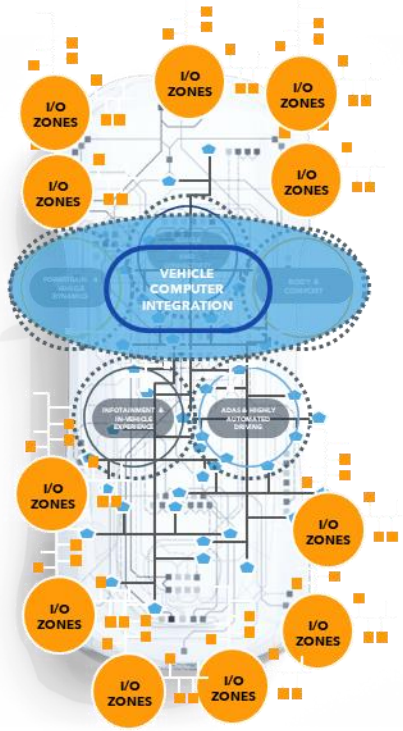
DOMAIN SW BENEFIT + SIMPLIFIED WIRING AND VEHICLE NETWORK

DOMAIN PLUS ZONALIZATION: X-DOMAIN ZONES



LOWER HW COST VS MORE COMPLEX SW

SDV - INTEGRATED VEHICLE COMPUTER + SIMPLE ZONES

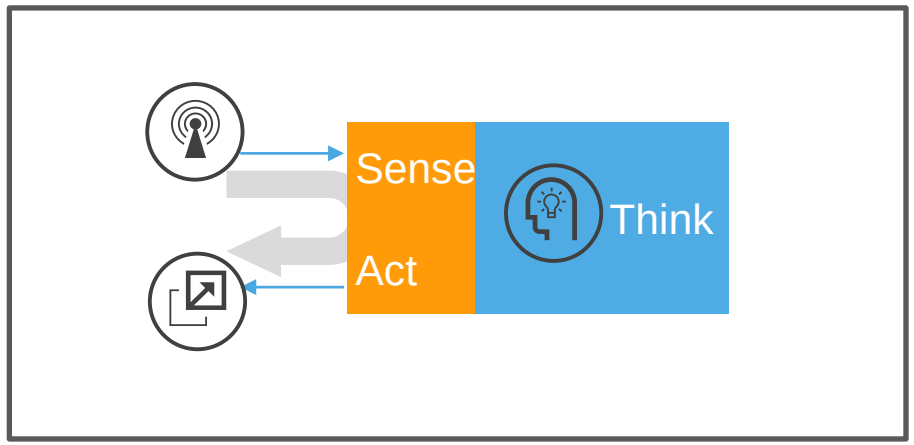


SIGNIFICANTLY REDUCES SW DEVELOPMENT COST VS. HIGHER HW COST FOR FUTURE-PROOFING

RE-DISTRIBUTING FUNCTIONS → CONNECTIVITY AND DISTRIBUTION BECOME CRUCIAL

THE HARDWARE-DEFINED VEHICLE

= One box, one function

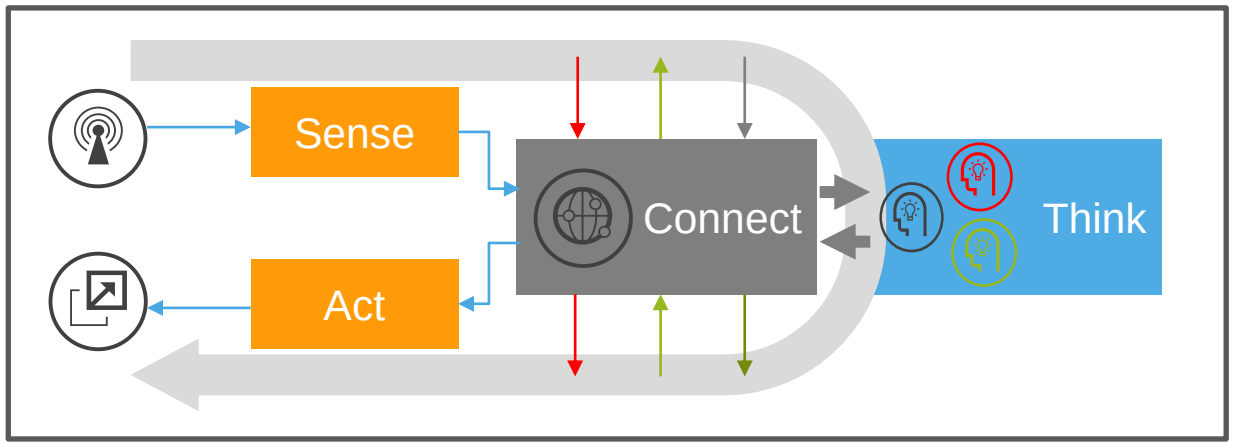


- Real time (RT) control loop is localized
- Sensors, actuators and processing tightly coupled for dedicated function
- High variability of implementations
- Optimized native networks

The Edge manages **Real Time Compute**

THE SOFTWARE-DEFINED VEHICLE

= Distributed functions

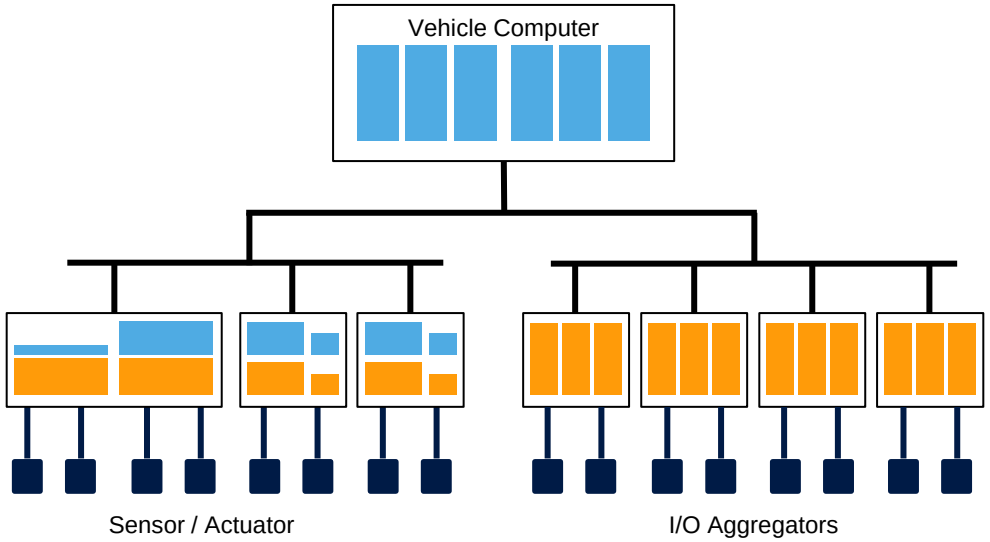


- Control loop extends across the car – and includes connectivity
- Sensors / actuators become application agnostic
- Multiple consumers of common sensor data
- Standardize on Ethernet/IP to minimize GW cost / protocol conversion
- Reduces cost and latency impact of gatewaying data

The Edge manages **IO Aggregation**

FUTURE SDV EDGE NETWORKS BE A COMBINATION OF RT COMPUTE AND IO AGGREGATION

Future SDV



High RT Compute Functions

Closely linked to specific, dedicated hardware

Tight control parameters (e.g. latency, jitter, …)

Limited value to migrate to SDV

SDV IO Aggregation

Generic sensor / actuator, available to multiple services

Avoid protocol conversion by bringing IP to the Edge

Leverages SW service infrastructure benefits to Edge

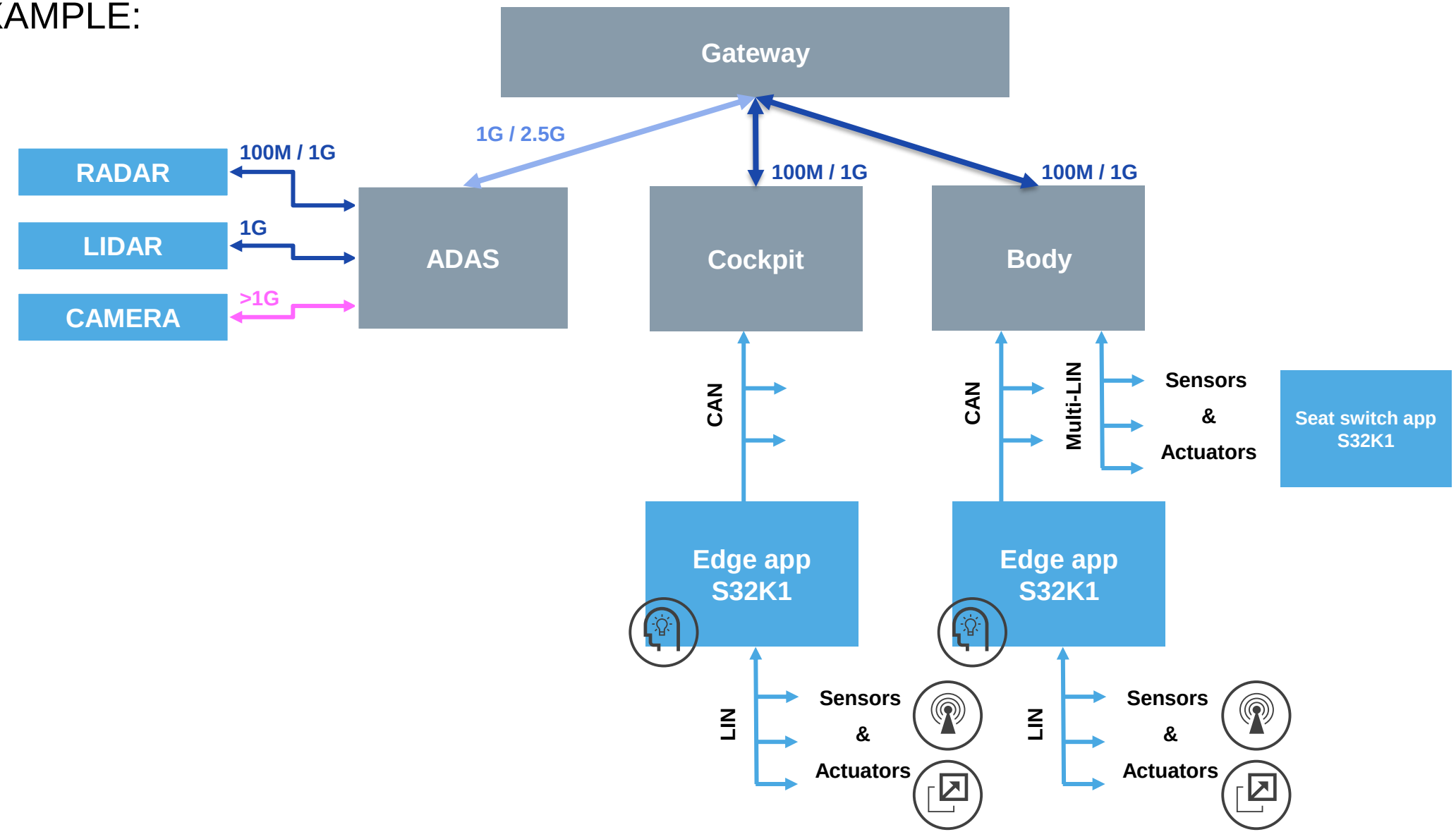
Range of solutions (pre-processed to MCU-less)

Examples: Powertrain, Chassis

Examples: Lighting, Body

LIN IN DOMAIN-BASED ARCHITECTURES

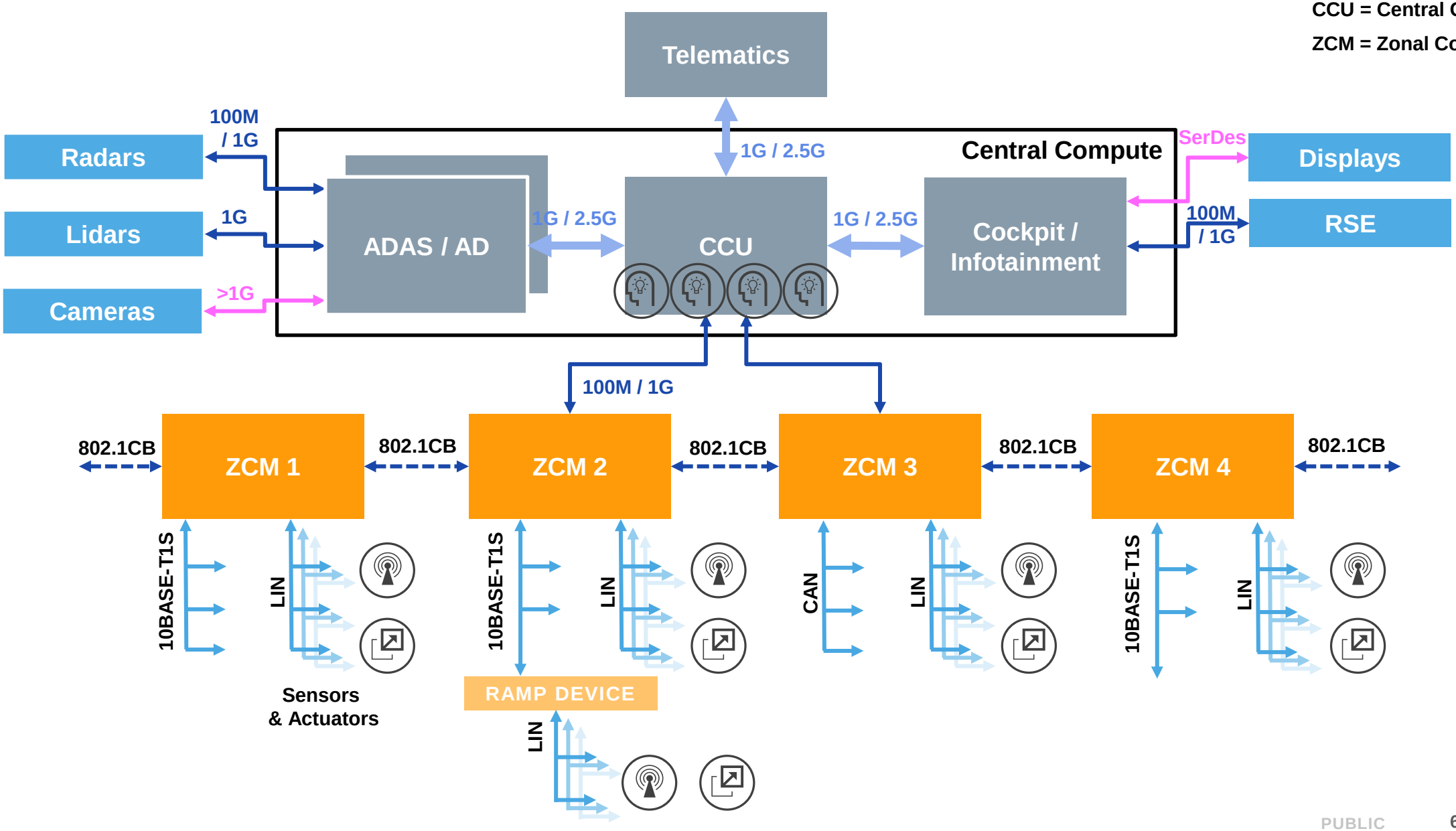
EXAMPLE:



GENERALIZED HYBRID ZONAL E/E ARCHITECTURE

CCU = Central Compute Unit

ZCM = Zonal Control Module



WHAT ARE THE REQUESTS FOR LIN ON CENTRAL MODULES

HIGHER PLURALITY OF LIN CHANNELS

Multi-LIN transceivers for central // zonal modules

BOM AND SIZE REDUCTION

Integrated commander termination resistors to reduce board space and component count

SCALABILITY

SPI link to external, scalable LIN controllers

MCU PIN OUT REDUCTION

LIN PORTFOLIO OVERVIEW

Application Specific Transceivers

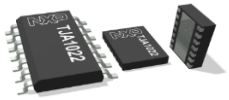
MC33660
ISO K-line Transceiver

+ LIN Controller
+ INH
+ 8 I/O Ports
+ Note Addressing

UJA1023
LIN I/O Responder

Multi-Channel LIN Transceivers

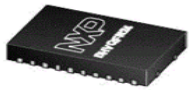
TJA1022
Dual LIN Transceiver



+ 2nd LIN Channel

+ 3rd & 4th LIN Channel

TJA1024
Quad LIN Transceiver



+ INH
+ Commander Termination

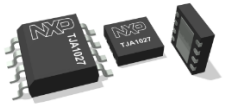
SJA:
+ LIN Control
+ LIN-SPI

TJA1124(A/B/C)
Quad LIN Transceiver

SJA1124(A/B/C)
Quad LIN Transceiver

Single Channel LIN Transceivers

TJA1027
Basic LIN Transceiver

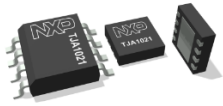


+ TxD Dominant Timeout

TJA1029
Core LIN Transceiver

+ INH
+ WAKE

TJA1021*
Standard LIN Transceiver



+ High-Speed LIN

MC33662
Advanced LIN Transceiver

LIN Mini-SBCs Transceivers

+ 70 mA Voltage Regulator

TJA1028*
Mini LIN SBC

+ LIN Switch
+ LED Driver

+ Watchdog
+ 1-2 Wake Up
+ Limp
+ LED Driver
+ Cyclic Wake Up
+ EoL Configure
+ 85 mA LDO

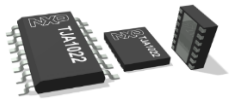
UJA1018
Led Lighting LIN SBC

TJA1128
Mini LIN SBC

**: SOI3+ capacity improvement program. Est. Release in 23FEB*

MULTI-CHANNEL LIN IS THE KEY IN FUTURE ARCHITECTURE

TJA1022
Dual LIN Transceiver



+ 3rd & 4th LIN Channel

TJA1024
Quad LIN Transceiver

+ INH
+ Commander Termination

TJA1124(A/B/C)
Quad LIN Transceiver

+ LIN Control
+ LIN-SPI

SJA1124(A/B/C)
Quad LIN Transceiver

Function	TJA1022	TJA1024	TJA1124	SJA1124
# LIN channels	2	4	4	4
Wake-up Source Recognition	Yes	Yes	Yes	Yes
TxD Dom. TO	Yes	Yes	Yes	Yes
INH	-	-	Yes	Yes
High-Speed LIN	-	-	-	Yes
SPI-to-LIN bridge	-	-	-	Yes
LIN controller	-	-	-	Yes
MCU Voltage	3V3 & 5 V	3V3 & 5 V	3V3 & 5 V	3V3 & 5 V
Int. commander Termination	-	-	Yes	Yes
Package Options	SO14, HVSON14, DHVQFN24	DHVQFN24	DHVQFN24	DHVQFN24

Variant	Commander Pull-up Resistor
SJA1124A	900Ω - 1100Ω (±10%) or OFF
SJA1124B	900Ω - 1010Ω (±5.5%)
TJA1124A	900Ω - 1100Ω (±10%)
TJA1124B	900Ω - 1100Ω (±10%) OFF in low power mode
TJA1124C	900Ω - 1010Ω (±5.5%)

TJA1124: QUAD LIN WITH INTEGRATED COMMANDER TERMINATION

Key Features

4 x LIN transceivers

- Fully LIN 2.x / ISO17987 / SAE J2602 compliant

4 x **Integrated LIN commander termination**

- Multiple variants targeting different OEM requirements (see below)

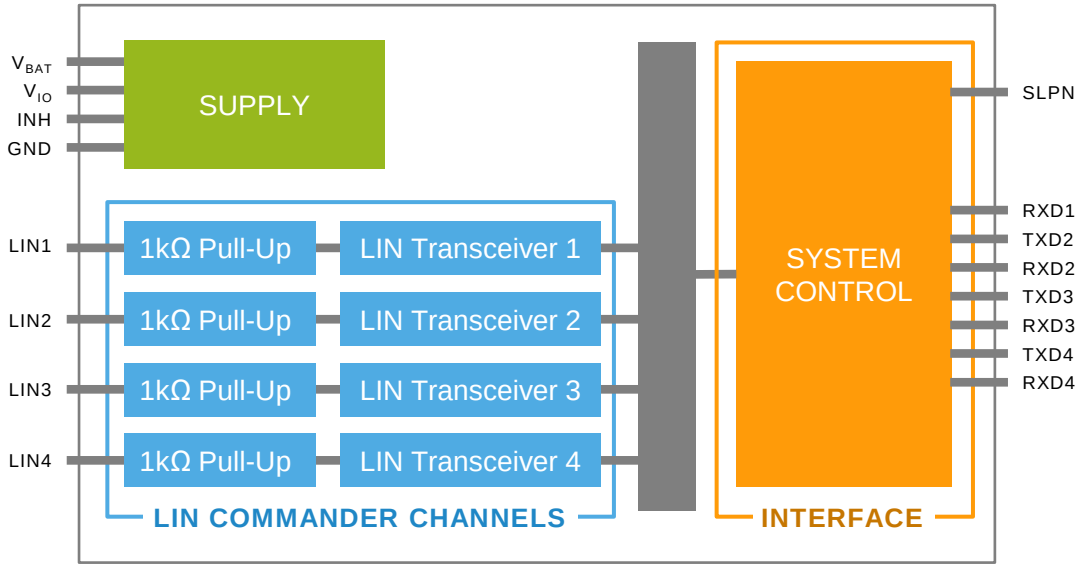
INH_N function to control LDO or wake up MCU

VIO input for **direct interfacing** with 3.3 V and 5 V MCUs

Low current consumption: Sleep mode current: typ. 8 µA

Bus terminals short-circuit proof to battery and ground

Small Package DHVQFN24 5.5 mm x 3.5 mm x 0.85 mm



Variant	Commander Pull-up Resistor
TJA1124A	900Ω - 1100Ω (±10%)
TJA1124B	900Ω - 1100Ω (±10%) OFF in low power mode
TJA1124C	900Ω - 1010Ω (±5.5%)

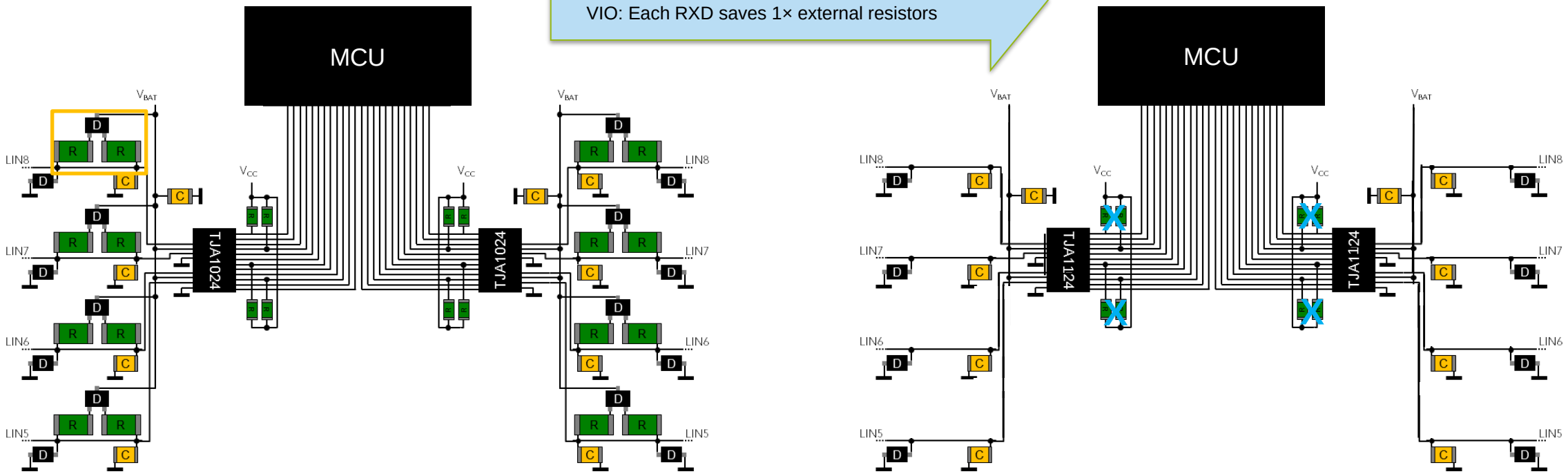
TJA1124: SCALE BIG WITH SMALL FOOTPRINT
EXAMPLE: 8-CHANNEL LIN APPLICATION

2 x TJA1024
DHVQFN24

PCB area and BOM reduction
Saves 2× resistors + 1x diode
per LIN channel

2 x TJA1124
DHVQFN24

PCB area and BOM reduction
VIO: Each RXD saves 1× external resistors



INH_N enables SBC wake-up or voltage regulator activation

SJA1124: QUAD LIN WITH INT. LIN CONTROLLER, COMMANDER TERMINATION AND SPI

Key Features

4 x LIN transceivers with commander controllers

- Fully LIN 2.x / ISO17987 / SAE J2602 compliant

4 x **Integrated LIN commander termination**

- Multiple variants targeting different OEM requirements (see below)

SPI for data transfer, configuration and diagnosis

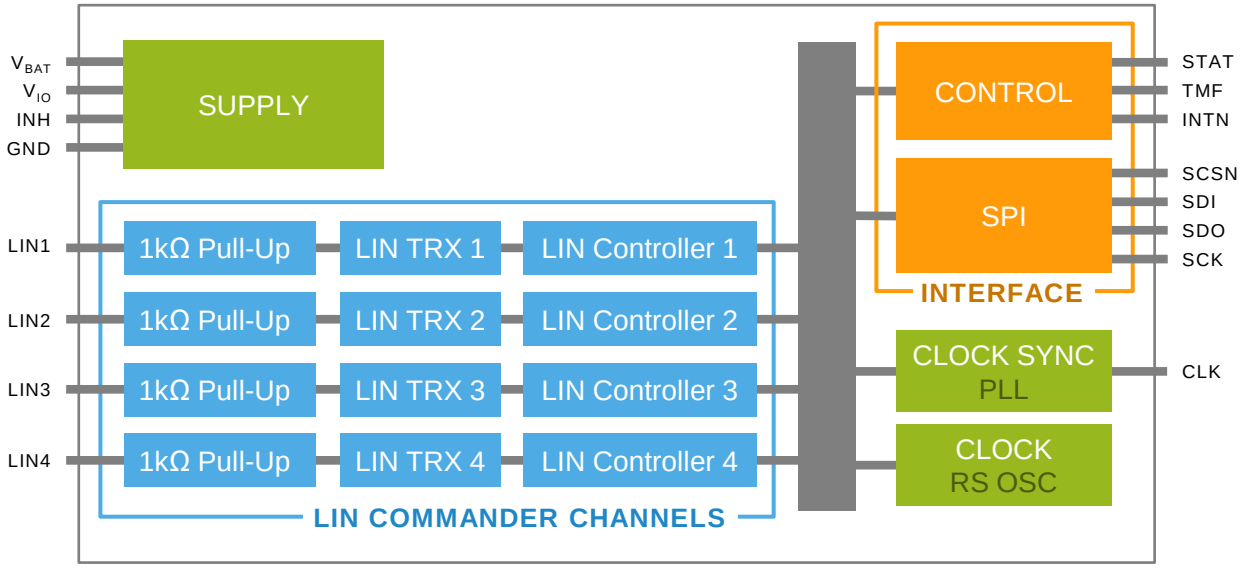
INH_N function to control LDO or wake up MCU

VIO input for **direct interfacing** with 3.3 V and 5 V MCUs

Low current consumption: Sleep mode current: typ. 12 µA

Bus terminals short-circuit proof to battery and ground

Small Package DHVQFN24 5.5 mm x 3.5 mm x 0.85 mm



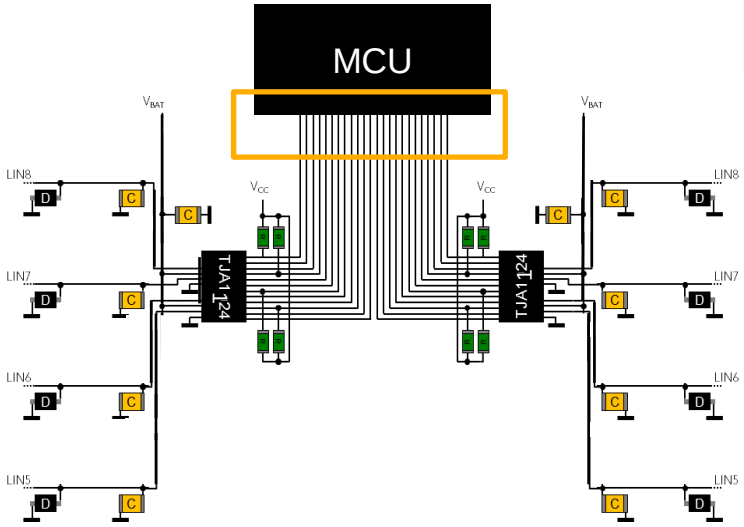
Variant	Commander Pull-up Resistor
SJA1124A	900Ω - 1100Ω (±10%) or OFF
SJA1124B	900Ω - 1010Ω (±5.5%)

SJA1124: SCALE BIG WITH SMALLER FOOTPRINT
EXAMPLE: 8-CHANNEL LIN APPLICATION

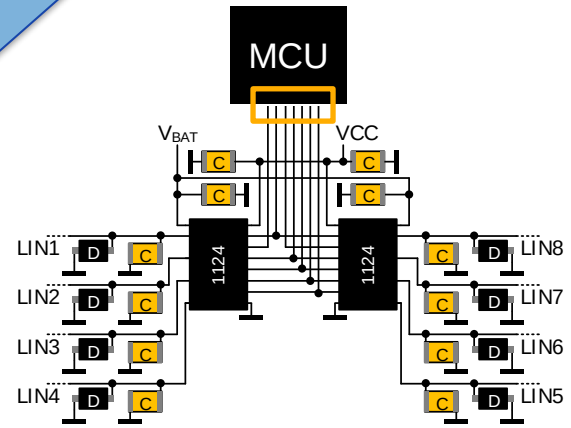
MCU pin count reduction as a benefit of SPI

MCU independent from # LIN channels as a benefit of integrated LIN controllers

2 x TJA1124
HVQFN24

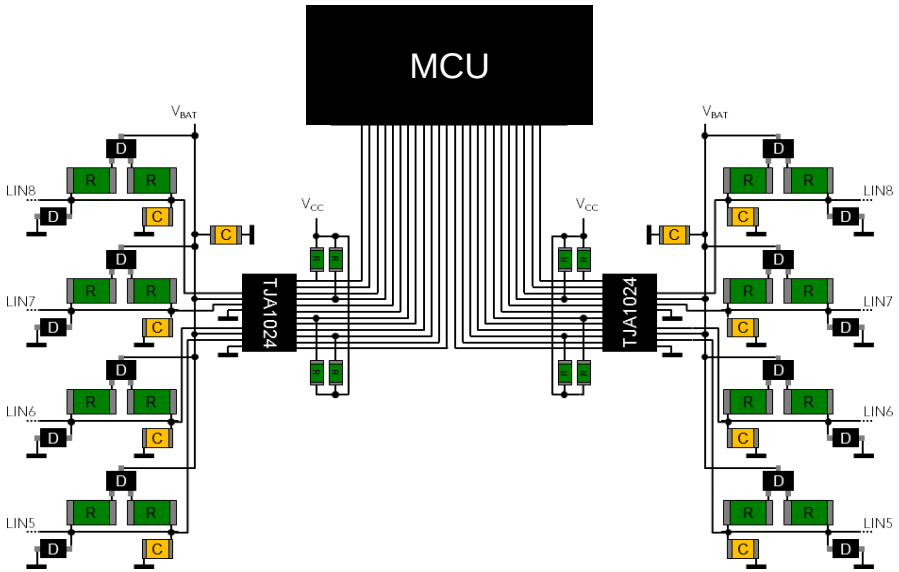


2 x SJA1124
HVQFN24

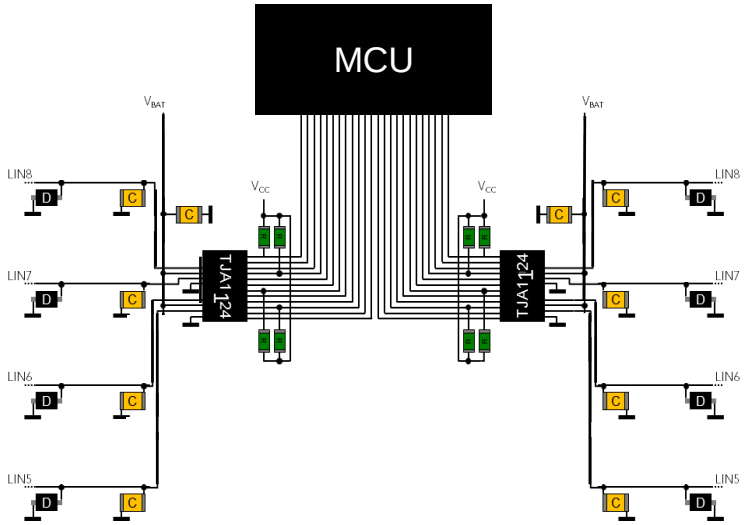


TJA1124 AND SJA1124 – REDUCE PCB AREA AND SAVE BOM TO A MINIMUM

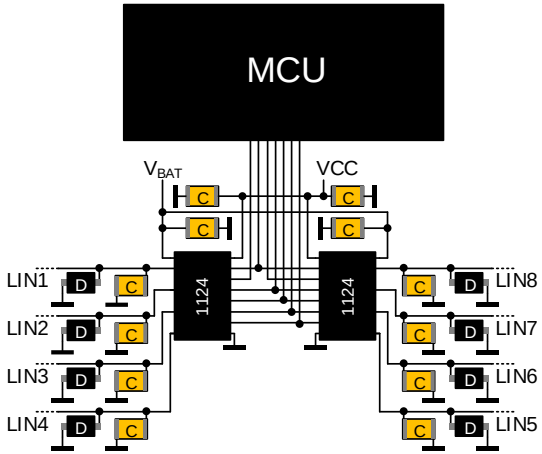
2 x TJA1024
HVQFN24



2 x TJA1124
HVQFN24



2 x SJA1124
HVQFN24



From big footprint to SMALL and SMALLER

SPI TO LIN RE-USE EXAMPLE: 2 × SJA1124 AND MCU

TMF: enables synchronous LIN frame transmission

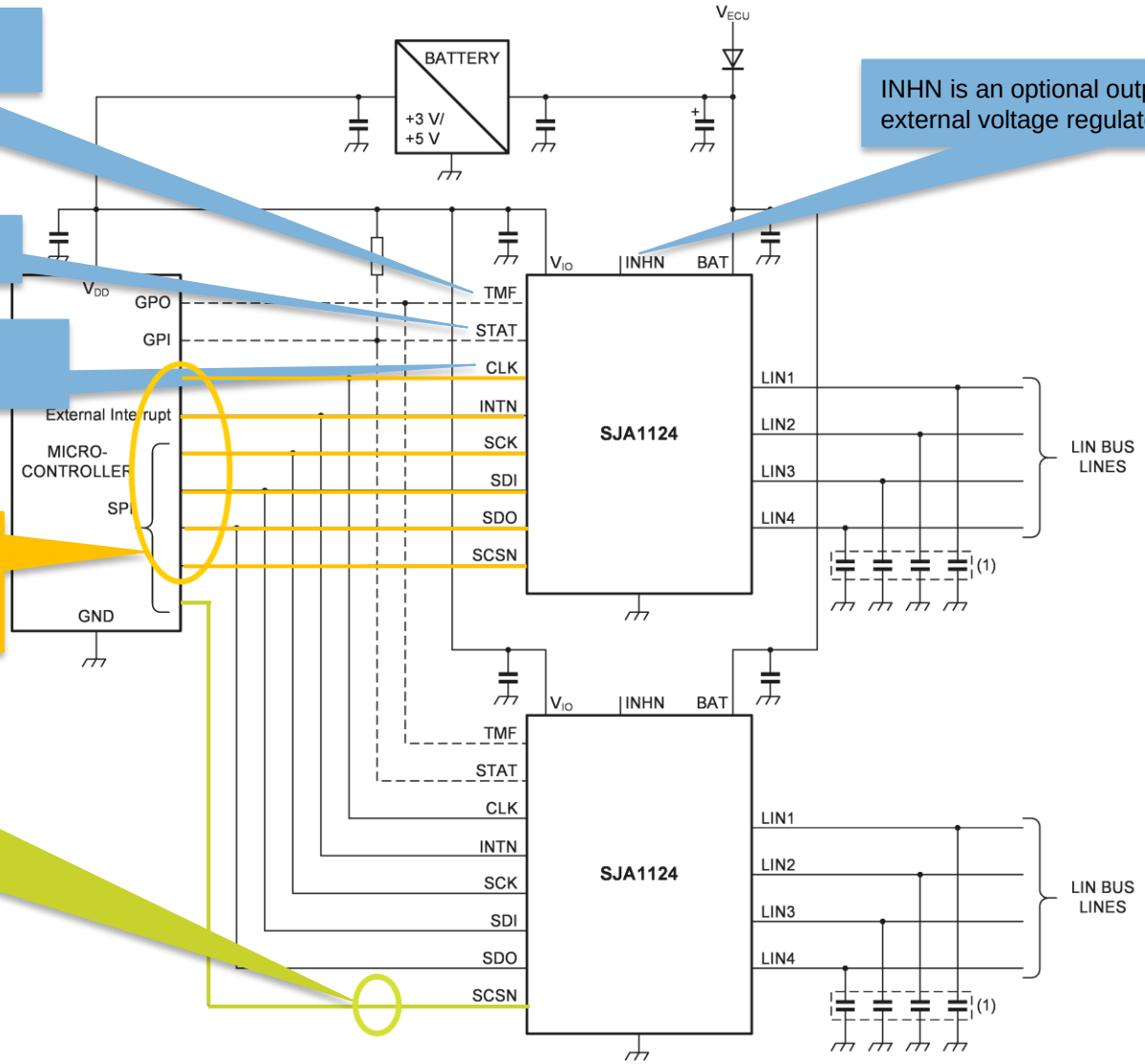
STAT: provides status of SPI interface

CLK is the clock reference input for the baud rate generator (0.4 … 10 MHz)

LIMITED PIN COUNT
Only 5 pins + CS are needed to interface with **one SJA1124**

SCALABILITY
An additional 4 LIN channels **= only 1 chip select pin** on MCU.
With classical transceivers, this would require 8 extra pins.

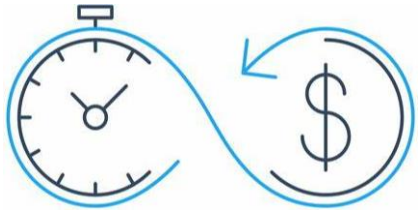
INHN is an optional output pin to enable an external voltage regulator or to wake-up an SBC



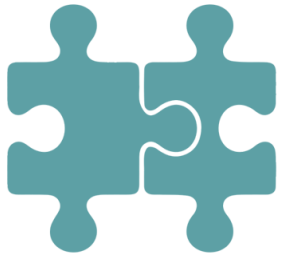
SJA1124 REAL TIME DRIVER

- SJA1124 utilizes the SPI interface to connect the MCU to the LIN controllers
- Specific AUTOSAR SW driver available for customers = **hassle-free HW + SW solution**

AUTOSAR: SW standardization



Simple integration



System solution: + NXP MCU RTD

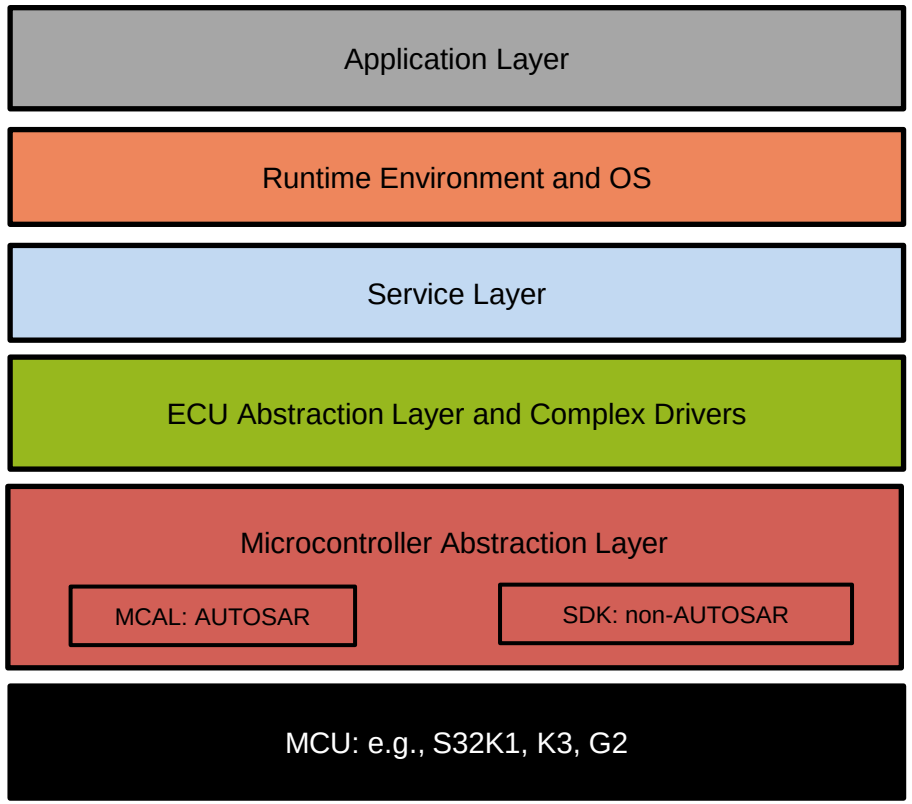
EAR (Early Access Release) with S32K1 RTD

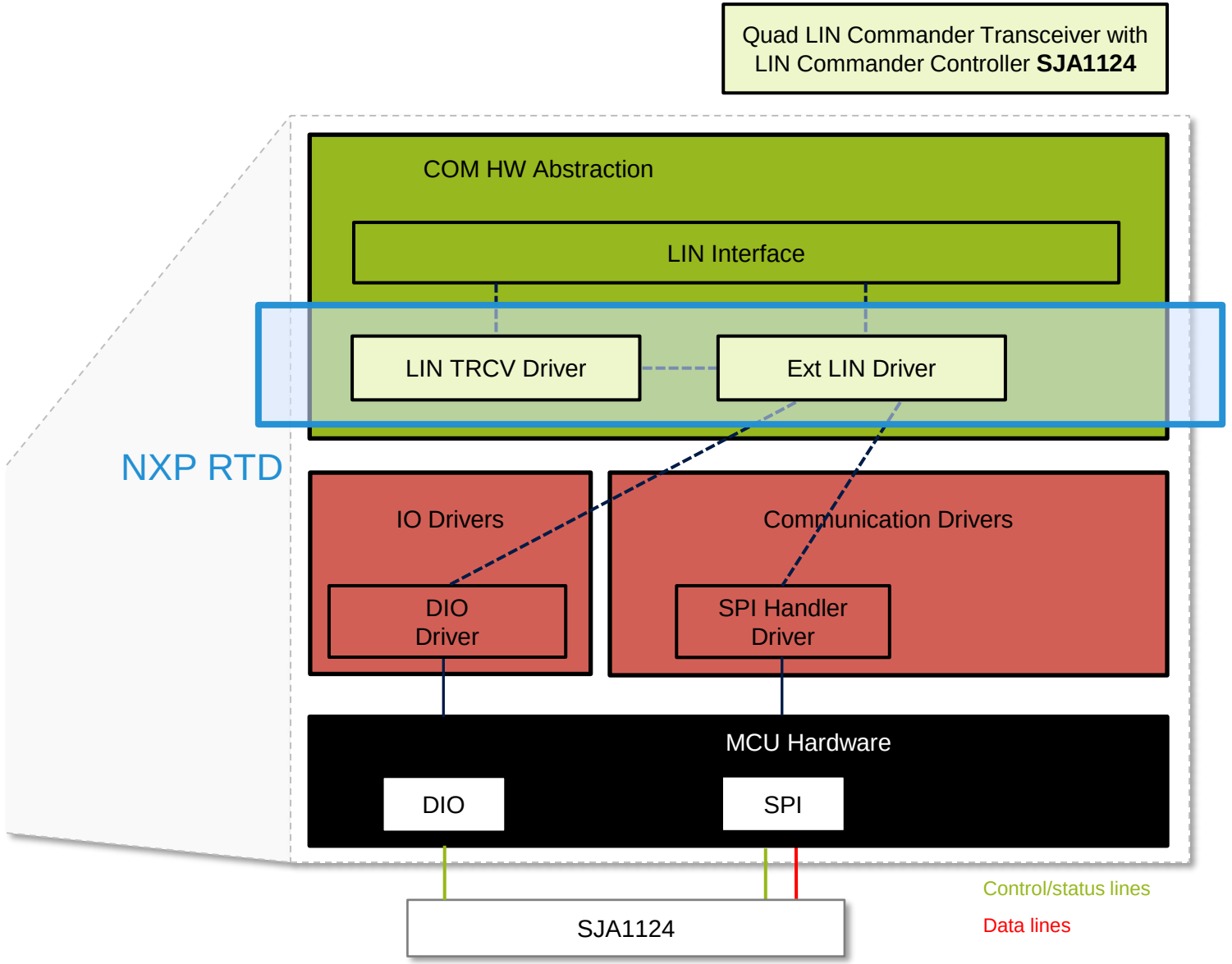
Example code with S32K3 and S32G2/3 RTD

Release to Market (Production Grade) planned 2024

SJA1124 REAL TIME DRIVER

AUTOSAR Layered Architecture





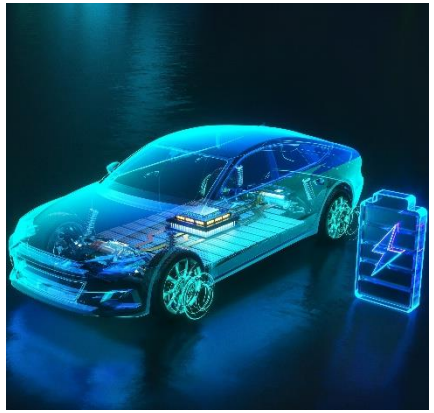
Reference: https://www.autosar.org/fileadmin/standards/R22-11/CP/AUTOSAR_EXP_LayeredSoftwareArchitecture.pdf

TYPICAL APPLICATIONS FOR MULTI-CHANNEL LIN

AUTOMOTIVE

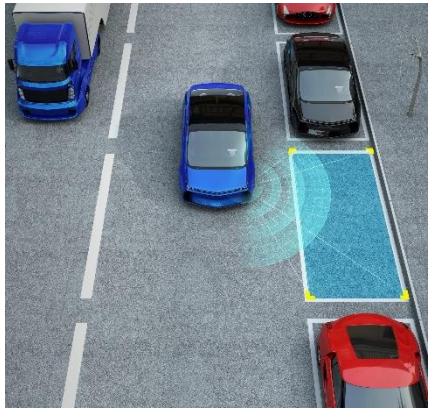
HVAC

Ambient Mood Lighting



Body Control Module

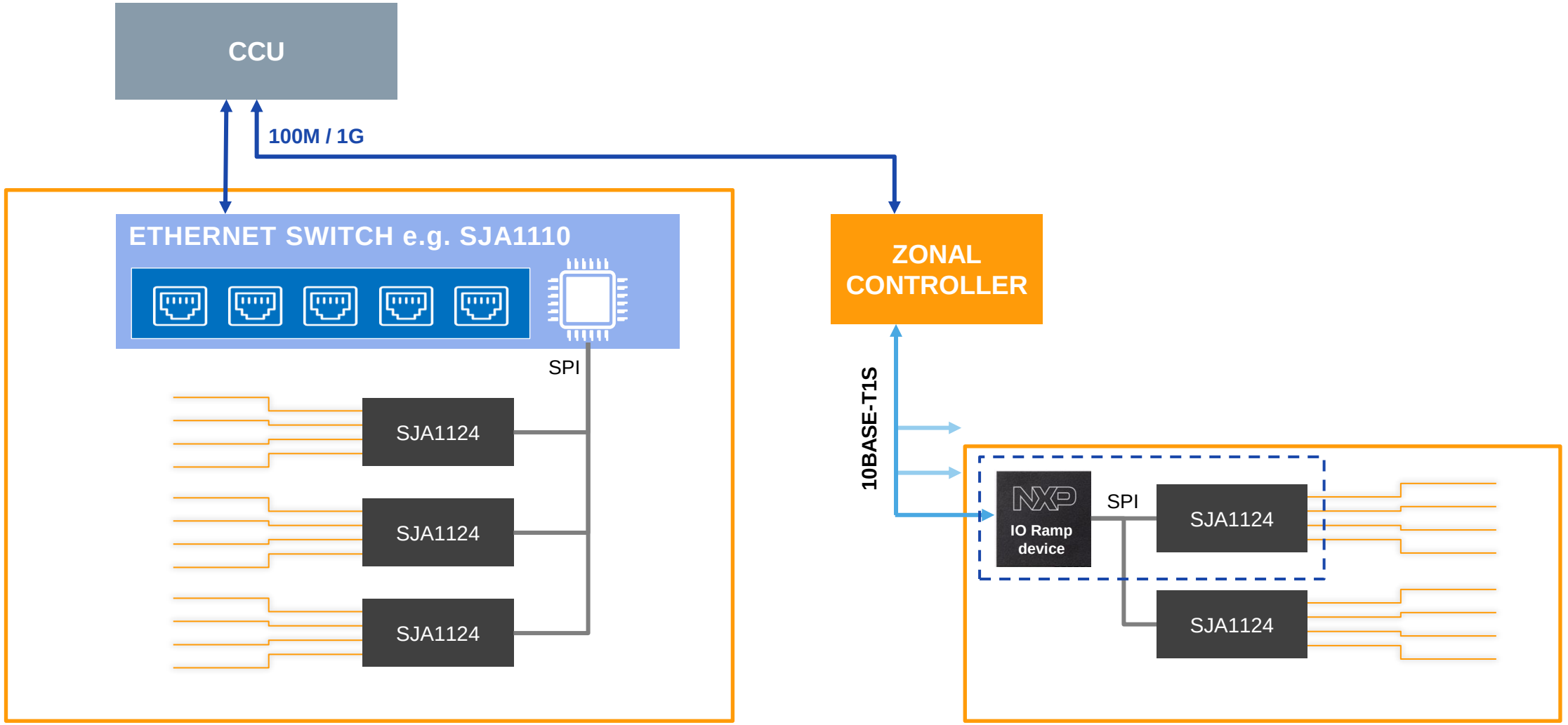
Cockpit Domain Control



Ultra-sonic Park Assistance

With a target host MCU **that does not have enough I/Os or LIN controllers** but needs > 4 LIN channels.

UNDER STUDY – ADDITIONAL CONCEPTS FOR LIN INTEGRATION



ADDITIONAL IN-VEHICLE NETWORKING TALKS OF INTEREST

Wednesday:

- 10:30 – 11:20, The Atrium Study
  TJA1445/65 CAN (SIC) Partial Networking in the Software-Defined Electric Vehicle

- 1:00 – 1:50, Mosaic Ballroom
  Next Generation of CAN – How CAN SIC and CAN XL support Future Vehicle Network Architecture

- 2:00 – 3:30, The Atrium Study
  TJA1104 / TJA1121 – the New MACsec enabled BASE-T1 PHYs for Automotive Ethernet solutions

- 4:00 – 4:50, The Atrium Study
  10BASE-T1S Multidrop Ethernet

Q&A

TECHNOLOGY SHOWROOM

JOURNEYS BY DESIRED ENGAGEMENT

Self-guided tour
Live-streaming at set times
Guided tours

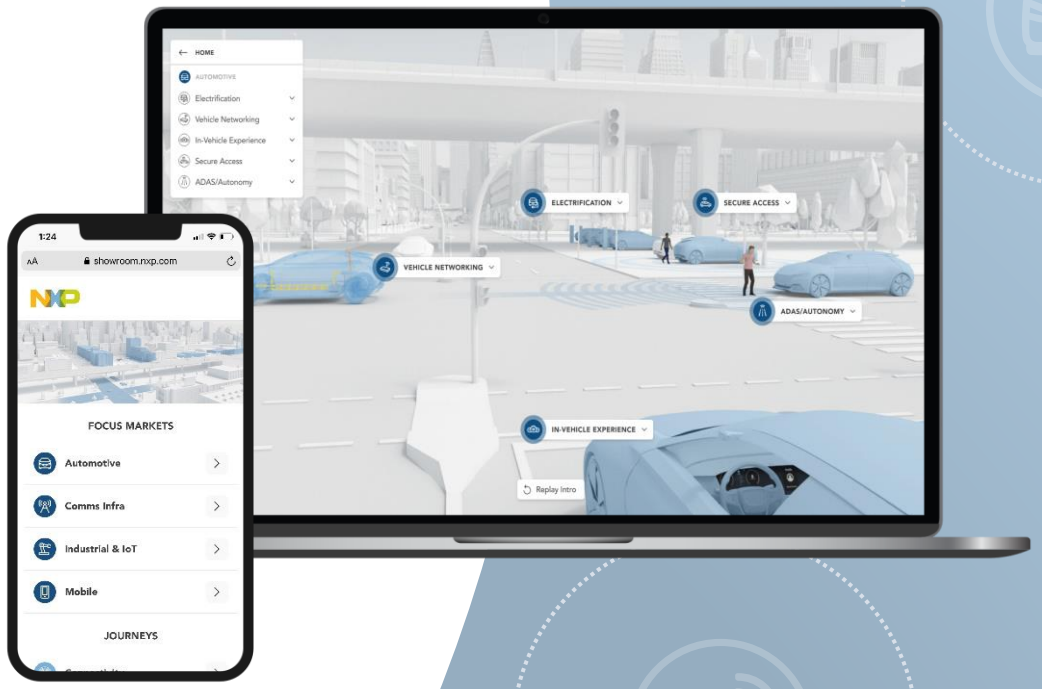
60+ VIRTUAL DEMOS

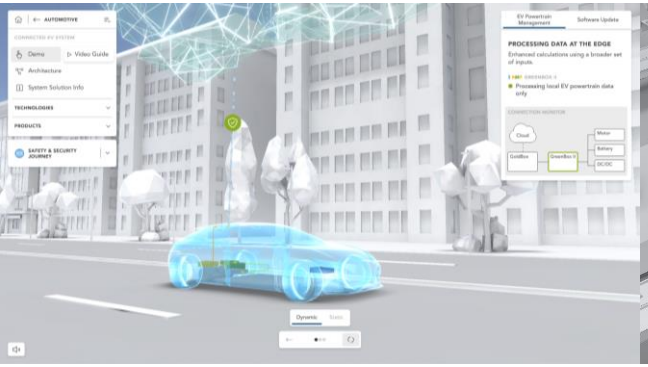
Focus on system solutions
Set up along NXP verticals

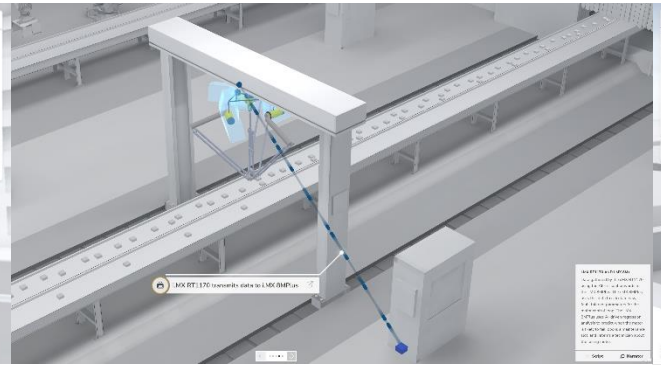
JOURNEYS BY DESIRED FOCUS

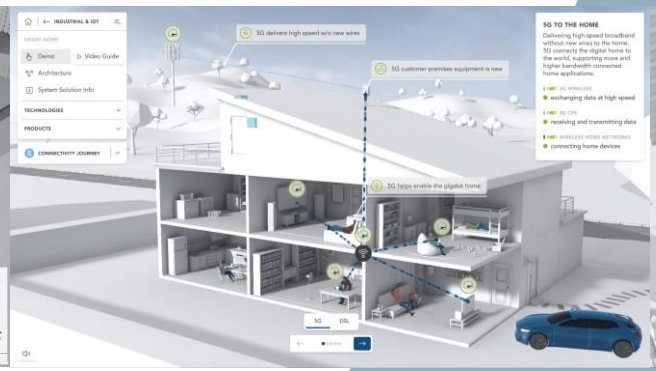
Edge & AI/ML
Safety & Security
Connectivity
Advanced Analog
Low Power Innovation
Sustainability

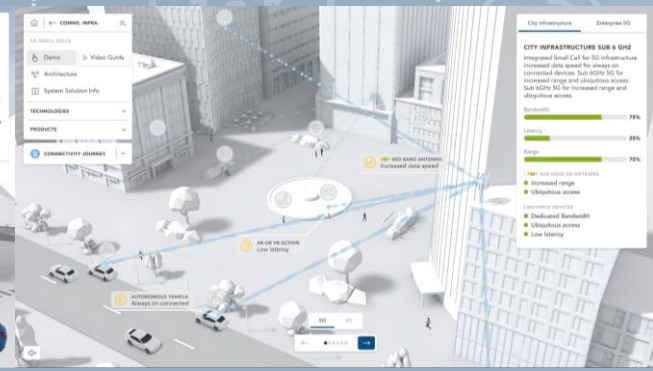
SHOWROOM.NXP.COM











SECURE CONNECTIONS
FOR A SMARTER WORLD