Designing with I²C-Bus Devices

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SECURE CONNECTIONS
FOR A SMARTER WORLD

NXP Secure Interfaces & Power Solutions

Signal Integrity & Routing Solutions

- Signal Switches & Re-drivers
  - USB 3.1, USB Type-C
  - Thunderbolt
  - PCIe, SATA, SAS
  - DP, HDMI, VGA
  - Audio, Data
  - Memory Interface

Industry leader in high-speed switching.

Lowest-power consumption re-drivers

Load Switches

- Over Voltage Protection
- Over Current Protection
- Reverse Current Protection
- Under voltage Lockout
- Thermal Shutdown
- Low R_{ON}
- Low Quiescent Current

HV Load switching with 100V surge protection.

Interface Solutions

- DisplayPort Bridges
- UARTS
- Comparators
- I^2C Bus Buffers
- I^2C Bus Controllers
- I^2C Muxes & Switches
- Voltage Level Translators

Industry's largest I^2C Portfolio for Mobile, Computing and Industrial.

Wireless Connectivity & Smart Sensor Solutions

- NTAG Smart Sensors
- NFMI Radio
- Audio over BLE
- RF & IF Discretes
  - Transceivers
  - LNA's
  - Mixers
  - Switches

Integrated temperature logging solutions.

Ultra low-power single-chip solution, providing robust wireless audio streaming.

Security & Authentication

- Anti-Counterfeit Solution

Industry's smallest package with lowest power.

Power Solutions

- USB Power Delivery
- AC-DC Controllers
- DC-DC Boost Converters
- Direct Charging (Rapid Battery Charging)
- Wireless Charging (Qi/A4WP)
- Micro-PMIC
- Powerline Communication Modem

High efficiency power conversion.

Support of multi-charging protocols (Direct, USB-PD, QC, BC1.2, and proprietary).

Bus Peripherals

- Real Time Clocks
- GPIO Expanders
- Temperature Sensors
- LCD Drivers
- LED Controllers
- Capacitive Sensors
- Stepper Motor Controllers
- EEPROM
- Watch IC
- Data Converter
- DIP Switches

Ultra low-power RTC's.

Widest portfolio of GPIO Expanders.

Smart Audio Solutions

- Class AB Amplifiers
- Class D Amplifiers
- Smart Amplifiers (/w integrated DSP)
- Software
- Speaker Protection
- Audio DAC & ADC

Best-in class speaker protection hardware and software Class D Amplifier solutions.

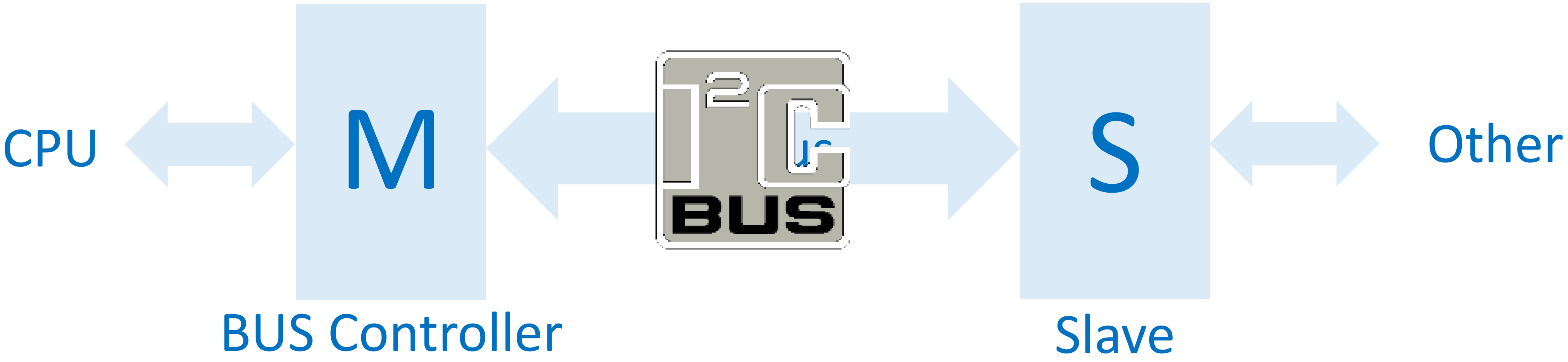
Agenda

- Introduction to I^2C
- I^2C-Bus Communication Protocol
- I^2C-Bus Pull-up Resistor Calculation
- I^2C Interface Signals
- I^2C-Bus Tools

Introduction to I²C-Bus

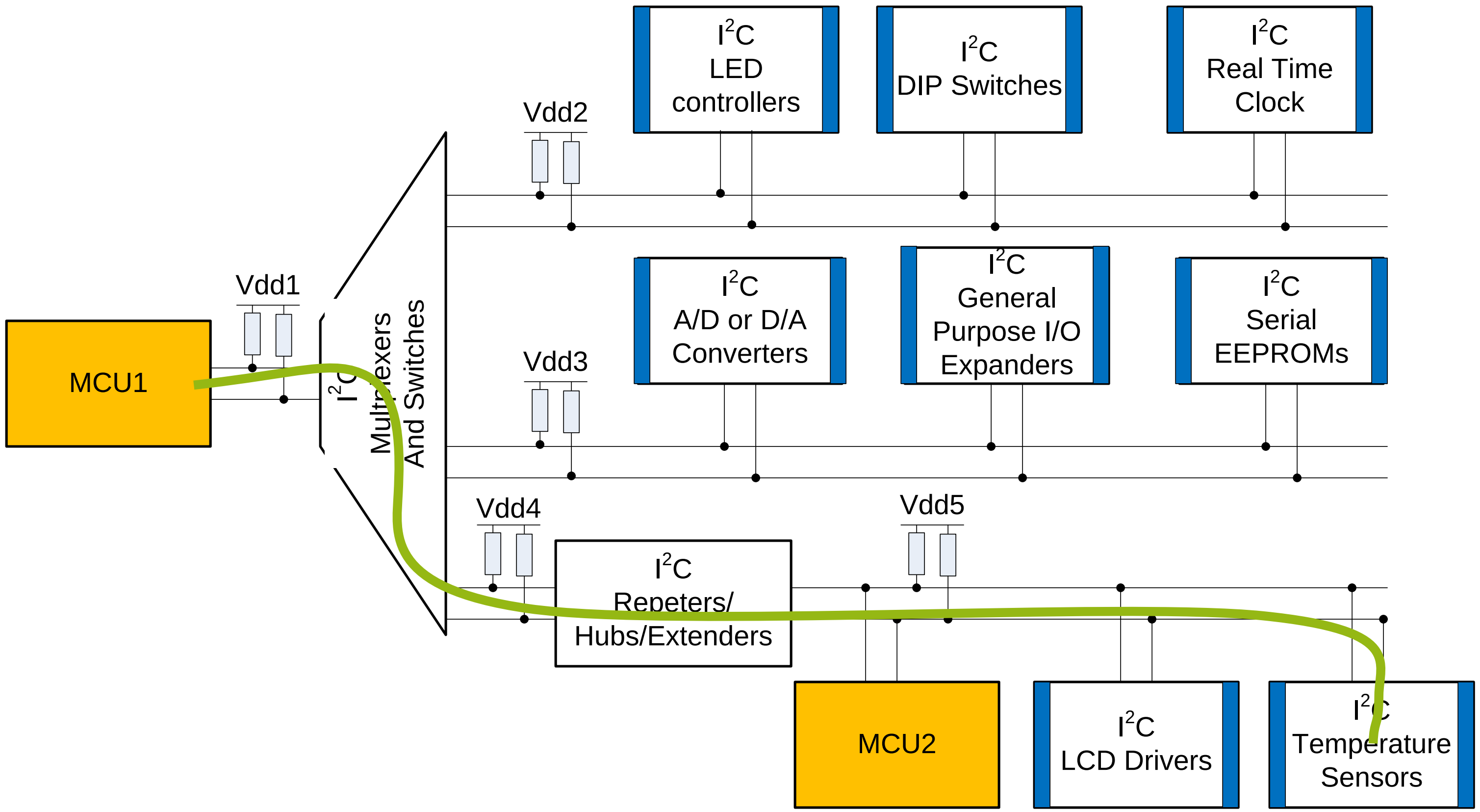
What is I^{2}C?

- A communication bus for slow speed digital data
- I^{2}C = *Inter Integrated Circuit* (Philips invented in the 1980s)
- Original purpose to link a CPU to other circuits in television sets
- Links one or more SLAVE devices
- To a MASTER (one or more BUS CONTROLLERS)



What is I²C?

- I²C BUS can have:
  - Multiple masters
  - Multiple slaves
- Only one master talks to one slave at a time
- All the slaves on the same bus must have different address
- Slow speed device cannot understand higher speed transfer

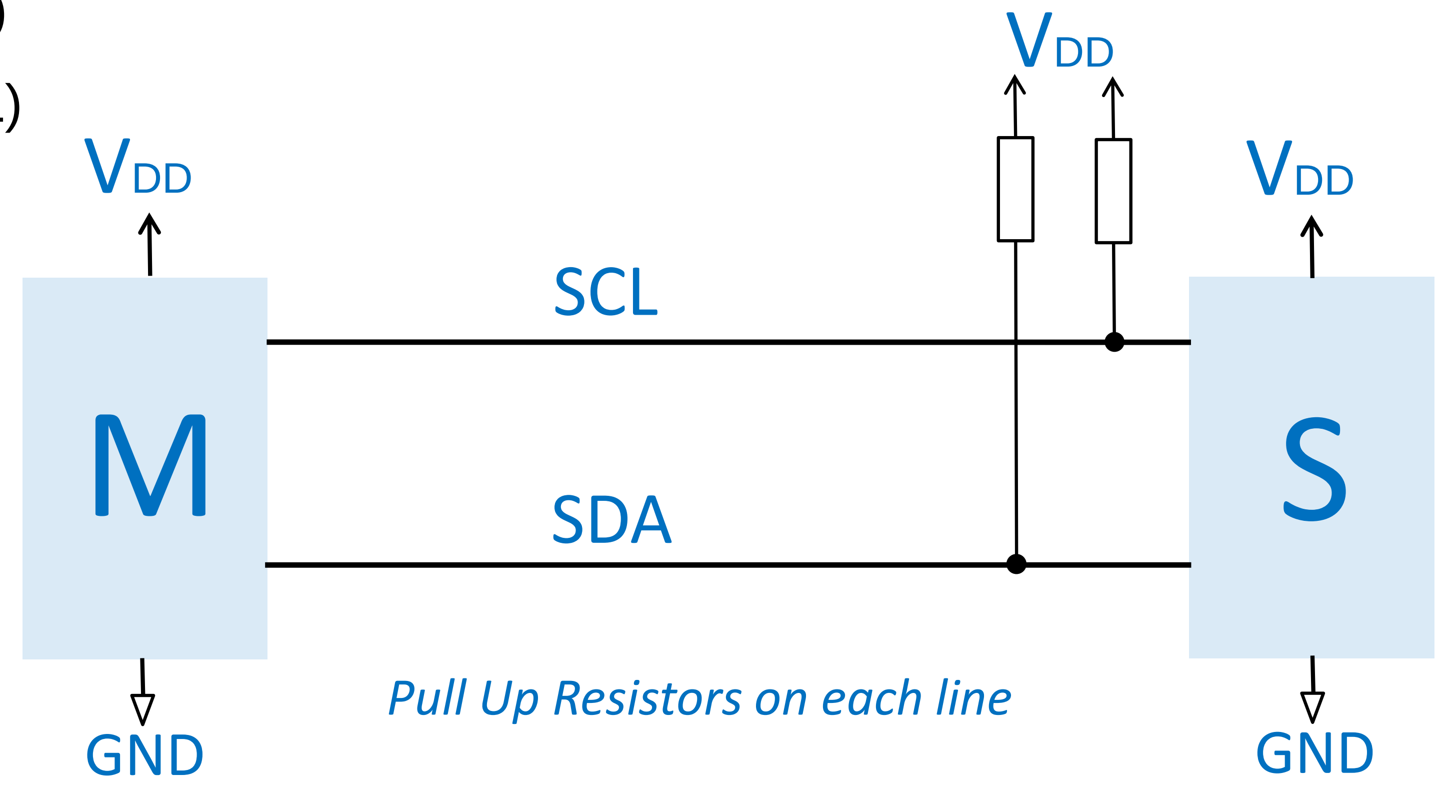


I^2C-Bus Physical Layer

Physical Layer = Electrical Connections

Two Wires: Data and Clock *(plus ground and supply)*

- Data line (SDA)
- Clock line (SCL)



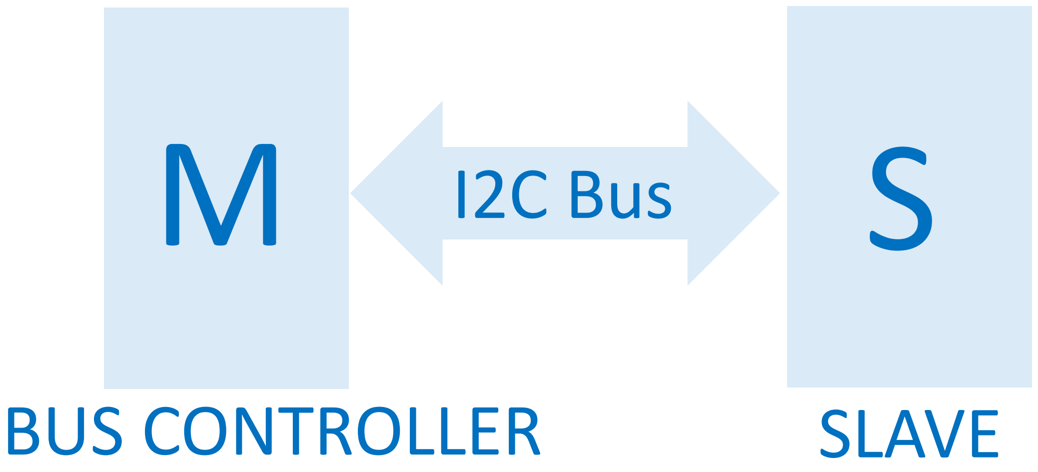
I^{2}C-Bus Communication Protocol

What is the I^{2}C Protocol Layer?

Protocol Layer = Data Format, Traffic, Collision Arbitration

An I^{2}C Bus must have:

- Two node types (Master and Slave)
- Minimum of ONE Slave and ONE Bus Master



I^2C Interface Protocol

I^2C BUS constructs off 9 bit block

START condition:
When SCL is HIGH then SDA goes
from HIGH to LOW

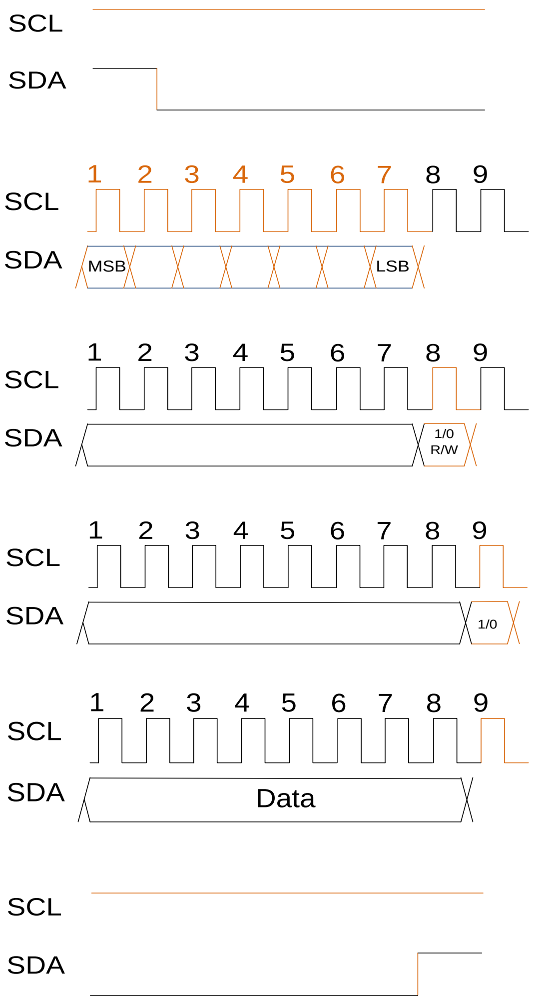
Address bit
7 bit after START condition

Read or Write bit
After 7 bit address, the 8th bit is Read or Write bit
1 = Read cycle or 0 = Write cycle

ACK
Synchronization bit between master and slave
0 = ACK and 1 = NACK

Data Byte
8-bit after address byte is data byte from master or slave

STOP condition:
When clock line (SCL) is HIGH
then the data line (SDA) goes LOW to HIGH



All slaves on this bus
pay attention !!!

Master wants
to talk slave with this address

Master wants to read or write
0: Write cycle
1: Read cycle

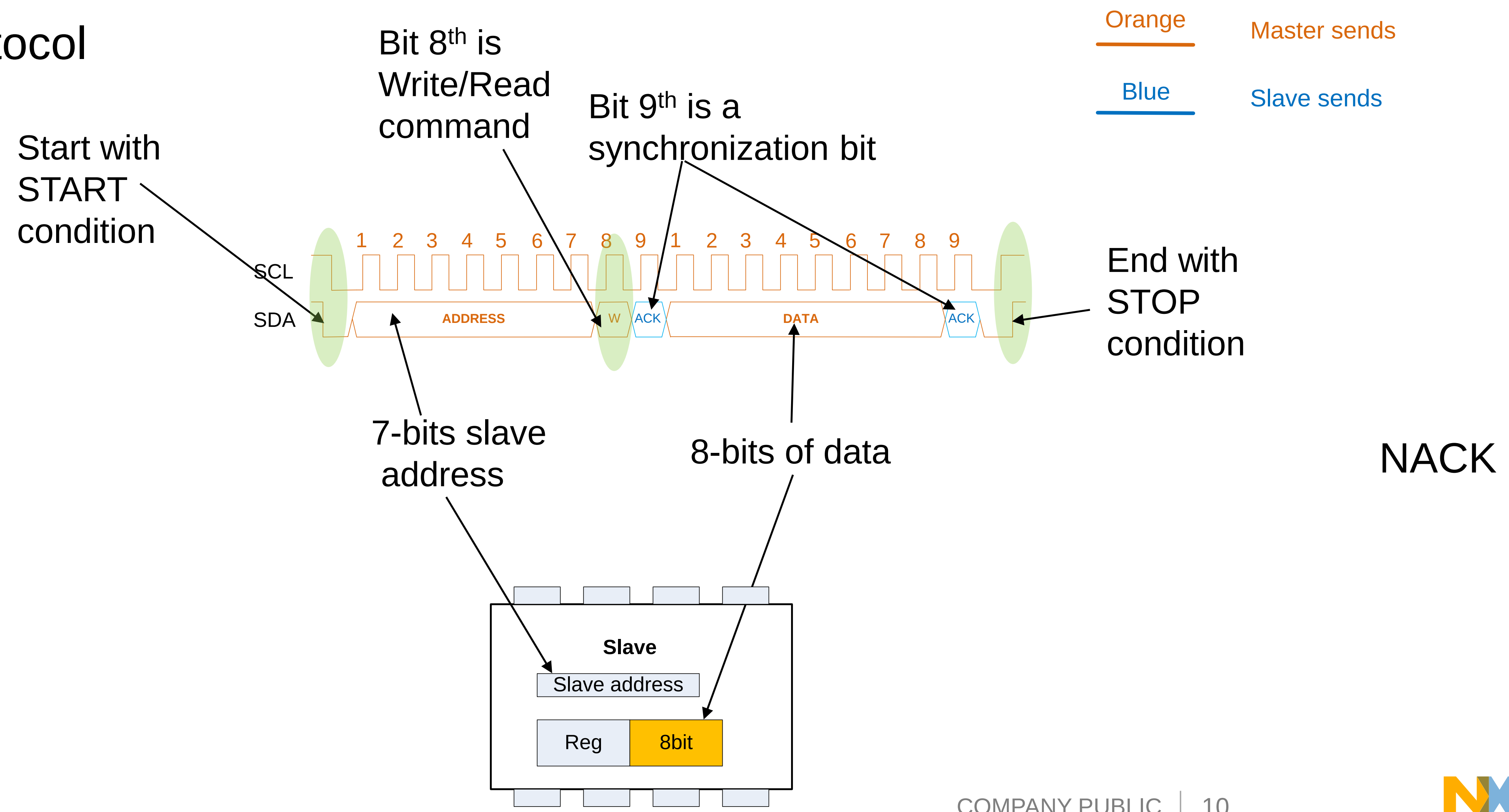
Slave or master:
0: I am here or data received
1: not me or data not received

Data byte
Master sends data when write cycle
Slave sends data when read cycle

Master notifies the slave this is the end of transaction

Complete I²C Interface Protocol

I²C protocol

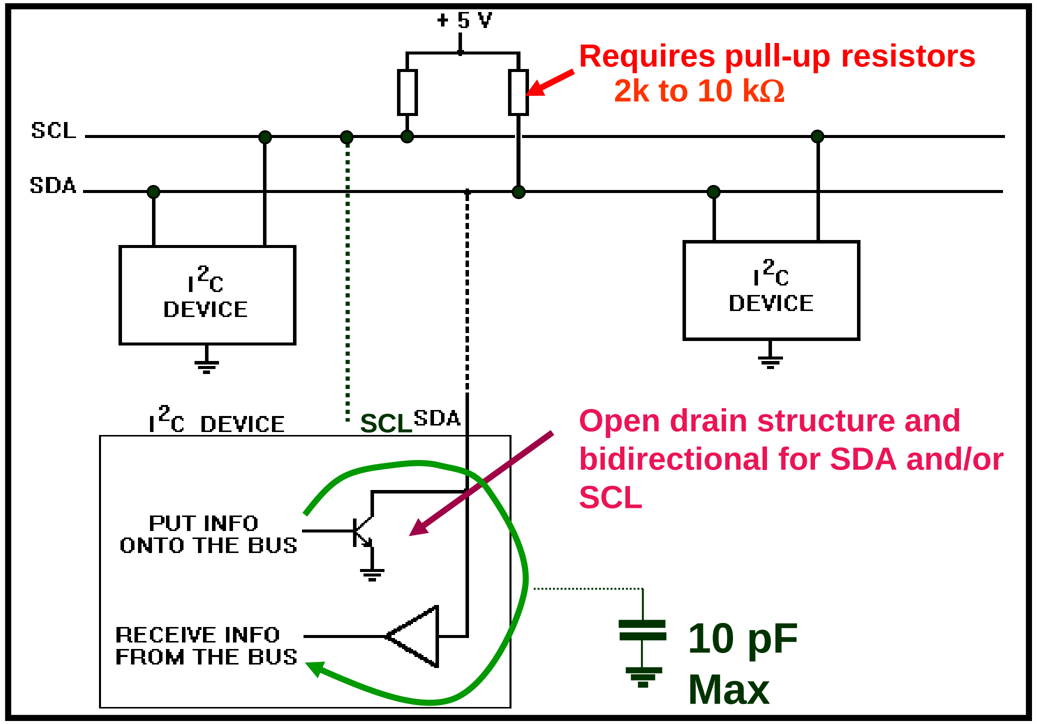


I^{2}C-Bus Pull-up Resistor Calculation

I/O (SDA & SCL) Driver Architecture

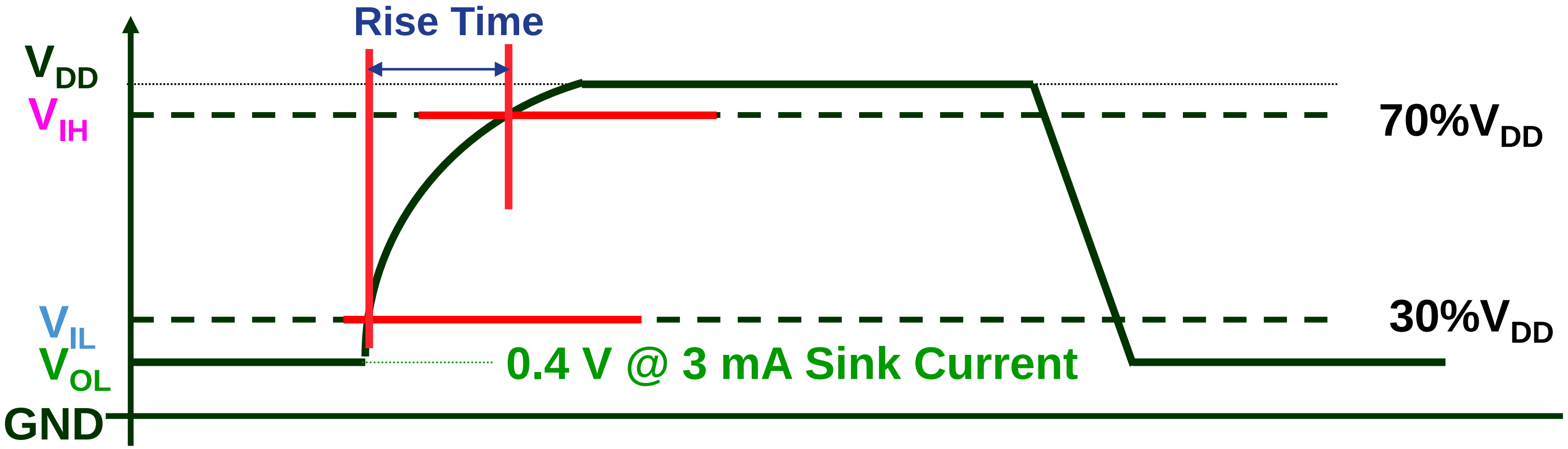
SDA and SCL are open drain/collector

- Required pull-up resistors to pull the line to logic “1”



Key Electrical Parameters

	Standard Mode	Fast Mode	Fast Mode Plus	High Speed Mode	
Bit Rate (kb/s)	0 to 100	0 to 400	0 to 1000	0 to 1700	0 to 3400
Max Load (pF)	400	400	560	400	100
Rise time (ns)	1000	300	120	160	80
Noise filter (ns)	-	50	10	10	10



Calculating Pull-up Resistors

1) $R_{MIN} < R_{PU} < R_{MAX}$

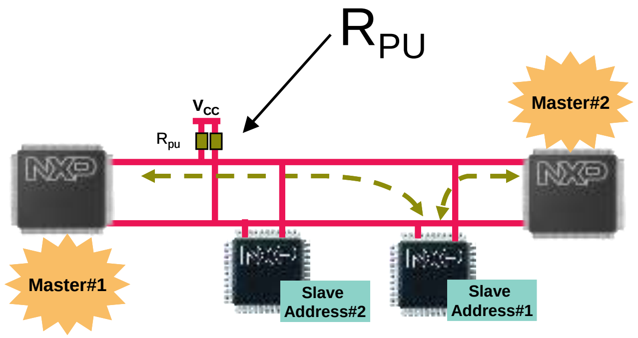
2) $R_{MIN} = (V_{DDMAX} - V_{OLMAX}) / I_{OLMAX}$

V_{DDMAX}	V_{OLMAX}	R_{MIN}			
		I_{OLMAX} = 3mA	I_{OLMAX} = 6mA*	I_{OLMAX} = 12mA**	I_{OLMAX} = 30mA***
2.7 V	0.6 V	700 Ω	350 Ω	175 Ω	70 Ω
3.6 V	0.6 V	**1.0 kΩ**	**500 Ω**	250 Ω	**100 Ω**

* I^2C Bus with a buffer
** EXPxxxx bus
*** I^2C Fast-mode Plus Bus

3) $R_{MAX} * C_{MAX} = 1.18*t_r$

MODE	Frequency	t_r	C_{MAX}	R_{MAX}
Standard	100 kHz	1000 ns	400 pF	**2.96 kΩ**
Fast Mode	400 kHz	300 ns	400 pF	**885 Ω**
Fast Mode Plus	1000 kHz	120 ns	560 pF	**252 Ω**



Glossary

R_{PU}: Pull-up resistor
R_{MIN}: Minimum pull-up resistor
R_{MAX}: Maximum pull-up resistor
V_{DDMAX}: Maximum supply rail
V_{OLMAX}: Maximum output voltage low
I_{OLMAX}: Maximum sink current
C_{MAX}: Maximum load capacitance
t_r: Rise time

How to Calculate the I²C-Bus Pull-up Resistors?

Minimum value

There is a minimum resistor value determined by the I²C spec limit of 3 mA

$R = (Vdd_{max} – Vol_{max})/ 0.003A$

Example: using a 5±0.5 V bus: $R = (5.5V – 0.4V)/ 0.003A = 1.7\ k\Omega$

Maximum value

Determined by the I²C-bus rise time requirements:

$V(t1) = 0.3*Vdd = Vdd\ (1–1/e^{t1/RC})$; then $t1 = 0.3566749*RC$

$V(t2) = 0.7*Vdd = Vdd\ (1–1/e^{t2/RC})$; then $t2 = 1.2039729*RC$

$t = t2–t1 = 0.8472979*RC$

For standard-mode I²C-bus: t = rise time = 1000ns (1 µs)

so RC = 1180.2 ns

Example: at a bus load of 400 pF: $R_{max} = 2.95\ k\Omega$

For fast-mode:

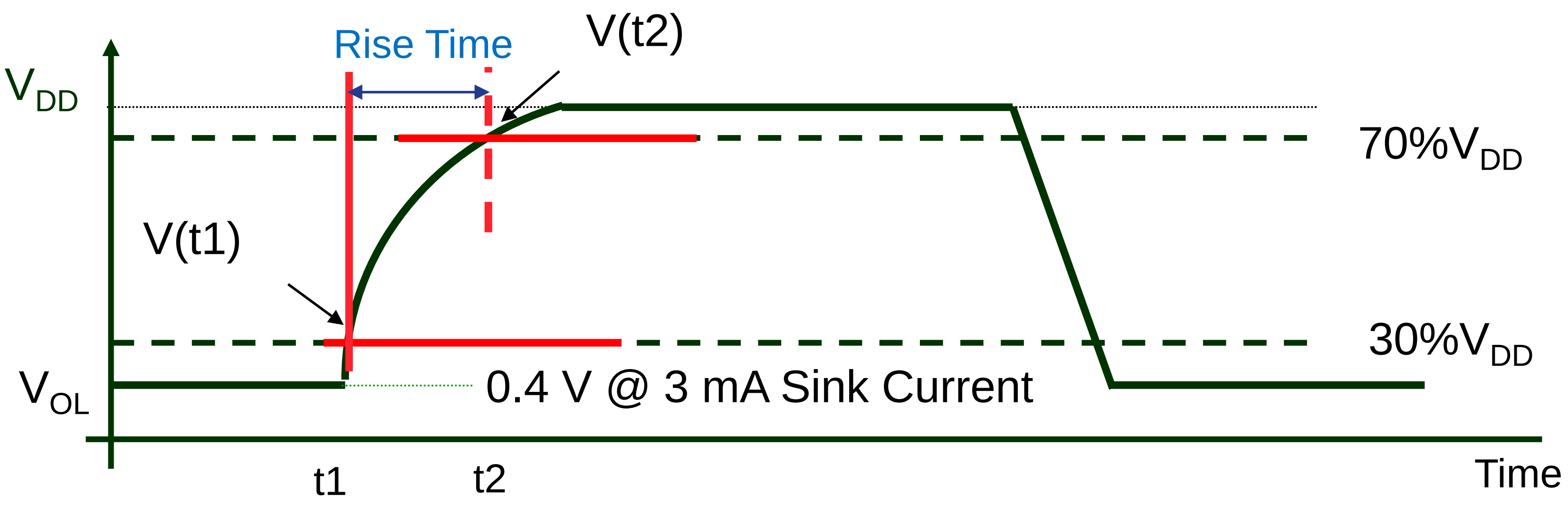
I²C-bus rise time = 300 ns @ 400 pF: $R_{max} = 885\ \Omega$

How Does User Derive the Rise Time for I^{2}C-Bus?

I^{2}C-bus rise time is determined as in the following:

1) V(t1) = 0.3*V_{DD} = V_{DD} (1–1/et1/RC) → t1 = 0.3566749*RC (EQ1)
2) V(t2) = 0.7*V_{DD} = V_{DD} (1–1/et2/RC) → t2 = 1.2039729*RC (EQ2)
3) Subtract EQ1 from EQ2 → $t_{\text{rise time}}$ = t2–t1 = 0.8472979*RC or

   R*C = 1.18*$t_{\text{rise time}}$



Effect of Pull-up Resistors

- Minimum pull-up resistor limits the maximum current sink that affects the voltage output low (VOL).
  - Increasing pull-up resistor above RMIN leads to decreasing VOL and higher noise margin
  - Decreasing pull-up resistor below RMIN leads to increasing VOL and lower noise margin

- Maximum pull-up resistor affects the rise time and speed
  - Increasing pull-up resistor above RMAX leads to slower/possible rise time violation or lower speed
  - Decreasing pull-up resistor below RMAX leads to faster rise time and speed

Bus Loading and Timing Relationship

The I^2C bus specifications require certain bus rise times. Those times are defined with the time measured between the bus LOW and HIGH limit levels of 30% and 70% of VDD.

From the expression $V(t) = VDD*(1 - 1/e^{t/\tau})$, and as shown on the curve at the right, the time for the bus to rise to 30%VDD is 0.357τ.

The time to rise to 70%VDD is $1.204\ \tau$, so the I^2C rise time, to rise from 30% to 70% of VDD, is $(1.204 - 0.357) = 0.847*\tau$.

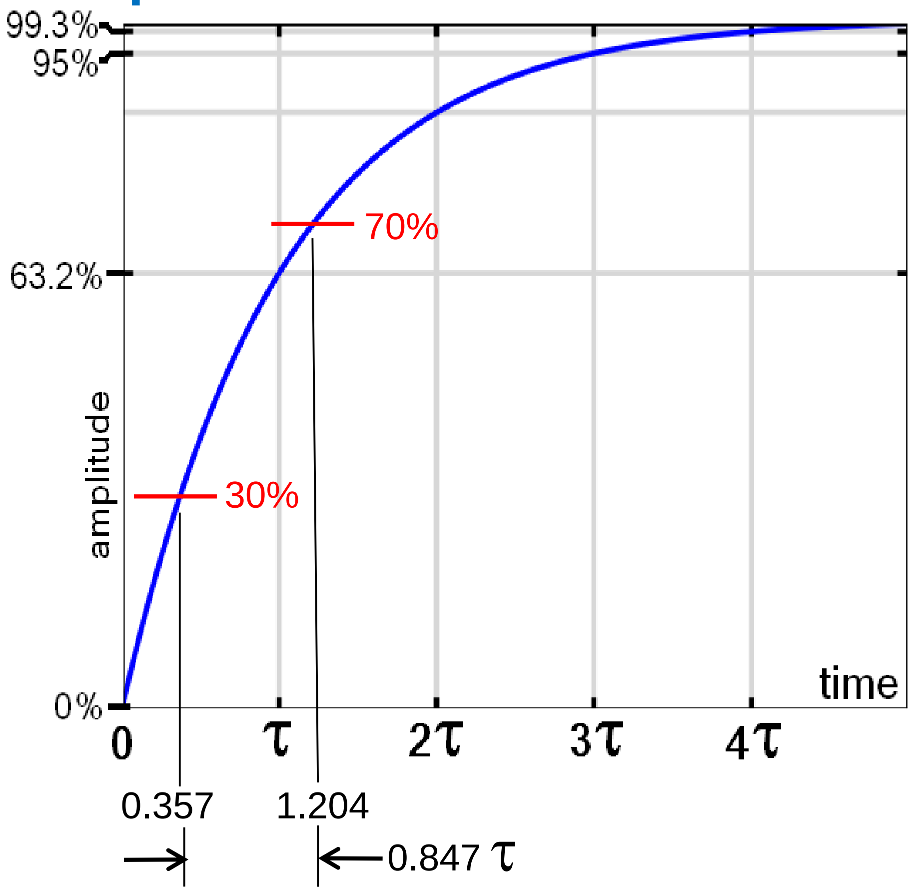
Because $\tau = RC$, meeting the I^2C rise time requirements means the pull-up "R" and bus capacitance "C" must satisfy the relationship:

0.847 RC <= I^2C rise time specification

or RC <= I^2C rise time specification / 0.847

or <u>RC <= I^2C rise time specification x 1.18</u>

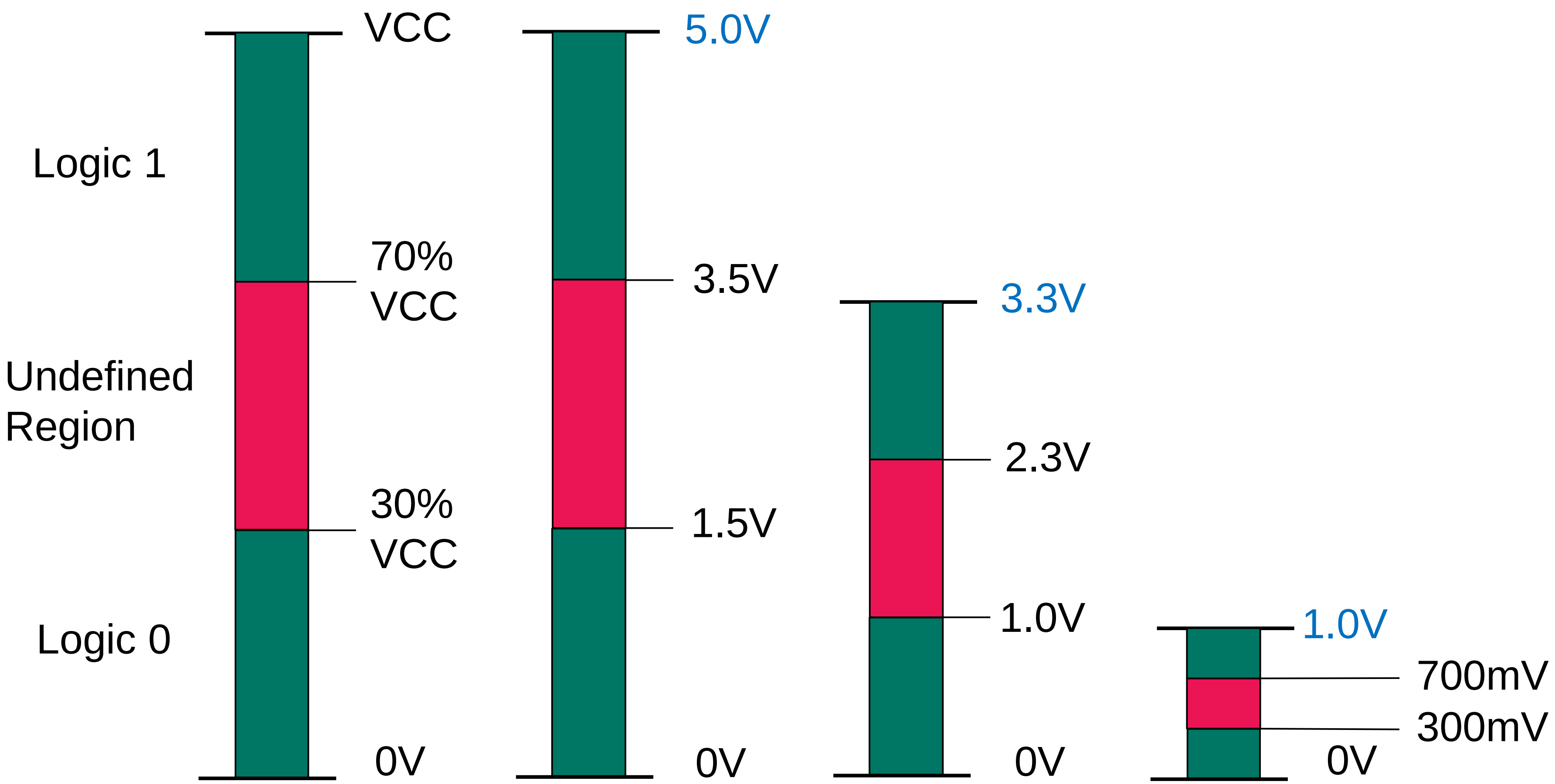
For example, to meet the Fast-mode 300 ns rise requirement, the RC product must be less than
1.18 x 300 <= 354 ns.



τ = RC. R= Ohms, C= Farads, t= secs.
I^2C rise time requirement = 0.847RC
1/0.847 = 1.18
RC requirement < 1.18 x I^2C rise time

I²C Interface Signals

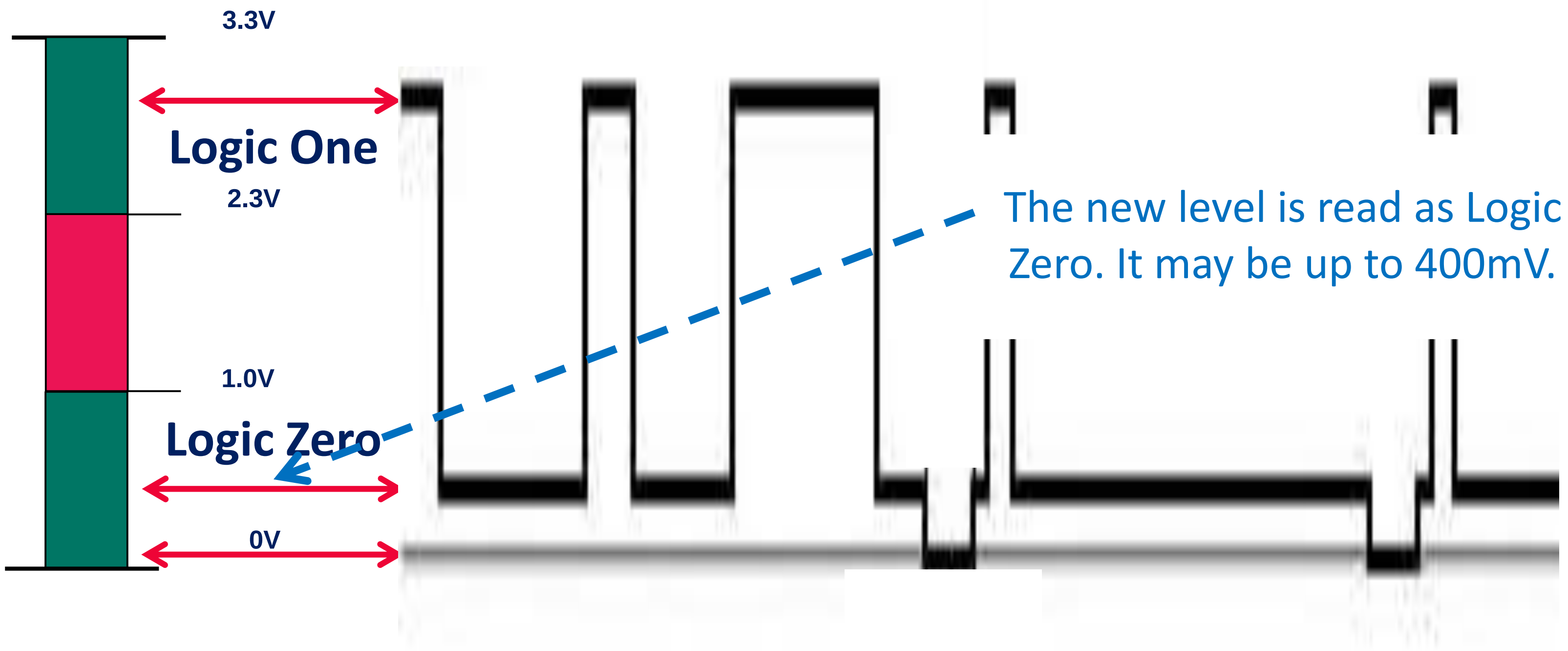
I²C Logic Levels and Thresholds

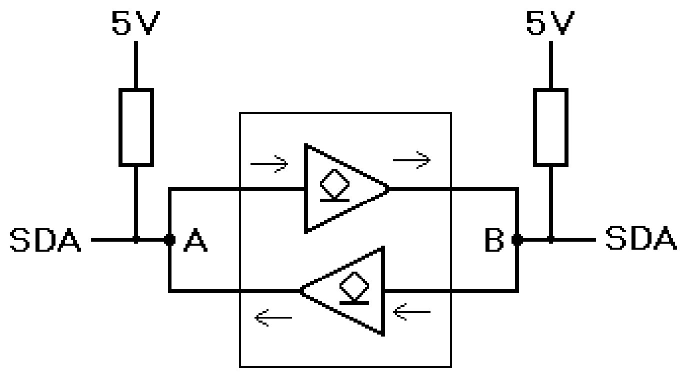


Comparison of I²C Bus logic levels for different supply voltages

"Three Level" I^{2}C Signals

- The I2C Bus has two logical levels (zero and one)
- There are now 3 signal levels, but only 2 logical levels
- This is caused by different strength Drivers, or by Bus Buffer "Offset"





I²C Signals (Oscilloscope Plot)

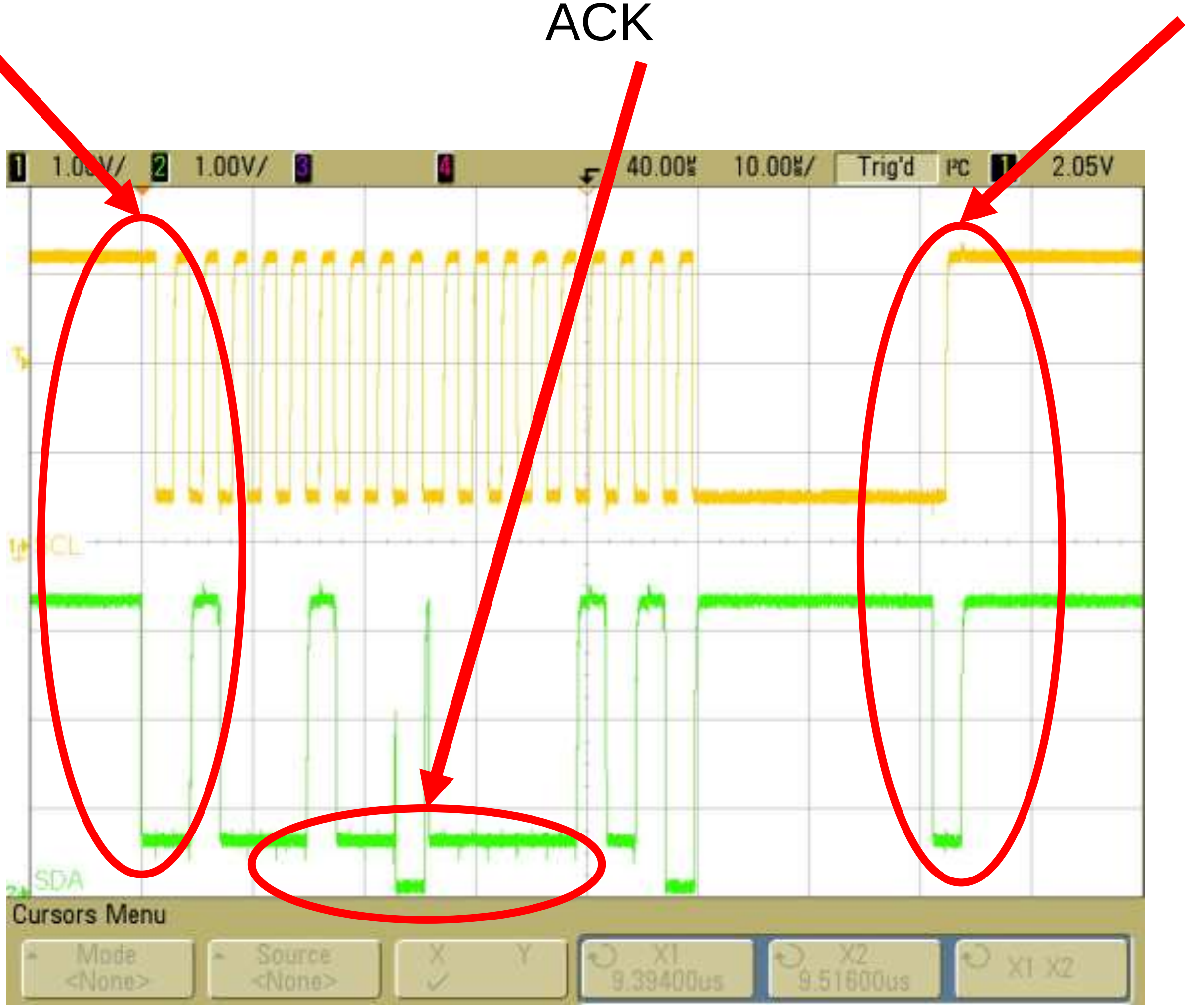
Start

ACK

stoP

SCL
(Clock)

SDA
(Data)



I^{2}C-Bus Tools

Fm+ I²C-Bus Demonstration System

PC/GUI

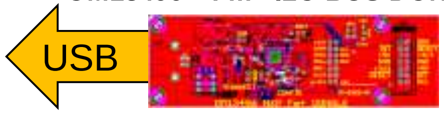
MASTER

Total Phase Aardvark

The Boardshop Win-I2CUSB DLL Dongle

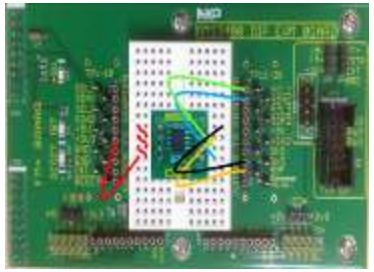
OM13260 - Fm+ I2C-BUS DEVELOPMENT BOARD

OM13496 – Fm+ I2C-BUS DONGLE



SLAVE

OM13490 – DIP EVM BOARD

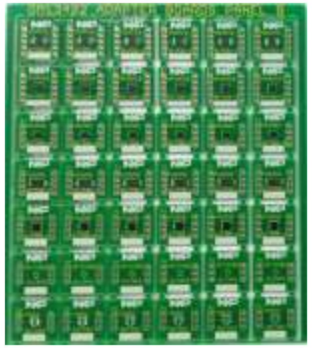


OM13303 - GPIO TARGET

OM13399 – BRIDGE BOARD

OM13488 – 16-bit GPIO Daughter Card

DIP ADAPTER BOARD



OM13398 – PCA9617A BUS BUFFER BASE BOARD

OM13487 – LM75 type TS Daughter Card

Fm+ I²C-Bus Development Board Kit (OM13320)

Box Content

OM number	12 NC Number	Description (50 Chrs max)	Description (35 Chrs max)	NXP Device Cross Reference
OM13260	9352 959 14598	FM+ I2C-bus Development Board (RoHS)	FM+ I2C-bus Dev Brd (RoHS)	PCA9665, PCA9672, PCA9901, PCA9955
OM13303	9352 959 15598	GPIO Target Board (RoHS)	GPIO Target Brd (RoHS)	none
OM13398	9353 020 74598	PCA9617A Bus Buffer Demo Brd (RoHS)	PCA9617A Bus Buffer Brd (RoH	
OM13399	9353 020 75598	Bridge Board (9pin to Fm+) (RoHS)	Bridge Board (9pin to Fm+) (RoH	

Fm+ Development Board Kit
OM13320

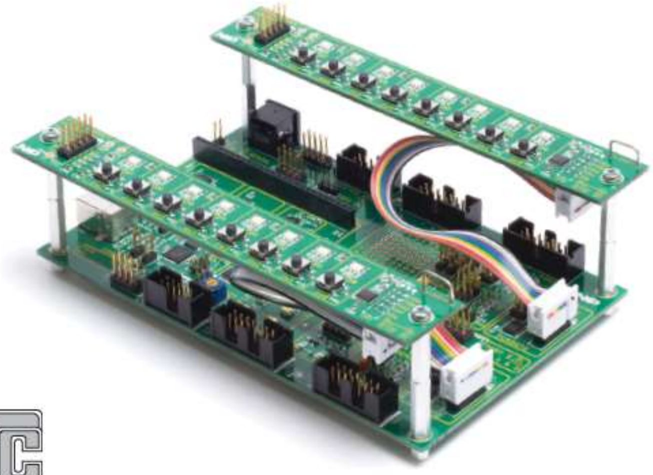
- Explore the I2C-Bus
- Run demonstrations of NXP's I2C Fm+ Slaves and Bus Controllers
- Develop I2C Hardware
- Expand this kit with add-on I2C Daughter Cards

BOX CONTENTS:

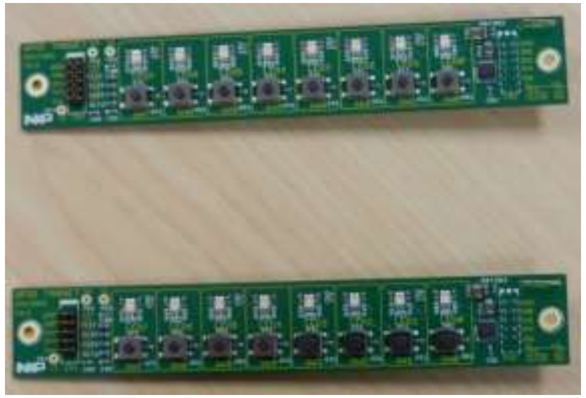
OM13260 Fm+ Development Board

Plus

- OM13303 GPIO Target BRD (x2)
- OM13398 PCA9617A Bus Buffer Demo Board
- OM13399 Bridge Board
- Cables and Mounting Hardware



Fm+ I^{2}C-Bus Development Board Kit (OM13320)



GPIO Target Board OM13303 (2x)

Fm+ Development Board OM13260

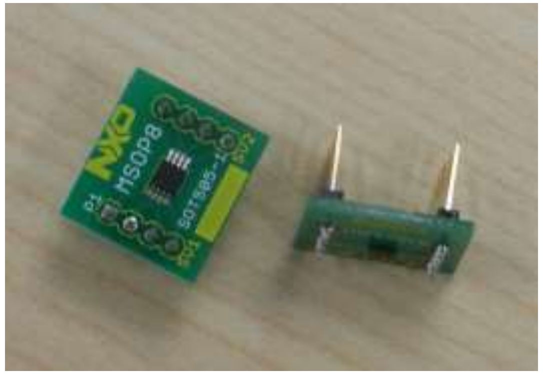
Bus Buffer Board OM13398

Bridge Board OM13399

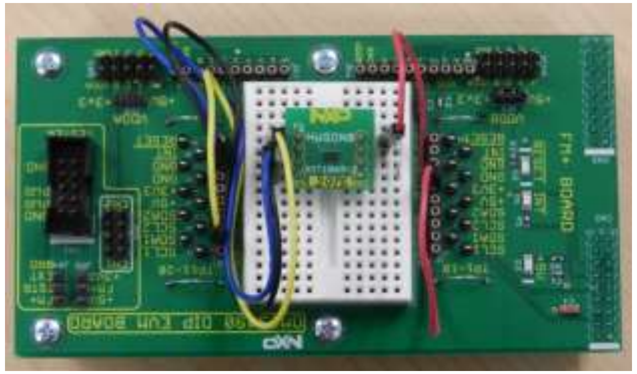
DIP Adapter Boards

Breakout Board (A through G)

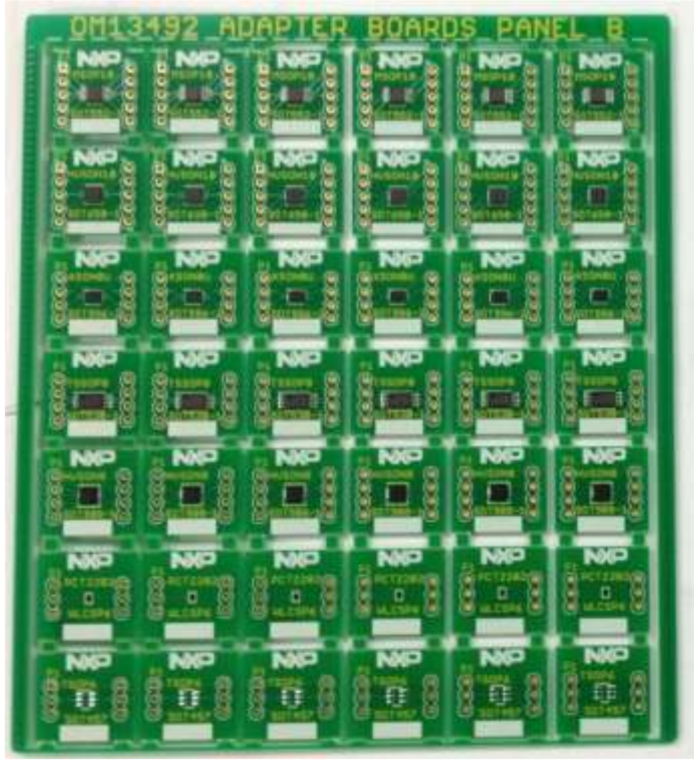
- Prepare any I²C device as a DIP module for the Fm+ I²C Bus EVM Board OM13490
- UM10754 (https://www.nxp.com/docs/en/user-guide/UM10754.pdf)



Example DIP Adapters



Example set up



OM number	12 NC Number	Description (50 Chrs max)	Description (35 Chrs max)	NXP Device Cross Reference
OM13491		Breakout Board A (RoHS)	Breakout Board A (RoHS)	SO8, VSSOP8, XQFN8, HWSON8, MSOP8
OM13492		Breakout Board B (RoHS)	Breakout Board B (RoHS)	TSOP6, WLCSP6, HVSON8, TSSOP8, XSON8U, HVSON10, MSOP10
OM13493		Breakout Board C (RoHS)	Breakout Board C (RoHS)	DQFN14, 16, 20 and 24
OM13494		Breakout Board D (RoHS)	Breakout Board D (RoHS)	HVQFN16, 20 and 24
OM13495		Breakout Board E (RoHS)	Breakout Board E (RoHS)	TSSOP14, 16, 20 and 24
OM13497		Breakout Board F (RoHS)	Breakout Board F (RoHS)	QSOP16, XFBGA16, XQFN16, TSSOP28
OM13498		Breakout Board G (RoHS)	Breakout Board G (RoHS)	VFBGA24, XFBGA24, HTSSOP28

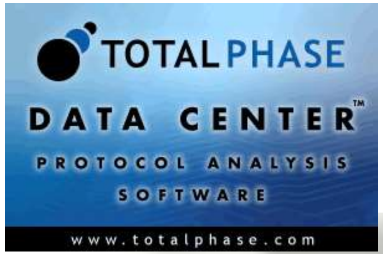
Total Phase Debugging Tools

- Third party, industry leading, diagnostic tools
- Aardvark (I^2C Host Adapter)

- Beagle (I^2C Protocol Analyzer)

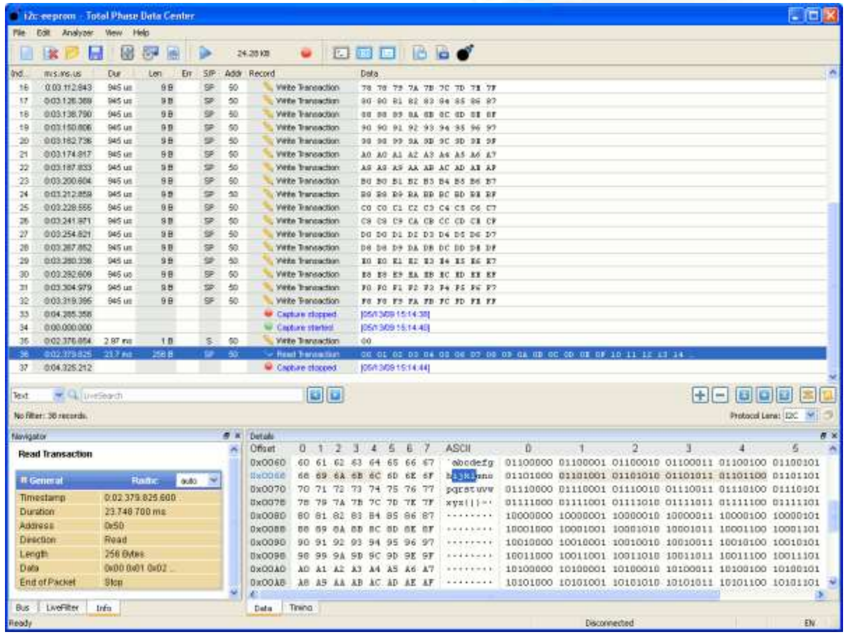
- Plugs in to the Fm+ Development Board
- Plugs in to the new Daughter Cards (allows standalone operation)

Aardvark (Master) and Beagle (Monitor)



- Third Party tools for I^{2}C control and data logging
- Bundled software (for Win7/64, MAC, Linux)
- Not supplied by NXP (buy your own tools)

http://www.totalphase.com/products/beagle_ism/



https://www.totalphase.com/products/aardvark-i2cspi/

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