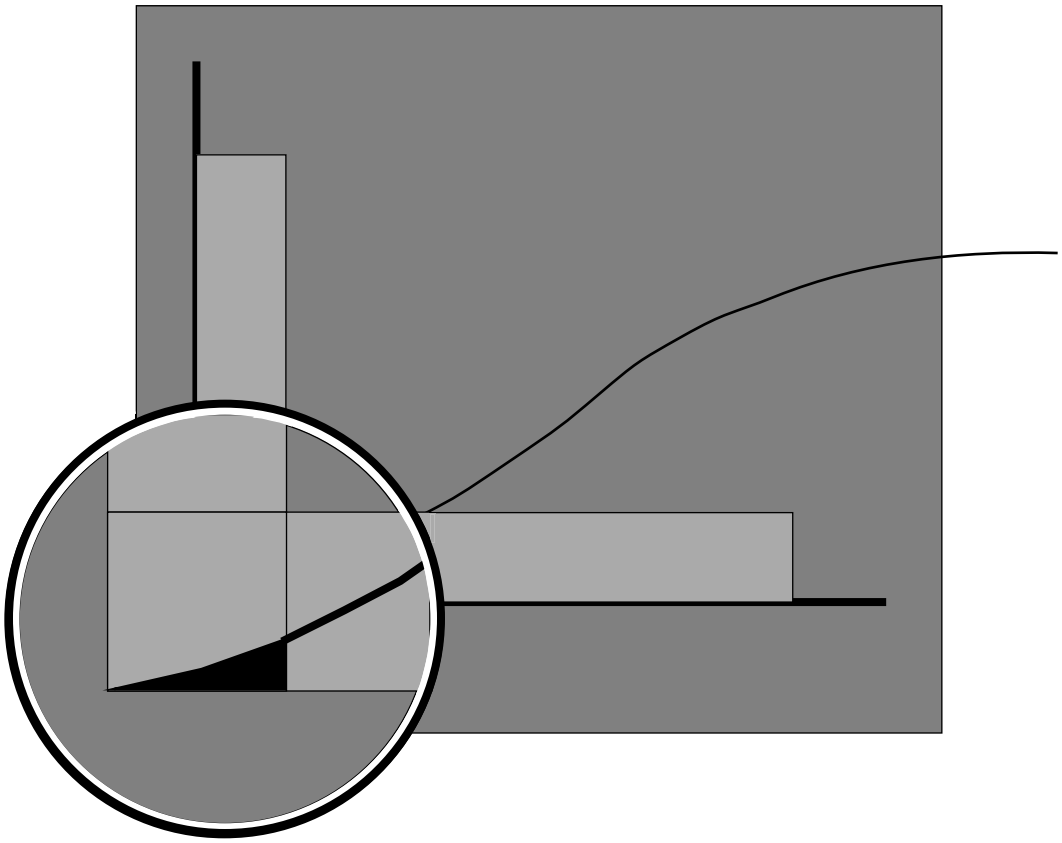
SECTION 6

DSP56166 ON-CHIP SIGMA/DELTA CODEC



SECTION CONTENTS

6.1 INTRODUCTION

This section describes the DSP56166 Sigma-Delta (∑Δ∑Δ) over sampled voice band codec block. It discusses the general block diagram of the A/D and D/A sections, the handshake between the DSP5616 core and the codec, as well as the last decimation antialiasing filter and first interpolation reconstruction filter performed in software by the DSP5616 core.

6.2 GENERAL DESCRIPTION

The ∑Δ oversampled voice band codec block is built using HCMOS technology and utilizes switched capacitor technology in some circuits. The codec contains one A/D converter and one D/A converter. It also contains two reference voltage generators, a current bias generator, and a master clock circuit (see Figure 6-1).

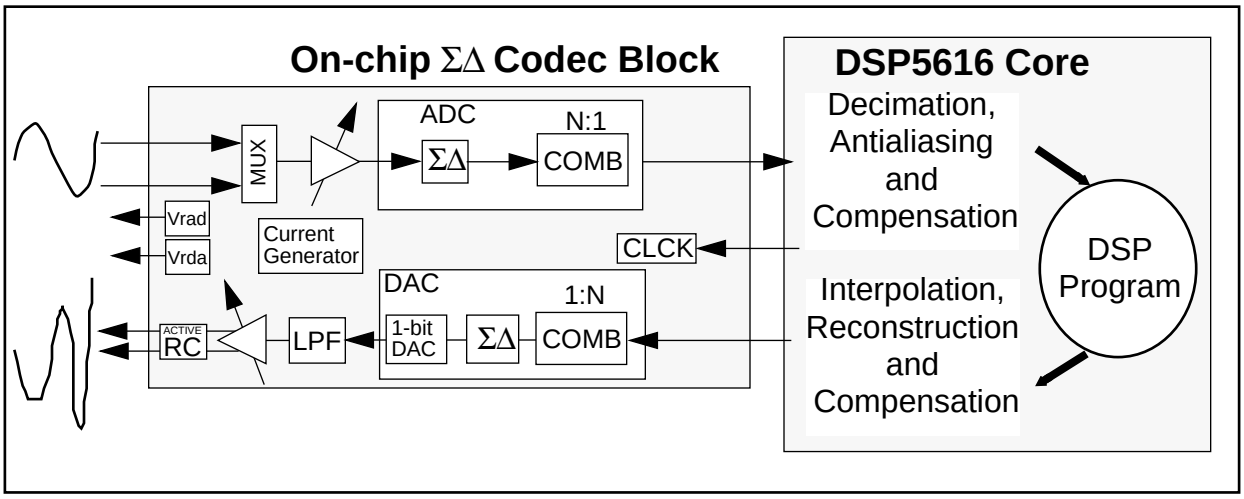


Figure 6-1 DSP56166 On-chip ∑Δ Functional Diagram

The A/D converter consists of an analog ∑Δ modulator with selectable input gain, a digital low-pass comb filter, and a parallel bus interface. The analog modulator is a second-order ∑Δ loop implemented using fully differential CMOS switched capacitor circuitry. The analog modulator input is selectable from one of two pins. The analog modulator output is the input to a third-order digital comb filter which provides low-pass filtering and decimation. The final 16-bit result is output through a parallel interface to the global data bus of the DSP5616 core.

The D/A converter consists of a second-order comb interpolating filter, a digital ∑Δ modulator, a 1-bit DAC, a two-pole Butterworth low pass filter, a selectable attenuator, and an active RC low pass output stage. The interpolator takes in 16-bit two's complement numbers from the DSP5616 core and upsamples them to a high frequency. The modulator

changes these 16-bit words into a 1-bit stream. The 1-bit DAC converts this 1-bit stream into ±2 volt differential analog levels. The output of the DAC is filtered by the switched capacitor Butterworth filter which attenuates the out-of-band shaped modulator noise. The selectable attenuator provides volume control in increments of 5 dB per step. The active RC low pass filter provides reconstruction filtering and driver capabilities.

This ∑Δ codec block has been designed for maximum flexibility. The user can select any value between 65 and 128 as the decimation (interpolation) ratio for the A/D (D/A) converters. Operating at its nominal sampling rate of 2 MHz, the A/D converter provides a 16-bit digital output with more than 60 dB S/(N+D) for input signals. The D/A converter nominally takes in a 16-bit word at a 16 KHz rate, and has a fully differential analog output which provides more than of 60 dB S/(N+D).Table 6-1 summarizes the main features of the codec block.

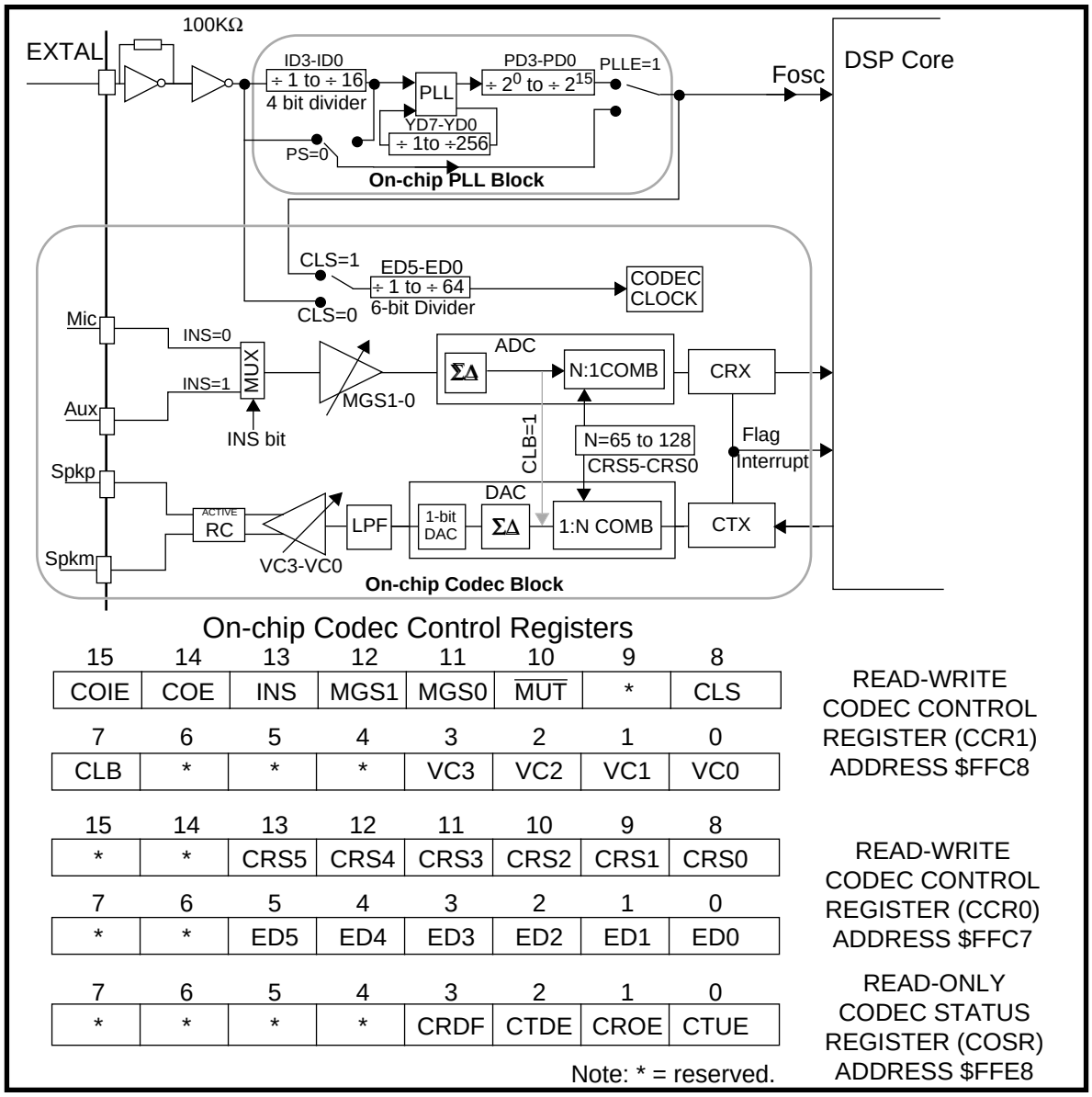
Table 6-1 On-chip Codec Main Features

- 16-bit resolution
- Dynamic Range of 80 dB
- More than 60 dB S/(N+D)
- Operates at clock rates between 100 KHz and 3 MHz
- No off-chip component required
- Internal voltage reference (2/5 of positive power supply)
- Low power HCMOS

The last decimation filtering stage of the A/D section as well as the first interpolation filtering stage of the D/A section is implemented by software in the 16-bit DSP core in order to reduce the codec cell die area.

6.3 CODEC BLOCK DIAGRAM

A general block diagram of the DSP56166 codec and its programming model can be seen in Figure 6-2.



On-chip Codec Control Registers

15	14	13	12	11	10	9	8	
COIE	COE	INS	MGS1	MGS0	$\overline{\text{MUT}}$	*	CLS	READ-WRITE CODEC CONTROL REGISTER (CCR1) ADDRESS $FFC8
7	6	5	4	3	2	1	0	
CLB	*	*	*	VC3	VC2	VC1	VC0	
15	14	13	12	11	10	9	8	
*	*	CRS5	CRS4	CRS3	CRS2	CRS1	CRS0	READ-WRITE CODEC CONTROL REGISTER (CCR0) ADDRESS $FFC7
7	6	5	4	3	2	1	0	
*	*	ED5	ED4	ED3	ED2	ED1	ED0	
7	6	5	4	3	2	1	0	
*	*	*	*	CRDF	CTDE	CROE	CTUE	READ-ONLY CODEC STATUS REGISTER (COSR) ADDRESS $FFE8

Note: * = reserved.

Figure 6-2 DSP56166 Codec General Block Diagram

6.4 ANALOG I/O DEFINITION

This section describes the Motorola DSP56166 Codec analog input and output characteristics (see Figure 6-3).

There are two analog inputs, MIC and AUX. Selection between MIC or AUX is made via one control bit (INS bit) and can be changed any time desired. The electrical specifications of the two pins are identical.

The analog output consists of a fully differential driver stage, with each output having an operating range of Vrda = 1.0 Vp. The output op-amp is capable of driving a load of 1 kΩ in series with 50 nF between the differential outputs.

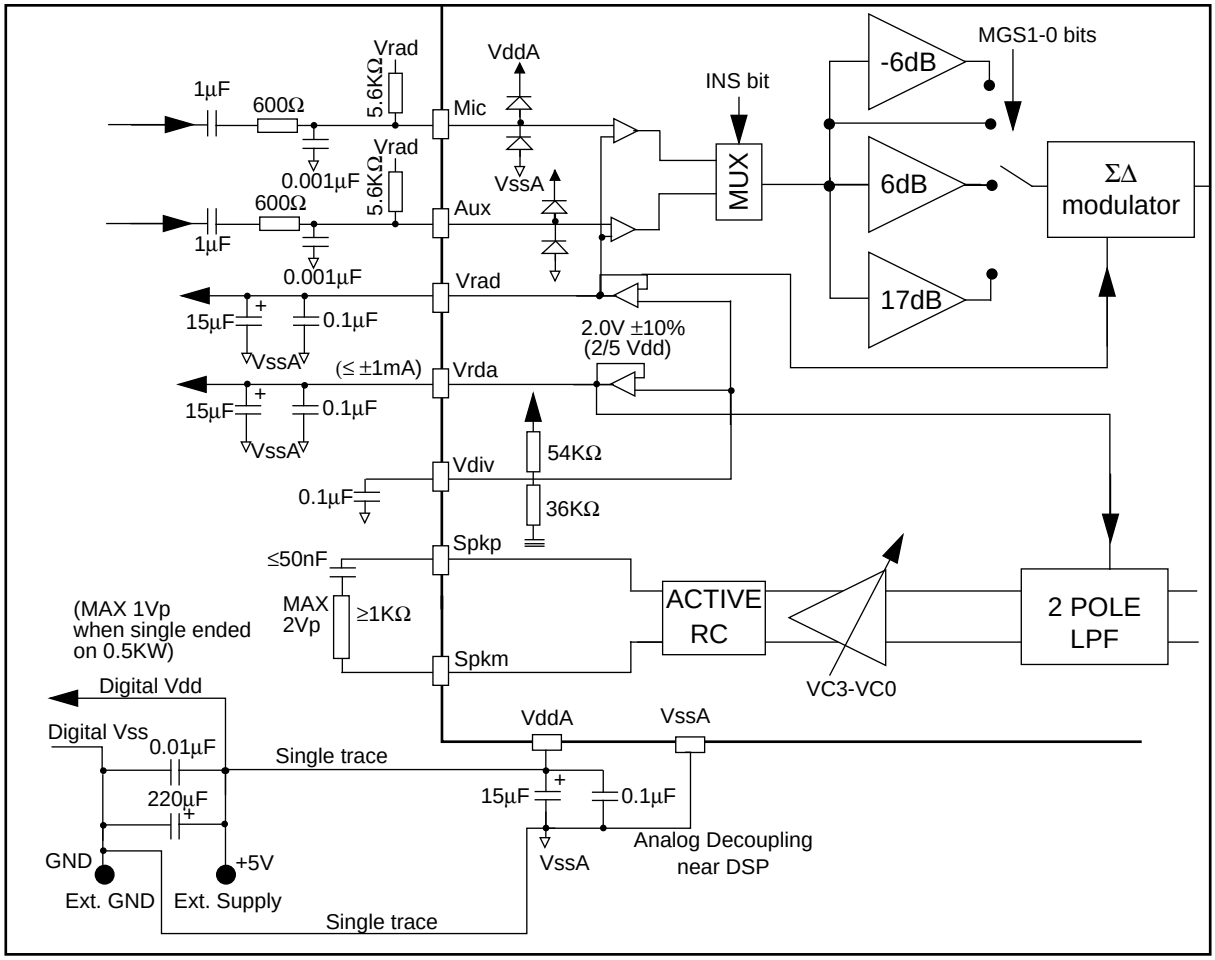


Figure 6-3 DSP56166 Codec Analog Input and Output Diagram

The reference voltages for the A/D and D/A converters are generated by two on-chip voltage references. Current bias for the opamps in the analog blocks are set by the on-chip current bias generator.

6.5 INTERFACE WITH THE DSP5616 CORE

This section discusses the use of each bit in the codec control registers.

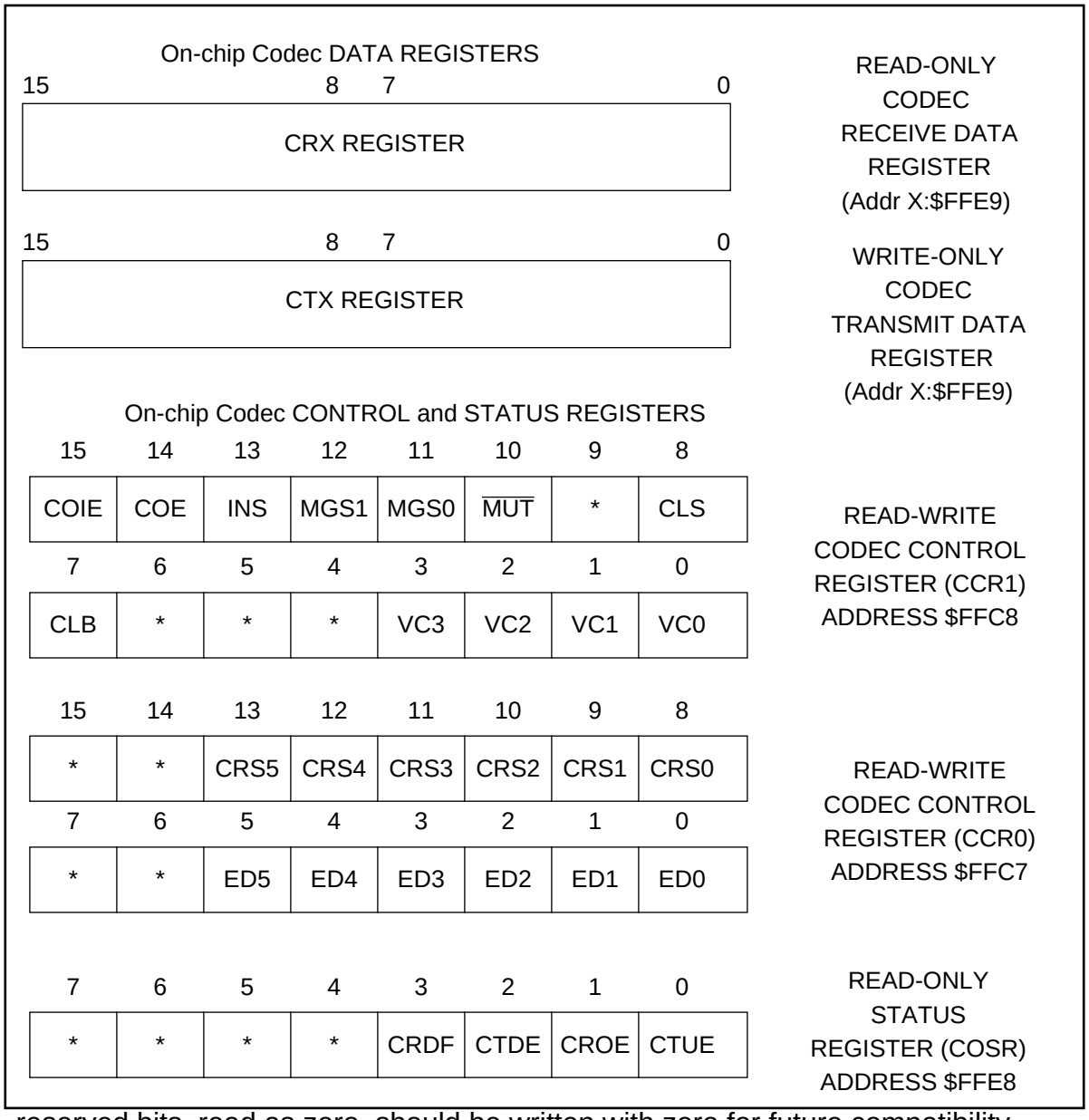
6.5.1 Interface Definition

The ∑Δ Codec is seen from the core as a memory mapped on-chip peripheral. Data memory locations are dedicated for the receive data register, transmit data register, status register, and control registers. One interrupt vector is assigned to the ∑Δ Codec.

The A/D section (receive) and the D/A section (transmit) are synchronous; that is, a common interrupt vector is used by the two sections to notify the DSP core that an input sample is to be read and/or that an output sample is to be written.

6.5.2 On-chip Codec Programming Model

Figure 6-4 shows the memory mapped registers used with the on-chip codec.There are five registers mapped into four memory locations.



* - reserved bits, read as zero, should be written with zero for future compatibility.

Figure 6-4 On-chip Codec Programming Model

6.5.3 Codec Receive Register CRX

The CRX Codec Receive register is used for A/D to DSP core data transfers. The CRX register is viewed as a 16-bit read-only register by the DSP core. The CRX register is loaded with 16-bit data from the A/D section comb filter output. This transfer operation sets the CRDF bit in the codec status register COSR. Reading CRX clears CRDF. CRDF assertion will generate an interrupt if the COIE bit is set by the user.

6.5.4 Codec Transmit Register CTX

The CTX Codec Transmit register is used for DSP core to D/A data transfers. The CTX register is viewed as a 16-bit write-only register by the DSP core. Writing the CTX register clears the CTDE bit in the codec status register COSR. CTDE assertion will generate an interrupt if the COIE bit is set by the user.

6.5.5 Codec Control Register CCR0

The Codec Control register CCR0 is a 16-bit read/write register used to direct the on-chip codec operation. The CCR0 controls the clocking scheme and decimation/interpolation ratio of the ∑Δ codec. The CCR0 bits are described in the following sections.

All of the CCR0 bits are cleared by DSP hardware and software reset.

6.5.5.1 CCR0 Input Divider Bits (ED5-ED0) Bits 0-5

The six input divider bits are used to divide the input clock to the codec by any number between 1 and 64. If ED is the value contained in the six bits, the input clock is divided by ED+1.

Care should be taken to remain in the Codec operating range between 100KHz and 3 MHz.

Note: When the CLS bit is set in the CCR1 register (PLL output selected as input clock), the value programmed in the ED divider should be greater than 1 (minimum 2) for proper codec operation.

6.5.5.2 CCR0 Codec Ratio Select Bits (CRS5-0) Bits 13-8

The Codec Ratio Select bits are used by the DSP core to program the decimation and interpolation ratio of the codec comb filter. The ratio values available are given in Figure 6-13.

Table 6-2 Decimation/Interpolation Ratio Control

CRS5-CRS0	Decimation Interpolation Ratio Rate	A/D Comb Filter DC Gain		D/A Comb Filter DC Gain	
$00	65	$4(65^3)/2^{21}$	-5.617 dB	65/128	-5.886 dB
$01	66	$4(66^3)/2^{21}$	-5.219 dB	66/128	-5.753 dB
$02	67	$4(67^3)/2^{21}$	-4.827 dB	67/128	-5.622 dB
$03	68	$4(68^3)/2^{21}$	-4.441 dB	68/128	-5.494 dB
$04	69	$4(69^3)/2^{21}$	-4.060 dB	69/128	-5.367 dB
$05	70	$4(70^3)/2^{21}$	-3.686 dB	70/128	-5.242 dB
$06	71	$4(71^3)/2^{21}$	-3.316 dB	71/128	-5.119 dB
$07	72	$4(72^3)/2^{21}$	-2.951 dB	72/128	-4.998 dB
$08	73	$4(73^3)/2^{21}$	-2.592 dB	73/128	-4.877 dB
$09	74	$4(74^3)/2^{21}$	-2.237 dB	74/128	-4.759 dB
$0A	75	$4(75^3)/2^{21}$	-1.887 dB	75/128	-4.643 dB
$0B	76	$4(76^3)/2^{21}$	-1.542 dB	76/128	-4.527 dB
$0C	77	$4(77^3)/2^{21}$	-1.202 dB	77/128	-4.414 dB
$0D	78	$4(78^3)/2^{21}$	-0.866 dB	78/128	-4.302 dB
$0E	79	$4(79^3)/2^{21}$	-0.534 dB	79/128	-4.192 dB
$0F	80	$4(80^3)/2^{21}$	-0.206 dB	80/128	-4.082 dB
$10	81	$4(81^3)/2^{21}$	0.118 dB	81/128	-3.974 dB
$11	82	$4(82^3)/2^{21}$	0.437 dB	82/128	-3.868 dB
$12	83	$4(83^3)/2^{21}$	0.753 dB	83/128	-3.763 dB
$13	84	$4(84^3)/2^{21}$	1.065 dB	84/128	-3.659 dB
$14	85	$4(85^3)/2^{21}$	1.374 dB	85/128	-3.558 dB
$15	86	$4(86^3)/2^{21}$	1.678 dB	86/128	-3.454 dB
$16	87	$4(87^3)/2^{21}$	1.980 dB	87/128	-3.354 dB
$17	88	$4(88^3)/2^{21}$	2.277 dB	88/128	-3.254 dB
$08 $09	72 73	$125^3/2^{21}$ 1	-0.618 dB 0 dB	125/128 1	-0.206 dB 0 dB
$0A	74	$2(105^3)/2^{21}$	0.859 dB	105/128	-1.720 dB
$0B	75	$2(81^3)/2^{21}$	0.118 dB	81/128	-3.974 dB
$0C $0D	76 77	$125^3/2^{21}$ 1	-0.618 dB 0 dB	125/128 1	-0.206 dB 0 dB
$0E	78	$2(105^3)/2^{21}$	0.859 dB	105/128	-1.720 dB
$0F	79	$2(81^3)/2^{21}$	0.118 dB	81/128	-3.974 dB

Table 6-2 Decimation/Interpolation Ratio Control - continued

CRS5-CRS0	Decimation Interpolation Ratio Rate	A/D Comb Filter DC Gain		D/A Comb Filter DC Gain	
$18	89	$2(89^3)/2^{21}$	-3.449 dB	89/128	-3.156 dB
$19	90	$2(90^3)/2^{21}$	-3.157 dB	90/128	-3.059 dB
$1A	91	$2(91^3)/2^{21}$	-2.869 dB	91/128	-2.963 dB
$1B	92	$2(92^3)/2^{21}$	-2.584 dB	92/128	-2.868 dB
$1C	93	$2(93^3)/2^{21}$	-2.303 dB	93/128	-2.774 dB
$1D	94	$2(94^3)/2^{21}$	-2.024 dB	94/128	-2.682 dB
$1E	95	$2(95^3)/2^{21}$	-1.748 dB	95/128	-2.590 dB
$1F	96	$2(96^3)/2^{21}$	-1.476 dB	96/128	-2.499 dB
$20	97	$2(97^3)/2^{21}$	-1.206 dB	97/128	-2.409 dB
$21	98	$2(98^3)/2^{21}$	-0.938 dB	98/128	-2.320 dB
$22	99	$2(99^3)/2^{21}$	-0.674 dB	99/128	-2.231 dB
$23	100	$2(100^3)/2^{21}$	-0.412 dB	100/128	-2.144 dB
$24	101	$2(101^3)/2^{21}$	-0.153 dB	101/128	-2.058 dB
$25	102	$2(102^3)/2^{21}$	0.104 dB	102/128	-1.972 dB
$26	103	$2(103^3)/2^{21}$	0.358 dB	103/128	-1.887 dB
$27	104	$2(104^3)/2^{21}$	0.610 dB	104/128	-1.804 dB
$28	105	$2(105^3)/2^{21}$	0.859 dB	105/128	-1.720 dB
$29	106	$2(106^3)/2^{21}$	1.106 dB	106/128	-1.638 dB
$2A	107	$2(107^3)/2^{21}$	1.351 dB	107/128	-1.556 dB
$2B	108	$2(108^3)/2^{21}$	1.593 dB	108/128	-1.476 dB
$2C	109	$2(109^3)/2^{21}$	1.833 dB	109/128	-1.396 dB
$2D	110	$2(110^3)/2^{21}$	2.072 dB	110/128	-1.316 dB
$2E	111	$2(111^3)/2^{21}$	2.307 dB	111/128	-1.238 dB
$2F	112	$2(112^3)/2^{21}$	2.541 dB	112/128	-1.160 dB
$30	113	$(113^3)/2^{21}$	-3.248 dB	113/128	-1.083 dB
$31	114	$(114^3)/2^{21}$	-3.018 dB	114/128	-1.006 dB
$32	115	$(115^3)/2^{21}$	-2.791 dB	115/128	-0.930 dB
$33	116	$(116^3)/2^{21}$	-2.565 dB	116/128	-0.855 dB
$34	117	$(117^3)/2^{21}$	-2.341 dB	117/128	-0.780 dB
$35	118	$(118^3)/2^{21}$	-2.120 dB	118/128	-0.707 dB
$36	119	$(119^3)/2^{21}$	-1.820 dB	119/128	-0.633 dB
$37	120	$(120^3)/2^{21}$	-1.682 dB	120/128	-0.561 dB
$38	121	$(121^3)/2^{21}$	-1.465 dB	121/128	-0.488 dB
$39	122	$(122^3)/2^{21}$	-1.251 dB	122/128	-0.417 dB
$3A	123	$(123^3)/2^{21}$	-1.039 dB	123/128	-0.346 dB
$3B	124	$(124^3)/2^{21}$	-0.827 dB	124/128	-0.258 dB
$3C	125	$(125^3)/2^{21}$	-0.618 dB	125/128	-0.206 dB
$3D	126	$(126^3)/2^{21}$	-0.410 dB	126/128	-0.137 dB
$3E	127	$(127^3)/2^{21}$	-0.204 dB	127/128	-0.068 dB
$3F	128	1	0 dB	1	0 dB

As shown in Figure 6-13, the value selected as decimation and interpolation ratio also affects the DC gain of the comb filter in the A/D and D/A sections. The global DC gain of the A/D and D/A sections is discussed in detail in Section 6.6.

6.5.5.3 CCR0 Reserved Bits 6-7 and 14-15

These bits are reserved. They should be written as zero by the user program to insure future compatibility.

6.5.6 Codec Control Register CCR1

The Codec Control Register CCR1 is a 16-bit read/write register used to direct the operation of the on-chip codec. The CCR1 controls the receive and transmit audio gains, the codec clocking source, the selection of the analog input, the muting of the analog output, the codec power down, the codec enable, and the codec interrupt enable. The CCR1 bits are described in the following sections.

All of the CCR1 bits are cleared by DSP hardware and software reset.

6.5.6.1 CCR1 Audio Level Control Bits (VC3-VC0) Bits 0-3

Audio gain control is employed in the last stage of the on-chip codec D/A section. Bits VC0-VC3 control the volume between -15 dB and 40 dB as shown in Figure 6-13.

Table 6-3 Audio Level Control

VC3	VC2	VC1	VC0	Relative Level in dB
0	0	0	0	-15
0	0	0	1	-10
0	0	1	0	-5
0	0	1	1	0
0	1	0	0	5
0	1	0	1	11
0	1	1	0	17
0	1	1	1	23
1	0	0	0	5
1	0	0	1	11
1	0	1	0	17
1	0	1	1	23
1	1	0	0	29
1	1	0	1	35
1	1	1	0	35
1	1	1	1	40

A 16-bit full scale positive value of $7FFF written to the D/A should produce a voltage level equal to Vrda = +1Vp singled-ended and Vrda = +2Vp differential at the output when the volume control bits VC3-VC0 are set to the level of 0 dB and when the DC gain of the D/A comb filter is unity (decimation ratio of 128).

The digital reconstruction-interpolation filter performed by the DSP core can also be used to control the output audio level in conjunction with the four VC3-VC0 bits. The gain of this filter can be adjusted in order to modify the relative level and the step between levels. Table 6-4 gives an example where the gain of the interpolation digital filter is adjusted in order to provide output volume control between -15dB and +40dB in 5dB steps.

Table 6-4 Audio Level Control with DSP Filter Gain

VC3	VC2	VC1	VC0	Relative Level dB	Digital Filter Gain	Final Output Level
0	0	0	0	-15	0	-15
0	0	0	1	-10	0	-10
0	0	1	0	-5	0	-5
0	0	1	1	0	0	0
0	1	0	0	5	0	5
0	1	0	1	11	-1	10
0	1	1	0	17	-2	15
0	1	1	1	23	-3	20
1	0	0	0	5	0	5
1	0	0	1	11	-1	10
1	0	1	0	17	-2	15
1	0	1	1	23	-3	20
1	1	0	0	29	-4	25
1	1	0	1	35	-5	30
1	1	1	0	35	0	35
1	1	1	1	40	0	40

6.5.6.2 CCR1 Codec Loop Back Bit (CLB) Bit 7

The Codec Loop Back Bit selects the input to the analog back end of the DAC. This bit is cleared for normal DAC operation. When CLB is set, the output of the A/D ∑Δ analog modulator is used as input to the analog back end of the DAC, as shown in Figure 6-2.

6.5.6.3 CCR1 Clock Select Bit (CLS) Bit 8

This bit is used to select the source of the codec clock. When the CLS bit is cleared, the squared version of Fext is selected as the codec clock input. When this bit is set, the codec input clock is derived from the PLL output, as shown in Figure 6-2.

Note: When CLS is set, the value programmed in the ED divider should be greater than one (minimum two) for proper codec operation.

6.5.6.4 CCR1 Mute Bit ($\overline{\text{MUT}}$) Bit 10

The mute bit is used to mute the output signal. When the $\overline{\text{MUT}}$ bit is cleared, the output signal is muted. When the $\overline{\text{MUT}}$ bit is set, the output signal is not muted.

6.5.6.5 CCR1 Microphone Gain Select Bits (MGS1-0) Bits 11 and 12

The Microphone Gain Select Bits are used by the DSP core to program the analog input gain. The values are given in Table 6-5. The analog modulator is guaranteed to be linear up to 3 dB below full scale saturation values. The full scale saturation analog value results in a maximum digital A/D output ($7FFF) when the A/D comb filter has a DC unity gain.

Table 6-5 Microphone Gain Control

MGS1	MGS0	Gain		Modulator full scale	Full scale linearity
		Actual	dB		
0	0	0.5	-6	2 Vp	1.414 Vp
0	1	1	0	1 Vp	0.707 Vp
1	0	2	6	500 mVp	354 mVp
1	1	7.07	17	141 mVp	100 mVp

6.5.6.6 CCR1 Input Select Bit (INS) Bit 13

The input select bit is used by the DSP to select between the two inputs — MIC and AUX. When INS is cleared, MIC is selected and when INS is set, the AUX input is selected.

6.5.6.7 CCR1 Codec Enable Bit (COE) Bit 14

The Codec Enable Bit enables the on-chip codec section. When this bit is cleared, the section is disabled and put in the power down mode. Setting the bit wakes-up and enables the on-chip codec section.

6.5.6.8 CCR1 Codec Interrupt Enable Bit (COIE) Bit 15

The Codec Interrupt Enable Bit enables the on-chip codec interrupt. When this bit is cleared the interrupt is disabled. Setting the bit enables the interrupt.

6.5.6.9 CCR1 Reserved Bits 4,5,6, and 9

These bits are reserved. They should be written as zero by the user program to insure future compatibility.

6.5.7 Codec Status Register COSR

The Codec Status Register COSR is an 8-bit read-only status register used by the DSP to interrogate the status and flags of the on-chip codec. The status bits and flag bits are described in the following paragraphs.

6.5.7.1 COSR Codec Transmit Underrun Error FLag Bit (CTUE) Bit 0

The Codec Transmit Underflow Error Flag Bit is set when a sample has to be transmitted to the codec section while the DSP has not yet written to the CTX transmit register (underrun error). In this case, the previous sample written to the CTX register is re-transmitted to the D/A section.

Hardware or software reset and the STOP instruction clear CTUE. CTUE is also cleared by reading the COSR with CTUE set followed by writing CTX. Clearing the COE bit in the Codec Control Register CCR1 does not affect CTUE.

6.5.7.2 COSR Codec Receive Overrun Error Flag Bit (CROE) Bit 1

The Codec Receive Overrun Error Flag bit is set when a new sample is received from the codec section while the previous received sample in the CRX receive register has not been read by the DSP (overrun error). In this case, the previous received sample is overwritten in the CRX register.

Hardware or software reset and the STOP instruction clear CROE. CROE is also cleared by reading the COSR with CROE set followed by reading CRX. Clearing the COE bit in the Codec Control Register CCR1 does not affect CTUE.

6.5.7.3 COSR Codec Transmit Data Empty Bit (CTDE) Bit 2

The Codec Transmit Data Empty (CTDE) bit indicates that the D/A Transmit register CTX is empty and can be written by the DSP. CTDE is set when the CTX register is transferred to the D/A comb filter input. CTDE is cleared when the CTX register is written by the DSP. CTDE is also set entering the codec power down mode (COE cleared) and by a DSP reset (Hardware $\overline{\text{RESET}}$ or RESET instruction) and the STOP instruction.

6.5.7.4 COSR Codec Receive Data Full Bit (CRDF) Bit 3

The Codec Receive Data Full (CRDF) bit indicates that the A/D Data Receive register CRX contains data from the codec A/D section. CRDF is set when data is transferred from the A/D comb filter output to the CRX register. CRDF is cleared when the CRX Register is read by the DSP. CRDF is also cleared entering the Codec power down mode (COE cleared), by a DSP reset (Hardware $\overline{\text{RESET}}$ or RESET instruction) and the STOP instruction.

6.5.7.5 COSR Reserved Bits 4-15

These bits are reserved. They will be read as zeros by the user program.

On-chip Codec Status Registers (COSR X:$FFE8)

7	6	5	4	3	2	1	0
*	*	*	*	CRDF	CTDE	CROE	CTUE

CRDF (read-only)	0	Data From A/D not received in CRX
	1	Data From A/D received in CRX
CTDE (read-only)	0	Data in CTX has not been transferred to D/A
	1	CTX empty
CROE (read-only)	0	No Receive Overrun Error
	1	Receive Overrun Error
CTUE (read-only)	0	No Transmit Underrun Error
	1	Transmit Underrun Error

On-chip Codec Control (CCR1) X:$FFC8

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

COIE	0	Codec interrupt disabled			
	1	Codec interrupt enabled			
COE	0	Codec disabled and put in power down			
	1	Codec enabled			
INS	0	MIC pin selected as A/D input			
	1	AUX pin selected as A/D input			
MGS1-0 Gain Select	00	MIC or AUX amplifier gain of -6dB	10	MIC or AUX amplifier gain of 6dB	
	01	MIC or AUX amplifier gain of 0dB	11	MIC or AUX amplifier gain of 17dB	
$\overline{\text{MUT}}$	0	Speaker output muted			
	1	Speaker output active			
CLS	0	Squared Fext selected as codec input clock			
	1	PLL block output selected as codec input clock			
CLB	0	Normal Codec operation			
	1	The input of the D/A digital ∑Δ modulator is the output of the A/D ∑Δ modulator			
VC3VC0 D/A output Gain in dB	$0	-15 dB Output volume gain	$8	5 dB Output volume gain	
	$1	-10 dB Output volume gain	$9	11 dB Output volume gain	
	$2	-5 dB Output volume gain	$A	17 dB Output volume gain	
	$3	0 dB Output volume gain	$B	23 dB Output volume gain	
	$4	5 dB Output volume gain	$C	29 dB Output volume gain	
	$5	11 dB Output volume gain	$D	35 dB Output volume gain	
	$6	17 dB Output volume gain	$E	35 dB Output volume gain	
	$7	23 dB Output volume gain	$F	40 dB Output volume gain	

On-chip Codec Control (CCR0) X:$FFC7

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

CRS0-5	$0-$3F	Continuous ratio from 65 to 128 (see Figure 6-13)	ED0-5	$0-$3F	Codec Clock Division from 1 to 64

Figure 6-5 On-Chip Codec Programming Model Summary

6.6 ON-CHIP CODEC GAIN AND FREQUENCY RESPONSE ANALYSIS

This section discusses the DC gain and the frequency response of the A/D and D/A blocks as a function of the decimation and interpolation ratios.

6.6.1 DC Gain and Frequency Response of the A/D Section

The DC gain and the frequency response of the A/D comb filter depends on the decimation rates selected by programming the six bits CRS5-CRS0 in the codec control register CCR0. The decimation rate can take any values between 65 and 128. A negative DC gain is introduced by scaling inside the comb filter in order to avoid any signal clipping caused by a positive DC gain of the comb filter itself. The A/D comb filter gains are given in Figure 6-13.

The digital output level out of the A/D section can be normalized to 0 dB or to any other value by changing the gain of the last decimation/antialiasing filter performed by the DSP core program. In addition to filtering and decimating, this last digital filter can also compensate the frequency response of the A/D comb filter.

The comb filter is a linear phase filter constructed as a cascade of digital integrators and differentiators which realizes the transfer function and frequency response of Figure 6-13.

$$H(z) = \frac{c}{128^3}\left[\frac{1 - z^{-D}}{1 - z^{-1}}\right]^3$$

$$F(f) = \frac{c}{128^3}\left(\frac{\sin\left(\frac{2\pi D}{2F} \times f\right)}{\sin\left(\frac{2\pi}{2F} \times f\right)}\right)^3$$

c=4 for D=[65,88]
c=2 for D=[89,112]
c=1 for D=[112,128]
D: decimation ratio
F: ∑Δ modulator clock

Figure 6-6 A/D Comb Filter Transfer Function

The cubic power is due to the order. The comb filter is ideal for decimation applications because it has zeros at the final output clock rate and all its multiples.

Figure 6-7 and Figure 6-8 show an example of the log magnitude response of the A/D comb filter using a master clock of 2.048 MHz and a decimation ratio of D=128.

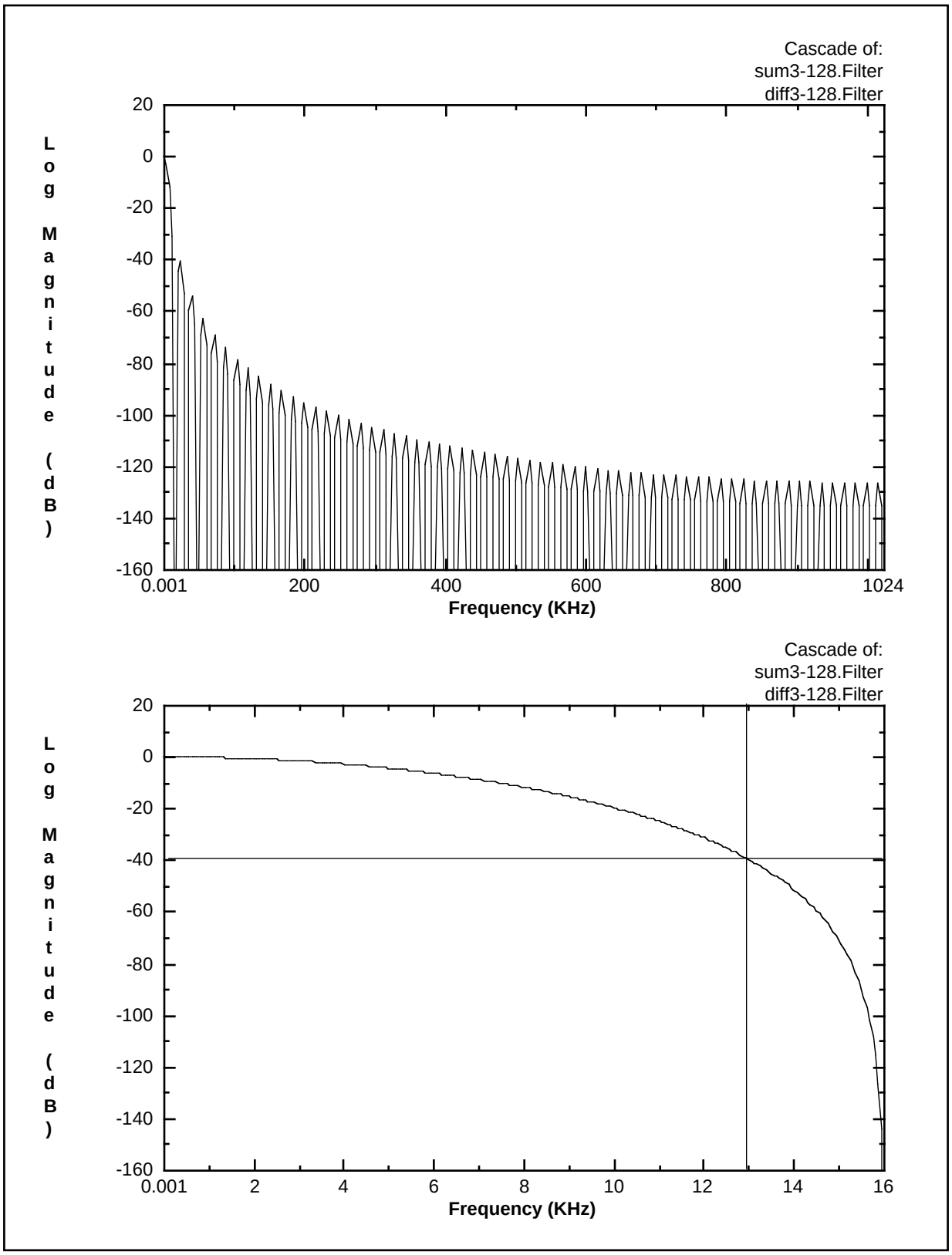


Figure 6-7 Log Magnitude Frequency Response of the A/D Comb Filter for F=2.048 MHz and D=128

These figures show the frequency response in the 0-1.024 MHz band and also the frequency response after decimation in the 0-16KHz and 0-4KHz bands.

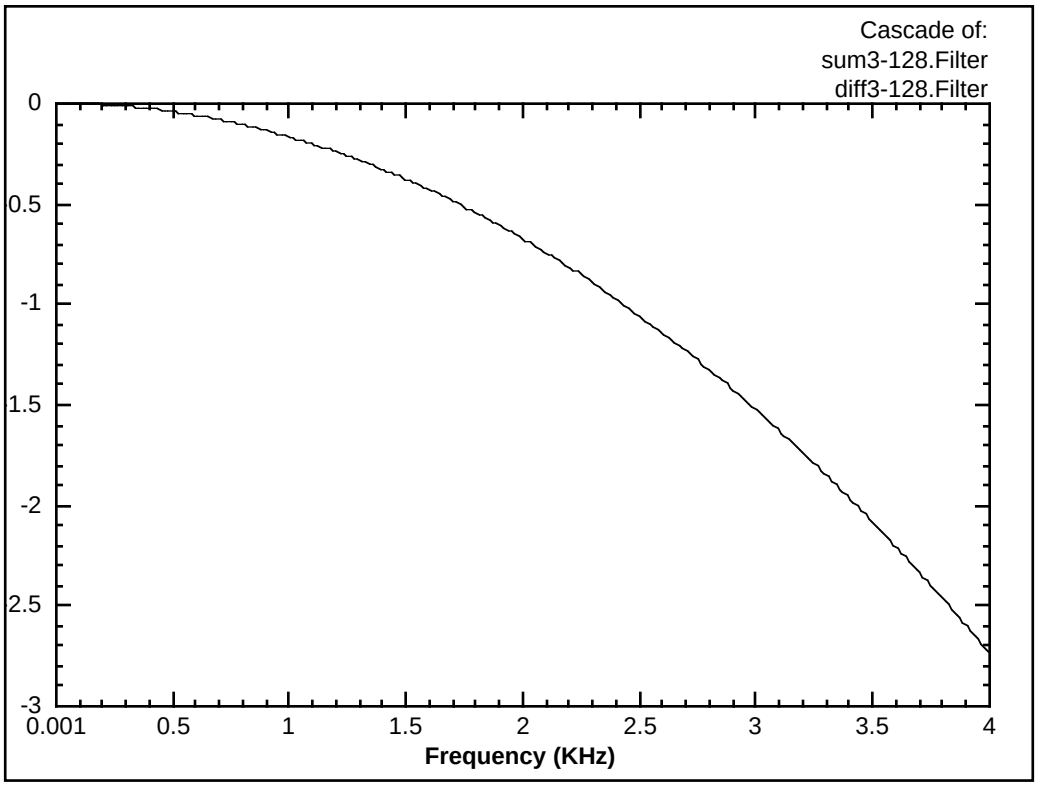


Figure 6-8 Log Magnitude Frequency Response of the A/D Comb Filter in the Band 0-4KHz for F=2.048 MHz and D=128

The output of the decimating comb filter is a 2's complement 16-bit word at the decimated rate which goes to the DSP core. It is hard limited to the range $8000-$7FFF to prevent roll over error. Figure 6-8 gives the frequency response of the A/D section in the 0-4KHZ band. It can be seen that this response is not flat in the band. The 3 dB drop-off can be compensated by the decimation filter inside the DSP core. The transfer function of the A/D comb is given on Figure 6-13

It is equal to:

$$F(f) = \frac{c}{128^3}\left(\frac{\sin\left(\frac{2\pi D}{2F}\times f\right)}{\sin\left(\frac{2\pi}{2F}\times f\right)}\right)^3$$

In the present example, D=128, c=1 and F=2.048 MHz, which gives:

$$F(f) = \frac{1}{(128)^3}\left(\frac{\sin\left(\frac{2\pi \times 128}{2 \times 2.048} \times f\right)}{\sin\left(\frac{2\pi}{2 \times 2.048} \times f\right)}\right)^3$$

The transfer function of the decimation filter will have to be shaped by 1/F(f) in order to flatten the response of the A/D section.

Table 6-6 gives a 4 biquad IIR low pass filter who's transfer function has been shaped accordingly.

Figure 6-9 shows the frequency response of the filter and the effects on the overall response of the D/A section.

Table 6-6 Example of a Four Biquad IIR Decimation and Compensation Filter

```
; Source filter file: "adcomp128.IIR.Filter"

_filter_type    equ     BIQUAD_FILTER_TYPE

_NSTAGES        equ     4               ; number of stages

                dc      $02b2           ; gain = 0.04211689868/2
                ; Biquad stage no. 1
                dc      -$1237          ; d2_1 = 0.284627003/2
                dc      $e93c           ; d1_1 = -0.3557032662/2
                dc      $316a           ; n2_1 = 0.7720730807/2
                dc      $4186           ; n1_1 = 1.023796768/2
                ; Biquad stage no. 2
                dc      -$28f8          ; d2_2 = 0.6401634264/2
                dc      $e8df           ; d1_2 = -0.3613604173/2
                dc      $0d0c           ; n2_2 = 0.2038857781/2
                dc      $12dc           ; n1_2 = 0.2946510536/2
                ; Biquad stage no. 3
                dc      -$0c66          ; d2_3 = 0.1937047354/2
                dc      $d60d           ; d1_3 = -0.6554721197/2
                dc      $3454           ; n2_3 = 0.8176134701/2
                dc      $4328           ; n1_3 = 1.049344022/2
                ; Biquad stage no. 4
                dc      -$3951          ; d2_4 = 0.8955455145/2
                dc      $f4e3           ; d1_4 = -0.1736521771/2
                dc      $2ed3           ; n2_4 = 0.7316442217/2
                dc      $1b24           ; n1_4 = 0.42404578/2
```

NOTE: This filter, as well as all the figures representing filter responses, has been generated using ZOLA Technologies, Inc., DSP Designer™ software package.

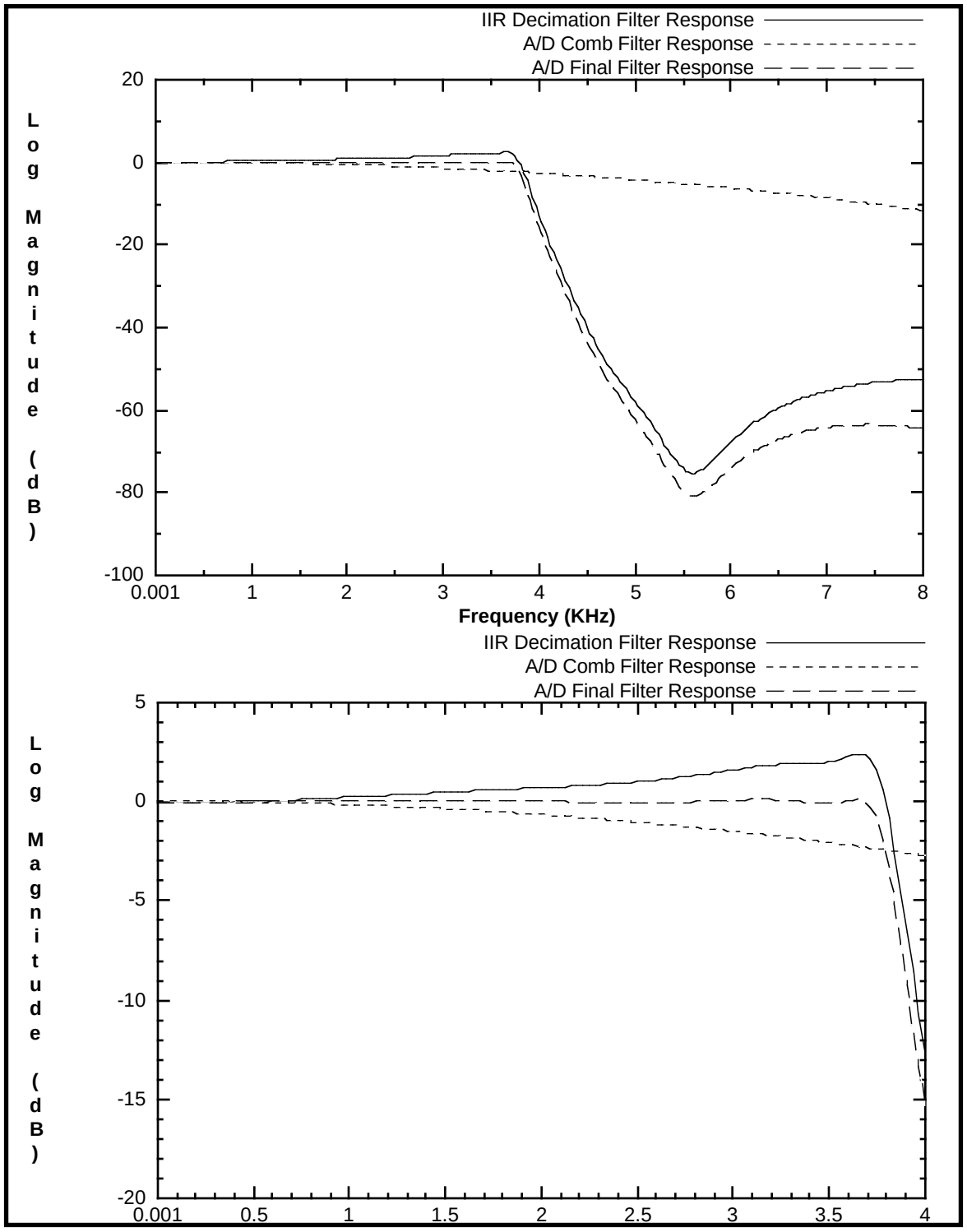


Figure 6-9 IIR Decimation and A/D Section Log Magnitude Frequency Response for F=2.048 MHz and D=128

6.6.2 DC Gain and Frequency Response of the D/A Section

The DC gain and the frequency response of the D/A section depend on the interpolation rates selected by programming the six bits CRS5-CRS0 in the codec control register CCR0. The interpolation rate can take any value between 65 and 128.

The D/A comb filter gains are given in Figure 6-13.

The D/A section of the on-chip codec is composed of three subsections which are described below.

The frequency responses of the different sections of the D/A are illustrated in Figure 6-10.

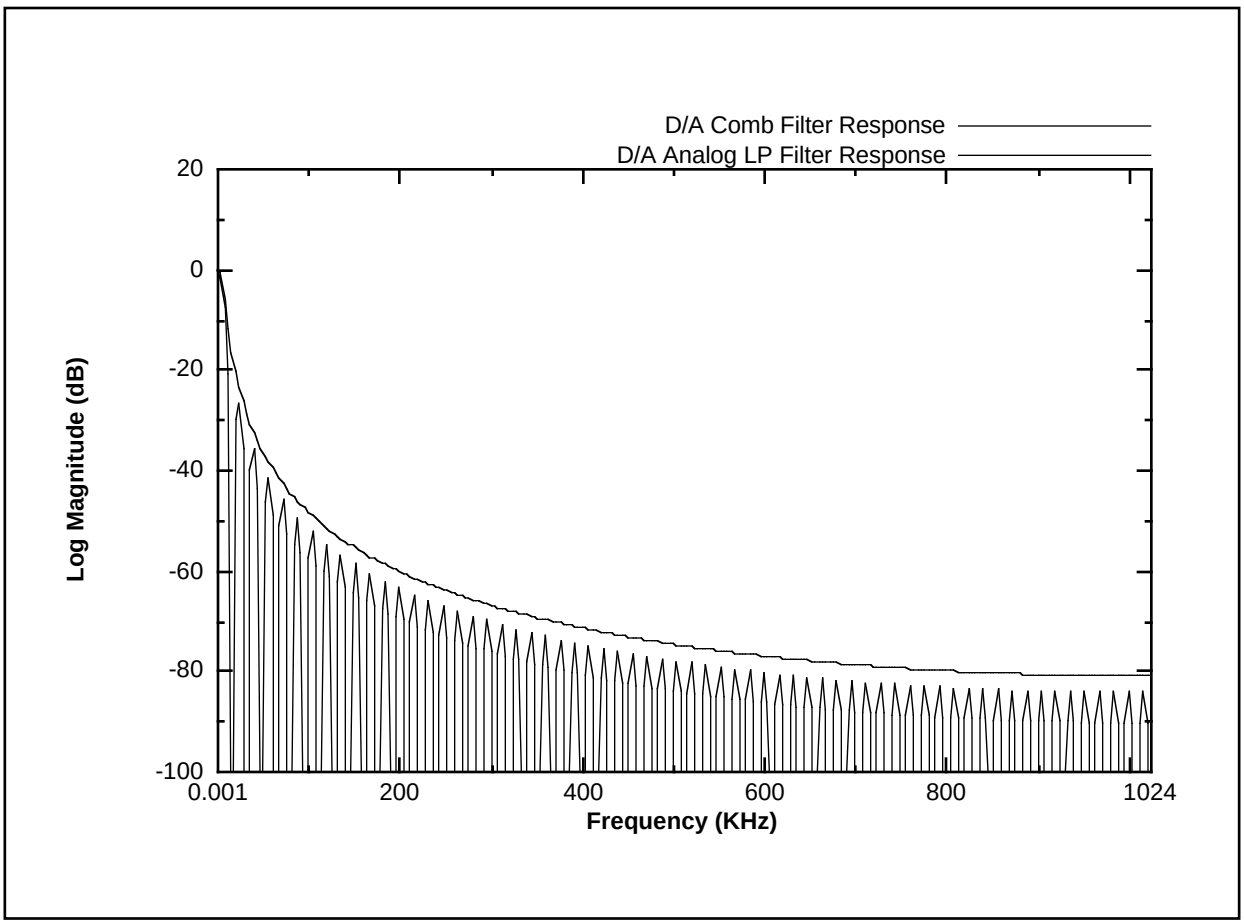


Figure 6-10 Log Magnitude Frequency Responses of the Three Sections of the D/A F=2048 MHz and D=128

6.6.2.1 D/A Second Order Digital Interpolation Comb Filter

The parallel interface of the D/A section receives a 2's complement 16-bit word from the DSP core at the initial data rate. The interpolating comb filter is a second order digital

comb filter. It is a linear phase filter that provides interpolation and anti-imaging on the input to the digital modulator. The comb filter is constructed as a sample and hold stage followed by a cascade of a digital differentiator and integrator which realizes the transfer function and the frequency response given in Figure 6-11.

$$H(z) = \frac{1}{128D}\left[\frac{1 - z^{-D}}{1 - z^{-1}}\right]^2$$

$$F(f) = \frac{1}{128D}\left(\frac{\sin\left(\frac{2\pi D}{2F} \times f\right)}{\sin\left(\frac{2\pi}{2F} \times f\right)}\right)^2$$

D: interpolation ratio
F: comb filter integrator clock

Figure 6-11 D/A Comb Filter Transfer Function

The power of two is due to the order of the filter. The comb filter is ideal for interpolation applications because it has zeros at the initial data rate and all its multiples.

Figure 6-12 shows an example of the log magnitude response of the D/A digital comb filter using a master clock of 2.048 MHz and a decimation ratio of D=128. The figure shows the frequency response of the comb filter in the 0-1024KHz band and also after decimation (0-16KHz).

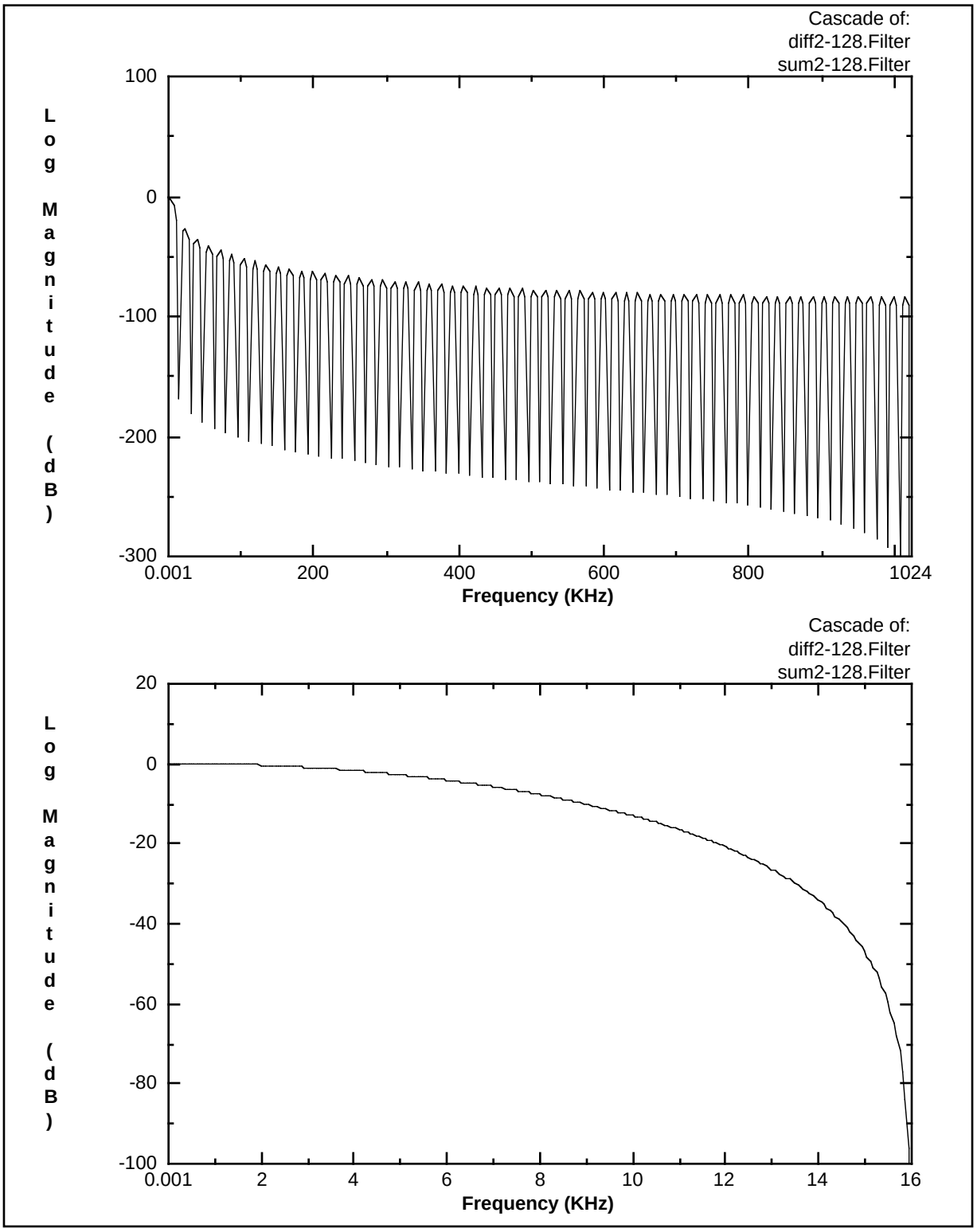


Figure 6-12 Log Magnitude Frequency Response of the D/A Comb Filter for F=2.048MHz and D=128

6.6.2.2 D/A Digital Modulator

The digital modulator is a second-order sigma-delta loop. It is made up of two digital integrators, a digital comparator, and a hard limit circuit. The output of the modulator is a 1-bit stream which contains the input signal plus a large amount of quantization noise which is shaped away from the baseband and towards the high frequencies. This 1-bit stream is then filtered by the analog low pass filter.

When the Codec Loop Back bit (CLB) of CCR1 is set, the input for the digital modulator is the output of the analog $\sum\Delta$ modulator of the A/D section.

6.6.2.3 D/A Butterworth Analog Low Pass Filter

The analog low-pass filter is a two-pole Butterworth switched capacitor filter. The purpose of this filter is to attenuate the out-of-band quantization noise and the images created by the upsampling.

Figure 6-13 gives the transfer function of the filter:

$$H(z) = \frac{(0.0003506002)}{(1 - 1.973345z^{-1} + 0.9736956z^{-2})}$$

Figure 6-13 Analog Low-pass Filter Transfer Function

Figure 6-14 shows the log magnitude response of the D/A analog low-pass filter. The figures show the frequency response of the filter in the 0-256KHz, 0-20KHz, 0-8KHz, and 0-4KHz bands.

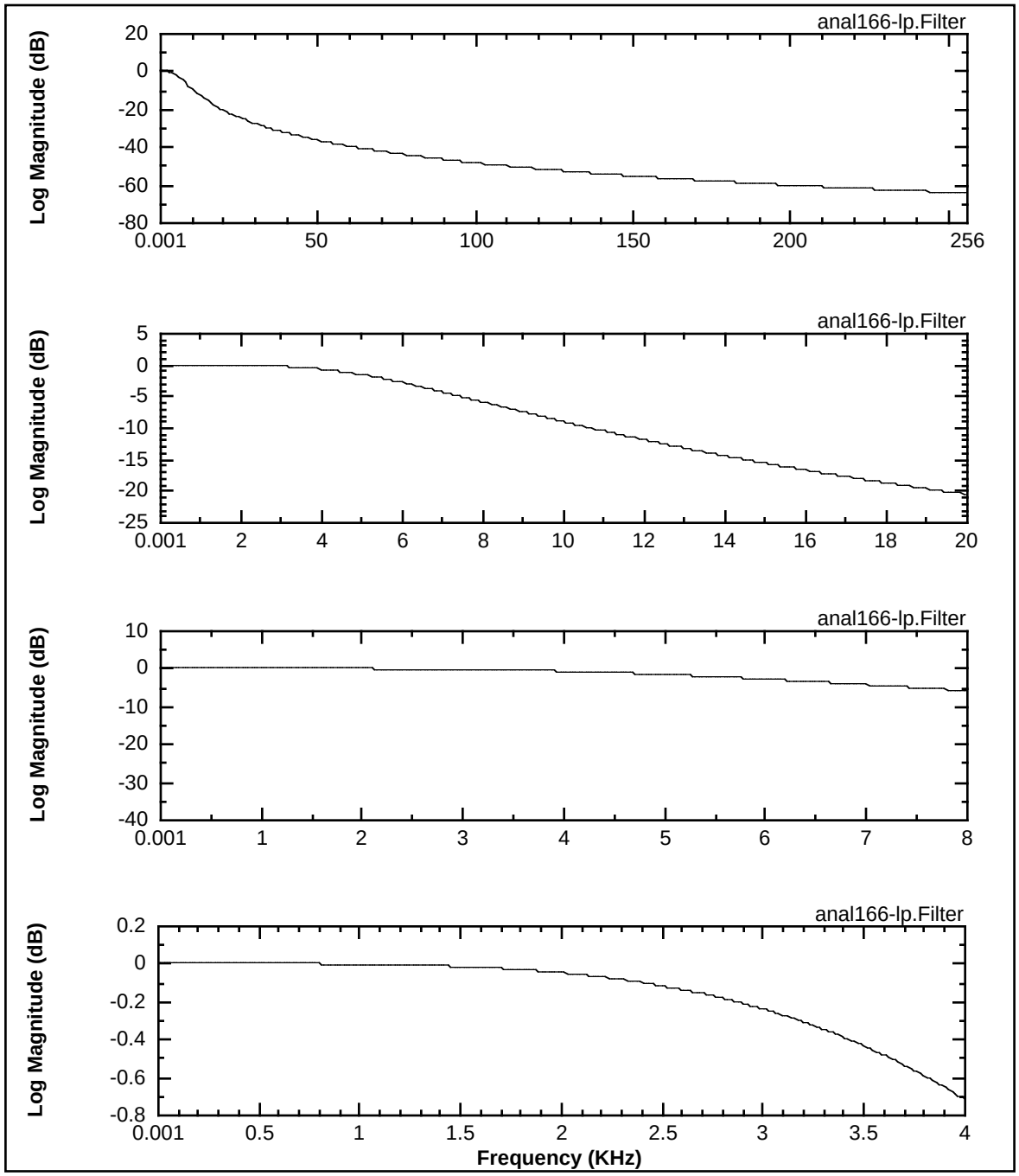


Figure 6-14 Log Magnitude Frequency Response of the D/A Analog Low-pass Filter for F=2.048MHz

6.6.2.4 Overall Frequency Response of the D/A Section

Figure 6-15 shows the D/A frequency response in the 0-128KHz band. Figure 6-16 shows the overall frequency response of the D/A section in the 0-16KHz and 0-4KHz bands.

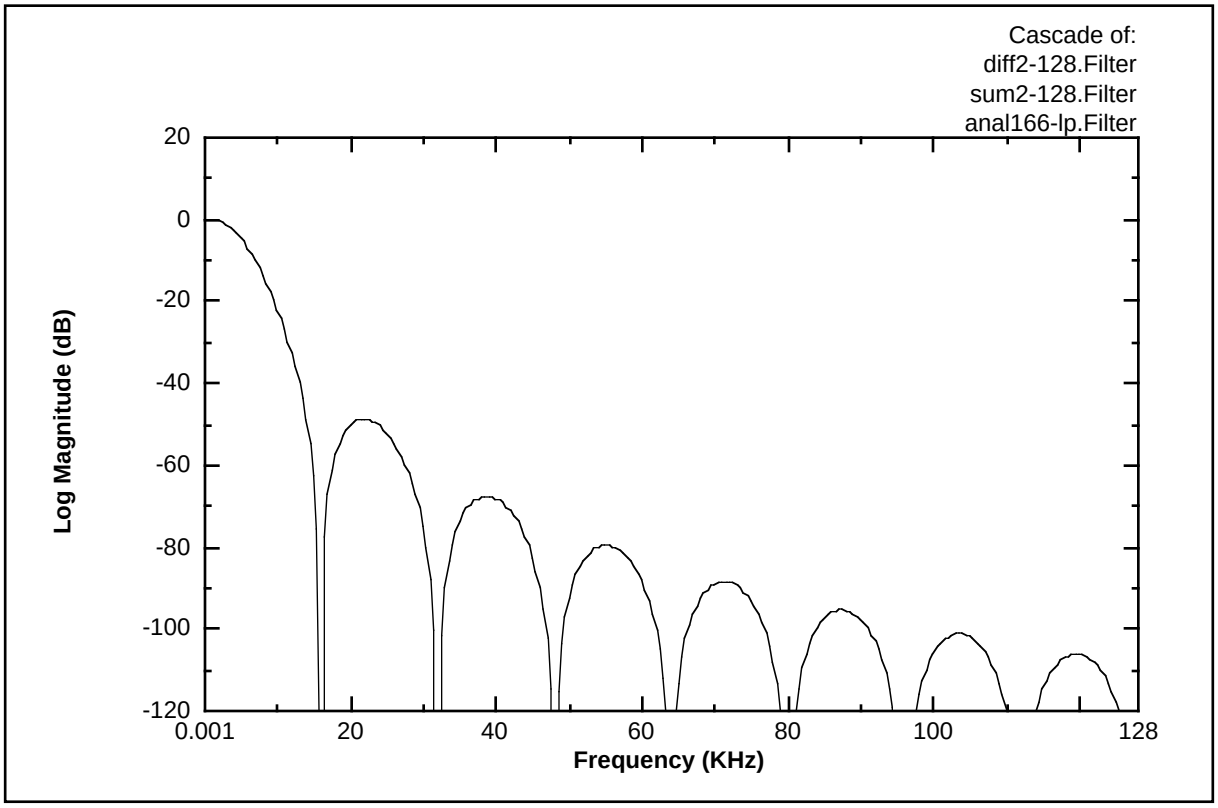


Figure 6-15 Log Magnitude Frequency Response of the D/A Section for F=2.048 MHz and D=128

It can be noted in Figure 6-16b that the frequency response is not flat in the 0-4KHz band. The interpolation filter performed by the DSP core can compensate for this droop in amplitude caused by the D/A hardware section.

The digital second order D/A comb filter is the only filter that needs to be compensated. Its transfer function is given in Figure 6-13.

It is equal to:

$$F(f) = \frac{1}{128D}\left(\frac{\sin\left(\frac{2\pi D}{2F}\times f\right)}{\sin\left(\frac{2\pi}{2F}\times f\right)}\right)^2$$

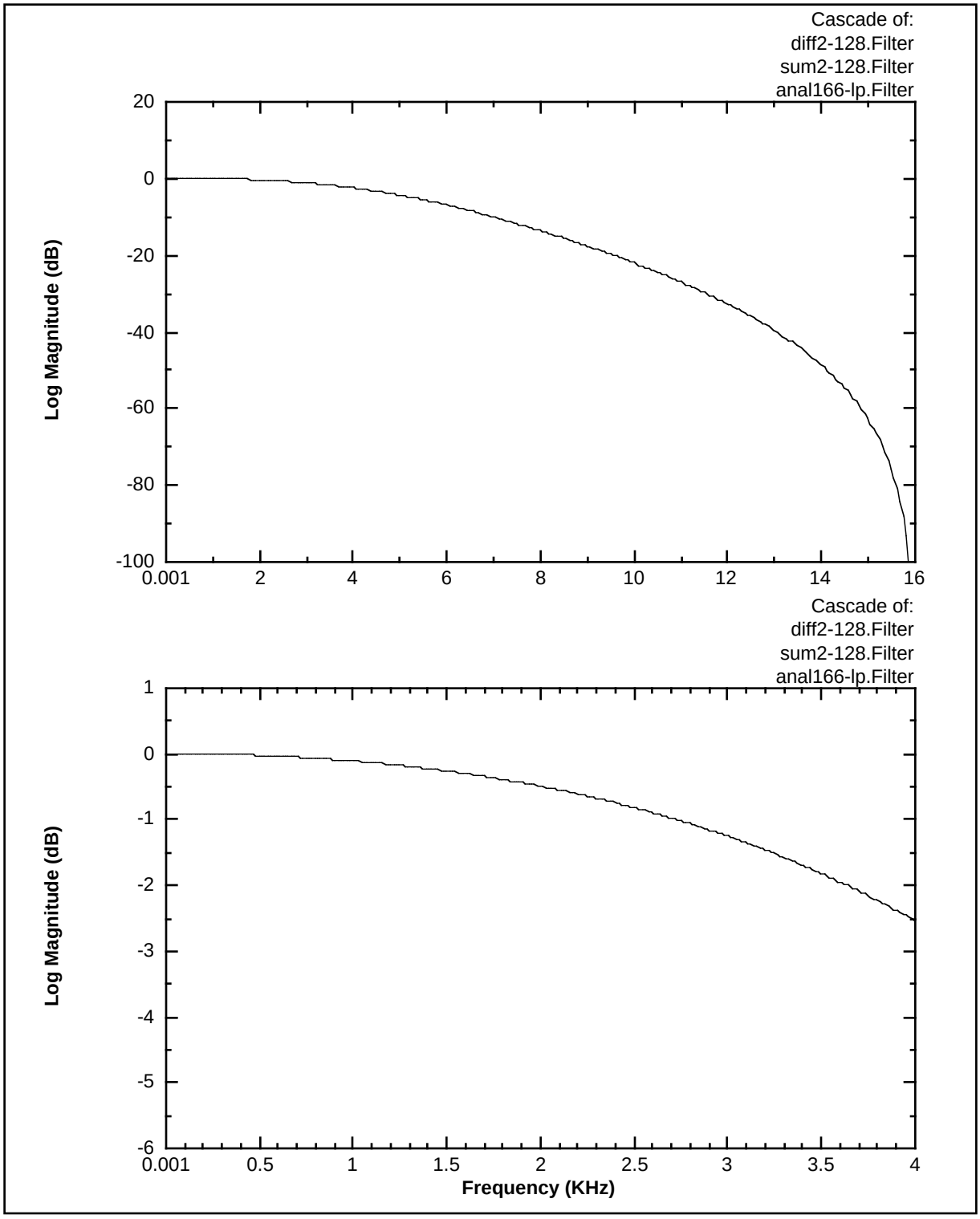


Figure 6-16 Log Magnitude Frequency Response of the D/A Section for F=2.048 MHz and D=128

In the present example, D=128 and F=2048 MHz, which gives:

$$F(f) = \frac{1}{(128)^2}\left(\frac{\sin\left(\frac{2\pi \times 128}{2 \times 2048} \times f\right)}{\sin\left(\frac{2\pi}{2 \times 2048} \times f\right)}\right)^2$$

The transfer function of the interpolation filter will have to be shaped by 1/F(f) in order to flatten the response of the D/A section.

Table 6-7 gives a 4 biquad IIR low pass filter who's transfer function has been shaped accordingly.

Figure 6-17 shows the frequency response of the filter and the effects on the overall response of the D/A section.

Table 6-7 Example of a Four Biquad IIR Interpolation and Compensation Filter

```
; Source filter file: "comp1282nd.IIR.Filter"

_filter_type    equ     BIQUAD_FILTER_TYPE
_NSTAGES        equ     4               ; number of stages

                dc      $0270           ; gain = 0.03807147513/2

                ; Biquad stage no. 1
                dc      -$18de          ; d2_1 = 0.3885309315/2
                dc      $e920           ; d1_1 = -0.3574372286/2
                dc      $329e           ; n2_1 = 0.7908895273/2
                dc      $43d3           ; n1_1 = 1.059754603/2
                ; Biquad stage no. 2
                dc      -$26b9          ; d2_2 = 0.6050537737/2
                dc      $ec15           ; d1_2 = -0.3112185033/2
                dc      $1014           ; n2_2 = 0.2512476586/2
                dc      $1146           ; n1_2 = 0.2698979411/2
                ; Biquad stage no. 3
                dc      -$0e57          ; d2_3 = 0.2240856408/2
                dc      $cf53           ; d1_3 = -0.7605800752/2
                dc      $3603           ; n2_3 = 0.8439490258/2
                dc      $4614           ; n1_3 = 1.094956692/2
                ; Biquad stage no. 4
                dc      -$38d6          ; d2_4 = 0.8880624617/2
                dc      $f59a           ; d1_4 = -0.162456827/2
                dc      $2f25           ; n2_4 = 0.7366593399/2
                dc      $1c8f           ; n1_4 = 0.4462262322/2
```

NOTE: This filter, as well as all the figures representing filter responses, has been generated using ZOLA Technologies, Inc., DSP Designer™ software package.

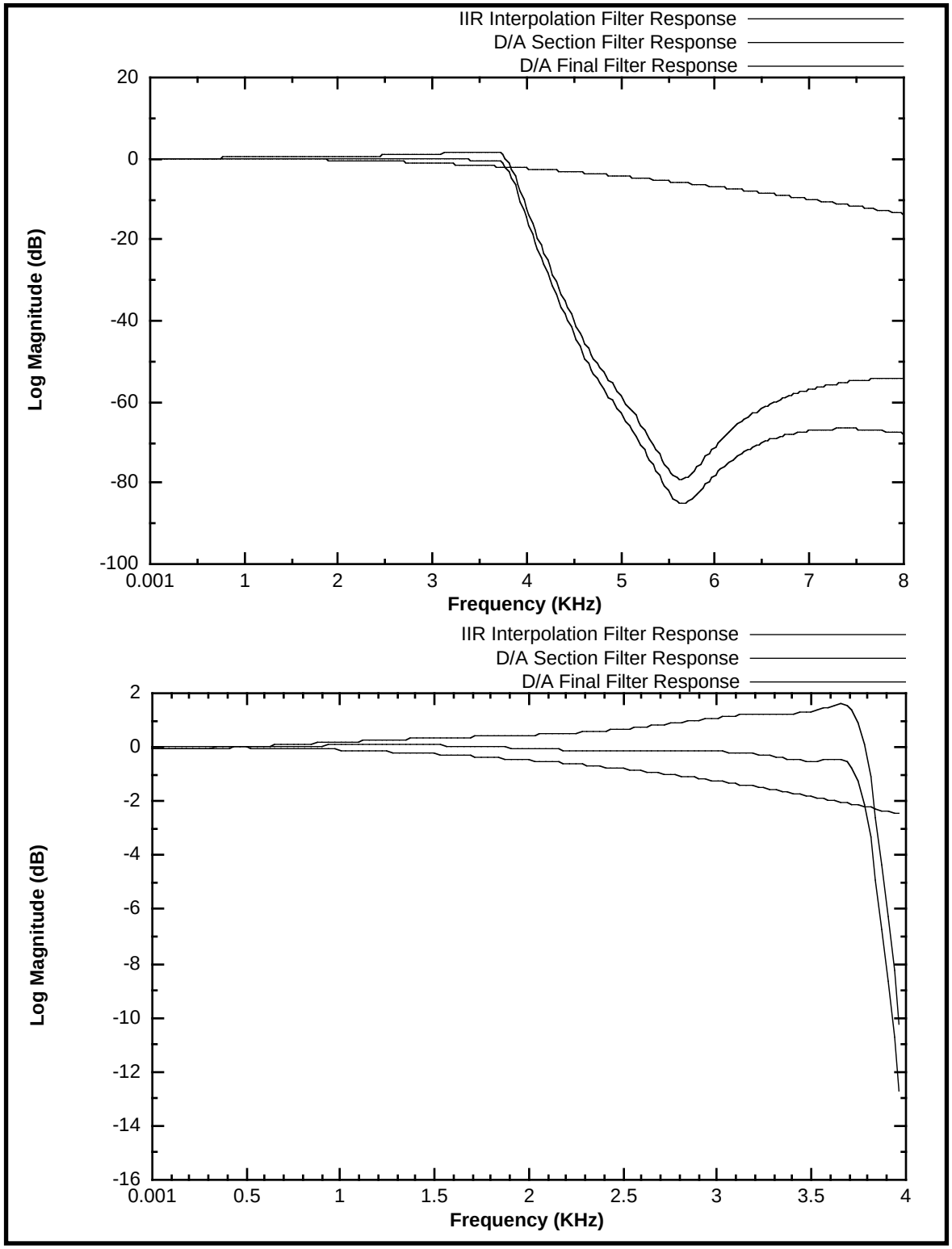


Figure 6-17 IIR Interpolation and D/A Section Log Magnitude Frequency Response for F=2.048 MHz and D=128