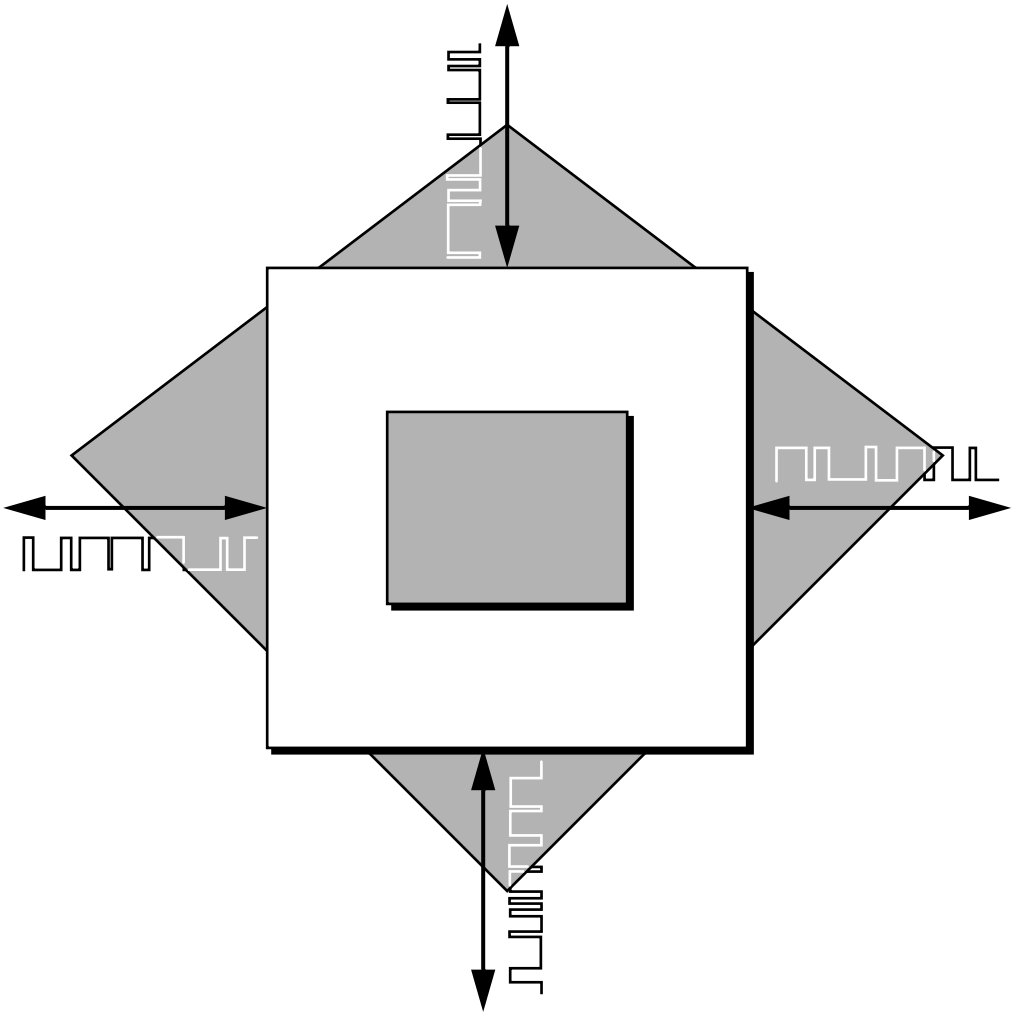
SECTION 6

GPIO



6.1 INTRODUCTION

The General Purpose I/O (GPIO) port consists of three bidirectional pins, each pin separately controlled. Functionality is controlled by the following three registers:

- GPIO Port E Control Register (PCRE)
- GPIO Port E Direction Control Register (PRRE)
- GPIO Port E Data Register (PDRE)

These registers are described in this section. This dedicated GPIO port is also referred to as Port E.

6.2 GPIO CONFIGURATION

The dedicated GPIO port on the DSP56602 supports three bidirectional pins. GPIO functionality is also available on some of the HI08, SSI, and timer pins when these pins are not otherwise being used by their peripherals. The following registers are provided for control of the three dedicated GPIO pins:

- PCRE—GPIO Port E Control Register
- PRRE— GPIO Port E Direction Control Register
- PDRE—GPIO Port E Data Register

On the peripherals that can be configured for GPIO, the following registers are used:

- HI08 (Port B)
  - HPCR—Host Port Control Register (GPIO on HI08)
  - HDDR—Host Data Direction Register (GPIO on HI08)
  - HDR—Host Data Register (GPIO on HI08)
- SSI (Ports C and D)
  - PCRC—GPIO Port C Control Register (GPIO on SSI0)
  - PRRC— GPIO Port C Direction Control Register (GPIO on SSI0)
  - PDRC—GPIO Port C Data Register (GPIO on SSI0)
  - PCRD—GPIO Port D Control Register (GPIO on SSI1)
  - PRRD— GPIO Port D Direction Control Register (GPIO on SSI1)
  - PDRD—GPIO Port D Data Register (GPIO on SSI1)

- Timer
  - TCSR0—Timer Control / Status Register (GPIO on the TIO0 pin)
  - TCSR1—Timer Control / Status Register (GPIO on the TIO1 pin)
  - TCSR2—Timer Control / Status Register (GPIO on the TIO2 pin)

These registers are discussed in more detail in their respective sections.

The dedicated GPIO programming model is shown in **Figure 6-1**.

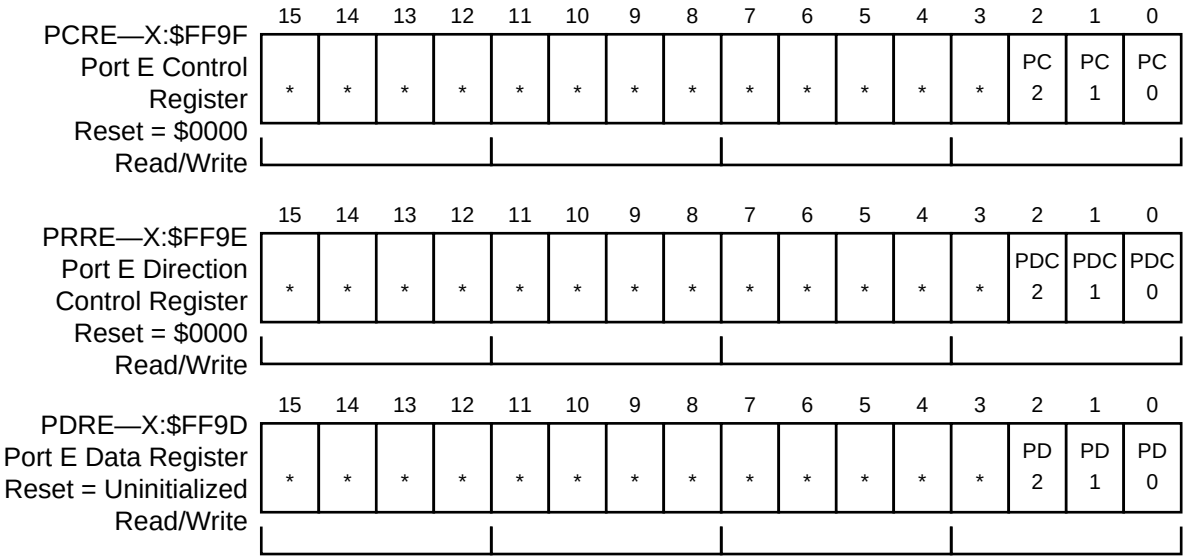


Figure 6-1 GPIO Port E Programming Model

6.3 GPIO PORT E CONTROL REGISTER (PCRE)

The 16-bit read / write GPIO Port E Control Register (PCRE) controls the functionality of GPIO pins. Each of the PC bits controls the functionality of the corresponding port pin. When a PC bit is set, the corresponding port pin is tri-stated or GPIO output with open drain defined by the direction control bit. When a PC bit is cleared, the corresponding port pin is configured as GPIO pin.

Although the PCRE has sixteen bits, only the bottom three bits are used. Hardware and software reset clear all PCRE bits.

6.4 GPIO PORT E DIRECTION REGISTER (PRRE)

The 16-bit read / write GPIO Port E Direction Register (PRRE) controls the direction of GPIO pins. When a port pin is configured as GPIO (its corresponding PC bit in the PCR is cleared), the PDC bit controls the port pin direction. When the PDC bit is set, its corresponding GPIO port pin is configured as output. When the PDC bit is cleared, the GPIO port pin is configured as input.

When the PC bit is set and the PDC bit is cleared, the corresponding port pin is tri-stated. When both the PC bit and the PDC bit are set, the corresponding port pin is configured for open-drain GPIO output. Although the PRR has sixteen bits, only the bottom three bits are used. Hardware and software reset clear all PRR bits.

The following table describes the port pin configurations.

Table 6-1 PCRE and PRRE Bits Functionality

PC Bit	PDC Bit	Port Pin Function
0	0	GPIO Input
0	1	GPIO Output
1	0	Tri-stated
1	1	GPIO Output as open drain

6.5 GPIO PORT E DATA REGISTER (PDRE)

The 16-bit read / write Port E Data Register (PDRE) is used to read or write data to and from GPIO pins. The PD bits are used to read or write data from and to the corresponding port pins if they are configured as GPIO (by the PC bits in the PCR). If a port pin is configured as a GPIO input, then the corresponding PD bit reflects the value present on this pin. If a port pin is configured as a GPIO output, then the value written into the corresponding PD bit is reflected on the this pin.