

HVP-MC56F82748 User's Guide

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1 High voltage controller cards overview

This document supports the HVP-MC3PH user's guide. It describes the HVP-MC56F82748 controller card. This card is based on the MC56F82748 digital signal controller and is intended to be used together with the HVP-MC3PH main board.

The Freescale high voltage development platform is a set of software and hardware tools for evaluation and development. It is ideal for rapid prototyping of MCU-based applications. The Freescale HVP-MC56F82748 hardware is a simple yet sophisticated design featuring a DSC series MCU built around the 32-bit 56800EX core.

The MC56F823xx/7xx is a low-power DSP MCU family offering outstanding power consumption at run-time in a compact 5×5 mm package with exceptional performance, precision and control for high-efficiency digital power conversion (MC56F827xx) and advanced motor control (MC56F823xx) applications. The MC56F827xx includes advanced high-speed and high-accuracy peripherals, such as high-resolution pulse width modulation (PWM) with 312 ps resolution and dual high-speed 12-bit analog-to-digital

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converters (ADCs) with built-in PGA sampling of up to 1.25 mega samples per second (MSPS) at 12 bits. Faster application-specific control loops are driven via a 32-bit DSP core with single-cycle math computation, fractional arithmetic support and parallel moves.

2 Reference documents

[Table 1](#) provides a list of reference documents about the HVP-MC56F82748 hardware. All of these documents are available online at freescale.com/HVP.

Table 1. Reference documents

Filename	Description
HVP-MC56F82748 Quick Start Package	This is a quick start guide with supporting files for getting started with the HVP-MC56F82748 hardware.
HVP-MC56F82748 User's Guide	This document provides overview and detailed information about the HVP-MC56F82748 hardware.
HVP-MC3PH User's Guide	This document provides overview and detailed information about the HVP-MC3PH hardware.
HVP-MC56F82748 Schematics	This document contains PDF schematics for the HVP-MC56F82748 hardware.
HVP-MC56F82748 Design Package	This is a zip file containing all design source files for the HVP-MC56F82748 hardware.

3 DSC-based controller cards features

- Usage of target MCU MC56F82748VLH (MC56F84763VLH-optional)
- JTAG isolation up to 5 kV
- Compatible with CodeWarrior 10.x
- Design optimized for low noise, high interference immunity
- On-board isolated power supply, allowing safe debugging
- Controller card supporting standalone operation

[Figure 1](#) shows a block diagram of the HVP-MC56F82748 design. The primary components and their placement on the board is described in [Figure 2](#).

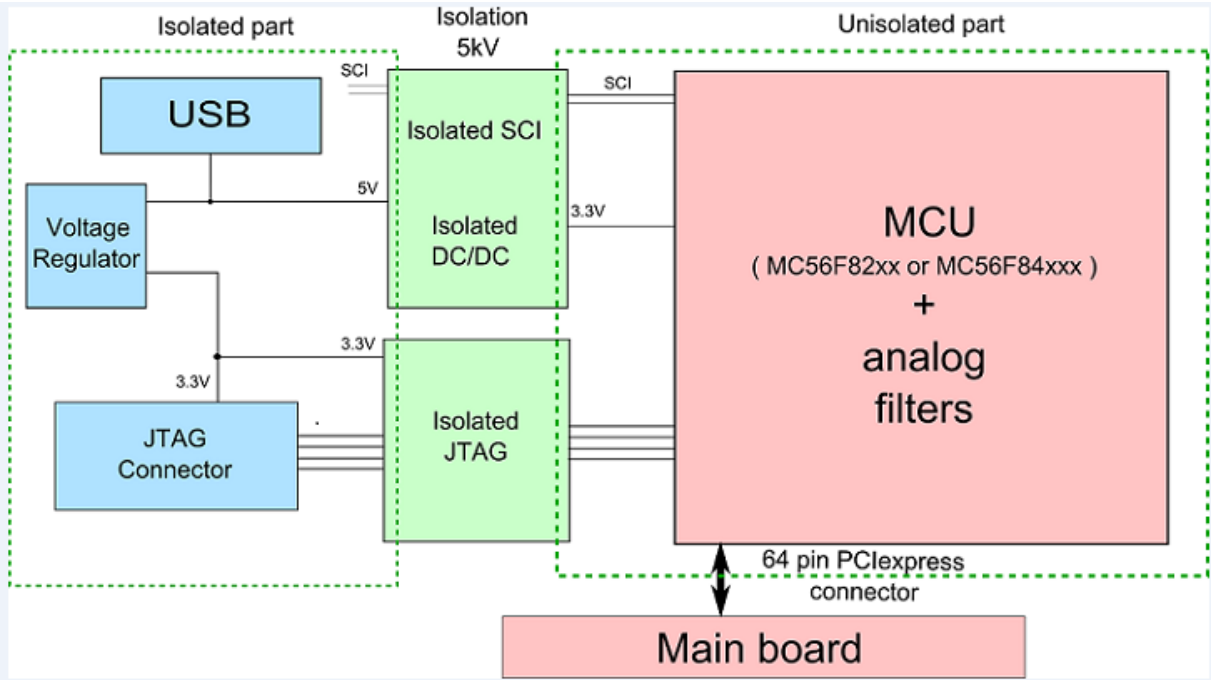


Figure 1. HVP-MC56F82748 block diagram

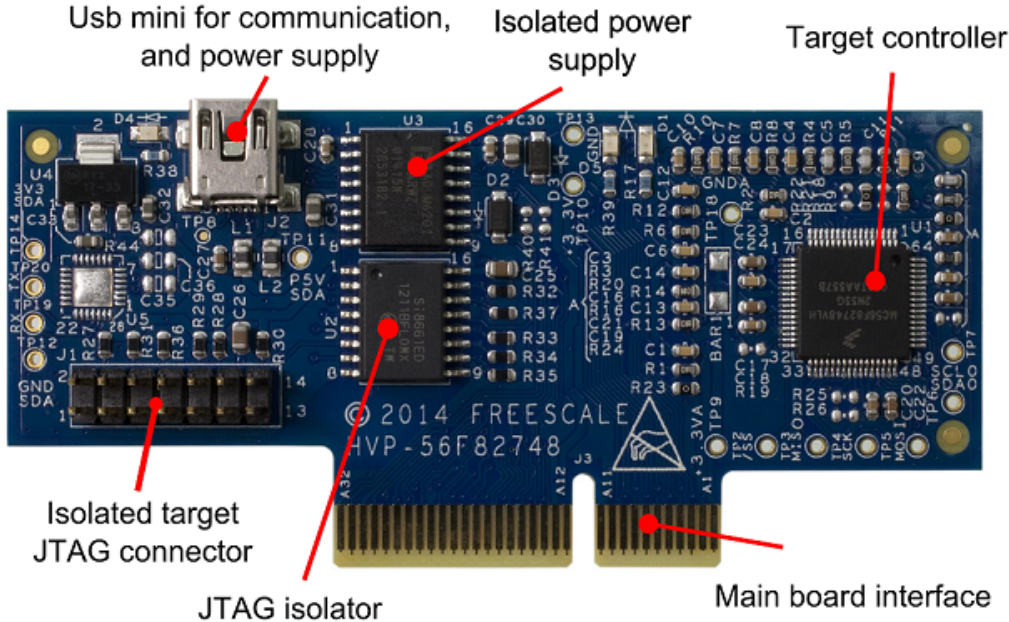


Figure 2. HVP-MC56F82748 controller card description

3.1 Power supply

There are two power supply options available on the controller card. It can be powered either from the USB connector or from the main board 3.3 V supply. When the controller card is unplugged from the HVP-MC3PH, the USB voltage is regulated using a 3.3 V on-board linear regulator to produce the power. In this case, the controller card is powered from the USB during standalone operation. Only digital circuits are powered, while analog circuits remain unpowered. Thus, the ADC measurement cannot be evaluated. When the card is inserted into the main board, power is drawn from the main board and the analog circuits work. If the analog circuits need to be evaluated during standalone operation, the test points placed on the controller card (TP10 and TP9) need to be shorted.

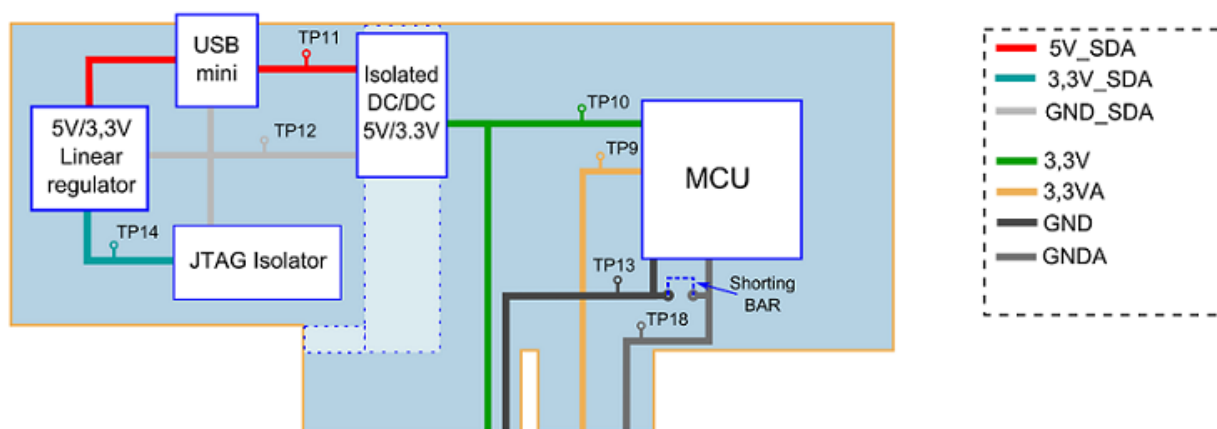


Figure 3. HVP-MC56F82748 power distribution

3.2 Clocking

The controller card does not include any clock source. Thus, the controller must be clocked from the internal clock of MC56F82748VLH.

3.3 JTAG target debug interface

The DSC debug JTAG connector J1 is a standard 2×7-pin connector providing connection for an external debugger with access to the MC56F82748 MCU. The + 3.3 V power supply must be provided by the external debugger or using the mini USB connector to provide power for isolation circuits.

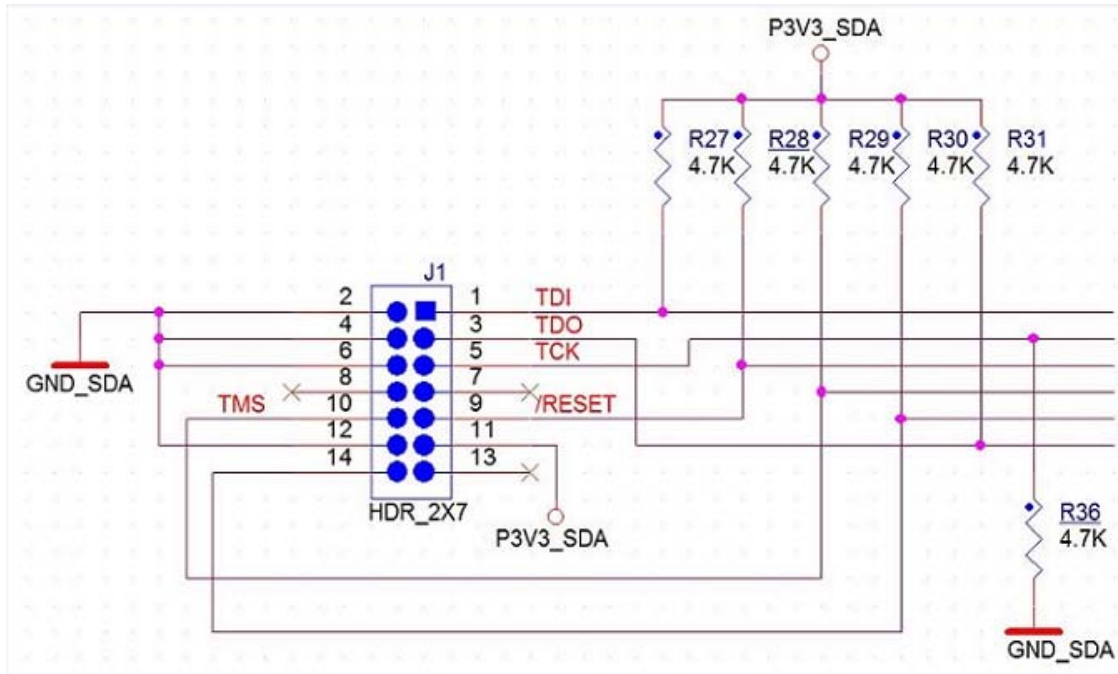


Figure 4. JTAG connector

Table 2. JTAG connector J1 signal description

Pin	Function	MCU Signal
1	TDI	TDI / GPIOD0
2,4,6,12	GND	–
3	TDO	TDO / GPIOD1
5	TCK	TCK / GPIOD2
7,8,13	NC	–
9	$\overline{\text{RESET}}$	–
10	TMS	TMS / GPIOD3
11	3,3V	–
14	$\overline{\text{TRST}}$	NC

3.4 On-board LEDs, testpoints and connectors

Table 3. Test points, LEDs and connectors

Ref. des.	Name	Functionality
TP9	+ 3.3 VA	+ 3.3 V analog power supply for analog circuits (not powered during standalone operation)
TP10	+3.3 V	+ 3.3 V digital power supply for logic circuits
TP11	P5V_SDA	+ 5 V from mini USB connector

Table 3. Test points, LEDs and connectors (continued)

Ref. des.	Name	Functionality
TP12	GND_SDA	GND connected to the mini USB connector (isolated side)
TP13	GND	GND connected to the target controller (non-isolated side)
TP14	P3V3_SDA	+ 3.3 V for OpenSDA, provided by linear voltage regulator
TP18	GNDA	Analog GND
TP2	/SS	General use test point
TP3	MISO	General use test point
TP4	SCK	General use test point
TP5	MOSI	General use test point
TP6	SDA0	General use test point
TP7	SCL0	General use test point
TP19	Rx	UART1_Rx
TP20	Tx	UART1_Tx
D1	–	User LED 2
D4	–	Isolated side + 3.3 V power indicator
D5	–	Non-isolated side + 3.3 V power indicator
J1	–	Isolated target JTAG connector
J2	–	Galvanically isolated USB for power and SCI communication
J3	–	Controller card connector

3.5 Assembling options for comparator functionality

The DSC controller card with the MC56F82748VLH device supports advanced algorithms that utilize the internal analog comparators. The comparator functionality can be used for example for dead-time compensation, phase over-current protection, BLDC control, or PFC over-current protection. Since there are just four analog comparators, these configurations can be switched by assembling zero resistors. All possible configurations are described in [Table 4](#).

Table 4. Comparators functionality

Functionality	Configurations number and comparator channels assignment				
	1–Default	2	3	4	5
Phase currents on ACMP	NO	YES – A,C,D	YES – A,C,D	NO	NO
Phase voltages on ACMP	NO	NO	NO	YES – A,B,D	YES – A,B,D
All BEMF on one ADC	YES	YES	YES	NO	NO
PFC1 Over-Current	YES – C	NO	NO	NO	YES – C
PFC2 Over-Current	YES – B	YES – B	NO	NO	NO

Table 4. Comparators functionality (continued)

Functionality	Configurations number and comparator channels assignment				
	1–Default	2	3	4	5
DCB Over-Current	YES – D	NO	NO	YES – C	NO
DCB Over-Voltage	NO	NO	YES – B	NO	NO
TACHO	YES – A	NO	NO	NO	NO
Populated	R20,R21,R23	R18,R20	R18,R20	R18,R19,R22,R24,R25,R26	R18,R19,R22,R24,R25,R26
Non-populated	R18,R19,R22,R24,R25,R26	R19,R21,R22,R24,R25,R26	R19,R21,R22,R24,R25,R26	R20,R21,R23	R20,R21,R23

3.6 Using the MC56F84763V controller

The DSC-based controller cards are populated with the MC56F82748VLH device by default. However, this controller card is compatible also with the MC56F84763V device. If the MC56F84763V controller needs to be evaluated, then the U1 needs to be replaced.

3.7 Serial port

On the HVP-MC56F82748 controller card, there are two serial communication interfaces used for communication with the main board or computer. Serial lines are connected to UART0 (PTC2 / PTC3) and UART1 (PTC11 / PTC12). The UART1 can be used also for communication via the mini USB using on-board USB to UART. The USB to UART convertor is not populated by default; the parts R40, R41, R44, C35, C36, and U6 need to be populated according to the schematic. For information about the connection of SCI lines on the main board refer to the HVP-MC3PH user's guide.

The connection of serial communication lines is described in [Figure 5](#).

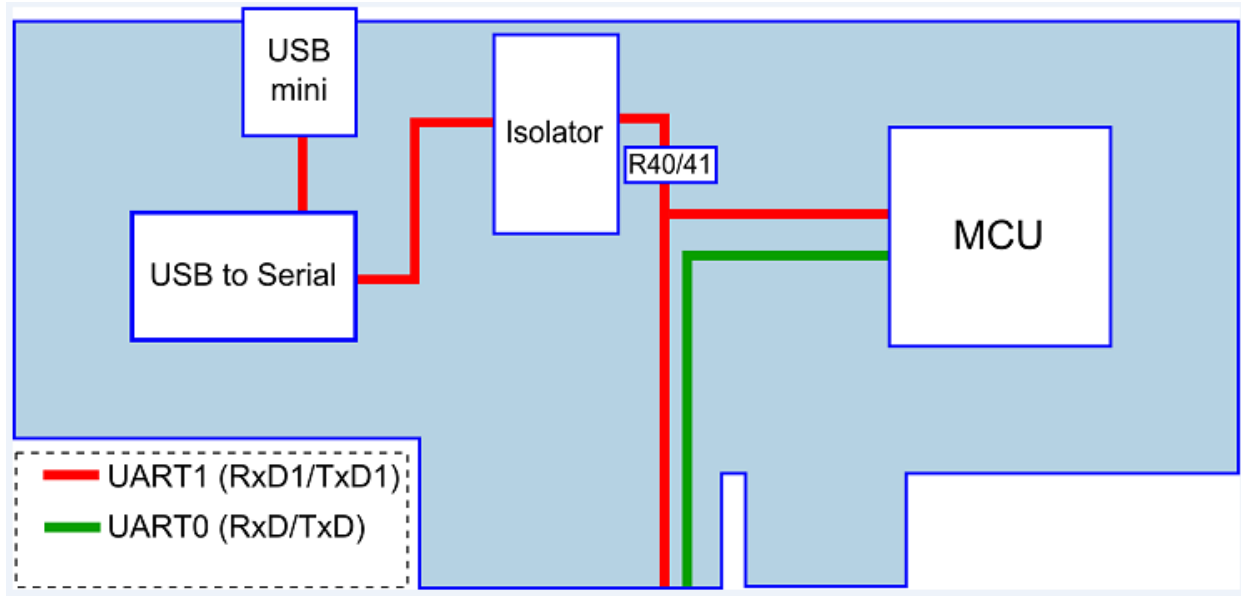


Figure 5. Serial lines block diagram

3.8 HVP-MC56F82748 – HVP-MC3PH interface description

The interface between the controller card and the main board is provided by 64-pin PCI express edge connector. [Figure 6](#) describes the functionality of each pin of this interface.

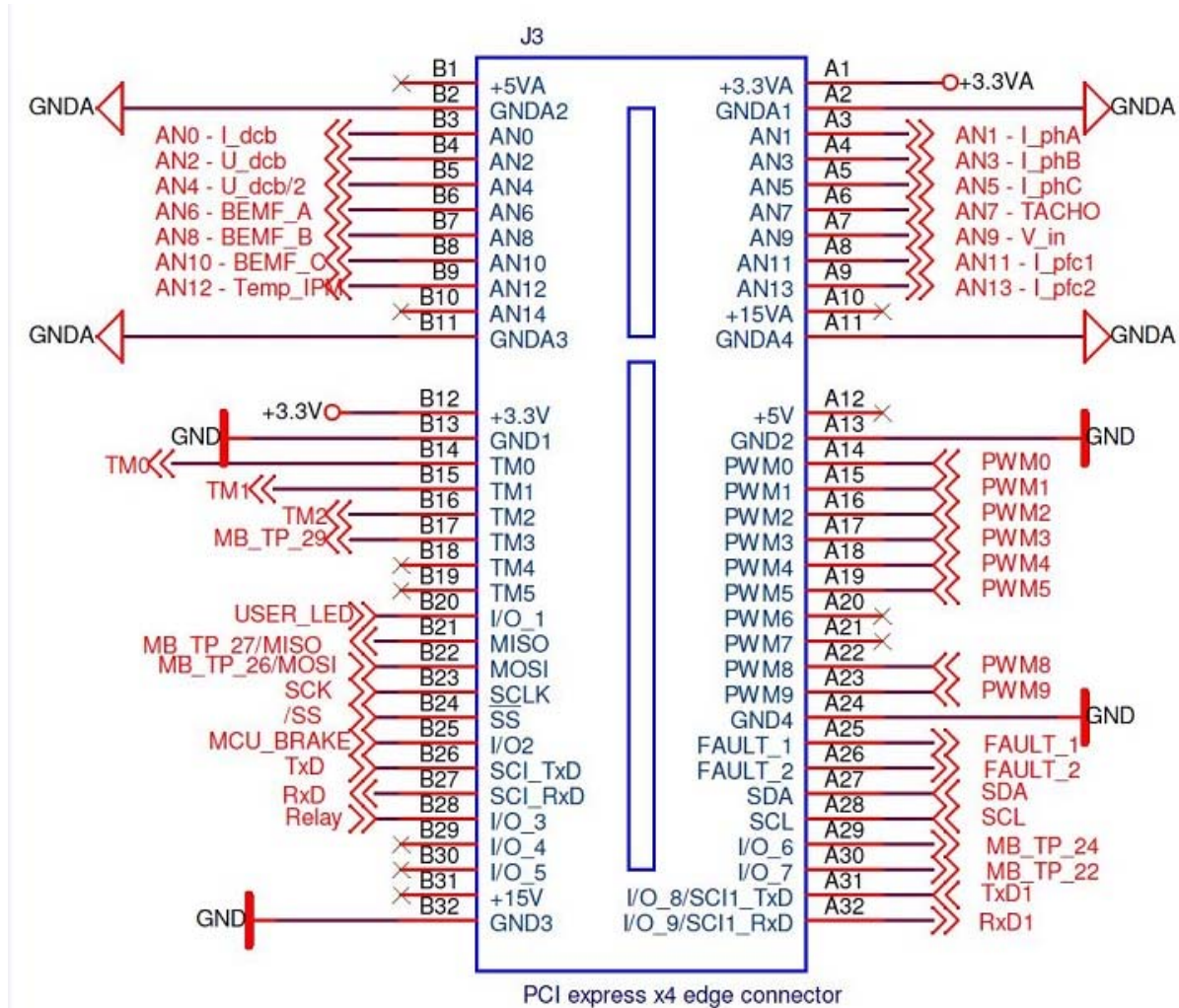


Figure 6. Main board interface

4 Revision history

Table 5. Document revision history

Rev. number	Date	Substantive change(s)
0	12/2014	Initial release

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