i.MX31ADS Hardware Getting Started

User's Guide

Document Number: IMX31ADSHGSG
Rev. 2.1
11/27/2006

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
+1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064, Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

***For Literature Requests Only*:**
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Contents

About This Book

About This Book

The i.MX31ADS Hardware Getting Started Guide describes the kit contents, procedures for assembling the components, identifies connectors, jumpers, and switch configurations and the factory default settings.

Audience

This document is targeted to individuals who work with the i.MX31ADS board. An understanding of the i.MX31 multimedia applications processor is required.

Organization

This document is organized into the following chapters.

Chapter 1 i.MX31ADS Kit Contents and Revision Identification

Chapter 2 Kit Assembly

Chapter 3 Powering Up the i.MX31ADS

Chapter 4 Connector Descriptions and Locations

Chapter 5 Jumper Configuration

Chapter 6 Switch Configuration

Chapter 7 Factory Defaults

Revision History

The following table summarizes revisions to this document since the previous releases; Rev. 1 and Rev 2.0.

Revision	Location	Revision
2.0	Throughout document	Edited text and reorganized content.
2.0	Section 1.2	Added Revision Identification section.
2.0	Section 3	Added Powering up the i.MX31ADS section.
2.0	Section 5 and 6	Separated Jumper and Switch sections
2.0	Section 7	Moved Factory Defaults to end.
2.1	Section 7, Table 16	Changed default jumper settings for the following: JP14 from 1-2 to Put jumper JP22 from Not Assembled to 2-3 Added jumper JP26

Conventions

This document uses the following notational conventions:

- Courier monospaced type indicates commands, command parameters, and code examples.
- Bold type indicates the elements of command lines that must be entered exactly as shown.
- Italic type indicates replaceable command parameters that the user must provide.

Definitions, Acronyms, and Abbreviations

The following list defines the abbreviations used in this document.

DSP	digital signal processor
JTAG	joint test access group

Suggested Reading

The following documents will aid in your understanding of this document:

- *i.MX31ADS Application Development System User's Manual* (Order Number: MCIMX31ADSRM)
- *MC13783 Power Management and Audio Component Data Sheet* (Order Number: MC13783)

1 i.MX31ADS Kit Contents and Revision Identification

This section provides identification of the i.MX31ADS contents as well as the board and processor revision identification.

1.1 Kit Contents

Your i.MX31 Applications Development System contains the items in the following list. Figure 1 shows each component identified by number.

1. i.MX31ADS CPU board
2. i.MX31ADS Baseboard
3. MC13783 Power Management and Audio board
4. 1 Giga-bit NAND Flash card
5. Sharp Sync QVGA display
6. Keypad
7. iMagic IM8012 Compact Camera module
8. 5V/5A universal power supply kit
9. RS232 standard serial cable
10. High Speed USB cables with miniAB connectors for OTG
11. High Speed USB cable with standard A to mini B connectors
12. Ethernet cables (2) with RJ45-8 connectors
13. Head phones

The following kit components are not identified in Figure 1:

- Mini USB adapter
- CD: *User Information for the i.MX31ADS*
- Palm M125/M130 stylus pack
- *MCIMX31 and MCIMX31L Chip Errata* document, (order number: MCIMX31CE)
- Warranty card, Freescale, 920-75133
- Contact information sheet; *Technical Information Center, Freescale Semiconductor Inc.*, (order number: BR1530)

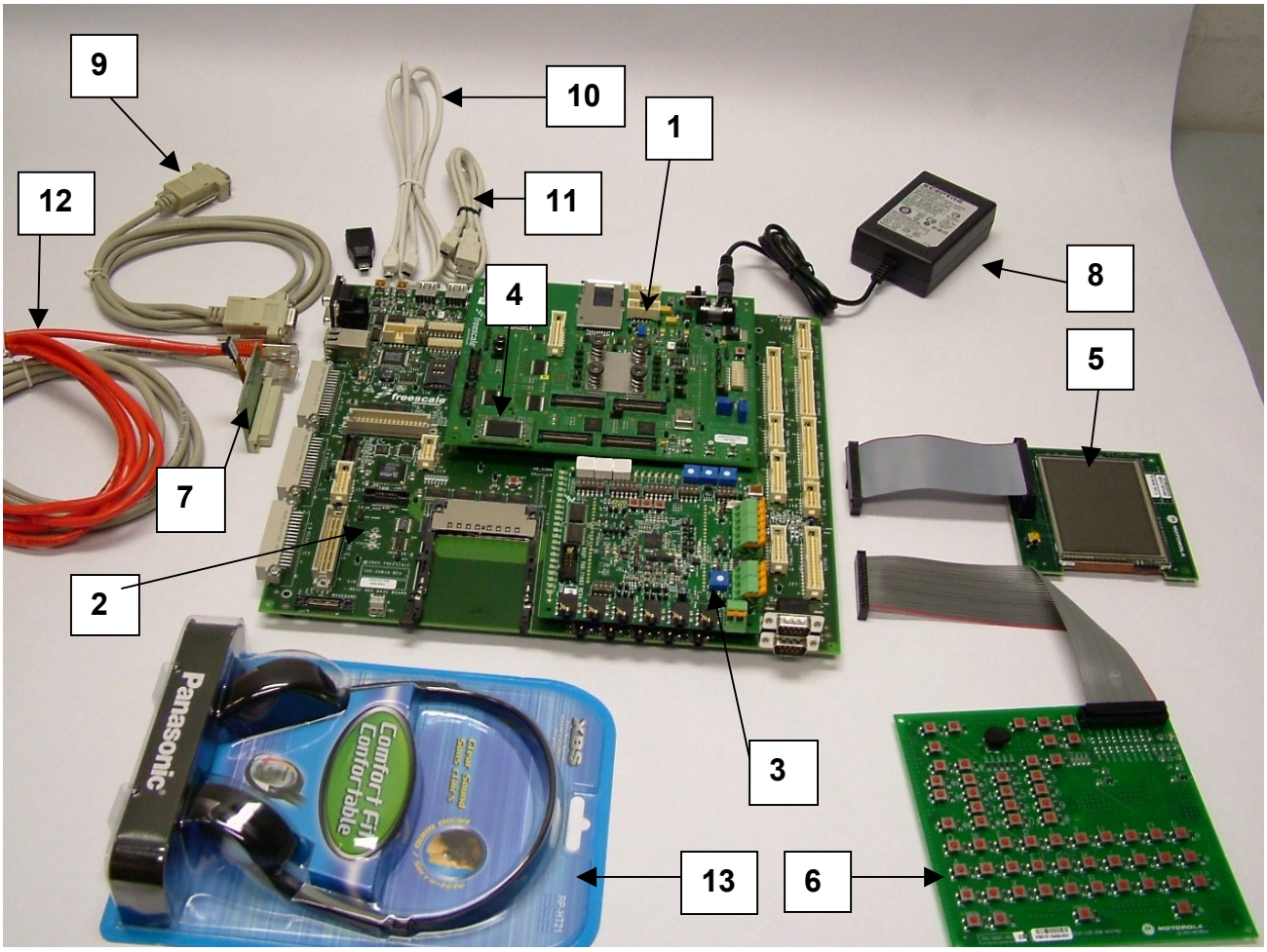

Figure 1. Components of the i.MX31ADS Kit

1.2 i.MX31ADS Revision Identification

The i.MX31ADS kit contains several circuit board and silicon revision labels. This section discusses these revision label locations and identification.

1.2.1 i.MX31 Processor Revision Identification

The i.MX31 processor mask is used to indicate the silicon revision of the chip. The mask is usually 4-5 letters and numbers, beginning with a number. The mask revision number is located on the bottom left corner of the i.MX31 processor on the CPU board.

To determine which silicon revision is in your i.MX31ADS kit, refer to the i.MX31 Chip Errata document, which lists the silicon revision for each mask at the beginning of the document. You may also use the Chip Errata document to determine any silicon issues with your specific silicon revision.

1.2.2 CPU Board Revision Identification

The CPU board has the following revisions associated with it and are identified in Figure 2.

1. Layout revision (letter)
2. Assembly revision (number)
3. Bill of Materials (BOM) revision (letter—this is not labelled on the CPU board)

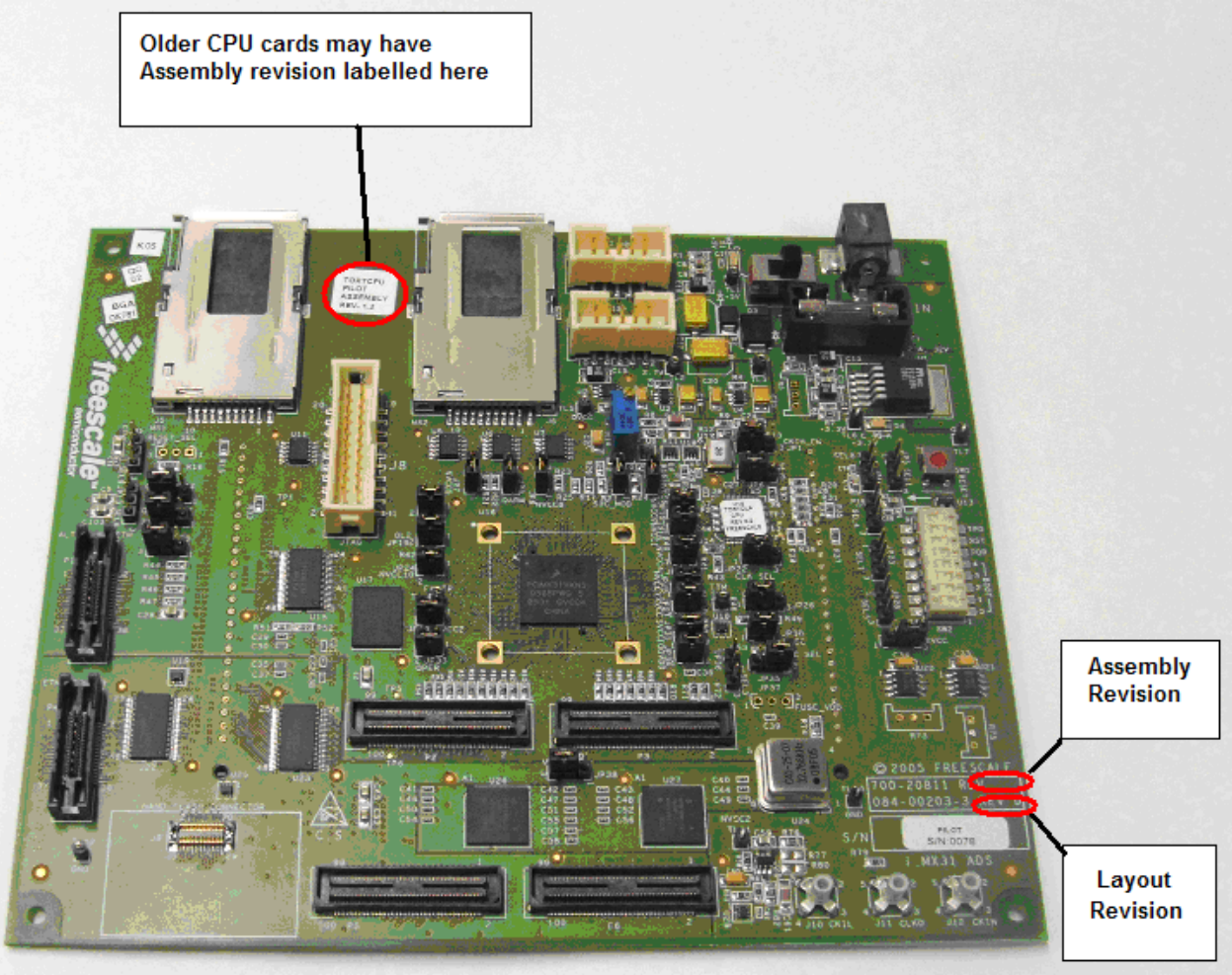

Figure 2. CPU Board Revision Identification

1.2.3 Baseboard Revision Identification

The Baseboard has the following revisions associated with it and are shown in Figure 3.

1. 1. Layout revision (letter)
2. 2. Assembly revision (number)
3. 3. Bill of Materials (BOM) revision (letter)

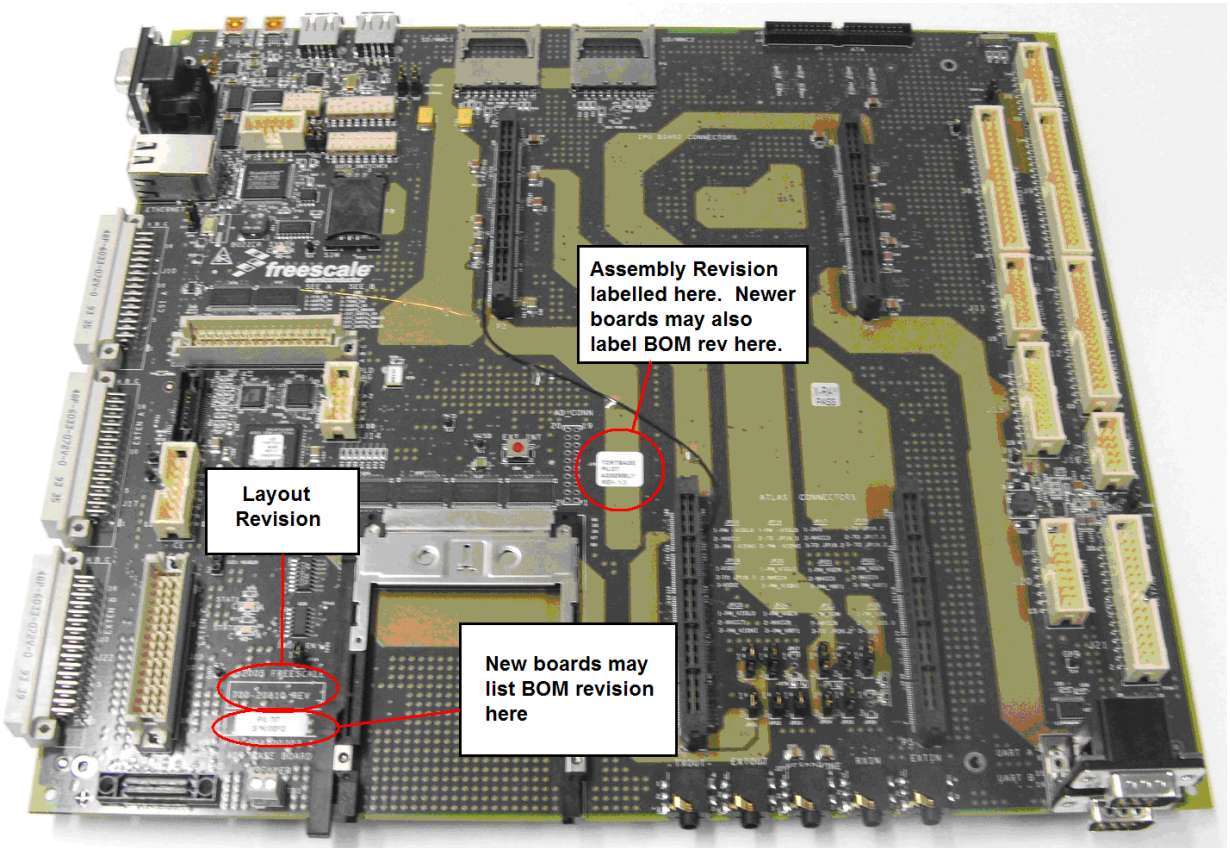

Figure 3. Baseboard Revision Identification

1.2.4 MC13783 Board Revision Identification

The MC13783 board revision can be found at the location shown in Figure 4.

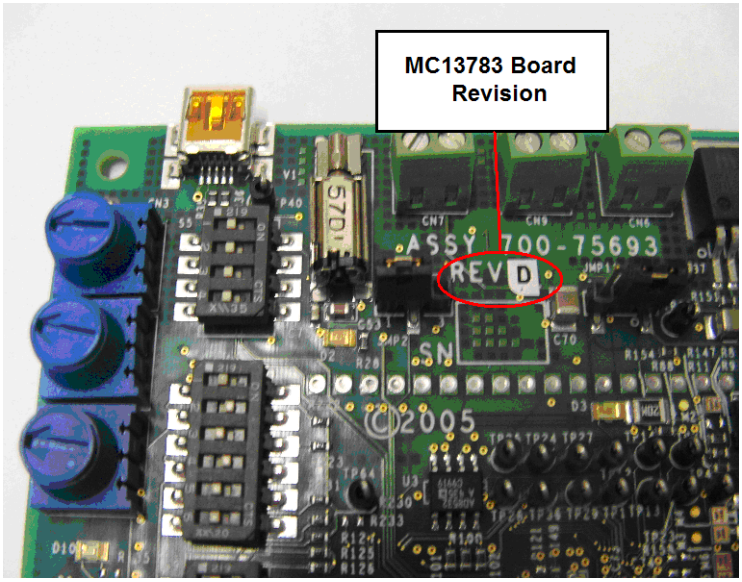

Figure 4. MC13783 APMB Revision Identification

2 Kit Assembly

This section explains how to assemble the various components of the i.MX31ADS kit.

2.1 Assembling the CPU to Baseboard

To connect the CPU to the Baseboard, lay the Baseboard on a flat work surface. Install the CPU board as shown in Figure 5. The connectors are keyed so that the board can only be plugged in correctly.

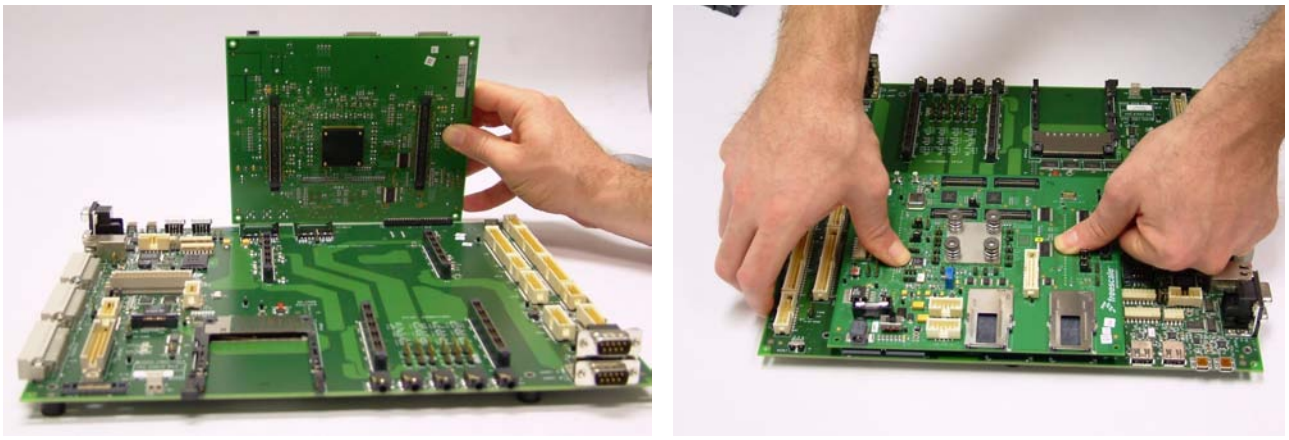

Figure 5. Connecting the CPU to the Baseboard

2.2 Assembling the MC13783 Board to the Baseboard

Install the MC13783 board has shown in Figure 6. The connectors are keyed so that the board can only be plugged in correctly.

Configure the MC13783 power source jumpers as instructed in Section 5, “i.MX31ADS Jumper Configurations”.

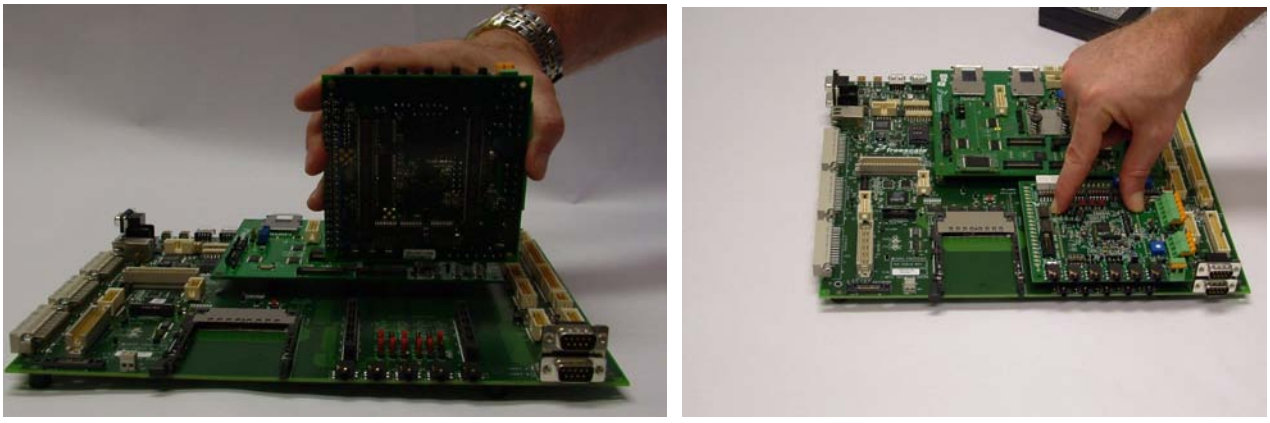

Figure 6. Connecting the MC13783 Board to the Baseboard

2.3 Connecting Power to the CPU

Connect the female end of the AC cable to the power supply module. Add the adaptor plugs necessary for your location to the other end and plug it into an appropriate AC outlet.

Connect the barrel connector into J3 on the CPU board as shown in Figure 7.

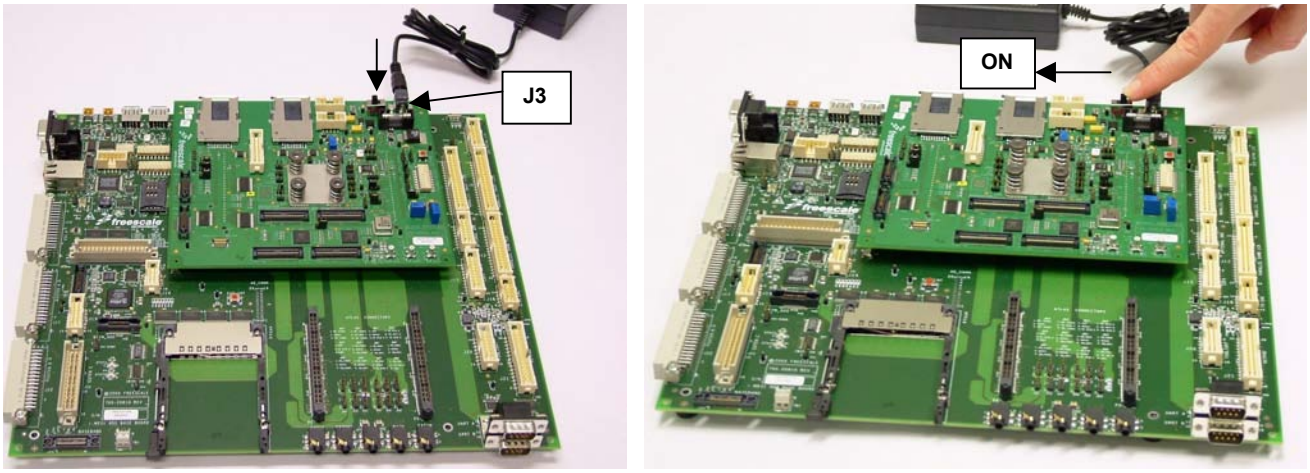

Figure 7. Connecting Power to the CPU

2.4 Turning System Power On

On the CPU board, toggle S1 to the ON position as shown in Figure 7. D1 illuminates, indicating that external power has been applied.

3 Powering up the i.MX31ADS

This section provides the instructions to verify that the board functions properly after kit assembly. Follow steps 1 through 8 to power up the assembled i.MX31ADS.

1. Power down the ADS board. Turn S1 on the CPU board to the OFF position.
2. Connect the QVGA display to the i.MX31ADS Baseboard.

   The QVGA is item 5 pictured in Figure 1. Included in the ADS kit is a 34-signal ribbon. Connect one end of this ribbon to the J11 connector on the QVGA. Connect the other end of this cable to the J12 connector on the i.MX31ADS Baseboard labeled “Parallel Dumb LCD”.
3. Connect the serial cable from the i.MX31ADS Baseboard to a host computer.

   The serial cable is item 9 pictured in Figure 1. Connect the male end to the external UART on the Baseboard. The external UART is the top UART next to the Ethernet port connector. Connect the other end to the host computer.
4. Verify that the Boot mode is set to load from NOR flash.

   All i.MX31ADS kits are shipped with the latest version of the Freescale Linux BSP loaded into NOR Flash. On the CPU board, set SW2 switches 1-5 as [ON – ON – OFF – ON – OFF]. Please see Section F for more details on these switch settings. Verify that all settings match the factory default settings described in Section 7.

5. Open HyperTerminal or a similar terminal application on the host PC.
   Configure the COM port settings as follows:
   Baudrate = 115200
   Data bits = 8
   Parity = None
   Stop bits = 1
   Flow Control = None
6. Power on the board by switching S1 on the CPU board to the ON position.

If all connections are made properly, you will see RedBoot™ load on HyperTerminal as shown in Figure 8.

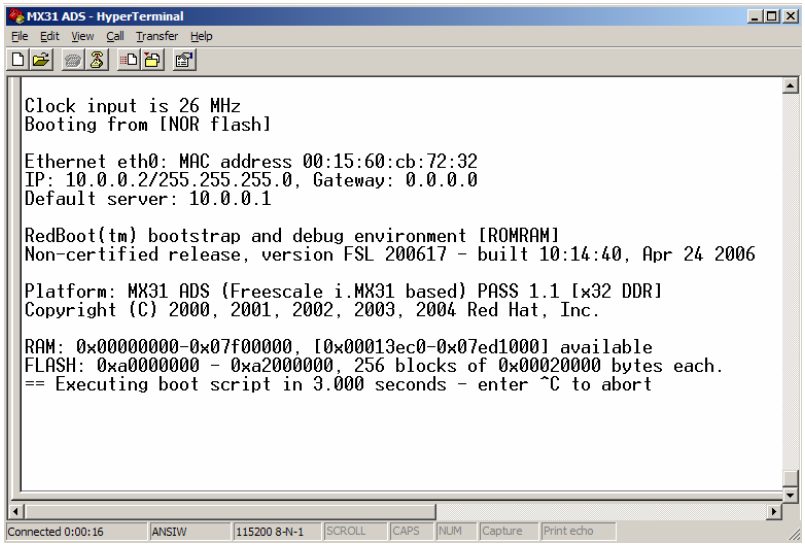

Figure 8. RedBoot Loading on the i.MX31ADS

Note that certain revision numbers and dates listed in script in Figure 8 may differ as new Linux board support package (BSP) revisions are released and loaded onto production i.MX31ADS boards.

After a few seconds delay, the Linux BSP will load, leading to a login prompt on the terminal. A Freescale Linux penguin similar to the image in Figure 9 appears on the QVGA display.

Figure 9. Image Displayed on QVGA when Linux Booted on i.MX31ADS

At this point, the Linux BSP is now loaded and the i.MX31ADS is functioning correctly.

4 Connector Descriptions and Locations

This chapter provides the connector descriptions and their locations for the Baseboard, CPU, MC13783 boards.

4.1 CPU Connections

The following list identifies the CPU connectors, as shown in Figure 10.

- JI – Baseboard (under board, not shown)
- J2 – Baseboard (under board, not shown)
- J3 – +5V Power In
- J4 – PC Test Header
- J5 – Memory Stick 1
- J6 – Memory Stick 2
- J7 – CPLD In-circuit Programming
- J8 – RV ICE, JTAG
- J9 – NAND Flash
- J10 – Clock In Low SMB
- J11 – Clock Out SMB
- J12 – Clock In High SMB
- P1 – Alternate ETM
- P2 – Samtec LA, SDA0:12; SD16:31
- P3 – Samtec LA, SD control; SD0:15
- P4 – Primary ETM
- P5 – Samtec LA, D0:15; WEIM control
- P6 – Samtec LA, WEIM A0:25; RESET, WD_RST, DMA
- U16 – i.MX31 CPU

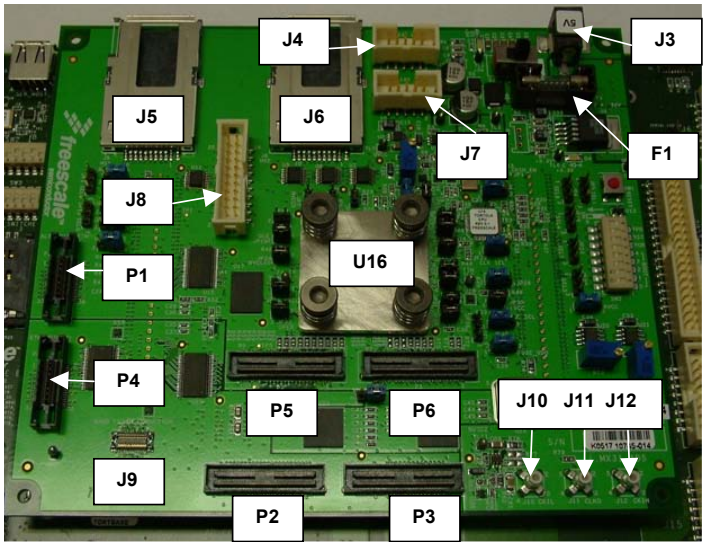

Figure 10. CPU Board Connector Locations

4.2 Baseboard Connections

The following list identifies the Baseboard connectors, as shown in Figure 11 and Figure 12.

- J1 – OTG High Speed USB
- J2 – OTG Full Speed USB
- J3 – ATA
- J4 – USB High Speed Host
- J5 – USB Full Speed Host
- J6 – Smart Serial LCD
- J7 – External UART B (RS-232, DCE)
- J8 – Smart Parallel LCD II
- J9 – Smart Parallel LCD I
- J10 – CSI A (Image Sensor)
- J11 – Synchronous LCD + (optional signals)
- J12 – Synchronous LCD (Sharp)
- J13 – CSI B (Image Sensor)
- J14 – CPLD In-circuit Programming
- J15 – CSPI (channel 3)
- J16 – TV Encoder
- J17 – Extension 1
- J18 – MC13783 Analog (AD) (not populated)
- J19 – CE Bus
- J20 – Funlight and Push Button Switch (from MC13783)
- J21 – Keypad
- J22 – Extension 2
- J23 – Extension 3
- J24 – Baseband
- J25 – YMU782B Voice Transmission Output (10K)
- J26 – YMU782B External Analog Output (600 ohms)
- J27 – YMU782B Stereo Headphone
- J28 – YMU782B Voice Input
- J29 – YMU782B External Analog Input
- JP13 – I2C (I2C1 or I2C3)
- P1 – CPU (under CPU board, not shown)
- P2 – CPU (under CPU board, not shown)
- P3 – SD/MMC 1
- P4 – SD/MMC 2
- P5 – MC13783 Board

- P6 – MC13783 Board
- P7A – UARTC RS-232 DCE
- P7B – External UART A RS-232 DCE
- P8 – SIMM
- P9 – CodeTest/LA Data, Address, Control
- P10 – LA, Address, Control
- P11A – UARTA RS-232 DTE
- P11B – UARTB RS-232 DTE
- T1 – Ethernet
- TB1 – YMU782B Speaker Out
- U1 – FIR Transceiver
- U30 – PCMCIA

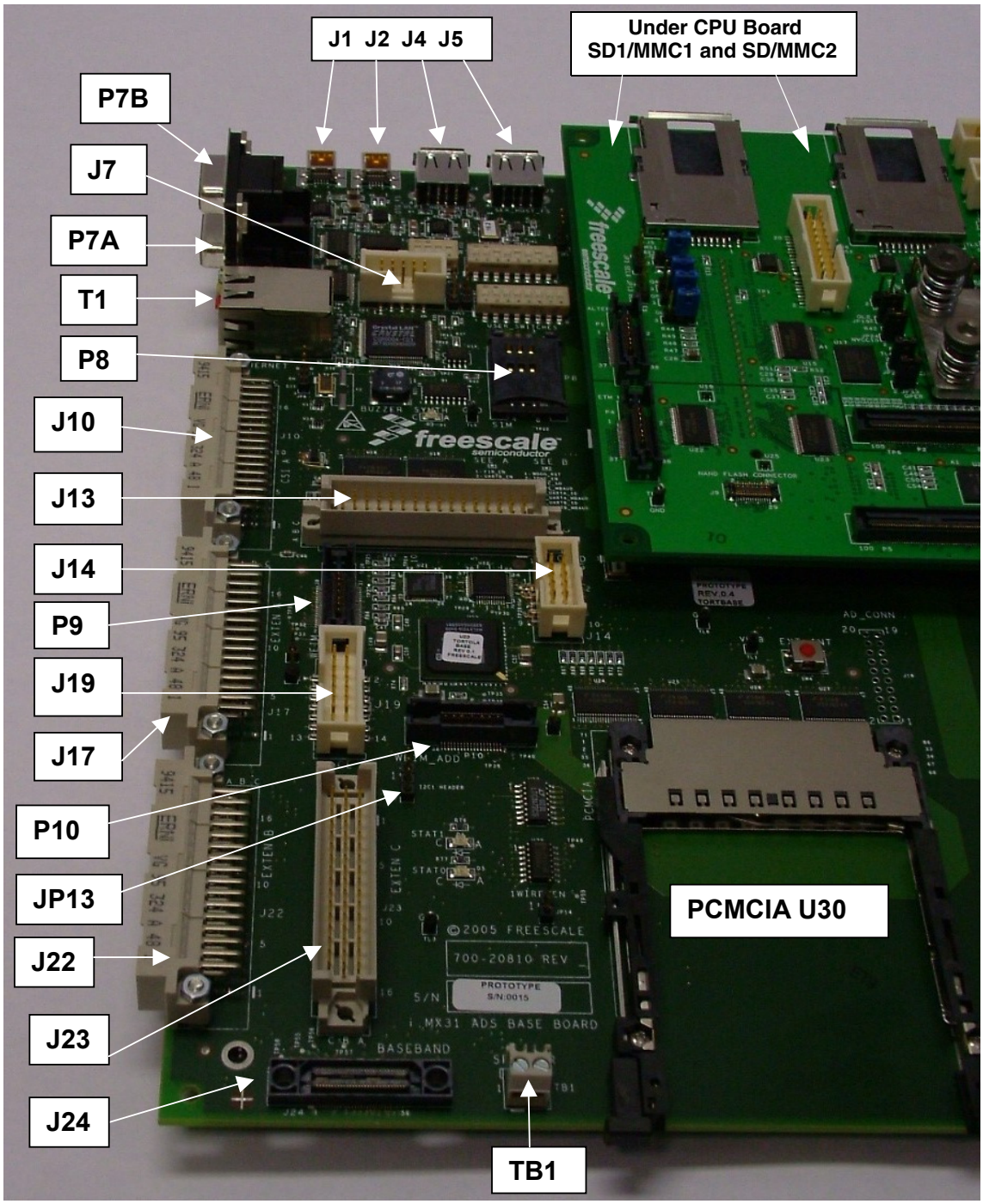

Figure 11. Baseboard Connectors—Left View

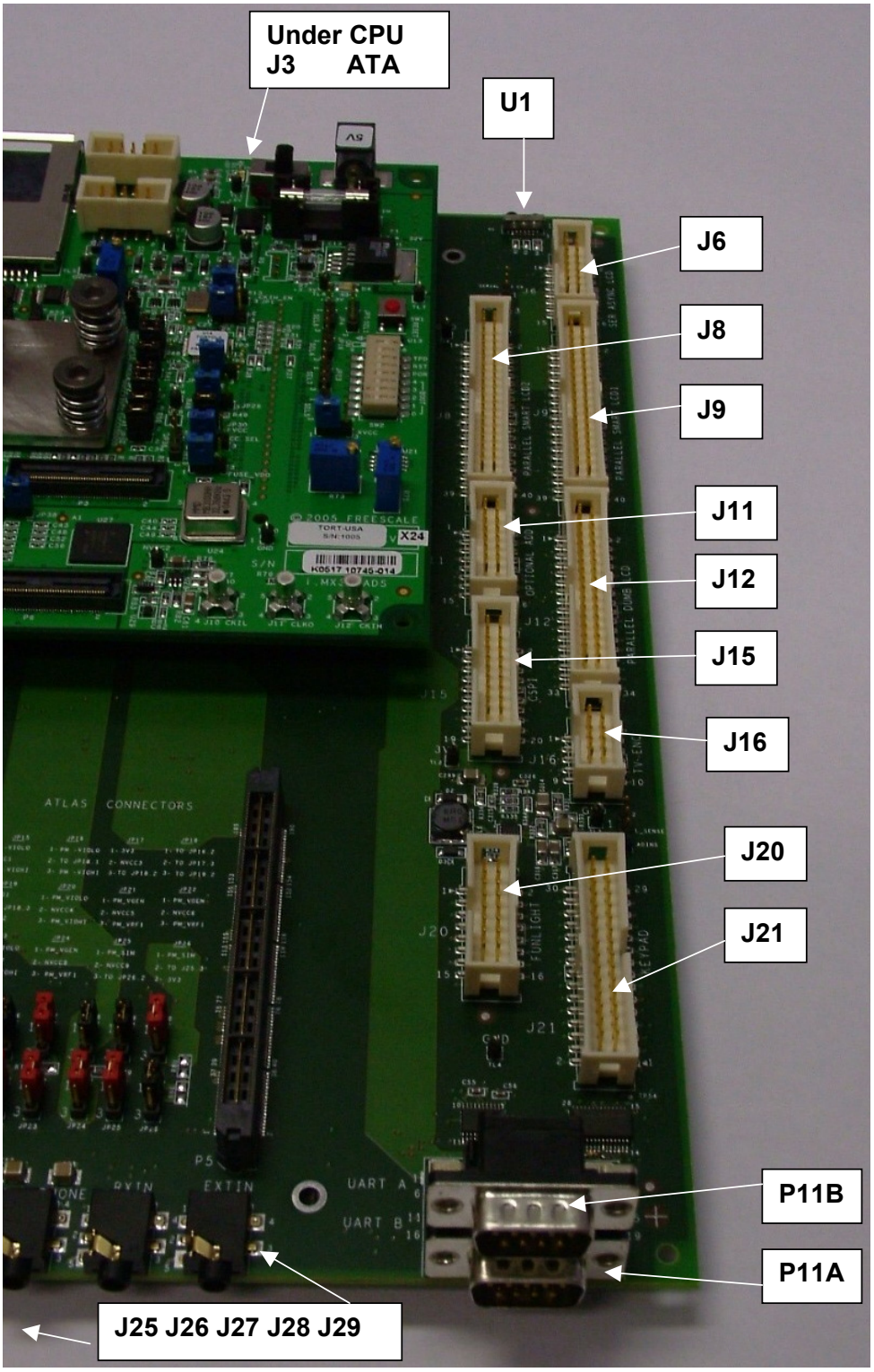

Figure 12. Baseboard Connectors—Right View

4.3 MC13783 Power Management and Audio Board Connectors

The following list identifies the MC13783 connectors, as shown in Figure 13.

- J1 – Stereo Audio IN
- J2 – Stereo Audio OUT
- J3 – Mic 2 IN
- J4 – Mic 1 Line IN
- J5 – Baseboard (under board, not shown)
- J6 – Baseboard (under board, not shown)
- J7 – TXIN Audio
- J8 – Stereo Headphone
- CN1 – Right Stereo Speaker Out
- CN2 – Ear Piece Speaker Out
- CN3 – OTG Full Speed USB
- CN4 – Clock OUT SMA
- CN5 – Left Stereo Speaker Out
- CN6 – Battery Charger In
- CN7 – External Battery In
- CN8 – Touchscreen (not populated)
- CN9 – Li Cell Battery In
- CN10 – CLIA/B External Clock In

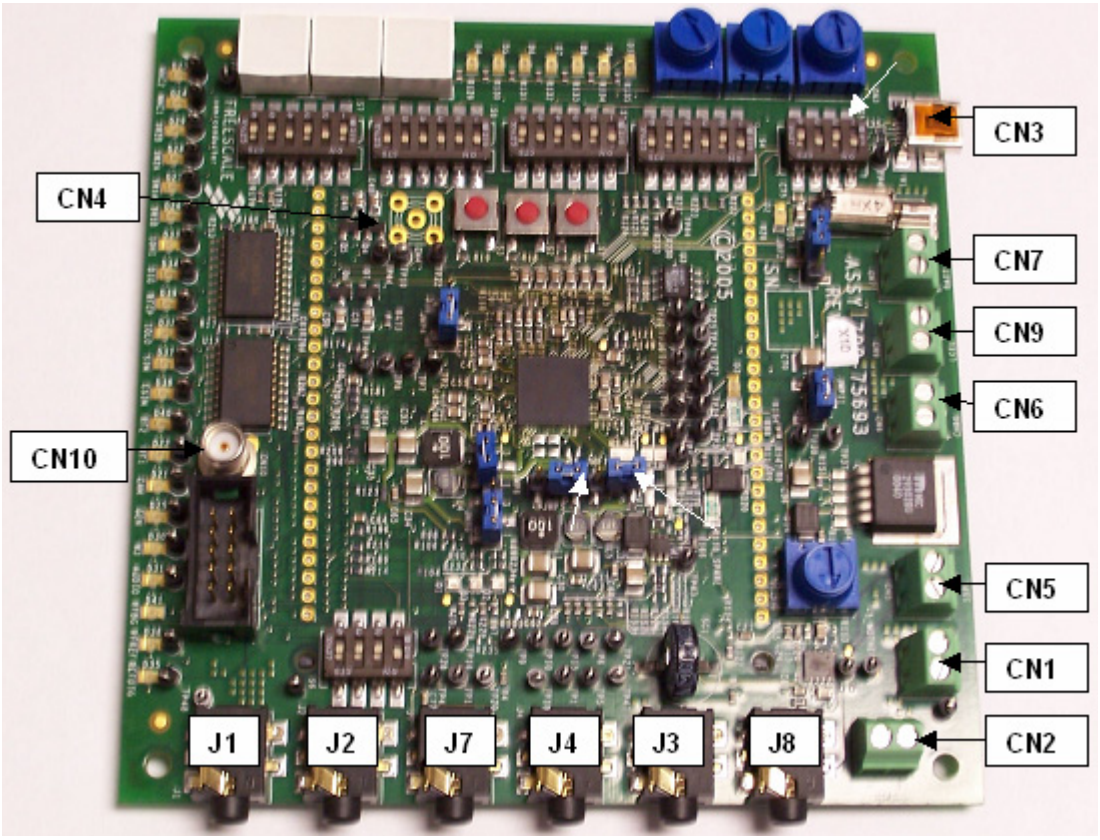

Figure 13. MC13783 Board Connectors

5 i.MX31ADS Jumper Configurations

The following sections explain how to configure the jumpers for the i.MX31 Application Development System.

5.1 Power Up Jumper Configurations

The i.MX31ADS Baseboard can be powered from either the CPU's on-board regulators or the MC13783 board. The factory settings of the i.MX31ADS are set for the MC13783 board. This section provides instructions for configuring the jumpers of the i.MX31ADS for the different options. If you use the MC13783 chip for i.MX31 power management or for audio codecs, power-up from the on-board CPU regulators.

5.1.1 Power Up from On-Board CPU Regulators

The NVCC, QVCC, and PLL Voltages must be changed from the factory defaults to power the board from the CPU's on-board regulators.

5.1.1.1 NVCCx Voltage to Power Up from CPU

The SELx jumpers control the corresponding NVCCx power supply when powering from the CPU regulators. These jumpers are identified in Table 1 and shown in Figure 14.

To set the voltage operation for NVCC, select from either of the two jumpers as follows:

- Jumper 1-2 to select +2.7V
- Jumper 2-3 to select +1.8V

Notes:
1. Shunts are not shown in picture.
2. NVCC2 and NVCC10 connect to memory components that operate at 1.8V and are fixed at that power and are not configurable.

WARNING

Do not install these jumpers when the MC13783 board is used.

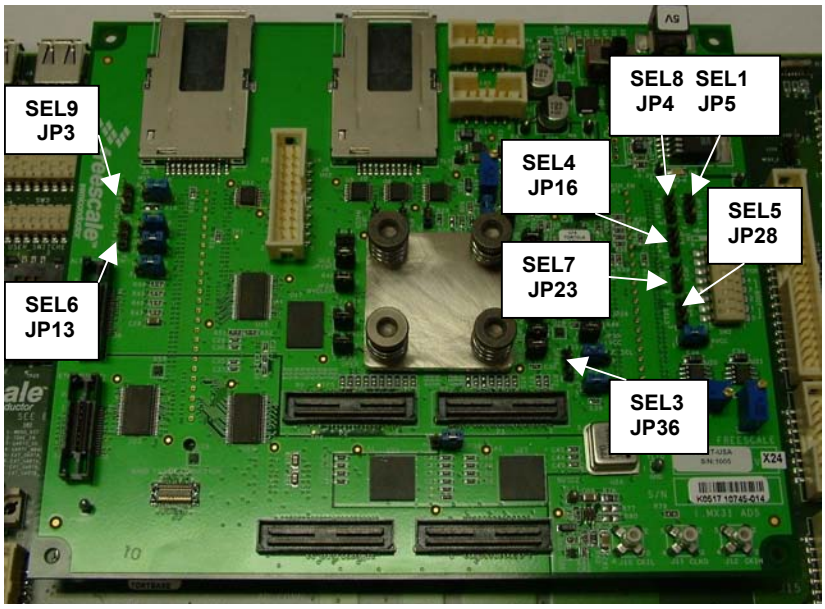

Figure 14. NVCCx Jumper Selection for Power Up using CPU Board

5.1.1.2 QVCC and PLL Voltages to Power Up from CPU

To power up using the CPU regulators, the QVCC and PLL voltages must be configured in addition to the NVCCx jumper configuration. These jumpers are identified in Table 1 and shown in Figure 15.

After the NVCCx and QVCC jumper configurations, the following steps must be ensured:

1. Power to QVCC_ARM = 1.6V ±3% as measured on JP8
2. MC13783 board is not connected to the Baseboard
3. All jumpers are removed under the MC13783 board

Table 1 provides the jumper configurations to power up from the CPU board.

Table 1. CPU Board Jumper Configuration

Jumper	Connection
JP4	2-3
JP5	2-3
JP12	1-2
JP13	1-2

Table 1. CPU Board Jumper Configuration (continued)

Jumper	Connection
JP16	1-2
JP17	1-2
JP20	1-2
JP23	1-2
JP28	2-3
JP32	1-2
JP35	1-2
JP36	2-3
JP38	1-2

Table 2 provides the jumper configurations for the Baseboard.

Table 2. Baseboard Jumper Configuration

Jumper	Connection
JP15	Do Not Jumper
JP16	Do Not Jumper
JP18	Do Not Jumper
JP20	Do Not Jumper
JP21	Do Not Jumper
JP23	Do Not Jumper
JP24	Do Not Jumper
JP25	Do Not Jumper

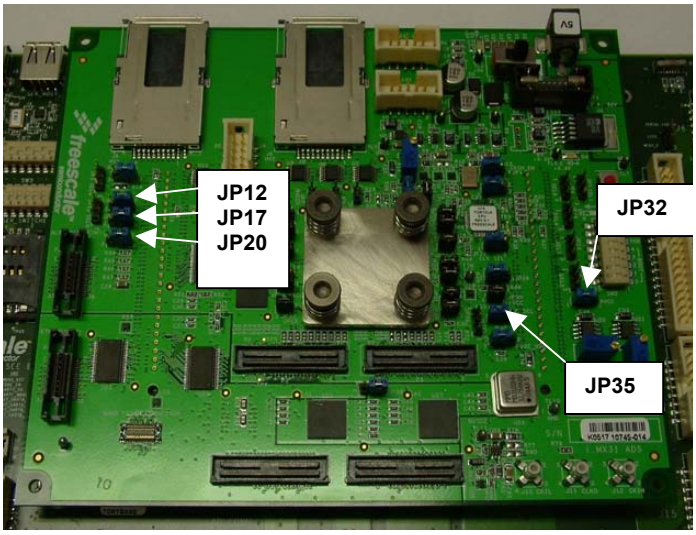

Figure 15. QVCCx and PLL Jumper Selection for Power Up using CPU Board

5.1.2 Power Up from MC13783

The i.MX31ADS factory default settings are set to use the MC13783 board to supply power to the i.MX31 processor. The factory default jumper settings are provided in Section 7, "Factory Defaults" on page 31.

5.1.2.1 NVCCx Voltage to Power Up from MC13783

To select the desired voltage source for the NVCCx power supply, remove the MC13783 board from the Baseboard. Configure the jumpers shown in Figure 16 by setting the jumpers according to the factory default settings in Section 7, "Factory Defaults" on page 31. Information concerning these jumpers also appears on the Baseboard silkscreen where the MC13783 connects. After all jumpers are configured, install the MC13783 as shown in Figure 6.

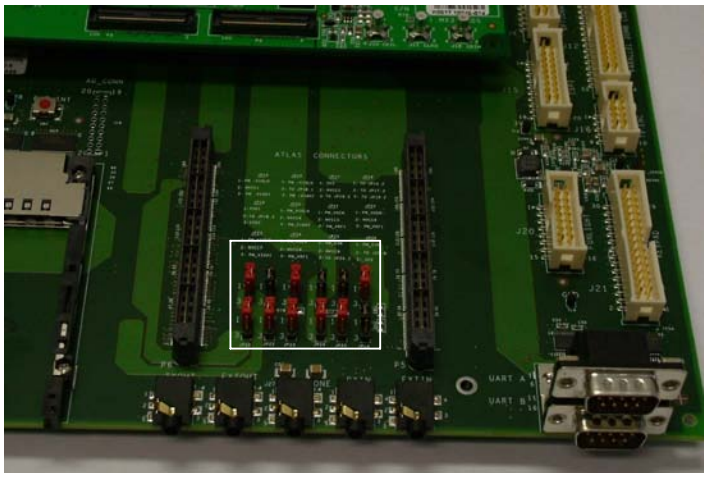

Figure 16. NVCCx Jumper Selection for Power Up using MC13783 Board

5.1.2.2 QVCC and PLL Voltages to Power Up from MC13783

To select the QVCC and PLL voltages for power up using the MC13783, all pins must be jumped using pins 2-3 for JP12 (QARM), JP17 (QPER), JP20 (QL2), JP32 (XVCC), and JP35 (FVCC SEL). The pins 2-3 select the MC13783 power regulators. See jumpers in Figure 15.

5.2 CPU Clock Source Jumper Configuration

To select the desired clock for the CPU, you must first select which clock to enable (high speed or low speed) and then select the source for that clock. Configuration of the non-selected clock input is not critical.

5.2.1 JP22 CPU Clock (CLK_SEL)

- Jumper 1 and 2 to select CKIH (26 MHz)
- Jumper 2 and 3 to select the CKIL (32 KHz)

5.2.2 JP1, 26 MHz Clock Source (CKIH_EN)

- Jumper 1 and 2 to select the onboard 26 MHz oscillator
- Jumper 2 and 3 to select the TV Encoder's oscillator output
- No jumper selects an external source connected to J12

5.2.3 JP26, 32 KHz Clock Source (CKIL_EN)

- Jumper 1 and 2 to select the onboard oscillator
- Jumper 2 and 3 to select the 32 KHz clock out from MC13783 board
- No jumper selects an external source connected to J10

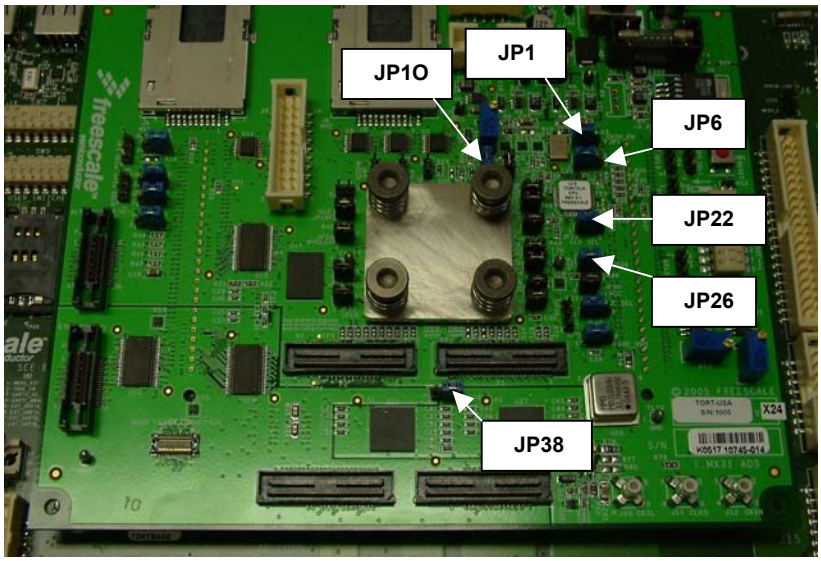

Figure 17. CPU Clock Source Selections

5.3 Remaining CPU Jumper Configuration

The following sections explain how to configure the remaining CPU jumper selections.

5.3.1 JP6, Baseboard LA DATA Enable

- Jumper 1 and 2 to disable Data to Baseboard LA connectors

NOTE
For stand-alone CPU operation, jumper 1-2

- Jumper 2 and 3 to enable Data to Baseboard LA connectors

NOTE
This configuration does not show DRAM bus activity.

5.3.2 JP38, DRAM Power (VDD SEL)

- Jumper 1 and 2 to connect DRAM memory to NVCC2

NOTE
For stand-alone CPU operation, jumper 1-2

- Jumper 2 and 3 to connect DRAM memory to PM_BKUP_DDR.

5.3.3 JP31, SVCC

- Jumper IN connects SVCC to UVCC and MVCC
- Jumper OUT SVCC is floating

NOTE
For normal operation, always have a shunt installed at JP31.

5.3.4 JP10, JTAG Mode (SJC_MOD)

The functions of JP10 in JTAG mode are:

- Jumper IN selects ARM JTAG
- Jumper OUT selects other JTAG

5.3.5 2-Pin Power Jumpers

All other 2-pin jumpers on the CPU Board are used for current measurement points. Measure current by removing the jumper and measuring the voltage drop across the one-ohm resistor provided. These jumpers are not required for normal operation.

5.4 Remaining Baseboard Jumper Configuration

The following sections explain how to configure the remaining Baseboard jumpers.

5.4.1 JP1, HS OTG VUSB Source

- Jumper 1 and 2 to select PHY
- Jumper 2 and 3 to select +5V IN

5.4.2 JP2, HS HOST VUSB Source

- Jumper 1 and 2 to select PHY
- Jumper 2 and 3 to select +5V IN

5.4.3 JP3, SERIAL LCD CS

- Jumper 1 and 2 to select LCS1
- Jumper 2 and 3 to select MCU3_2

5.4.4 JP6 and JP7, I^2C Connection – FS OTG PHY

- Jumper 1 and 2 to select I2C3
- Jumper 2 and 3 to select I2C1

NOTE

IC23 is a secondary function of the CSPI2_CLK and CSPI_SS2 pins. Both JP6 and JP7 must be jumpered the same way.

5.4.5 JP8, NVRAM – Ethernet PHY Enable

- Jumper 1 and 2 enables the NVRAM to the Ethernet PHY
- Jumper 2 and 3 disables the NVRAM to the Ethernet PHY

5.4.6 JP12, Keypad LIGHT SENSE

- Jumper 1 and 2 to select LIGHT SENSE
- Jumper 2 and 3 to select AD5

5.4.7 JP14, 1-Wire Enable

- Jumper IN enables 1-Wire
- Jumper OUT disables 1-Wire

NOTE

JP13 is NOT a jumper. It is the I2C1 connector.

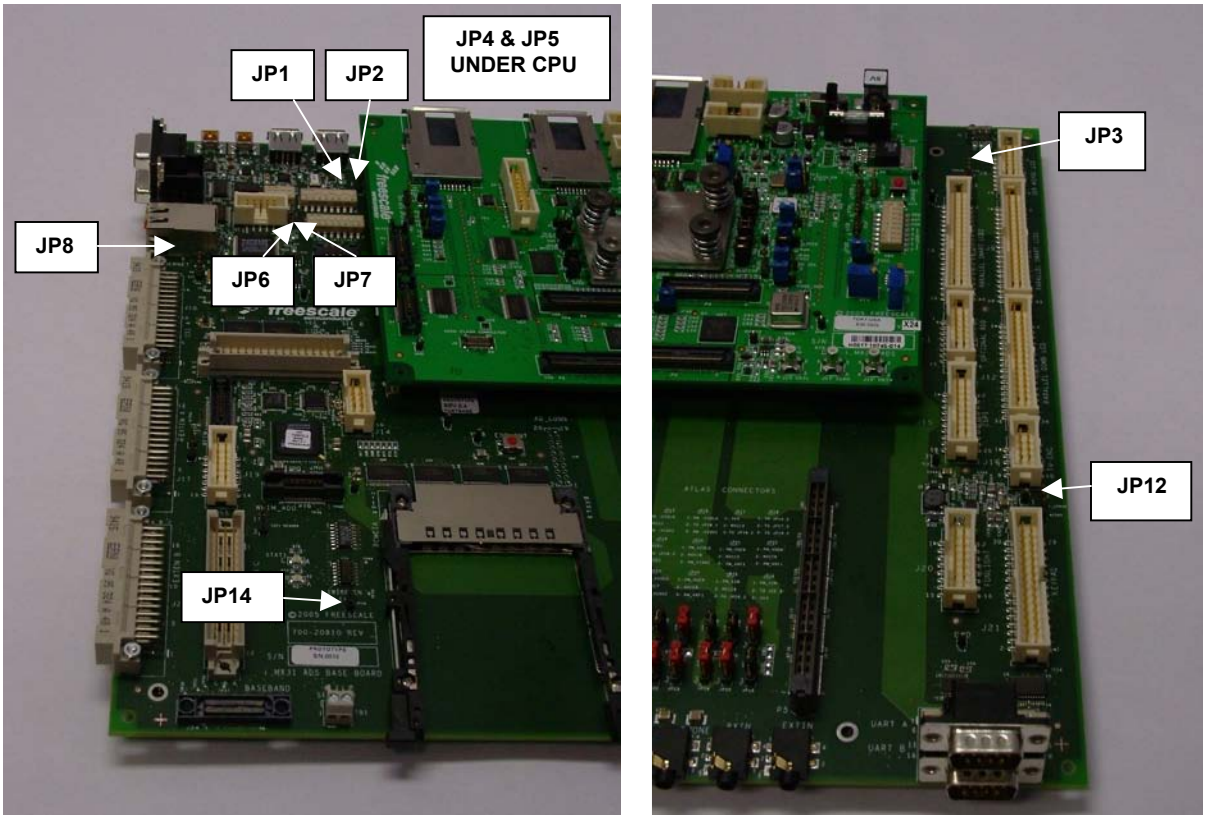

Figure 18. Remaining Baseboard Jumper Configuration

5.5 MC13783 Jumper Configuration

The following sections explain how to configure the MC13783 board jumpers.

5.5.1 JMP2 Vibrator/LED Select

- Jumper 1 and 2 to select Vibrator
- Jumper 2 and 3 to select the D2 LED

5.5.2 JMP4 TXIN Source Select

- Jumper 1 and 2 to select TXOUT from the MC13783 board
- Jumper 2 and 3 to select the source connected to J7

5.5.3 JMP5 and JMP7 SW1 Mode

- Jumper 1 and 2 to select independent operation of SW1A and SW1B
- Jumper 2 and 3 to select combined operation of SW1A and SW1B

NOTE

JMP5 and JMP7 must have the same number pins jumpered. Other settings are invalid and must not be used.

5.5.4 JMP6 and JMP8 SW2 Mode

- Jumper 1 and 2 to select independent operation of SW2A and SW2B
- Jumper 2 and 3 to select combined operation of SW2A and SW2B

NOTE

JMP6 and JMP8 must have the same number pins jumpered. Other settings are invalid and must not be used.

5.5.5 JMP11 BATT Power Source Select

- Jumper 1 and 2 to select the U4 regulator
- Jumper 2 and 3 to select the source connected to CN7

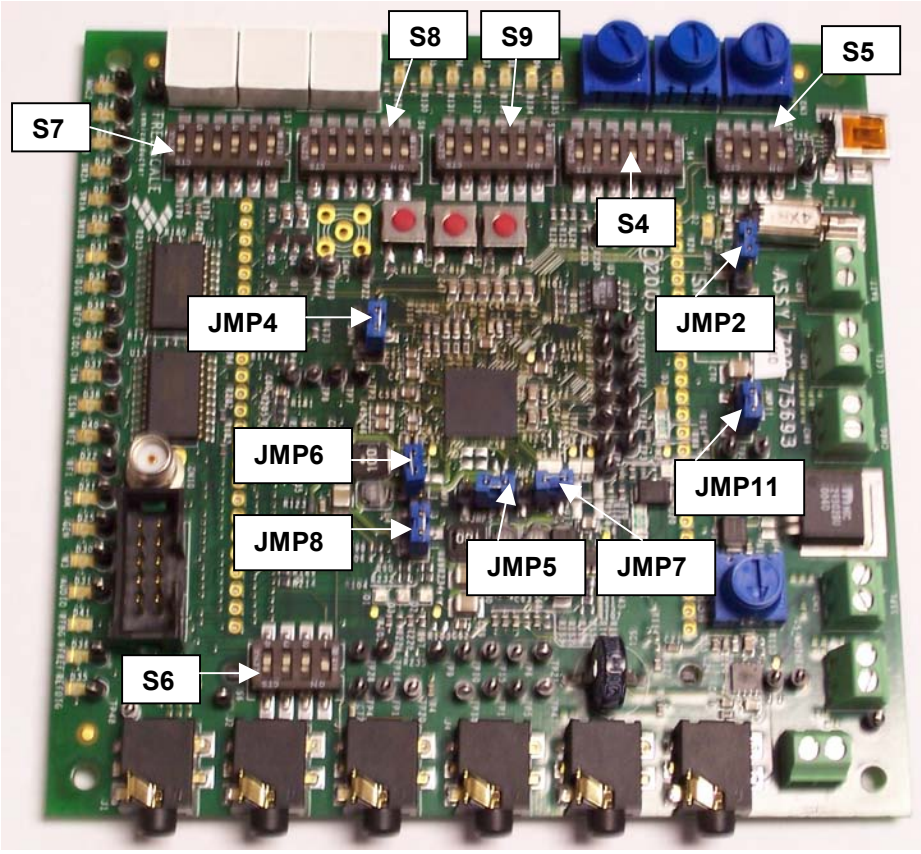

Figure 19. Remaining MC13783 Board Jumper Locations

6 i.MX31ADS Switch Configurations

The following sections explain how to configure the switches for the i.MX31 Application Development System.

6.1 CPU Switches

Figure 20 shows the CPU switch connections which are explained in the following sections.

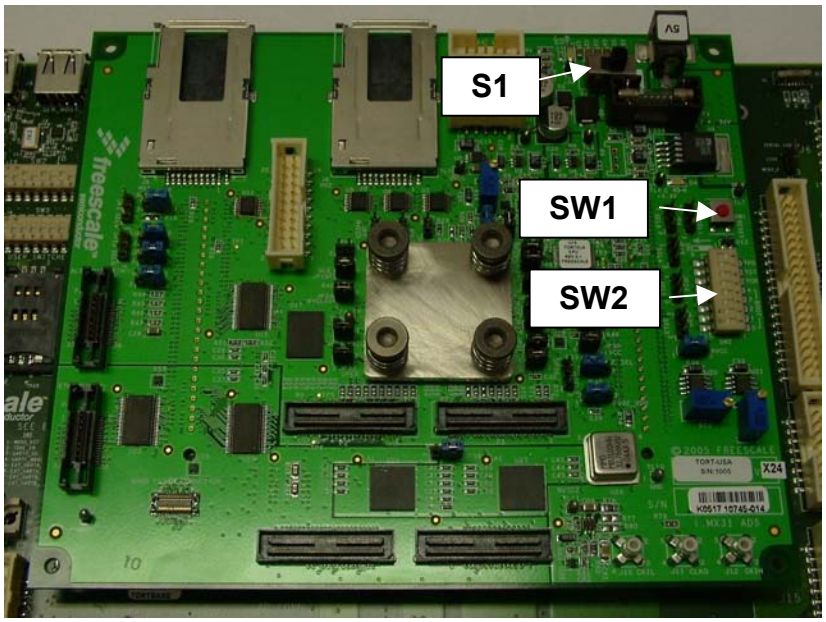

Figure 20. CPU Switches

6.1.1 SW1 RESET Switch

To reset the i.MX31ADS, depress the SW1 RESET switch. The effect of this switch is determine by SW2-6 (See Section 5.1.1.2, “QVCC and PLL Voltages to Power Up from CPU”, and “Section 6.1.2.2.1, “POR RESET, SW2-6”) and SW2-7 (See “Section 5.1.2.1, “NVCCx Voltage to Power Up from MC13783” and Section 6.1.2.2.2, “RESET OUT, SW2-7”.)

6.1.2 SW2 Subswitch Settings

SW2 is an eight-position DIP switch. It controls the Boot Mode, the connection of the output of the Push Button RESET, and tamper detect functions.

6.1.2.1 Boot Mode Switches, SW2-1through SW2-5

The BOOT switches determine where the CPU will begin program execution. Table 3 lists all the valid combinations of the Boot Mode Switches. Other combinations are reserved and must not be used. Table 3 identifies the boot mode switch settings.

Table 3. Boot Mode Switch Settings

Boot Mode Device Boot	BOOT4 SW2-5	BOOT3 SW2-4	BOOT2 SW2-3	BOOT1 SW2-2	BOOT0 SW2-1
UART/USB bootloader	ON	ON	ON	ON	ON
8-bit NAND Flash (2 Kbyte page) internal	ON	ON	ON	ON	OFF
8-bit NAND Flash (512-byte page) internal	ON	ON	ON	OFF	OFF
16-bit NAND Flash (2 Kbyte page) internal	ON	ON	ON	OFF	OFF
16-bit NAND Flash (512-byte page) internal	ON	ON	OFF	ON	ON
16-bit CS0 at D[15:0] internal	ON	ON	OFF	ON	OFF
M-System Disk on Chip	ON	OFF	ON	ON	ON
8-bit NAND Flash (2 Kbyte page) external	OFF	ON	ON	ON	ON
8-bit NAND Flash (512-byte page) external	OFF	ON	ON	ON	OFF
16-bit NAND Flash (2 Kbyte page) external	OFF	ON	ON	OFF	OFF
16-bit NAND Flash (512-byte page) external	OFF	ON	ON	OFF	OFF
16-bit CS0 at D[15:0] external	OFF	ON	OFF	ON	ON
Test mode	OFF	OFF	ON	OFF	OFF

6.1.2.2 Push Button Reset Connection Switches, SW2-6 and SW2-7

The two switches connect the active low reset out of a power on/push button reset component.

6.1.2.2.1 POR RESET, SW2-6

- Setting this switch ON, connects the RESET chip's output to POR of the i.MX31 processor.
- Setting this switch OFF leaves the POR unaffected by the PB RESET circuit.

6.1.2.2.2 RESET OUT, SW2-7

- Setting this switch ON connects the RESET chip's output to RESET_IN of the i.MX31 and RESET _OUT of the system.
- Setting this switch OFF leaves RESET_IN_B and RESET_OUT unaffected by the PB RESET circuit.

6.1.2.3 Tamper Detect, SW2-8

Setting this switch ON presents a 0 (zero) to the GPIO1_6 pin of the i.MX31 to be used as a tamper detect switch.

NOTE

If you do not want to use GPIO1_6 for Tamper Detect, leave SW2-8 off.

6.2 Baseboard Switches

The Baseboard has one four-position DIP switch (SW1) and two eight-position DIP switches (SW2 and SW3). One eight-position switch (SW3) in dedicated to user defined functions. The other two switches configure various features of the Baseboard. Figure 21 shows the Baseboard switches.

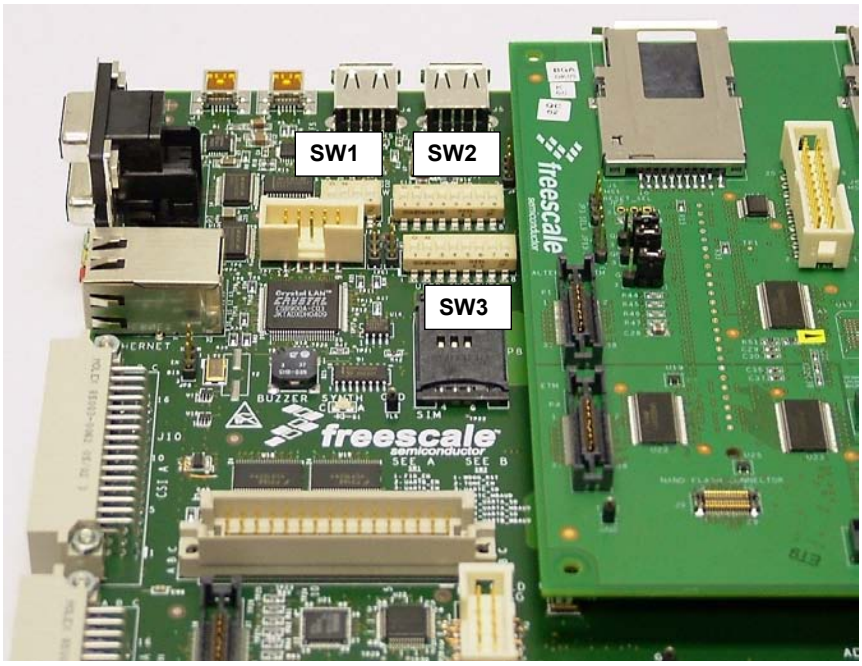

Figure 21. Baseboard Switches

6.2.1 SW1 – UART EN Switches

The SW1, UART Enable switches determine whether UARTA, UARTB, UARTC, and FIR interfaces are active on power up. When active on power-up, they are able to be used immediately by software without configuring the interface. Otherwise they are disabled until they are enabled by software. Each UART channel can connect to two different UART channels from the i.MX31 processor.

Table 4 lists the default UART channels.

Table 4. Baseboard SW1 Settings

Switch Designation	i.MX31 UART Channel Used	Setting	Effect
SW1-1 FIR EN	UART5	ON	Enabled
	None	OFF	Disabled
SW1-2 UARTB EN	UART3	ON	Enabled
	None	OFF	Disabled
SW1-3 UARTA EN	UART1	ON	Enabled
	None	OFF	Disabled

Table 4. Baseboard SW1 Settings (continued)

Switch Designation	i.MX31 UART Channel Used	Setting	Effect
SW1-4 UARTC EN	UART2	ON	Enabled
	None	OFF	Disabled

6.2.2 SW2 – RS-232 MBAUD, Shut Down, WDI, and Buzzer Enable Switches

The RS-232 transceivers used for the external UART channels and the UARTC channel can operate up to 1M BAUD, however they must be configured to do so. Not enabling high-baud-rate operation results is slower edges, which can reduce power and EMI. These transceivers may also be shut down to minimize current.

SW2 also has switches to enable or disable the Watch Dog Reset function to the MC13783 board. When enabled, software must pulse this output within a window of time or the MC13783 board will shut down the system. The Buzzer Enable connects the PWM output to the buzzer circuit. Table 5 provides the SW2 (Baseboard) switch settings.

Table 5. Baseboard SW2 Settings

Switch Designation	Setting	Effect
SW2-1 WDI Enable	ON	Connects the Watch Dog Reset to the MC13783 board
	OFF	Watch Dog Reset is not connected to the MC13783 board
SW2-2 Buzzer Enable	ON	PWM output is connected to the buzzer
	OFF	PWM output is not connected to the buzzer
SW2-3 UARTC Shut Down	ON	UARTC transceiver is shut down
	OFF	UARTC transceiver is enabled
SW2-4 UARTC MBAUD	ON	UARTC baud rate limited to 250kbps
	OFF	UARTC baud rate limited to 1Mbps
SW2-5 Ext UA Shut Down	ON	External UARTA transceiver is shut down
	OFF	External UARTA transceiver is enabled
SW2-6 Ext UA MBAUD	ON	External UARTA Baud Rate limited to 250kbps
	OFF	External UARTA Baud Rate limited to 1Mbps
SW2-7 Ext UB Shut Down	ON	External UARTB transceiver is shut down
	OFF	External UARTB transceiver is enabled
SW2-8 Ext UB MBAUD	ON	External UARTB Baud Rate limited to 250kbps
	OFF	External UARTB Baud Rate limited to 1Mbps

6.2.3 SW3 – USER Defined Switches

The setting of the switches may be read by software to implement user defined functions. These switches will appear on the bits D7–D0 as identified in Table 6.

Table 6. SW3 Switch Settings

Switch Designation	Setting	Effect
SW3-1 User Defined S0	ON	D0 reads low (zero)
	OFF	D0 reads high (one)
SW3-2 User Defined S1	ON	D1 reads low (zero)
	OFF	D1 reads high (one)
SW3-3 User Defined S2	ON	D2 reads low (zero)
	OFF	D2 reads high (one)
SW3-4 User Defined S3	ON	D3 reads low (zero)
	OFF	D3 reads high (one)
SW3-5 User Defined S4	ON	D4 reads low (zero)
	OFF	D4 reads high (one)
SW3-6 User Defined S5	ON	D5 reads low (zero)
	OFF	D5 reads high (one)
SW3-7 User Defined S6	ON	D6 reads low (zero)
	OFF	D6 reads high (one)
SW3-8 User Defined S7	ON	D7 reads low (zero)
	OFF	D7 reads high (one)

6.3 MC13783 Board Switches

The following sections explain how to configure the MC13783 board switches.

6.3.1 S4 – USB OGT Mode, USB OGT Enable, WDI Control

These switches select a mode of operation for the MC13783 board USB transceiver and also to enable it. The Watch Dog Interrupt also known as the Watch Dog Reset function of the MC13783 board can be enabled or disabled. When disabled software does not have to pulse the WDI signal to keep the MC13783 board operating.

Table 7. USB Mode Selections

USB MODE Selected	S4-1	S4-2	S4-3	S4-4
Differential, unidirectional (6 wire)	OFF	OFF	ON	OFF
Differential, bidirectional (4 wire)	ON	OFF	OFF	ON
Single Ended, unidirectional (6 wire)	OFF	ON	OFF	ON

Table 7. USB Mode Selections (continued)

USB MODE Selected	S4-1	S4-2	S4-3	S4-4
Single Ended, bidirectional (4 wire)	OFF	OFF	OFF	ON
All other combinations of S4-1, 2, 3, and 4 are invalid				

Table 8. USB Enable and WDI Settings

Switch Designation	Setting	Effect
S4-5 USBEN	ON	MC13783 board USB OGT transceiver is enabled.
	OFF	MC13783 board USB OGT transceiver is disabled.
S4-6 WDI EN	ON	WDI signal has a pull up (no WDI control required)
	OFF	WDI signal is not pulled up (must be pulsed)

6.3.2 S5 – Li Cell Emulation Switches

S5 is involved with emulation of a lithium battery that is used to back up SDRAM the when main battery power is lost. A super cap is provided on the board as the back up power source. The charging and discharging of the super cap can be controlled by these switches and the ramp up or down can be controlled by variable resistors. There is also an option to connect to an external battery to CN9. If this option is used, all the other S5 switches must be kept OFF.

Table 9. Li Cell Emulation Switches

Switch Designation	Setting	Effect
S5-1 Super Cap Enable	ON	On-board super cap SC1 enabled for back up
	OFF	On board super cap SC1 disabled for back up
S5-2 Li Cell Enable	ON	External Li Cell enabled for back up
	OFF	External Li Cell disabled for back up
S5-3 SC1 Charge Enable	ON	Allows SC1 to be charged
	OFF	Disables SC1 changing
S5-4 SC1 Discharge	ON	Discharges SC1
	OFF	SC1 is not discharged

- R150 sets the peak voltage that SC1 will charge to.
- R108 sets the charging ramp for SC1 to the voltage set by R150.
- R26 sets the rate of discharge for SC1 when S5 – 4 is closed.

NOTE

Leave S5-1, S5-3, and S5-4 OFF if a real Li Cell is being used.

6.3.3 S6 – USB Signal Direction Control Switches

Table 10. USB Signal Direction Switches

Switch Designation	Setting	Effect
S6-1 Bidirectional Selection	ON	UTXENB can control USB signal direction
	OFF	UTXENB does not control signal direction
S6-2 Unidirectional Selection	ON	UDATVP and USEOVM flow toward the i.MX31
	OFF	UDATVP and USEOVM control selected by S6-1
S6-3	X	Not used
S6-4	X	Not used

6.3.3.1 S7 – Digital Audio Direction Switches

The Frame Sync and the Bit Clock for the Primary (1) and Secondary (2) digital audio interfaces are bidirectional or unidirectional depending on the application. S7 switches determine the direction or enable GPO direction control, as identified in Table 11.

Table 11. Frame Sync and Bit Clock Direction Control Switches

Switch Designation	Setting	Effect
S7-1 FS1 and BCL1 DIR	ON	Signal direction controlled by GP02
	OFF	If S7-2 OFF, FS1 and BCL1 flow from i.MX31
S7-2 FS1 and BCL1 DIR	ON	FS1 and BCL1 signals flow toward the i.MX31
	OFF	Enable S7-1 control
S7-3 FS2 and BCL2 DIR	ON	Signal direction controlled by GP01
	OFF	If S7-4 OFF, FS2 and BCL2 flow from i.MX31
S7-4 FS2 and BCL2 DIR	ON	FS2 and BCL2 signals flow toward the i.MX31
	OFF	Enable S7-3 control
S7-5 Digital Audio 2 EN	ON	Enable TX2, FS2 and BCL2 buffers
	OFF	Disable TX2, FS2 and BCL2 buffers
S7-6 Digital Audio 1 EN	ON	Enable TX1, FS1 and BCL1 buffers
	OFF	Disable TX1, FS1 and BCL1 buffers

6.3.3.2 S8 – CLIA and CLIB (Audio Clock) Selects

The MC13783 board uses the Clock In signals A and B for the Stereo DAC or the Voice CODEC. From the Baseboard the CLIA signal is the 14.7 MHz clock for the DUART and CLIB signal is the CLKO output of the i.MX31. There is also a SMA connector, CN10, which may be selected as a clock source. S8 routes any of these sources to the CLIA and CLIB pins of the i.MX31.

Table 12. CLIA and CLIB Source Select Switches

Switch Designation	Setting	Effect
S8-1 CLIA enable A	ON	Select CLIA signal to CLIA pin of the MC13783 board
	OFF	CLIA not connected to CLIA of the MC13783 board
S8-2 CLIA enable B	ON	Select CLIA signal to CLIB pin of the MC13783 board
	OFF	CLIA not connected to CLIB of the MC13783 board
S8-3 CLIB enable A	ON	Select CLIB signal to CLIA pin of the MC13783 board
	OFF	CLIB not connected to CLIA of the MC13783 board
S8-4 CLIB enable B	ON	Select CLIB signal to CLIB pin of the MC13783 board
	OFF	CLIB not connected to CLIB of the MC13783 board
S8-5 CN10 enable A	ON	CLIA pin of the MC13783 board is connected to CN10
	OFF	CLIA pin of the MC13783 board is not connected to CN10
S8-6 CN10 enable B	ON	CLIB pin of the MC13783 board is connected to CN10
	OFF	CLIB pin of the MC13783 board is not connected to CN10

NOTE

For S8-1, S8-3, and S8-5 only one switch ON at a time is allowed. The same applies to the S8-2, S8-4, and S8-6 group.

6.3.3.3 S9 – Power-Up Mode Select Switches

There are three power-up mode select (PUMS) bits. Each bit has a pair of S9 switches that configure them. The PUMS bits have three valid states, ON, OFF and OPEN. The PUMS3 bit controls the power on sequence that the enabled voltages will follow. The PUMS2 and PUMS1 switches determine which voltages will be available and at what voltage levels. For any switch pair, do not set both switches ON. This will waste VATLAS power. See Chapter 5 of the MC13783 Power Management and Audio reference manual to determine the effect of these switch settings.

Table 13 provides the PUMSX switch settings, while Table 14 provides the PUMS settings.

Table 13. PUMSX Switch Settings

S9-B	S9-A	PUMSX
OFF	OFF	Open
OFF	ON	Ground
ON	OFF	VATLAS
ON	ON	Do not use

Table 14. PUMS Switch Assignments

S9-B	S9-A	PUMSX
S9-2	S9-1	PUMS1
S9-4	S9-3	PUMS2
S9-6	S9-5	PUMS3

7 Factory Defaults

The i.MX31ADS is configured to be powered from the MC13783 Power Management and Audio board.

- CPU board jumper part number: 700-20810
- DIP SWITCH (SW2): 1, 2, 4, 6, 7 ON; 3, 5, 8 OFF

The CPU factory jumper configurations are provided in Table 15.

Table 15. CPU Board Factory Jumper Configuration

Jumper	Connection
JP1	1-2
JP4	Don't Place a jumper
JP5	Don't Place a jumper
JP6	1-2
JP7	Put Jumper
JP8	Put Jumper
JP9	Put Jumper
JP10	Put Jumper
JP11	Put Jumper
JP12	2-3
JP13	Don't Place a jumper
JP14	Put Jumper
JP15	Put Jumper
JP16	Don't Place a jumper
JP17	2-3
JP18	Put Jumper
JP19	Put Jumper
JP20	2-3
JP21	Put Jumper
JP22	1-2
JP23	Don't Place a jumper

Table 15. CPU Board Factory Jumper Configuration (continued)

Jumper	Connection
JP24	Put Jumper
JP25	Put Jumper
JP26	1-2
JP27	Put Jumper
JP28	Don't Place a jumper
JP29	Put Jumper
JP30	Put Jumper
JP31	Put Jumper
JP32	2-3
JP33	Put Jumper
JP34	Put Jumper
JP35	2-3
JP36	Don't Place a jumper
JP38	2-3

Table 16 provides the Baseboard jumper and switch configuration. The Baseboard jumper part number is 700-20811.

Table 16. Baseboard Factory Jumper and Switch Configuration

Jumper or Switch	Jumper Description	Default Settings
JP1	VREF5V OTG	2-3
JP2	VREF5V HSH	2-3
JP3	SERLCD_CS	1-2
JP6	I2CX_SCL	2-3
JP7	I2CX_SDA	2-3
JP8	Ethernet NVRAM select	1-2
JP12	LIGHT_SENSE	1-2
JP14	1-Wire	Put jumper
JP15	NVCC1 select	1-2
JP16	Power select	2-3
JP18	Power select	1-2
JP19	Power select	Not assembled
JP20	NVCC4 select	1-2

Table 16. Baseboard Factory Jumper and Switch Configuration (continued)

Jumper or Switch	Jumper Description	Default Settings
JP21	NVCC5 select	2-3
JP22	NVCC6 select	2-3
JP23	NVCC7 select	2-3
JP24	NVCC8 select	2-3
JP25	NVCC9 select	2-3
JP26	NVCC6,NVCC9 power source select	1-2
SW1	Dip switch (1-4)	OFF, OFF, OFF, OFF
SW2	Dip switch (1-8)	ON, ON, OFF, ON, OFF, ON, OFF, ON
SW3	Dip switch (1-8)	OFF, OFF, OFF, ON, ON, ON, ON, OFF

Table 17 provides the MC13783 Power Management and Audio board jumper and switch configurations. The MC13783 jumper part number is 700-20812.

Table 17. MC13783 Factory Jumper and Switch Configuration

Jumper or Switch	Default Settings
JMP2	1-2
JMP11	1-2
JMP5	2-3
JMP7	2-3
JMP4	1-2
JMP6	1-2
JMP8	1-2
S7	OFF, OFF, OFF, OFF, ON, ON
S8	ON, OFF, OFF, OFF, ON, OFF
S9	OFF, OFF, ON, OFF, OFF, OFF
S4	OFF, ON, OFF, ON, OFF, OFF
S5	All OFF
S6	OFF, ON, OFF, OFF