- Series inductance cancels out capacitance.
- Tie the capacitors to the GND plane directly with a via.
- Place the capacitors close to the power contact of the associated package designed from the schematic.

An example of good design practices for the BGA power decoupling design is the layout of the i.MX 7ULP EVK available on the NXP website upon product release. Contact your local sales office or field applications engineer to check the availability of information before product releases.

3.3. Stack-up recommendations

A high-speed design requires a good stack-up to have the right impedance for the critical traces. The constraints for the trace width may depend on several factors, such as the board stack-up and associated dielectric and copper thickness, required impedance, and required current (for power traces). The NXP reference design uses a minimum trace width of 3 mils for the DDR routing. The stack-up also determines the constraints for routing and spacing.

Consider the following when designing a stack-up and selecting material for your board:

- Board stack-up is critical for high-speed signal quality.
- Preplan the impedance of critical traces.
- High-speed signals must have reference planes on adjacent layers to minimize cross-talk.
- NXP i.MX 7ULP EVK equals Isola IT-180A.

The recommended stack-up for the 14 mm x 14 mm VP package is four to six layers. i.MX 7ULP EVK uses four layers. The stack-up information for i.MX 7ULP EVK is shown in Table 15 and Table 16.

Table 15. I.MX 7ULP EVK PCB stack-up information

Layer	Layer type	Finished copper weight
1	Top (component) side	1/2 oz
2	Ground plane	1 oz
3	Power plane	1 oz
4	Bottom side	1/2 oz

Table 16. i.MX 7ULP EVK PCB stack-up implementation

Layers	Single-ended		Differential					
	Trace width (mils)	Impedance (Ω)	Trace width (mils)	Trace spacing 'airgap' (mils)	Impedance (Ω)	Trace width (mils)	Trace spacing 'airgap' (mils)	Impedance (Ω)
TOP	4	50	4.5	4	90	3.9	5	100
BOTTOM	4	50	4.5	4	90	3.9	5	100

The recommended stack-up for the 10 mm x 10 mm VK package is eight layers (two ground planes, two power planes, and four signal layers).

3.4. DDR connection information

Figure 1 shows the block diagram of the LPDDR2/LPDDR3 interface of i.MX 7ULP EVK.

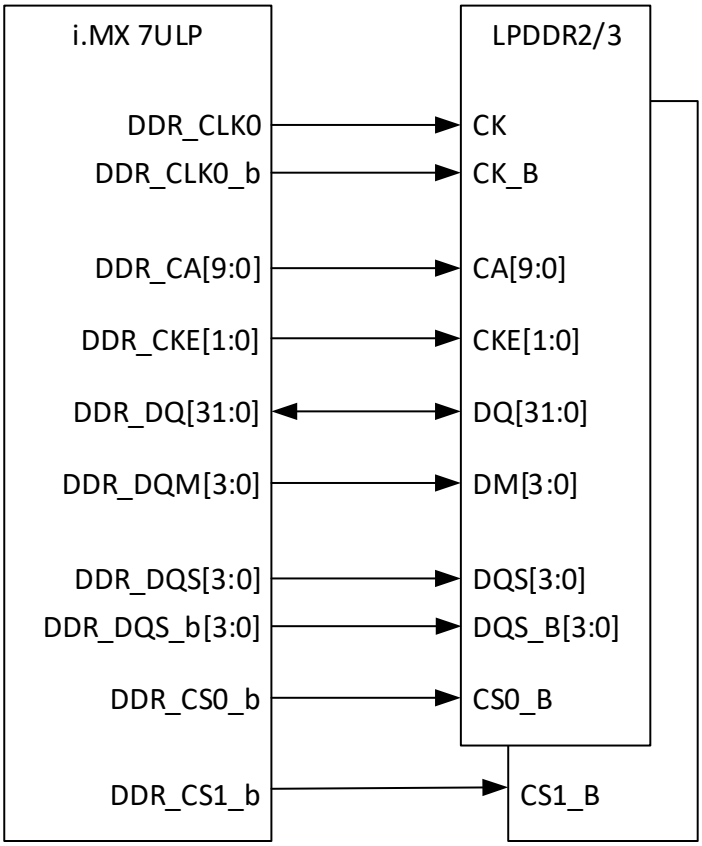

Figure 1. LPDDR2/LPDDR3 interface connections

3.4.1. DDR routing rules

The LPDDR2/3 routing can be accomplished in two different ways: routing all signals at the same length or routing them by the byte group.

Routing all signals at the same length can be more difficult because of the tight space between the DDR and the processor and the large number of required interconnections. However, it is the better way because it makes the signal-timing analysis straightforward. Ideally, all the signals should be routed at the same length. Table 17 explains the rules for routing the signals by the same length.

Table 17. DDR routing by the same length

Signals	Total length	Recommendations
Address and bank	Clock length	Match the signals ±25 mils of the value specified in the length column.
Data and buffer	Clock length	Match the signals ±25 mils of the value specified in the length column.
Control signals	Clock length	Match the signals ±25 mils of the value specified in the length column.
Clock DDR_CLK0 and DDR_CLK0_b	Longest trace ≤ 3 inches	Match the signals for the differential clock pair within ±5 mils.
DDR_DQS[3:0] and DDR_DQS_b[3:0]	Clock length	Match the DQS signals ±10 mils of the value specified in the length column.

Routing by a byte group requires a better control of the signals in each group. It is also more difficult for the analysis and constraint settings. However, its advantage is that the constraint to match the lengths can be applied to a smaller group of signals. This is often more achievable when the constraints are properly set. Table 18 explains the rules for routing the signals by byte groups.

Table 18. LPDDR2/LPDDR3 routing by byte groups

Chip signals	Group	Length (mils)		Recommendations
		Min	Max	
DDR_CLK0 DDR_CLK0_b	Clock	As short as possible	2.25 inches	Match the signals ±5 mils. 2.25 inches is recommended.
DDR_CA[9:0] DDR_RAS DDR_CAS DDR_SDWE	Address and command	Clock (min) – 200	Clock (min)[1]	Match the signals ±25 mils.
DDR_D[7:0] DDR_DQM0 DDR_SDQS0 DDR_SDQS0_b	Byte group 1	—	Clock (min)	Match the signals of each byte group ±25 mils. Match the differential signals of the DQS ±10 mils.
DDR_D[15:8] DDR_DQM1 DDR_SDQS1 DDR_SDQS1_b	Byte group 2	—	Clock (min)	
DDR_D[23:16] DDR_DQM2 DDR_SDQS2 DDR_SDQS2_b	Byte group 3	—	Clock (min)	
DDR_D[31:24] DDR_DQM3 DDR_SDQS3 DDR_SDQS3_b	Byte group 4	—	Clock (min)	
DDR_CA[9:0] DDR_CKE[1:0] DDR_CS0_b DDR_CS1_b	Control signals	Clock (min) – 200	Clock (min)	Match the signals ±50 mils.

1. Clock (min) — The shortest length of the clock group signals because this group has a ±5 mil matching tolerance.

3.5. High-speed routing recommendations

The following list provides the recommendations for routing the traces of high-speed signals. Note that the propagation delay and the impedance control must match to achieve correct communication with the devices.

- High-speed signals must not cross gaps in the reference plane.
- Avoid creating slots, voids, and splits in the reference planes. Review the via voids to ensure they do not create splits (space out vias).
- Provide the ground return vias within a 100 mil distance from the signal layer-transition vias when transitioning between different reference ground planes.
- A solid ground plane must be directly under the crystal, associated components, and traces.
- Separate the parallel running traces by not less than 2x the dielectric width to the referenced ground plane.
- The clocks or strobes that are on the same layer need at least 2.5x the spacing from an adjacent trace (2.5x the height from a reference plane) to reduce cross-talk.
- All synchronous modules must have bus-length matching and relative clock-length control.
- If space is available, consider routing the pairs of high-speed signals together with a ground trace in between. The ground trace serves as a direct ground-return path. This technique is known as routing “triplets”.

For SD/eMMC interfaces:

- Match the data and the CMD trace lengths (the length delta depends on the bus rates).
- CLK must be longer than the longest signal in the data/CMD group (+5 mils).
- Similar DDR rules must be followed for data, address, and control, as for the SD module interfaces.

The following signals on the i.MX 7ULP are considered high-speed signals and must be routed according to the requirements stated in this document:

- MMDC signals (LPDDR2/LPDDR3 interface).
- USB OTG signals:
  - USB0_DP/USB0_DP (differential pair).
- USB HSIC signals:
  - HSIC_DATA.
  - HSIC_STROBE.
- MIPI DSI signals (MIPI display serial interface):
  - DSI_CLK_P/DSI_CLK_N (differential pair).
  - DSI_DATA0_P/DSI_DATA0_N (differential pair).
  - DSI_DATA1_P/DSI_DATA1_N (differential pair).
- uSDHC signals (SD/eMMC interfaces).

3.5.1. Ground plane recommendations

This section provides examples of good practices and how to avoid common mistakes when flowing the ground planes' layers. Figure 2 and Figure 3 show examples of common poor GND planes.

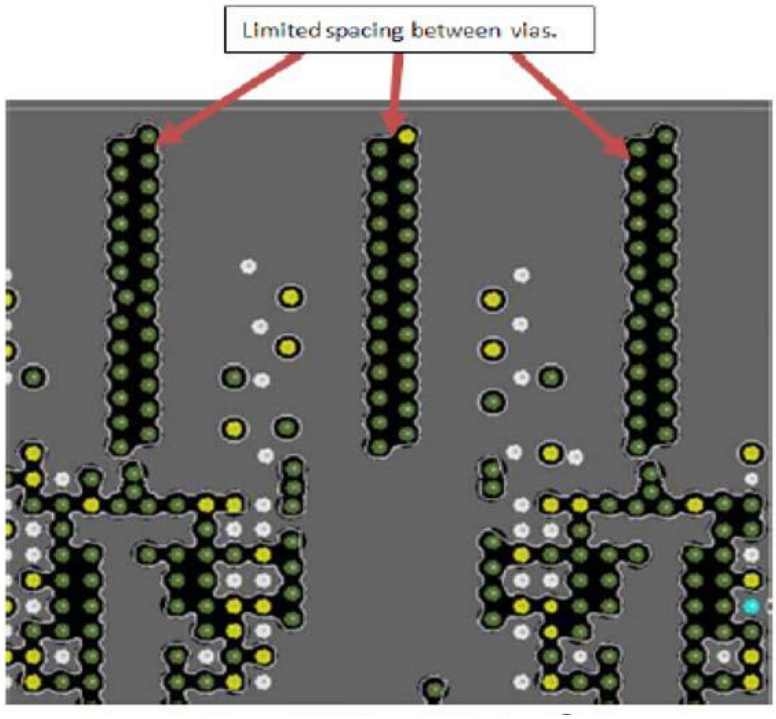

Figure 2. Poor GND plane 1

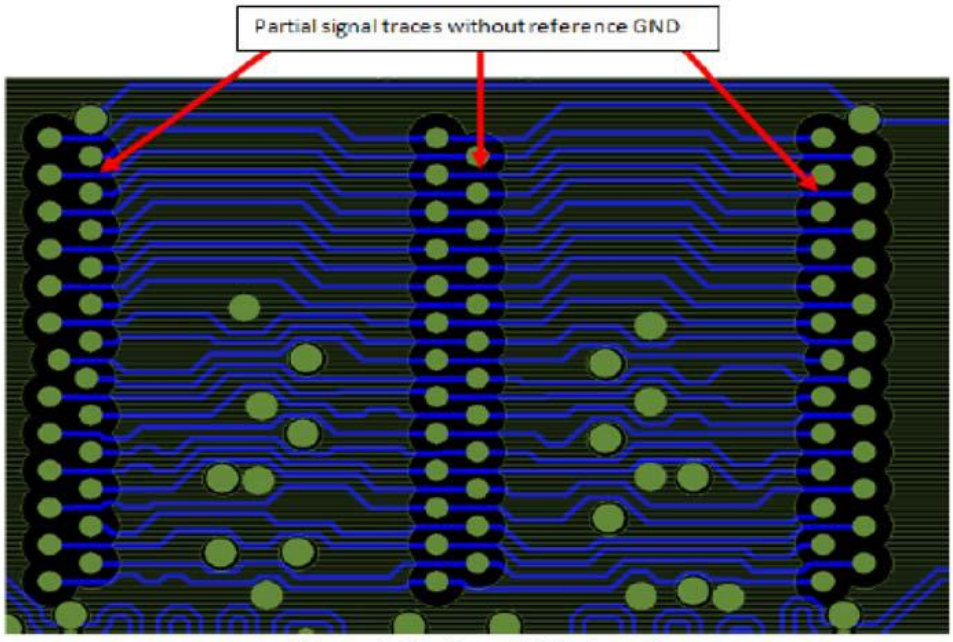

Figure 3. Poor GND plane 2

Spacing the vias some mils apart facilitates the GND copper flowing in the plane. Figure 4 and Figure 5 show good practices of GND planes.

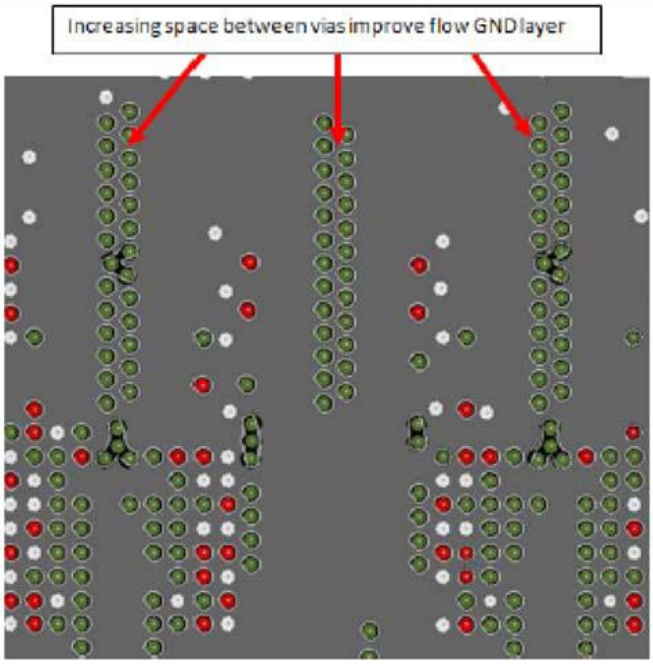

Figure 4. Good layout GND plane detail

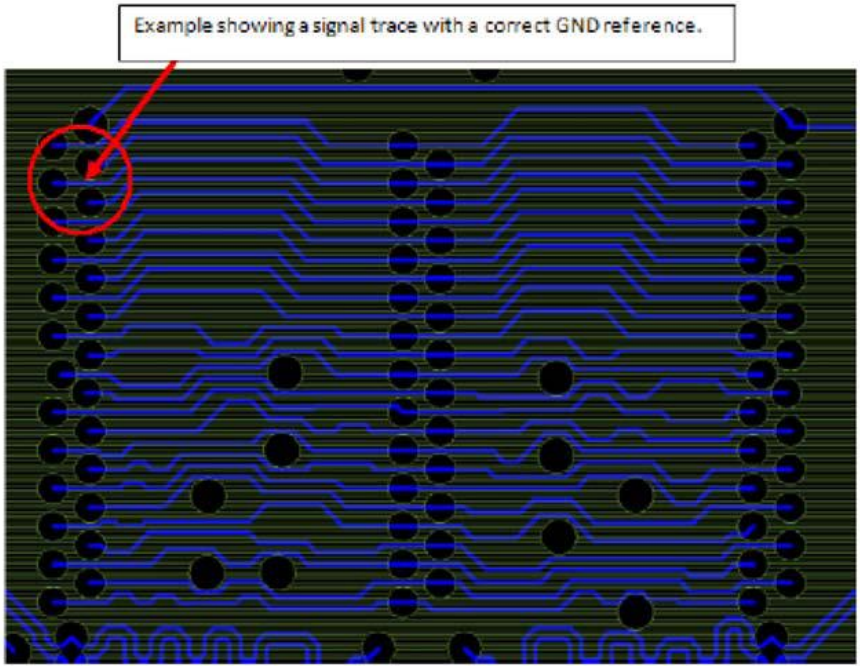

Figure 5. Good layout GND plane detail

3.6. DDR power recommendations

These recommendations apply to the DDR_VREF voltage reference plane:

- Use a 30 mil trace between the decoupling cap and the destination.
- Maintain a 25 mil clearance from other nets.
- Isolate the VREF and/or shield with GND.

Decouple using distributed 0.22 µF capacitors by the regulator, controller, and devices.

- Place 1.0 µF capacitors near the VREF source. One near the VREF pin on the controller and two between the controller and the devices.

3.7. USB recommendations

Follow these recommendations for the USB:

- Route the high-speed clocks and the DP and DM differential pair first.
- Route the DP and DM signals on the top or bottom layer of the board.
- The trace width and spacing of the DP and DM signals must meet the differential impedance requirement of 90 Ω.
- Route the traces over the continuous planes (power and ground).
  - Traces must not pass over any power/ground-plane slots or anti-etch.
  - When placing the connectors, make sure that the GND plane clear-outs around each pin have ground continuity between all pins.
- Maintain the parallelism (skew matching) between DP and DM, and match the overall differential length difference to less than 5 mils.
- Maintain symmetric routing for each differential pair.
- Do not route the DP and DM traces under the oscillators or parallel to the clock traces and/or data buses.
- Minimize the lengths of high-speed signals that run in parallel to the DP and DM pair.
- Keep the DP and DM traces as short as possible.
- Route the DP and DM signals with a minimum number of corners. Use 45-degree turns instead of 90-degree turns.
- Avoid layer changes (vias) on the DP and DM signals. Do not create stubs or branches.
- Provide the ground return vias within a 50 mil distance from the signal layer-transition vias when transitioning between different reference ground planes.

3.8. Impedance signal recommendations

Use Table 19 as a reference when updating or creating constraints in your software PCB tool to set up the impedance and the correct trace width.

Table 19. Impedance signal recommendations

Signal group	Impedance	Layout tolerance
All signals, unless specified	50 Ω single-ended	±10%

Signal group	Impedance	Layout tolerance
Differential signals: USB and MIPI DSI	90 Ω differential	±10%
Differential signals: DDR	100 Ω differential	±10%

Figure 6 shows the dimensions of a stripline and a microstrip pair. Figure 7 shows the differential pair routing.

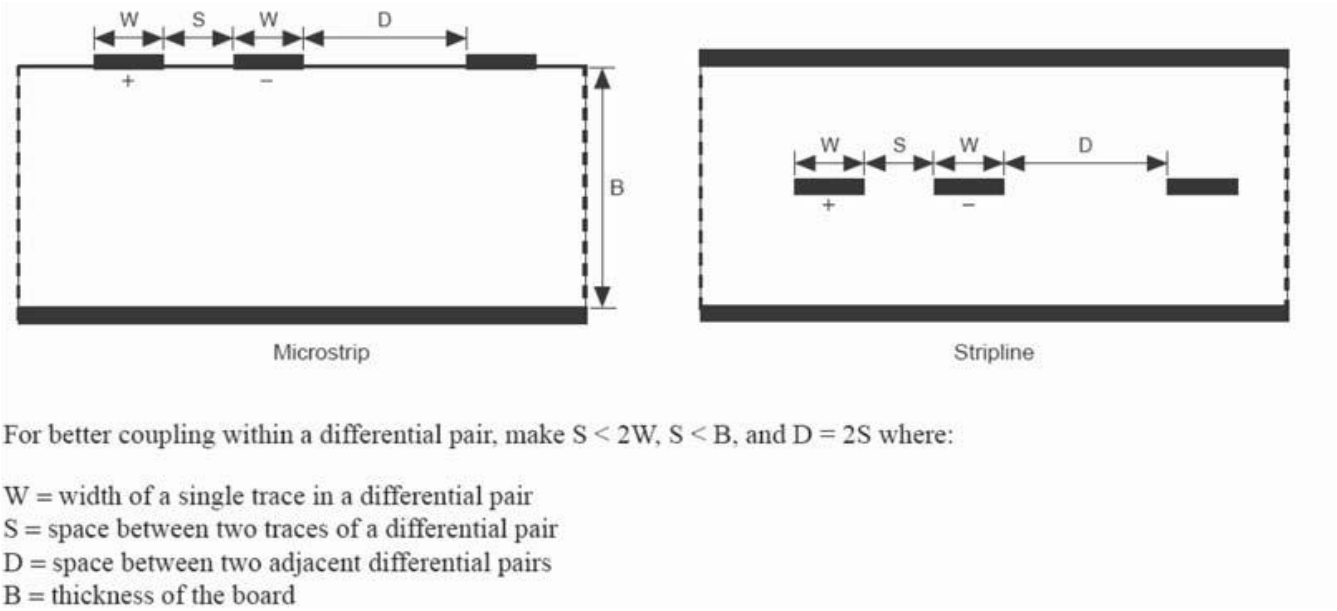

Figure 6. Microstrip and stripline differential pair dimensions

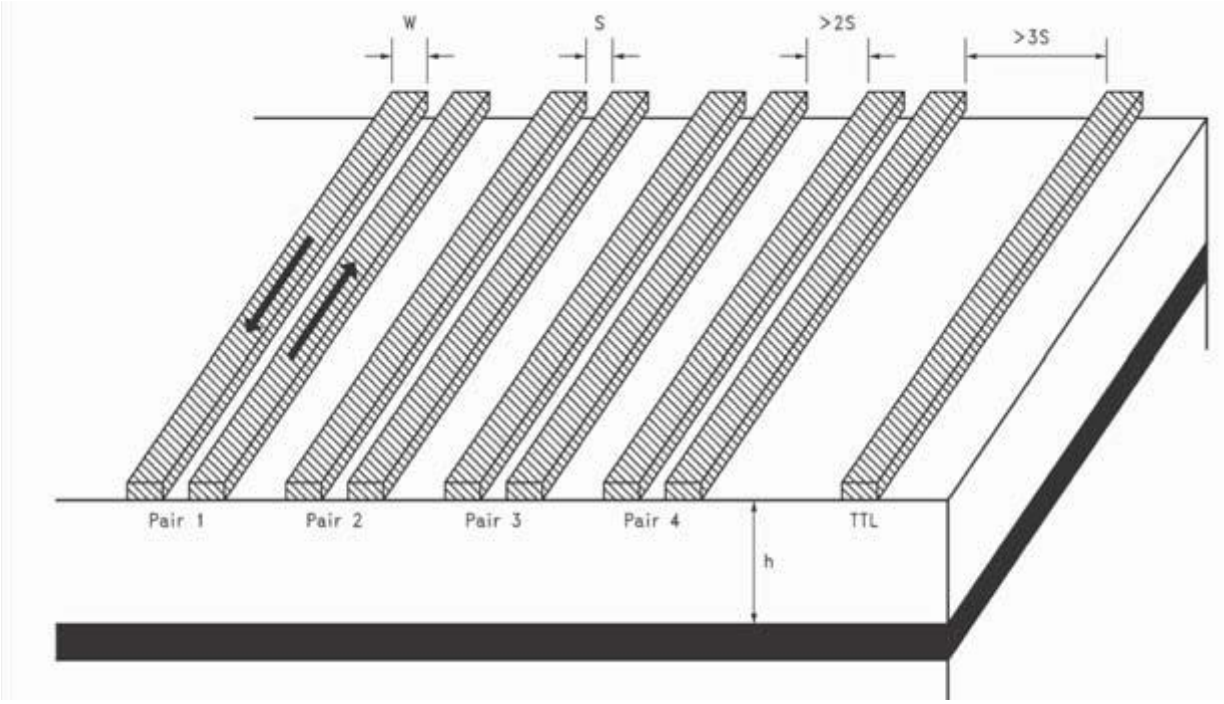

Figure 7. Differential pair routing

- The space between two adjacent differential pairs must be greater than or equal to twice the

space between the two individual conductors.

- The skew between the LVDS pairs must be within the minimum recommendation (±100 mils).

3.9. Reference resistors

NOTE

The reference resistor and the connection must be placed away from noisy regions. The noise induced on it may impact the internal circuit and degrade the interface signals.

3.10. ESD and radiated emissions recommendations

The PCB design must use solid power and ground planes. The recommendations for ESD immunity and radiated emissions performance are as follows:

- All components with ground chassis shields (USB jack, buttons, and so on) must connect the shield to the PCB chassis ground ring.
- Ferrite beads must be placed on each signal line connected to an external cable. These ferrite beads must be placed as close to the PCB jack as possible.

NOTE

Ferrite beads must have a minimum impedance of 500 Ω at 100 MHz (except for the ferrite on USB0 VBUS).

- Ferrite beads must not be placed on the USB DP/DM signal lines, because this can cause USB signal integrity problems. For radiated emissions problems due to USB, a common-mode choke can be placed on the DP/DM signal lines. However, it should not be required if the PCB layout is satisfactory. Ideally, the common-mode choke must be approved for high-speed USB use or tested thoroughly to verify that there are no signal integrity issues.
- It is highly recommended to use ESD protection devices on the ports connected to external connectors. See the reference schematic (available at www.nxp.com) for detailed information about the ESD protection implementation on USB interfaces.
- If possible, stitch all around the board with vias with a 100-mil spacing between them, and connect the vias to the GND planes with exposed solder mask to improve EMI.

3.11. Component placement recommendations

Adhere to these recommendations when placing components:

- Place the components in such way that short and/or critical routes can be easily laid out:
  - Critical routes determine the component location.
  - Position the devices to facilitate routes (minimize the length and crossovers).
- Consider placing these pairings adjacent:
  - i.MX and DDR.
  - PHY and associated jack.

- Jack and CODEC input.
- Bluetooth® (or other RF) and antenna.

3.12. Reducing skew and phase problems in deferential pairs' traces

The differential pair technology has evolved to require more stringent checking around phase control. This is evident from the higher data rates associated with parallel buses (such as DDR and LVDS). Simply put, the differential pair technology sends opposite and equal signals down a pair of traces. Keeping these opposite signals in phase is essential to ensure that they work as intended.

Figure 8 and Figure 9 show two examples of static routing where a match is achieved without the need to tune one element of the differential pair.

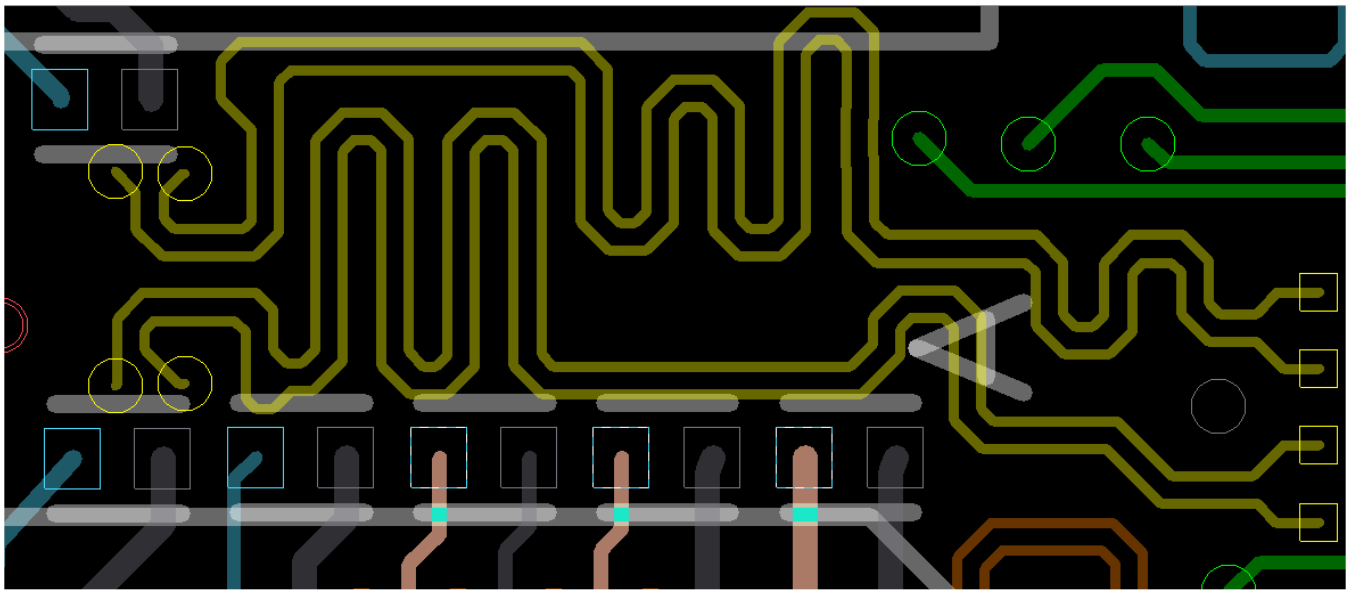

Figure 8. Yellow traces differential pairs 1

Figure 9 shows the addition of a delay trace to one element of the differential pair to avoid length mismatch (which reduces skew and phase problems). The green box marks the detail.

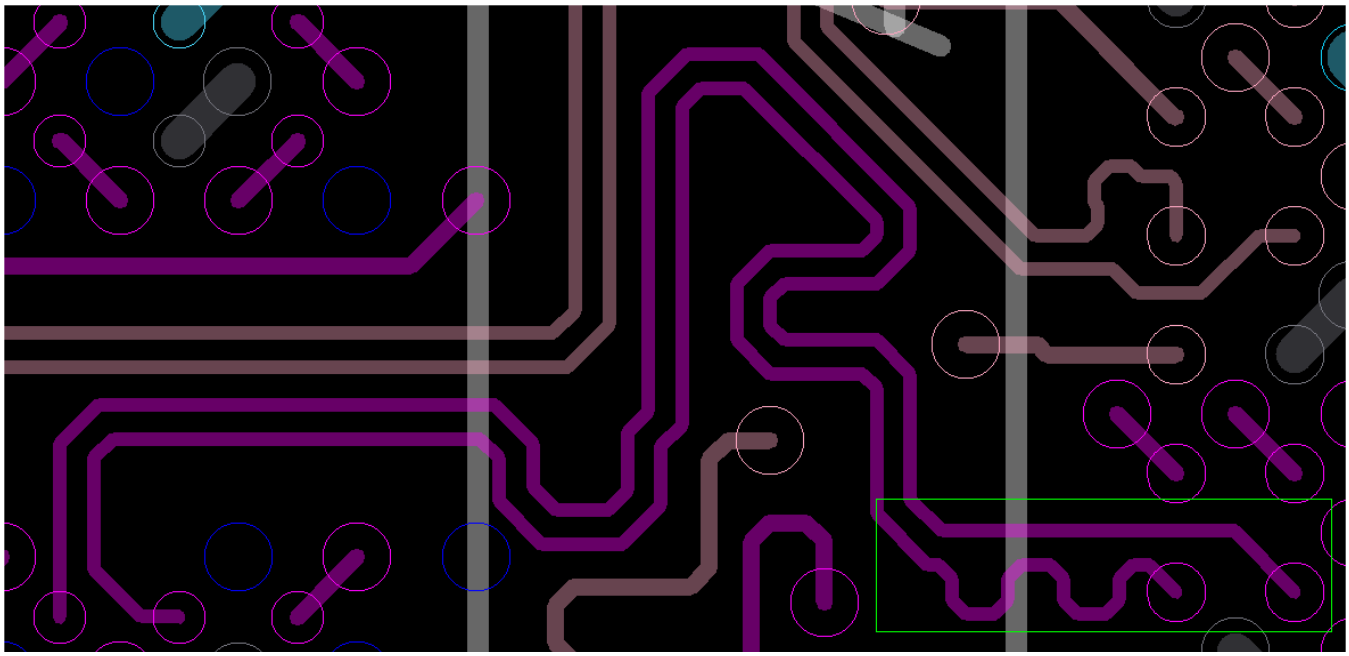

Figure 9. Small bumps added to the shorter differential pair

4. Avoiding board bring-up problems

4.1. Introduction

This chapter provides recommendations for avoiding typical mistakes when bringing up a board for the first time. These recommendations consist of basic techniques that have proven useful in the past for detecting board issues and addressing the three most typical bring-up pitfalls: power, clocks, and reset. A sample bring-up checklist is provided at the end of the chapter.

4.2. Using current monitor to avoid current pitfalls

Excessive current can damage the board. Avoid this problem by using a current-limiting laboratory supply set to the expected typical main current draw (at most). Monitor the main supply current with an ammeter when powering the board for the first time. The power supply's internal ammeter can be used (if it has one). By monitoring the main supply current and controlling the current limit, any excessive current can usually be detected before a permanent damage occurs.

4.3. Using current monitor to avoid voltage pitfalls

Using incorrect voltage rails is a common power pitfall. To avoid this mistake, create a basic table called "voltage report" before bringing up your board. This table helps you to validate that all the supplies are reaching the expected levels.

To create a voltage report, list the following:

- Board voltage sources.
- Default power-up values for the board voltage sources.
- The best location on the board to measure the voltage level of each supply.

Carefully determine the best measurement location for each power supply to avoid a large voltage drop (IR drop) on the board, which causes inaccurate current values to be measured. These guidelines help to produce the best current measurements:

- Measure as close to the load (in this case the i.MX 7ULP processor) as possible.
- Make two measurements: the first after the initial board power-up and the second while running a heavy use-case that stresses the i.MX 7ULP processor.

Ensure that the supplies that power the i.MX 7ULP meet the DC electrical specifications listed in the chip-specific data sheet.

Table 20. Voltage report example

Source	Net name	Expected (V)	Measured (V)	Measure point	Comment
Main	PSU_5V0	5.0		R39	
System 4.2 V	SYS_4V2	4.2		TP4	
PMIC Switcher 1	VDD_1V1	1.1		TP1	
PMIC Switcher 2	VDD_1V2	1.2		TP2	
PMIC Switcher 3	VDD_1V8	1.8		TP3	
PMIC LDO1	PMC_3V3	3.3			
PMIC LDO2	VDD_PTD	3.3/1.8			
PMIC LDO3	PMC_1V8	1.8			
SNVS	VDD_SNVS_3V0	3.0			
i.MX 7ULP	VDD_VBAT42	4.2			
i.MX 7ULP	VDD_DDR	1.2			
i.MX 7ULP	VDD_DIG1	1.1			
i.MX 7ULP	VDD_PMC18_DIG1	1.8			
i.MX 7ULP	VDD_PMC12_DIG0	1.2			
i.MX 7ULP	VDD18_DDR	1.8			
i.MX 7ULP	VDD_ANA33	3.3			
i.MX 7ULP	VDD_ANA18, VREFH_ANA18	1.8			
i.MX 7ULP	VDD_PMC18	1.8			
i.MX 7ULP	VDD_PMC11_DIG0_CAP	0.9			
i.MX 7ULP	VDD_PMC11_DIG1_CAP	1.05			
i.MX 7ULP	VDD_HSIC	1.2			
i.MX 7ULP	VDD_USB33	3.3			
i.MX 7ULP	VDD_USB18	1.8			
i.MX 7ULP	VDD18_IOREF	1.8			
i.MX 7ULP	VDD_DSI11	1.1			
i.MX 7ULP	VDD_DSI18	1.8			
i.MX 7ULP	VDD_PTA	3.3/1.8			
i.MX 7ULP	VDD_PTB	1.8			
i.MX 7ULP	VDD_PTC	3.3/1.8			
i.MX 7ULP	VDD_PTD	3.3/1.8			
i.MX 7ULP	VDD_PTE	3.3/1.8			
i.MX 7ULP	VDD_PTF	3.3/1.8			
i.MX 7ULP	DDR_VREF	0.6			

4.4. Checking for clock pitfalls

Problems with external clocks are another common source of board bring-up issues. Ensure that all your clock sources run as expected.

The EXTAL0/XTAL0 and EXTAL32/XTAL32 clocks are the main clock sources for the 24-MHz and 32-kHz reference clocks (respectively) on the i.MX 7ULP processor.

When checking crystal frequencies, use an active probe to avoid excessive loading. A parasitic probe prevents the 32.768-kHz and 24-MHz oscillators from starting up. Follow these guidelines:

- The EXTAL32 clock runs at 32.768 kHz (can be generated internally or applied externally).
- The EXTAL0/XTAL0 run at 24 MHz (used for the PLL reference).

4.5. Avoiding reset pitfalls

Follow these guidelines to ensure that the board boots in the correct boot mode.

- During the initial power-up, while asserting the RESET0_b reset signal, ensure that the 24-MHz clock is active before releasing RESET0_b.
- Follow the recommended power-up sequence specified in the i.MX 7ULP data sheet.
- Ensure that the RESET0_b signal remains asserted (low) until all voltage rails associated with the boot-up are powered and stable.

The GPIOs and internal fuses control how the i.MX 7ULP processor boots. For more details about the different boot modes, see the “System boot” chapter of the chip reference manual.

4.6. Sample board bring-up checklist

Note that the checklist incorporates the recommendations described in the previous sections. The blank cells should be filled in during the bring-up.

Table 21. Board bring-up checklist

Checklist item	Details	Owner	Finding and status
Note: The following items must be completed serially.			
Perform a visual inspection.	Check the major components to make sure that nothing is misplaced or rotated before applying power.		
Verify all i.MX voltage rails.	Confirm that the voltages match the data sheet requirements. Be sure to check the voltages not only at the voltage source, but also as close to the i.MX processor as possible (such as on a bypass capacitor). This reveals any IR drops on the board that may cause issues later on. All the i.MX voltage rails should be checked.		
Verify the power-up sequence.	Verify that the power-on reset (RESET0_b) is de-asserted (high) after all power rails have come up and are stable. See the i.MX data sheet for details about the power-up sequencing.		
Measure/probe the input clocks (32 kHz, 24 MHz, and others).	Without a properly running clock, the i.MX does not function properly.		
Check the JTAG connectivity.	This is one of the most fundamental and basic access points to the i.MX to allow debugging		

Table 21. Board bring-up checklist

Checklist item	Details	Owner	Finding and status
	and execution of low-level code.		
Note: The following items may be worked on in parallel with the other bring-up tasks.			
Access the internal RAM.	Verify the basic operation of the i.MX processor in the system. Perform a basic test by performing a write-read-verify on the internal RAM. No software initialization is necessary to access the internal RAM.		
Measure the boot mode frequencies: • Quad SPI (probe the slave select and measure the clock frequency). • eMMC/SD (measure the clock frequency).	This verifies the specified signals' connectivity between the i.MX 7ULP processor and the boot device and that the boot mode signals are properly set. See the "System boot" chapter in the reference manual for details about configuring various boot modes.		
Run the basic DDR initialization and test the memory.	Assuming the use of a JTAG debugger, run the DDR initialization and open a debugger memory window pointing to the DDR memory map starting address. Try writing a few words and verify whether they are read correctly. If not, recheck the DDR initialization sequence and whether the DDR is correctly soldered onto the board. It is also recommended to recheck the schematic to ensure that the DDR memory is connected to the i.MX 7ULP processor correctly.		

5. IBIS model

The IBIS model for each i.MX processor is provided on the NXP website upon product release. Contact your local sales office or field applications engineer to check the availability of information before product releases.

The IBIS model filename indicates which package it applies to:

- The 10 mm x 10 mm "VK" package has "VK" in the filename.
- The 14 mm x 14 mm "VP" package has "VP" in the filename.

5.1. References

See these references for more information about the IBIS models and how they are used:

- IBIS Open Forum:

  The IBIS Open Forum consists of EDA vendors, computer manufacturers, semiconductor vendors, universities, and end-users. It proposes updates and reviews, revises standards, and organizes summits. It promotes the IBIS models and provides useful documentation and tools.
- IBIS specification.

6. Using BSDL for board-level testing

6.1. BSDL overview

The boundary scan description language (BSDL) is used for board-level testing after the components are assembled. The interface for this test uses the JTAG pins. The definition is contained within the IEEE standard 1149.1.

6.2. How BSDL works

The BSDL file defines the internal scan chain (which is the serial linkage of the IO cells) within a device. The scan chain looks like a large shift register which provides the means to read the logic level applied to a pin or to output a logic state on that pin. Using JTAG commands, the test tool uses the BSDL file to control the scan chain so that the device-board connectivity can be tested.

For example, when using an external ROM test interface, the test tool would to the following:

1. Output a specific set of addresses and controls to the pins connected to the ROM.
2. Perform a read command and scan out the values of the ROM data pins.
3. Compare the values read with the known golden values.

Based on this procedure, the tool can determine whether the interface between the two parts is connected properly and does not contain shorts or opens.

6.3. Downloading the BSDL file

The BSDL file for each i.MX processor is provided on the NXP website upon product release. Contact your local sales office or field applications engineer to check the availability of information before product releases.

6.4. Pin coverage of BSDL

Each pin is defined as a port within the BSDL file. Open the file using a text editor to review how each pin works. The BSDL file defines these functions:

- -- PORT DESCRIPTION TERMS.
- -- in = input only.
- -- out = 3-state output (0, Z, 1).
- -- buffer = 2-state output (0, 1).
- -- inout = bidirectional.
- -- linkage = OTHER (vdd, vss, analog).

The appearance of “linkage” in a pin’s definition implies that the pin cannot be used with the boundary scan. These are usually power pins or analog pins that cannot be defined with a digital logic state.

6.5. Boundary scan operation

See these references for more information:

- The “Secured JTAG controller (SJC)” chapter in the chip reference manual for the definitions of the JTAG interface operations.
- The “Fusemap” chapter in the chip reference manual for the fusemap tables.

7. Development platforms

This chapter provides a complete list of the development platforms that are available from NXP to support the i.MX 7ULP processors.

Table 22. i.MX 7ULP EVK Revision B1

Version of i.MX used	i.MX 7ULP.
Schematic part number and revision	170-29163 Revision B1 (EVK SOM board). 170-29164 Revision B1 (EVK base board).
Features	SOM: • 1-GB LPDDR3. • 8-MB Quad SPI flash. • eMMC footprint. • Micro-SD 3.0 card socket. • USB 2.0 OTG with type C connector. • WiFi/Bluetooth. • PMIC NXP PF1550. Baseboard: • Full SD/MMC 3.0 card socket. • Audio codec and 3.5-mm audio jack. • 6-axis sensor with integrated linear accelerometer and magnetometer. • Gyroscope. • I^2C precision pressure sensor with altimetry. • Arduino connector. • ADC/DAC connector. • Battery socket. • HDMI connector. • MIPI display panel connector. • MFI interface. • USB HSIC interface.
Quick start guide	The quick start guide is available on the NXP website upon product release. Contact your local sales office or field applications engineer to check the availability of information before product releases.
Schematic	The schematic files are available on the NXP website upon product release. Contact your local sales office or field applications engineer to check the availability of information before product releases.
Layout	The layout files are available on the NXP website upon product release. Contact your local sales office or field applications engineer to check the availability of information before product releases.

Table 23. i.MX 7ULP EVK Revision C0

Version i.MX used	i.MX 7ULP.
Schematic part number and revision	170-38819 Revision C0 (EVK SOM board). 170-38818 Revision C0 (EVK base board).
Features	SOM: • 1-GB LPDDR3. • 8-MB Quad SPI flash. • eMMC footprint. • Micro-SD 3.0 card socket. • USB 2.0 OTG with type C connector. • WiFi/Bluetooth (LBEE5KL1DX). • PMIC NXP PF1550. Baseboard: • Full SD/MMC 3.0 card socket. • Audio codec and 3.5-mm audio jack. • 6-axis sensor with integrated linear accelerometer and magnetometer. • Gyroscope. • I^2C precision pressure sensor with altimetry. • Arduino connector. • ADC/DAC connector. • Battery socket. • HDMI connector. • MIPI display panel connector. • MFI interface. • USB HSIC interface.
Quick start guide	The quick start guide is available on the NXP website upon product release. Contact your local sales office or field applications engineer to check the availability of information before product releases.
Schematic	The schematic files are available on the NXP website upon product release. Contact your local sales office or field applications engineer to check the availability of information before product releases.
Layout	The layout files are available on the NXP website upon product release. Contact your local sales office or field applications engineer to check the availability of information before product releases.

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